的 TLIN1028S-Q1 汽车本地互联网络 (LIN) 收发器 70mA 系统基础芯片 (SBC)

1 特性

- AEC-Q100（1 级）：符合面向汽车的 应用
- 符合局域互联网络 (LIN) 物理层规范 ISO/DIS 17987–4.2，并符合适用于 LIN 的 SAE J2602 推荐实践要求
- 支持 12V 应用
- 宽工作范围
  - ±58V LIN 总线故障保护
  - 支持 3.3V 或 5V 的 LDO 输出
  - 睡眠模式：超低电流
    消耗支持以下类型的唤醒事件：
    - LIN 总线或通过 EN 引脚局部唤醒
  - 上电和断电无干扰运行
- 保护 特性：
  - ESD 保护
  - V_{SUP} 欠压保护
  - TXD 显性超时 (DTO) 保护
  - 热关断保护
  - 系统级未供电节点或接地断开失效防护
- V_{CC} 电源高达 70mA
- 采用 SOIC (8) 封装

2 应用

- 车身电子装置和照明
- 混合动力、电动和动力传动系统
- 汽车信息娱乐系统和仪表组
- 电器

3 说明

TLIN1028S-Q1 是一款本地互联网络 (LIN) 物理层收发器，符合 LIN 2.2A ISO/DIS 17987–4.2 标准，具有集成的低压降 (LDO) 稳压器。

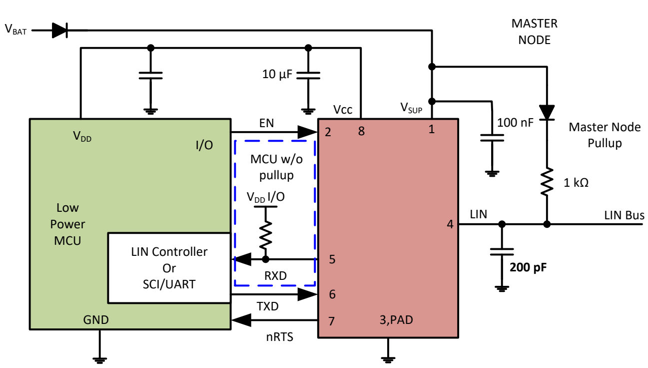
LIN 是一根单线制双向总线，通常用于低速车载网络，数据传输速率高达 20kbps。LIN 接收器支持数据传输速率高达 100kbps 的下线编程应用。TLIN1028S-Q1 将 TXD 输入上的 LIN 协议数据流转化为 LIN 总线信号。接收器将数据流转化为逻辑电平信号，此信号通过开漏 RXD 引脚发送到微处理器。TLIN1028S-Q1 通过为功率微处理器、传感器或其他器件提供一个电流高达 70mA的 3.3V 或 5V 电压轨，降低了系统的复杂性。TLIN1028S-Q1 具有经过优化的限流波形整形驱动器，可降低电磁辐射 (EME)。

器件信息(1)

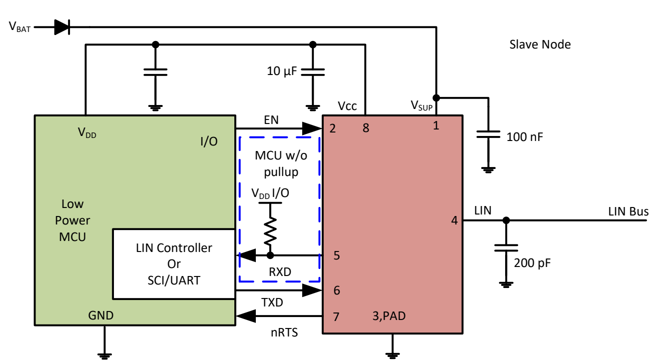
器件型号	封装	封装尺寸（标称值）
TLIN1028S-Q1	SOIC (8)	4.90mm x 3.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图，主模式



简化的原理图，从模式



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

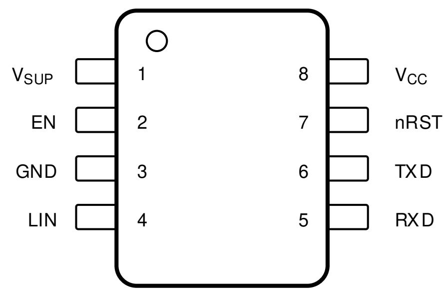
日期	修订版本	说明
2019 年 11 月	*	初始发行版

5 说明 （续）

睡眠模式可实现超低电流消耗，该模式允许通过 LIN 总线或引脚实现唤醒。LIN 总线有两种状态：显性状态（电压接近接地）和隐性状态（电压接近电池）。在受支配状态下，LIN 总线被内部上拉电阻器 (45kΩ) 和串联二极管拉高，所以没有为从属应用准备外部上拉组件 应用的高速串行链路的稳定性。主控 应用 需要一个外部上拉电阻器 (1kΩ) 加上一个符合 LIN 规范的串联二极管。

6 Pin Configuration and Functions

D Package
8-Pin (SOIC)
Top View



Not to scale

Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	V_{SUP}	HV Supply In	Device supply voltage (connected to battery in series with external reverse blocking diode)
2	EN	D I	Enable input
3	GND	GND	Ground (2)
4	LIN	HV I/O	LIN bus single-wire transmitter and receiver
5	RXD	D O	RXD output (open-drain) interface reporting state of LIN bus voltage
6	TXD	D I	TXD input interface to control state of LIN output
7	nRST	D O	Reset output (active low)
8	V_{CC}	Supply Out	Output voltage from integrated LDO

(1) HV - High Voltage, DI - Digital Input, DO - Digital Output, HV I/O - High Voltage Input/Output
(2) When the thermal pad is present, it must be soldered to ground plane.

7 Specifications

7.1 ABSOLUTE MAXIMUM RATINGS

		MIN	MAX	UNIT
V_{SUP}	Supply voltage range	–0.3	42	V
V_{LIN}	LIN Bus input voltage	–58	58	V
V_{CC50}	Regulated 5 V Output Supply	–0.3	6	V
V_{CC33}	Regulated 3.3 V Output Supply	–0.3	4.5	V
V_{nRST}	Reset output voltage	–0.3	V_{CC} + 0.3	V
V_{LOGIC_INPUT}	Logic input voltage	–0.3	6	V
V_{LOGIC_OUTPUT}	Logic output voltage	–0.3	6	V
I_{VCC}	V_{CC} supply current(2)		300	mA
I_O	Digital pin output current	–8	8	mA
$I_{O(nRST)}$	Reset output current	–5	5	mA
T_J	Junction temperature	–40	165	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device will enter thermal shutdown prior to hitting this limit but if the limit is reach the device may sustain permanent damage.

7.2 ESD RATINGS

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) classification level H2: V_{SUP}, LIN, and WAKE with respect to ground		±8000	V
		Human body model (HBM) classification level 3A: all other pins, per AEC Q100-002(1)		±4000	
		Charged device model (CDM) classification level C5, per AEC Q100-011	All pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 ESD RATINGS, IEC SPECIFICATION

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge per IEC 62228-2 (1), LIN, V_{SUP} terminal to GND	Contact discharge	±15000	V
		Indirect	±15000	V
$V_{(ESD)}$	Powered electrostatic discharge per SAE J2962-1(2)	Contact discharge	±8000	V
		Air discharge	±25000	
Transient	ISO 7637-2 and IEC 62215-3 transients per IEC 62228-2(1)	Pulse 1	-100	V
		Pulse 2a	75	
		Pulse 3a	-150	
		Pulse 3b	100	

(1) IEC 62228-2 ESD testing performed at third party. Different system-level configurations may lead to different results. Test reports availabel upon request.
(2) SAE J2962-1 Testing performed at 3rd party US3 approved EMC test facility, test report available upon request.

7.4 RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage	5.5		28	V
V_{LIN}	LIN bus input voltage	0		28	V
V_{LOGIC5}	Logic pin voltage	0		5.25	V
$V_{LOGIC33}$	Logic pin voltage	0		3.465	V
$I_{OH(DO)}$	Digital terminal HIGH level output current	-2			mA
$I_{OL(DO)}$	Digital terminal LOW level output current			2	mA
$C_{(VSUP)}$	V_{SUP} supply capacitor	100			nF

RECOMMENDED OPERATING CONDITIONS (continued)

		MIN	NOM	MAX	UNIT
$C_{(VCC)}$	V_{CC} supply capacitor	10			µF
ESR_{CO}	Output ESR requirements	0.001		2	Ω

7.5 THERMAL INFORMATION

THERMAL METRIC[1]		TLIN1028x D 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 POWER SUPPLY CHARACTERISTICS

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT						
V_{SUP}	Operational supply voltage (ISO/DIS 17987 Param 10)	Device is operational beyond the LIN defined nominal supply voltage range. See 图 5 and 图 6	5.5		36	V
V_{SUP}	Nominal supply voltage (ISO/DIS 17987 Param 10):	Normal and Standby Modes: Ramp VSUP while LIN signal is a 10 kHz square wave with 50 % duty cycle and swing between 5.5 V ≤ V_{LIN} ≤ 28 V. See 图 5 and 图 6	5.5		28	V
		Sleep Mode	5.5		28	V
UV_{SUPR}	Under voltage V_{SUP} threshold	Ramp Up		3.5	4.2	V
UV_{SUPF}	Under voltage V_{SUP} threshold	Ramp Down	1.8	2.1	2.5	V
U_{VHYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			1.5		V
I_{SUP}	Transceiver and LDO supply current	Transceiver normal mode dominant plus LDO output			80	mA
$I_{SUPTRXDOM}$	Supply current transceiver only	Normal Mode: EN = V_{CC}, bus dominant: total bus load where R_{LIN} ≥ 500 Ω and C_{LIN} ≤ 10 nF		1.2	5	mA
		Standby Mode: EN = 0 V, bus dominant: total bus load where R_{LIN} ≥ 500 Ω and C_{LIN} ≤ 10 nF		1	1.8	mA
$I_{SUPTRXREC}$	Supply current transceiver only	Normal Mode: EN = V_{CC}, Bus recessive: LIN = V_{SUP},		450	775	µA
		Standby Mode: EN = 0 V, LIN = recessive = V_{SUP}, I_{OZH} from processor ≤ 1 µA		38	55	µA
		Added Standby Mode current through the RXD pull-up resistor with a value of 100 kΩ: EN = 0 V, LIN = recessive = VSUP, RXD = GND[1]			55	µA
$I_{SUPTRXSLP}$	Sleep mode supply current transceiver only	5.5 V < V_{SUP} ≤ 28 V, LIN = V_{SUP}, EN = 0 V, TXD and RXD floating		17	33	µA
REGULATED OUTPUT V_{CC}						
V_{CC}	Regulated output	V_{SUP} = 5.5 to 28 V, I_{CC} = 1 to 70 mA	–2		2	%
$\Delta V_{CC(\Delta VSUP)}$	Line regulation	V_{SUP} = 5.5 to 28 V, ΔV_{CC}, I_{CC} = 10 mA			50	mV
$\Delta V_{CC(\Delta VSUPL)}$	Load regulation	I_{CC} = 1 to 70 mA, V_{SUP} = 14 V, ΔV_{CC}			50	mV

(1) RXD pin is an open drain output. In standby mode RXD is pulled low which has the device pulling current through V_{SUP} through the pull-up resisitor to V_{CC}. The value of the pull-up resistor impacts the standby mode current. A 10 kΩ resistor value can add as much at 500 µA of current.

POWER SUPPLY CHARACTERISTICS (continued)

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DROP}	Dropout voltage (5 V LDO)	V_{SUP} – V_{CC}, I_{CC} = 70 mA;		300	600	mV
V_{DROP}	Dropout voltage (3.3 V LDO)	V_{SUP} – V_{CC}, I_{CC} = 70 mA;		350	700	mV
UV_{CC5R}	Under voltage 5 V V_{CC} threshold	Ramp Up		4.7	4.86	V
UV_{CC5F}	Under voltage 5 V V_{CC} threshold	Ramp Down	4.2	4.45		V
UV_{CC33R}	Under voltage 3.3 V V_{CC} threshold (2)	Ramp Up		2.9	3.1	V
UV_{CC33F}	Under voltage 3.3 V V_{CC} threshold (2)	Ramp Down	2.5	2.75		V
$t_{DET(UVCC)}$	VCC undervoltage deglitch time. An UV_{CC} event will not be recognized unless it last longer than this. (2)	C_{nRST} = 20pF	1		15	µs
I_{CCOUT}	Output current	V_{CC} in regulation with 12 V V_{SUP}	0		70	mA
I_{CCOUTL}	Output current limit	V_{CC} short to ground			275	mA
PSRR	Power supply rejection ripple rejection	V_{RIP} = 0.5 V_{PP}, Load = 10 mA, f = 100 Hz, CO = 10 µF		60		dB
T_{SDR}	Thermal shutdown temperature	Internal junction temperature - rising	165			°C
T_{SDF}	Thermal shutdown temperature	Internal junction temperature - falling			150	°C
T_{SDHYS}	Thermal shutdown hysteresis			10		°C

(2) Specified by design

7.7 ELECTRICAL CHARACTERISTICS

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RXD OUTPUT TERMINAL (OPEN DRAIN)						
V_{OL}	Output low voltage	Based upon a 2 kΩ to 10 kΩ external pull-up to V_{CC}			0.2	V_{CC}
I_{OL}	Low level output current, open drain	LIN = 0 V, RXD = 0.4 V	1.5			mA
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, RXD = V_{CC}	–5	0	5	µA
TXD INPUT TERMINAL						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.5	V
I_{IH}	High level input leakage current	TXD = high	–5	0	5	µA
R_{TXD}	Internal pull-up resistor value		125	350	800	kΩ
LIN TERMINAL (REFERENCED TO V_{SUP})						
V_{OH}	HIGH level output voltage	LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 5.5 V to 36 V	0.85			V_{SUP}
V_{OL}	LOW level output voltage	LIN dominant, TXD = low, V_{SUP} = 5.5 V to 36 V			0.2	V_{SUP}
$V_{SUP\_NON\_OP}$	V_{SUP} where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11)	TXD & RXD open, V_{LIN} = 5.5 V to 42 V, Bus Load = 60 kΩ + diode and 1.1 kΩ + diode	–0.3		42	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987 Param 12)	TXD = 0 V, V_{LIN} = 36 V, R_{MEAS} = 440 Ω, V_{SUP} = 36 V, V_{BUSdom} < 4.518 V; 图 9	40	90	200	mA
$I_{BUS\_PAS\_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 13)	V_{LIN} = 0 V, V_{SUP} = 12 V Driver off/recessive, R_{MEAS} = 499 Ω; 图 10	–1			mA
$I_{BUS\_PAS\_rec1}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V_{LIN} ≥ V_{SUP}, 5.5 V ≤ V_{SUP} ≤ 36 V Driver off, R_{MEAS} = 1 kΩ; 图 11			20	µA
$I_{BUS\_PAS\_rec2}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V_{LIN} = V_{SUP}, Driver off, R_{MEAS} = 1 kΩ; 图 11	–8		8	µA
$I_{BUS\_NO\_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15)	GND = V_{SUP}, V_{SUP} = 12 V, 0 V ≤ V_{LIN} ≤ 28 V, R_{MEAS} = 1 kΩ; 图 12	–1		1	mA
$I_{BUS\_NO\_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 16)	0 V ≤ V_{LIN} ≤ 28 V, V_{SUP} = GND, R_{MEAS} = 10 kΩ; 图 13			8	µA
V_{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 17)	LIN dominant (including LIN dominant for wake up); 图 7, 图 8			0.4	V_{SUP}
V_{BUSrec}	High level input voltage (ISO/DIS 17987 Param 18)	LIN recessive; 图 7, 图 8	0.6			V_{SUP}

ELECTRICAL CHARACTERISTICS (continued)

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19)	$V_{BUS\_CNT} = (V_{IL} + V_{IH})/2$; 图 7, 图 8	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20)	$V_{HYS} = (V_{IL} - V_{IH})$; 图 7, 图 8			0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN term pull-up path (ISO/DIS 17987 Param 21)	By design and characterization	0.4	0.7	1.0	V
R_{SLAVE}	Pull-up resistor to V_{SUP} (ISO/DIS 17987 Param 26)	Normal and Standby modes	20	45	60	kΩ
I_{RSLEEP}	Pull-up current source to V_{SUP}	Sleep mode, V_{SUP} = 12 V, LIN = GND	–20		–2	µA
$C_{LIN,PIN}$	Capacitance of the LIN pin				55	pF
EN INPUT TERMINAL						
V_{IH}	High level input voltage		2		5.5	V
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{HYS}	Hysteresis voltage	By design and characterization	30		500	mV
I_{IL}	Low level input current	EN = Low	–5	0	5	µA
R_{EN}	Internal pull-down resistor		125	350	800	kΩ
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, nRST = V_{CC}	–5		5	µA
V_{OL}	Low-level output voltage	Based upon external pull up to V_{CC}			0.2	V_{CC}
I_{OL}	Low-level output current, open drain	LIN = 0 V, nRST = 0.4 V	1.5			mA
DUTY CYCLE CHARACTERISTICS						
$D1_{12V}$	Duty Cycle 1 (ISO/DIS 17987 Param 27)	$TH_{REC(MAX)} = 0.744 \times V_{SUP}$, $TH_{DOM(MAX)} = 0.581 \times V_{SUP}$, V_{SUP} = 5.5 V to 18 V, t_{BIT} = 50 µs (20 kbps), $D1 = t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See 图 14, 图 15)	0.396			
$D2_{12V}$	Duty Cycle 2 (ISO/DIS 17987 Param 28)	$TH_{REC(MIN)} = 0.422 \times V_{SUP}$, $TH_{DOM(MIN)} = 0.284 \times V_{SUP}$, V_{SUP} = 5.5 V to 18 V, t_{BIT} = 50 µs (20 kbps), $D2 = t_{BUS\_rec(MAX)}/(2 \times t_{BIT})$ (See 图 14, 图 15)			0.581	
$D3_{12V}$	Duty Cycle 3 (ISO/DIS 17987 Param 29)	$TH_{REC(MAX)} = 0.778 \times V_{SUP}$, $TH_{DOM(MAX)} = 0.616 \times V_{SUP}$, V_{SUP} = 5.5 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), $D3 = t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See 图 14, 图 15)	0.417			
$D4_{12V}$	Duty Cycle 4 (ISO/DIS 17987 Param 30)	$TH_{REC(MIN)} = 0.389 \times V_{SUP}$, $TH_{DOM(MIN)} = 0.251 \times V_{SUP}$, V_{SUP} = 5.5 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), $D4 = t_{BUS\_rec(MAX)}/(2 \times t_{BIT})$ (See 图 14, 图 15)			0.59	

7.8 AC SWITCHING CHARACTERISTICS

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

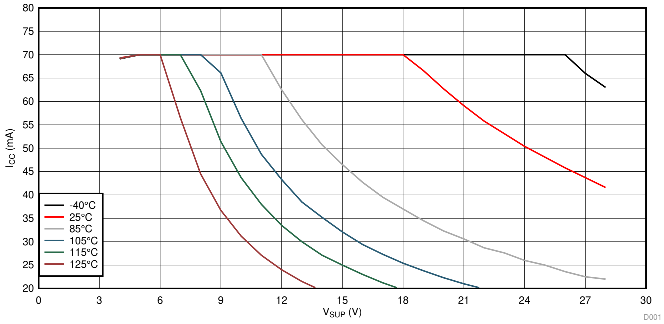
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE SWITCHING CHARACTERISTICS						
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See 图 16, 图 17 and 图 21)			6	µs
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time (ISO/DIS 17987 Param 32)	Rising edge with respect to falling edge, ($t_{rx\_sym} = t_{rx\_pdf} - t_{rx\_pdr}$), R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (图 16, 图 17 and 图 21)	–2		2	µs
t_{LINBUS}	LIN wakeup time (minimum dominant time on LIN bus for wakeup)	See 图 20, 图 24 and 图 25	25	100	150	µs
t_{CLEAR}	Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See 图 25	8	17	50	µs
t_{TXD_DTO}	Dominant state time out		20	34	80	ms
t_{EN}	Enable pin deglitch time	Time enable pin state change before initiating mode change or sampling TXD pine: See 图 18	3		12	µs

AC SWITCHING CHARACTERISTICS (continued)

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

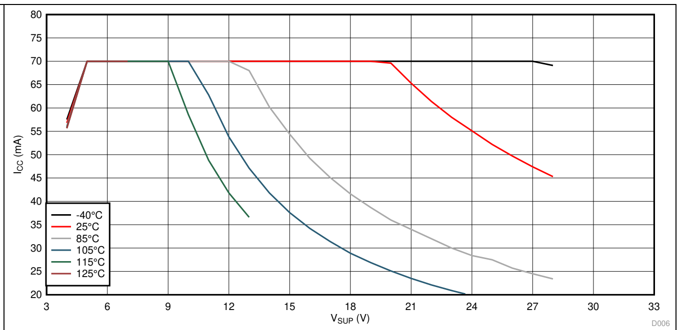
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{MODE_CHANGE}	Mode change delay time normal mode to sleep or standby mode	Time to change from normal mode to sleep or standby after TXD pin sampling after EN pin set low: See 图 18			20	µs
t_{MODE_CHANGE}	Mode change delay time sleep mode to normal mode	Time to change from sleep mode to normal mode through EN pin and not due to a wake event; RXD pulled up to V_{CC}: See 图 18			400	µs
t_{NOMINT}	Normal mode initialization time	Time for normal mode to initialize and data on RXD pin to be valid after t_{EN} See 图 18			35	µs
t_{PWR}	Power up time	Upon power up time it takes for valid data on RXD			1.5	ms

7.9 Typical Characteristics



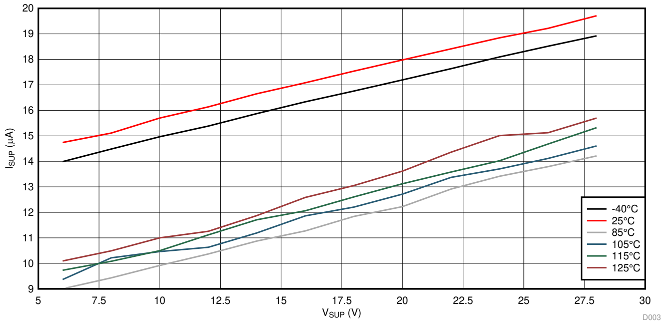
Package = D V_{CC} = 3.3 V   Temperature = Ambient

图 1. I_{CC} vs V_{SUP} vs Temperature



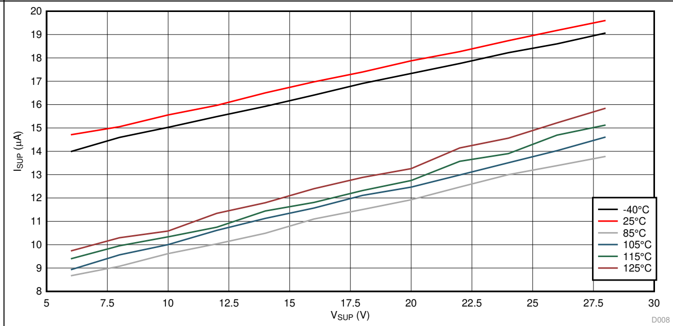
Package = D V_{CC} = 5 V   Temperature = Ambient

图 2. I_{CC} vs V_{SUP} vs Temperature



Package = D V_{CC} = 3.3 V   Temperature = Ambient

图 3. Sleep Mode Current Across V_{SUP} and Temperature



Package = D V_{CC} = 5 V   Temperature = Ambient

图 4. Sleep Mode Current Across V_{SUP} and Temperature

8 Parameter Measurement Information

8.1 Test Circuit: Diagrams and Waveforms

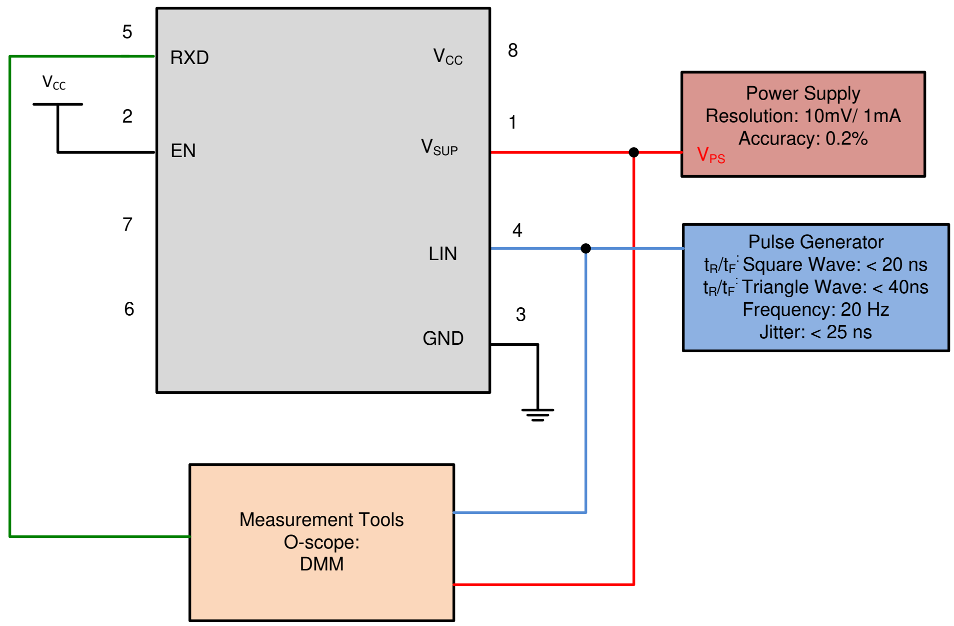


图 5. Test System: Operating Voltage Range with RX and TX Access

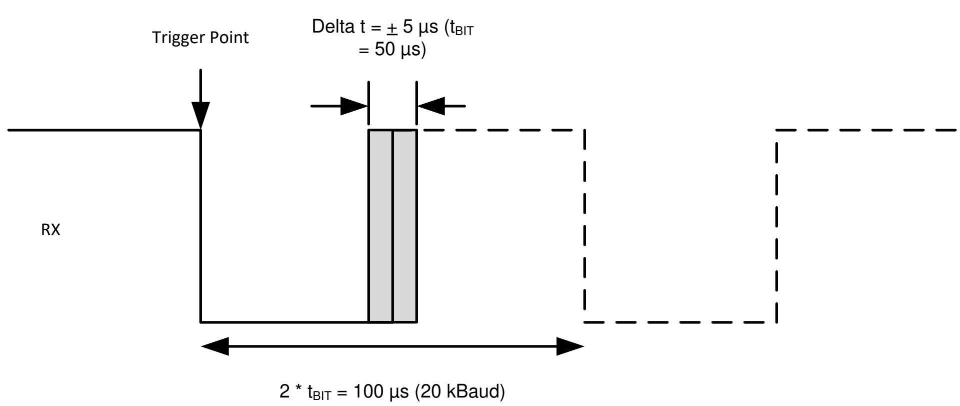


图 6. RX Response: Operating Voltage Range

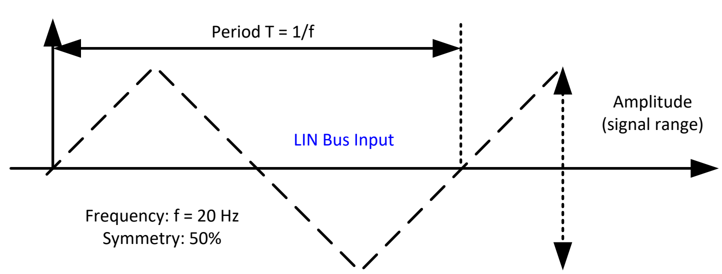


图 7. LIN Bus Input Signal

Test Circuit: Diagrams and Waveforms (接下页)

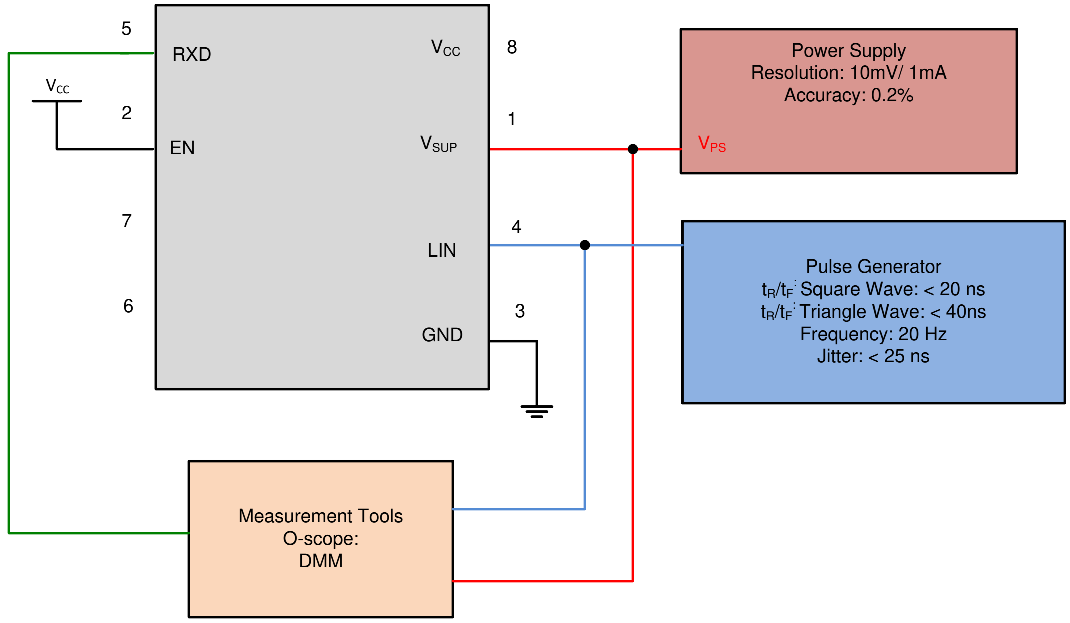


图 8. LIN Receiver Test with RX access

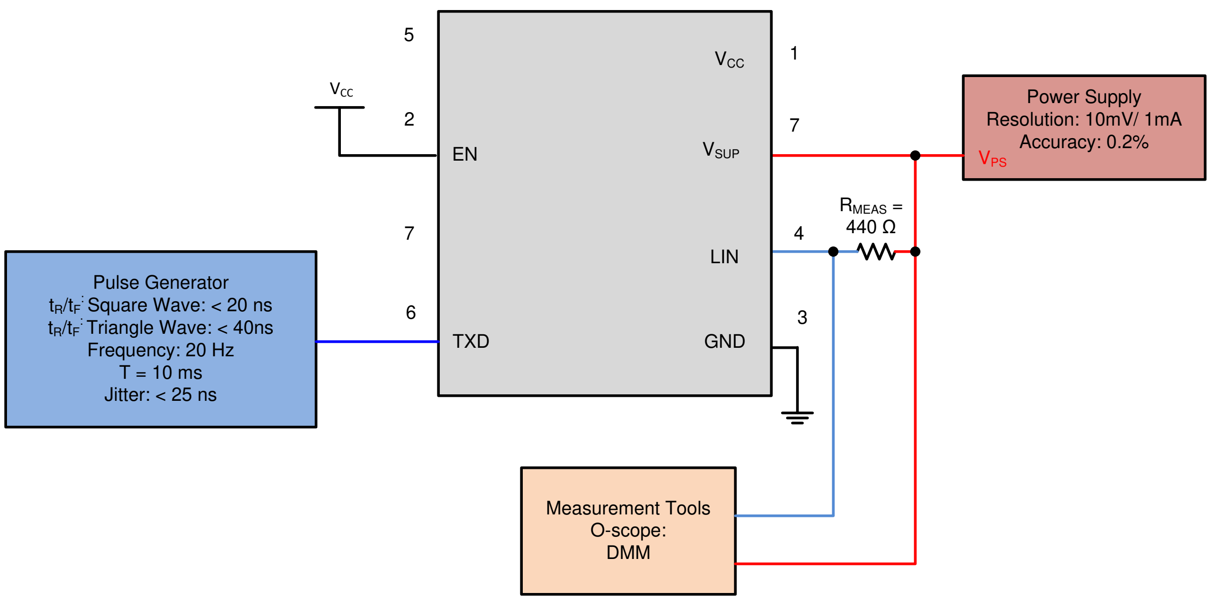


图 9. Test Circuit for I_{BUS_LIM} at Dominant State (Driver on)

Test Circuit: Diagrams and Waveforms (接下页)

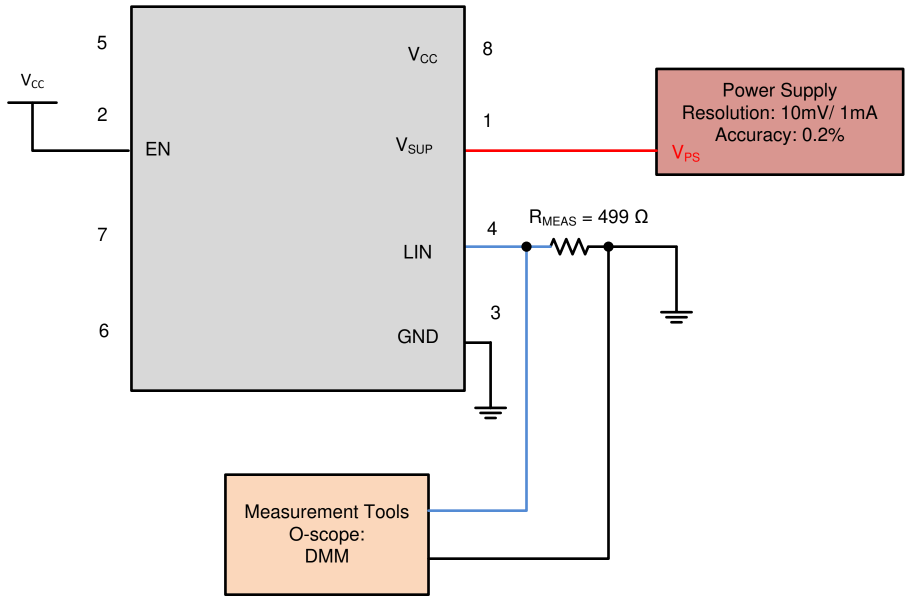


图 10. Test Circuit for $I_{BUS\_PAS\_dom}$; TXD = Recessive State V_{BUS} = 0 V

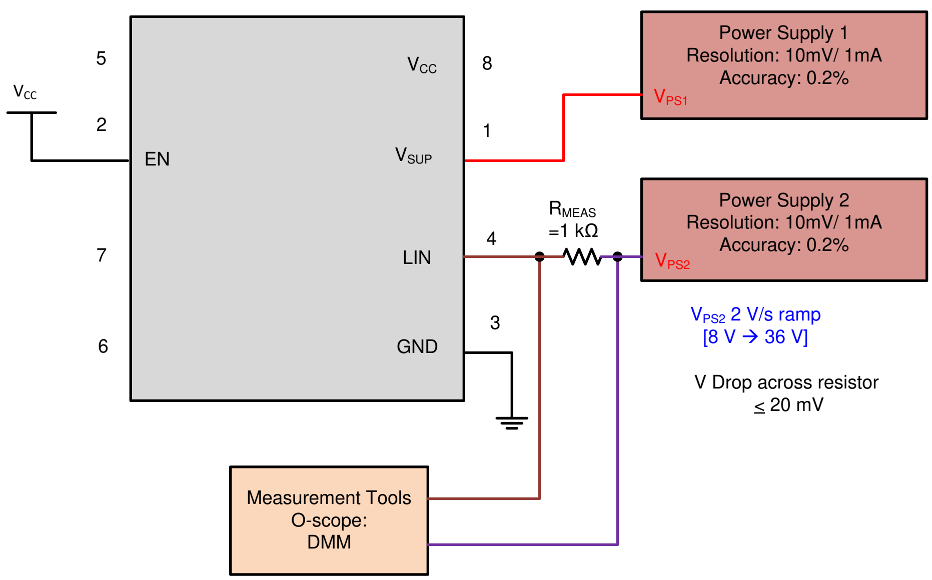


图 11. Test Circuit for $I_{BUS\_PAS\_rec}$

Test Circuit: Diagrams and Waveforms (接下页)

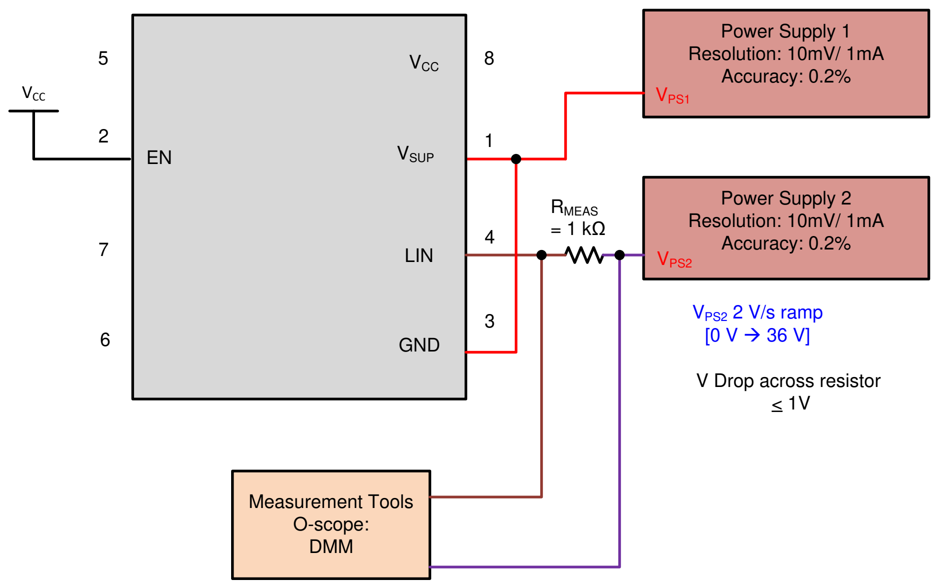


图 12. Test Circuit for $I_{BUS\_NO\_GND}$ Loss of GND

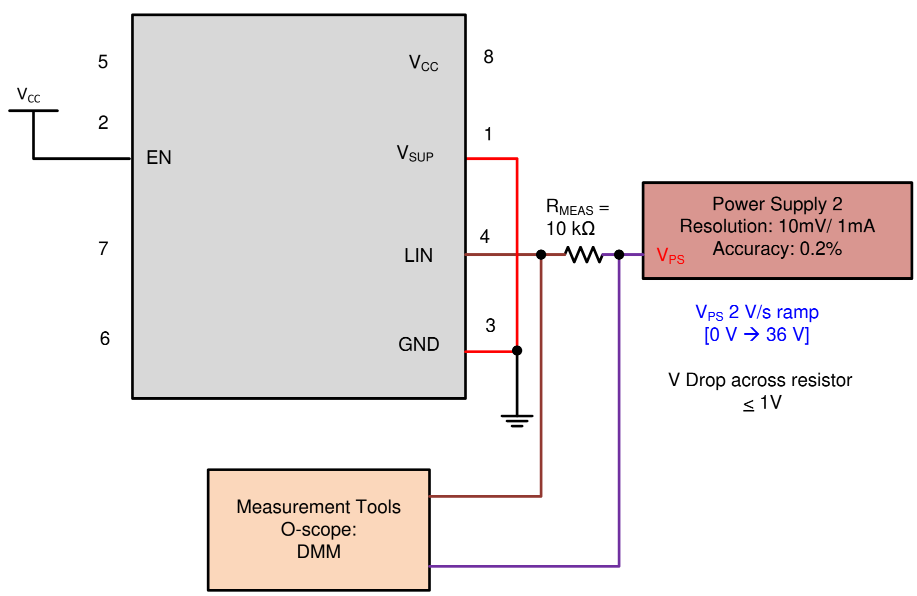


图 13. Test Circuit for $I_{BUS\_NO\_BAT}$ Loss of Battery

Test Circuit: Diagrams and Waveforms (接下页)

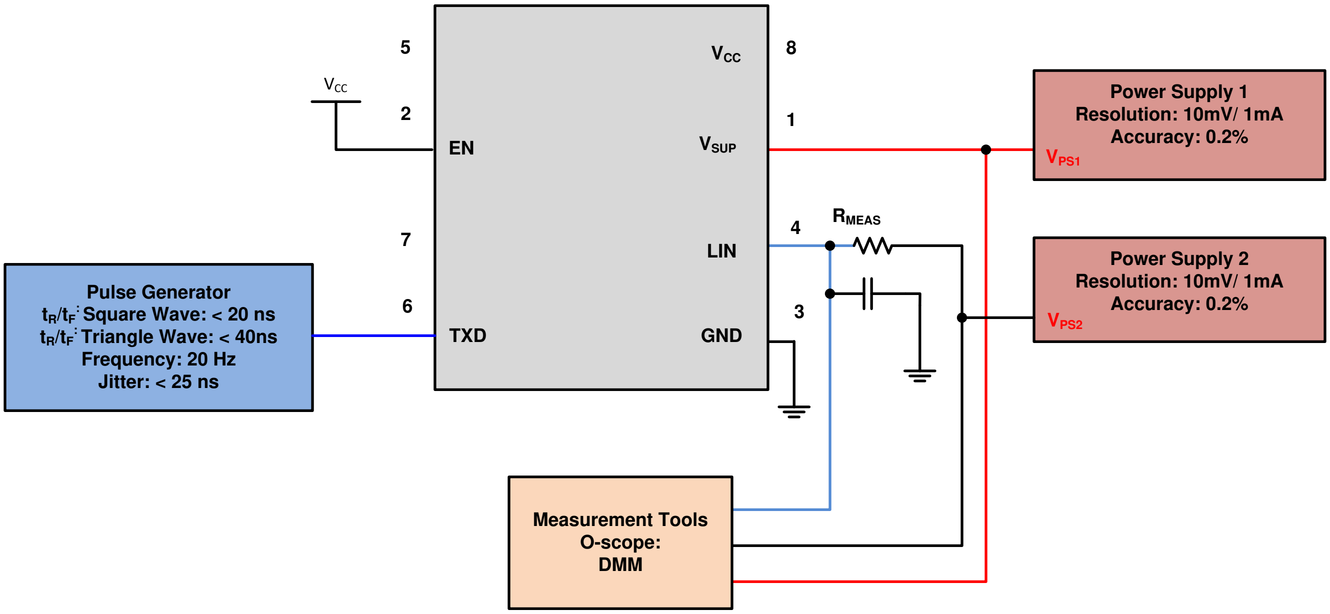


图 14. Test Circuit Slope Control and Duty Cycle

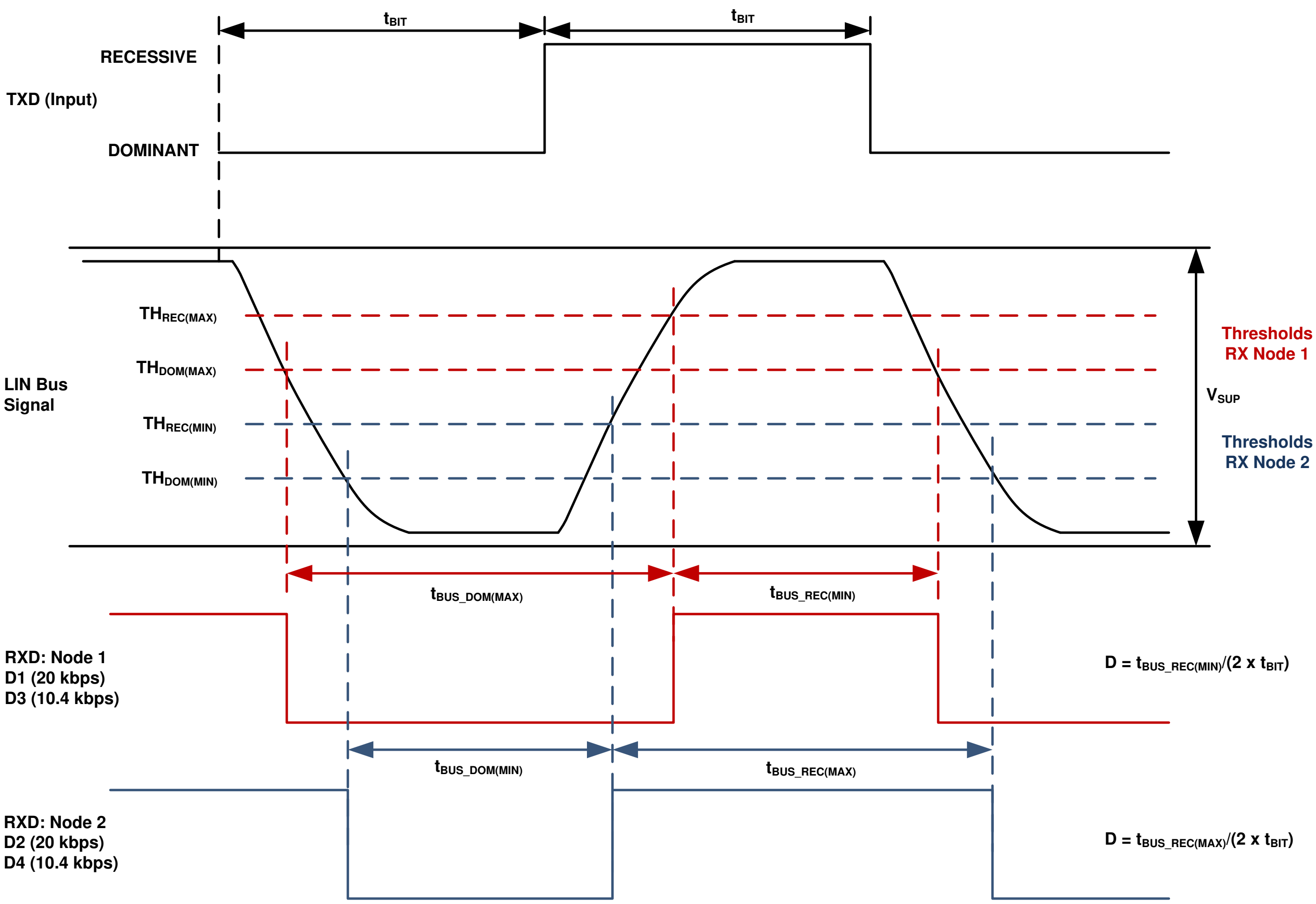


图 15. Definition of Bus Timing

Test Circuit: Diagrams and Waveforms (接下页)

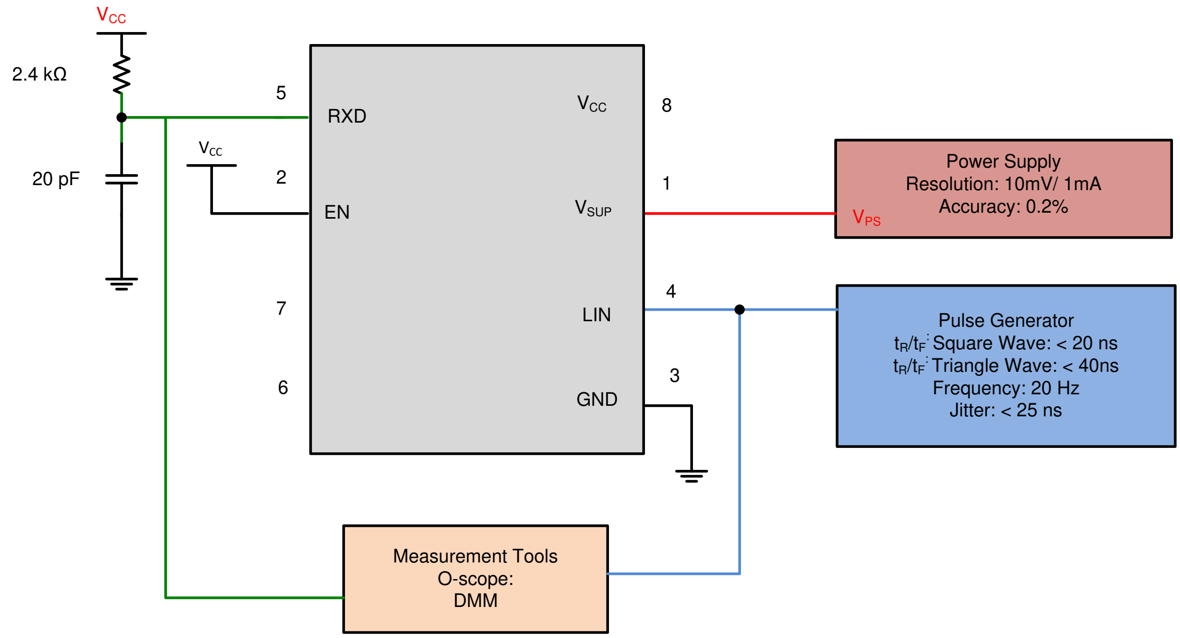


图 16. Propagation Delay Test Circuit

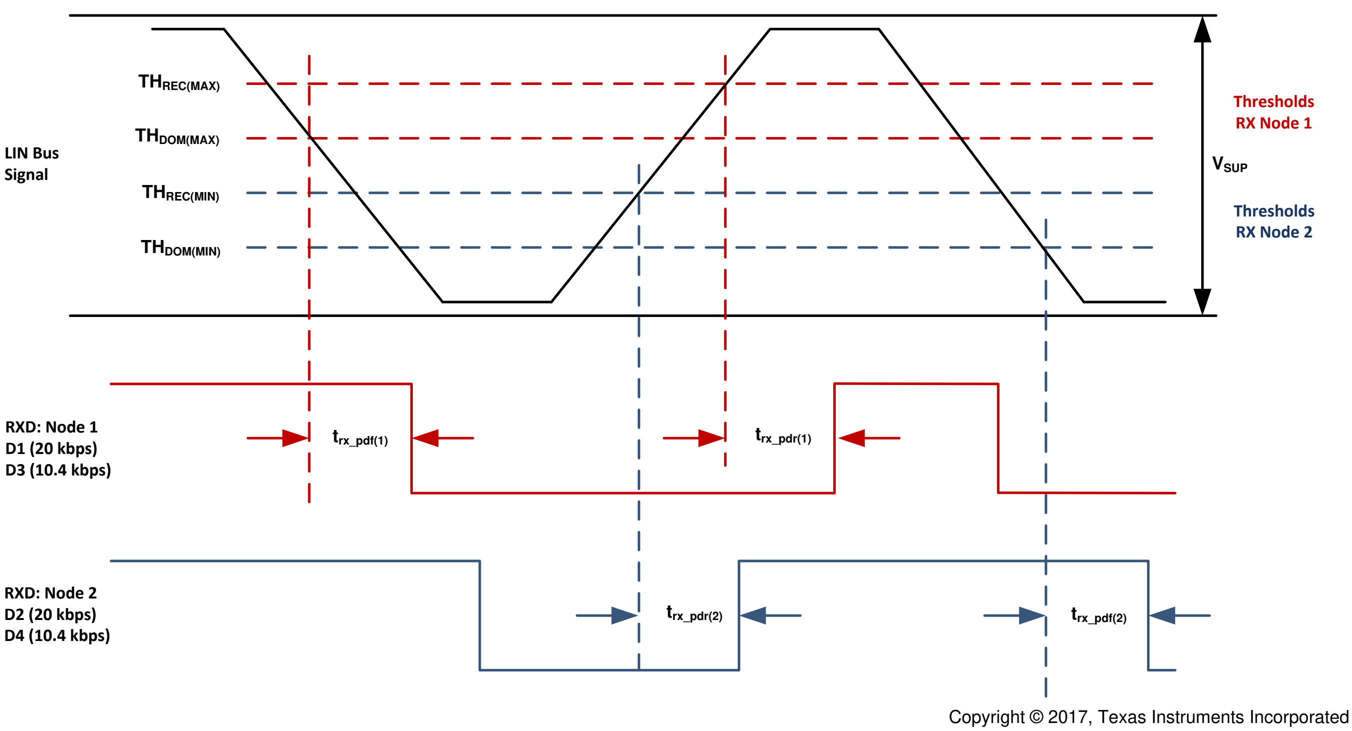


图 17. Propagation Delay

Test Circuit: Diagrams and Waveforms (接下页)

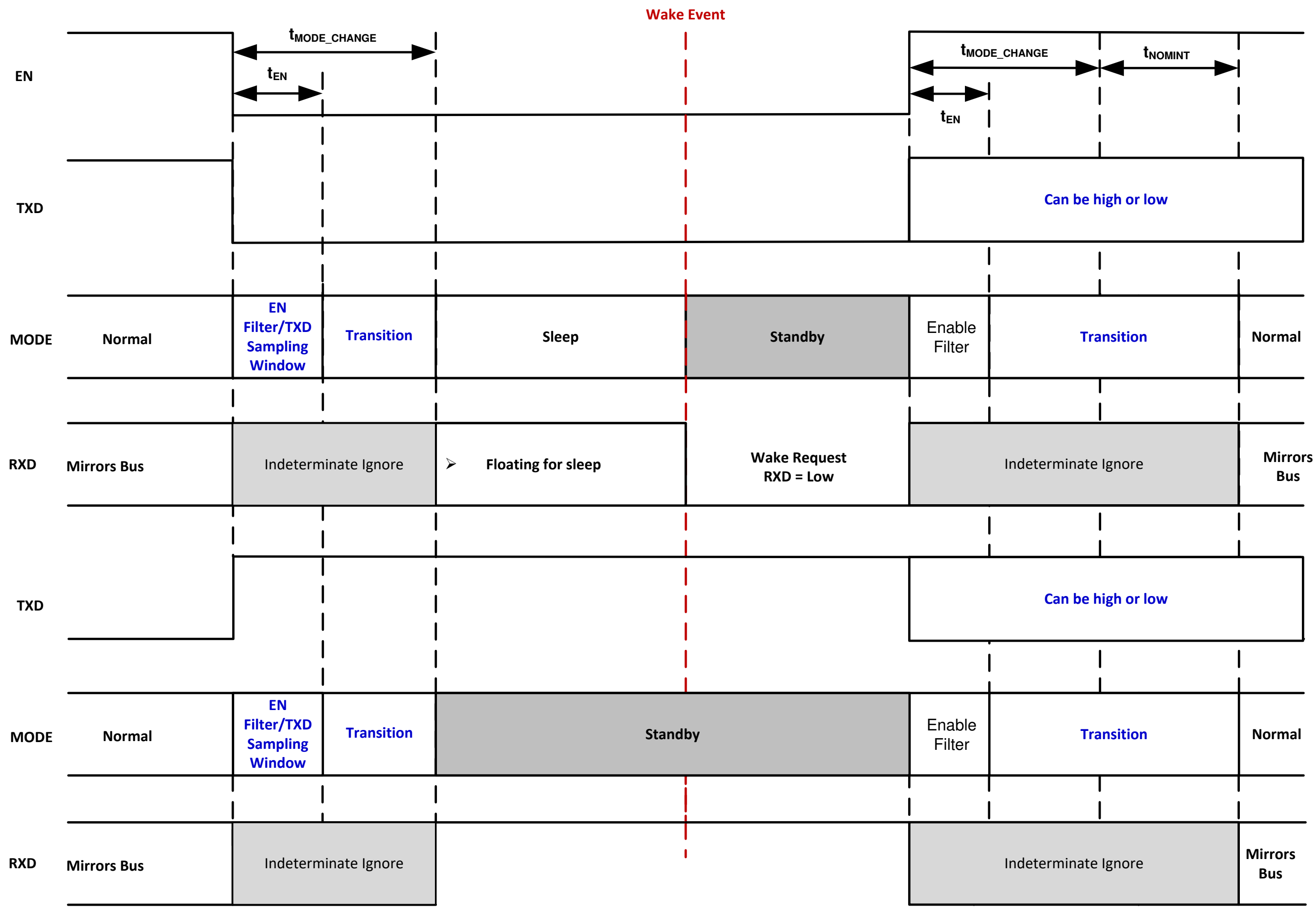


图 18. Mode Transitions

Test Circuit: Diagrams and Waveforms (接下页)

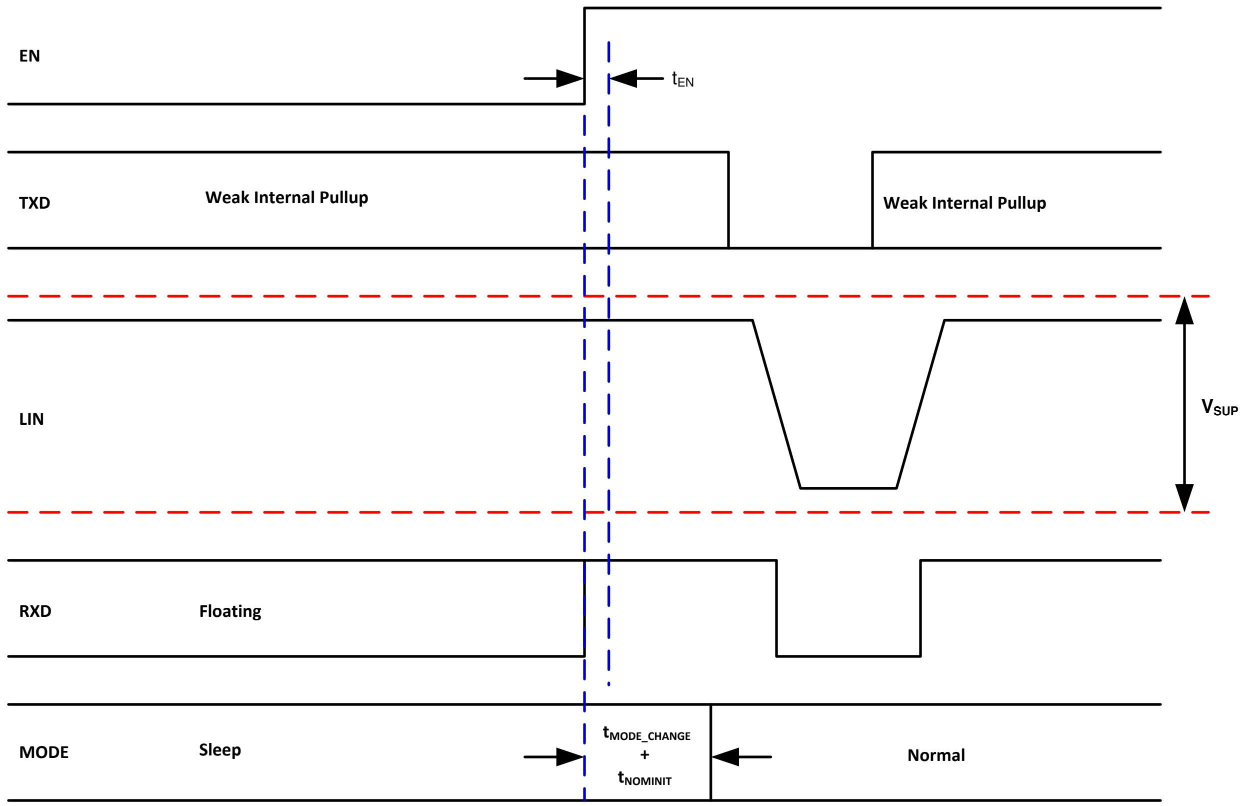


图 19. Wakeup Through EN

Test Circuit: Diagrams and Waveforms (接下页)

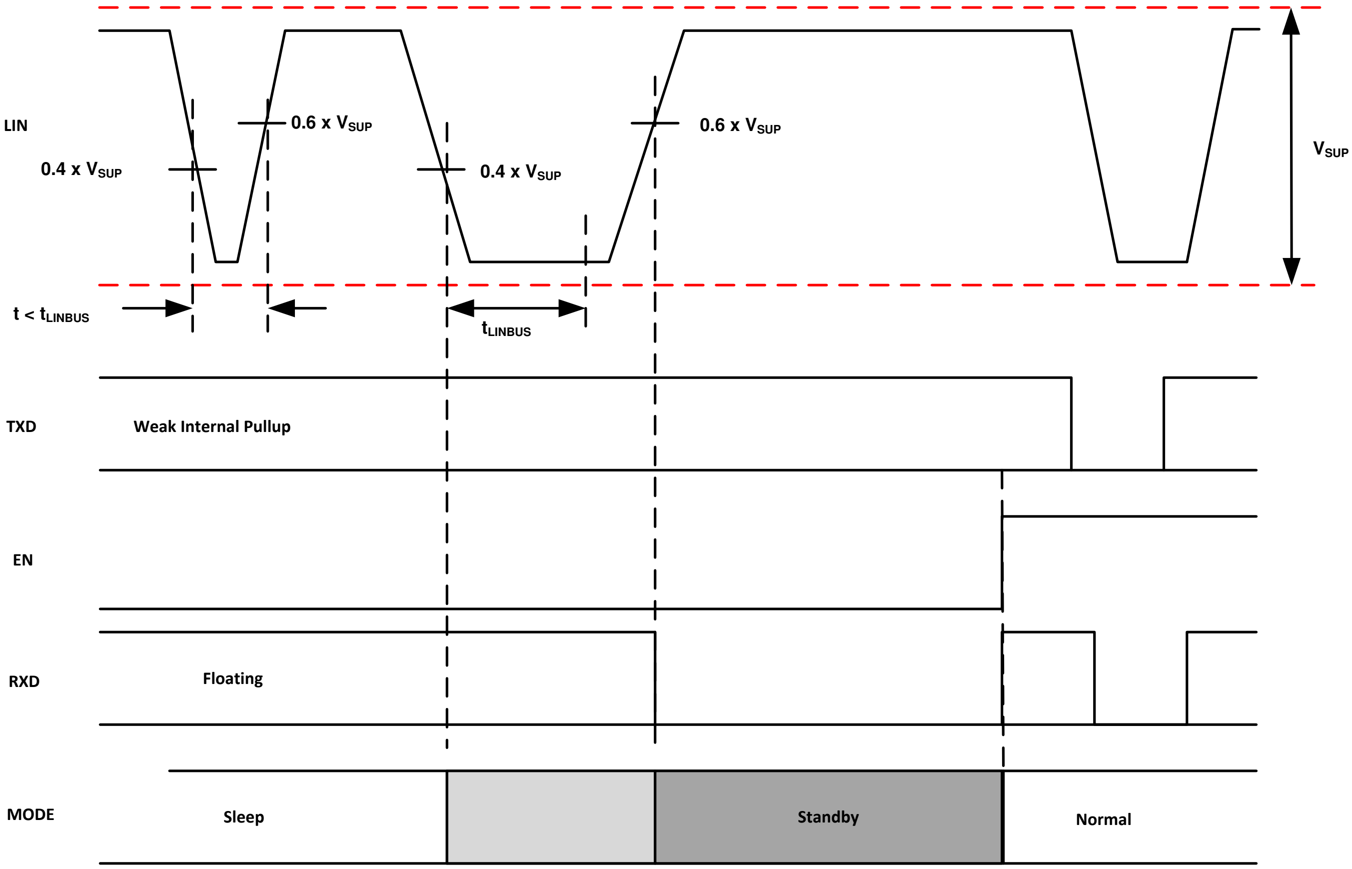


图 20. Wakeup through LIN

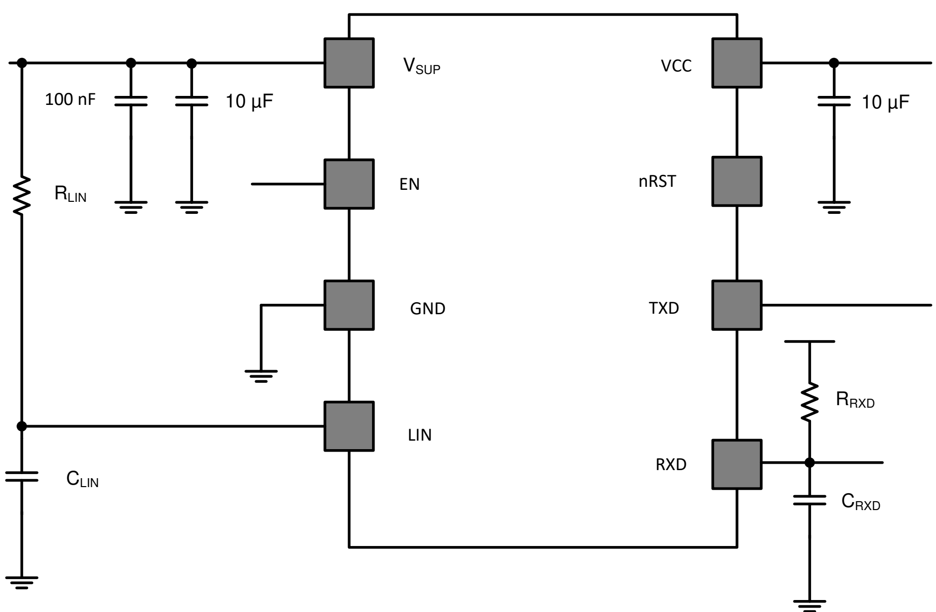


图 21. Test Circuit for AC Characteristics

9 Detailed Description

9.1 Overview

The TLIN1028S-Q1 LIN transceiver is a Local Interconnect Network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4.2 with integrated wake-up and protection features. The LIN bus is a single-wire, bidirectional bus that typically is used in low speed in-vehicle networks with data rates that range up to 20 kbps. The LIN receiver works up to 100 kbps supporting in-line programming. The device converts the LIN protocol data stream on the TXD input into a LIN bus signal using a current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The receiver converts the data stream to logic level signals that are sent to the microprocessor through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode.

Ultra-low current consumption is possible using the sleep mode. The TLIN1028S provides two methods to wake up from sleep mode: EN pin and LIN bus. The device integrates a low dropout voltage regulator with a wide input from V_{SUP} providing 5 V ±2% or 3.3 V ±2% with up to 70 mA of current depending upon system implementation. nRST is asserted high when V_{CC} increases above UV_{CC} and stays high as long as V_{CC} is above this threshold.

9.2 Functional Block Diagram

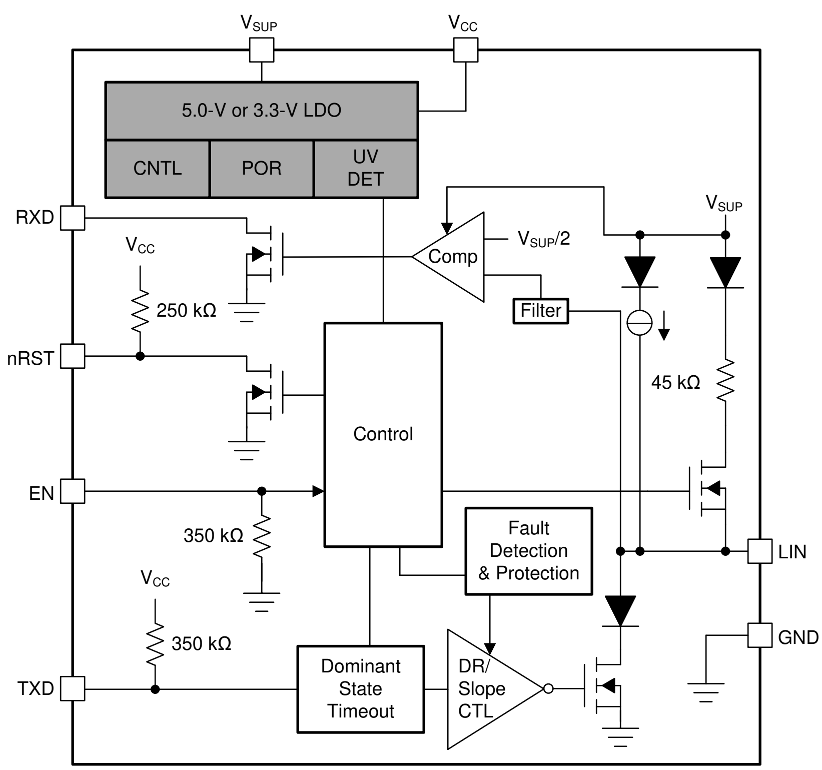


图 22. Functional Block Diagram

9.3 Feature Description

9.3.1 LIN (Local Interconnect Network) Bus

This high voltage input or output pin is a single wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 58 V. Reverse currents from the LIN to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

Feature Description (接下页)

9.3.1.1 LIN Transmitter Characteristics

The transmitter meets thresholds and AC parameters according to the LIN specification. The transmitter is a low side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor and series diode to V_{SUP} must be added when the device is used for a master node application.

9.3.1.2 LIN Receiver Characteristics

The receiver characteristic thresholds are ratio-metric with the device supply pin according to the LIN specification.

The receiver is capable of receiving higher data rates (> 100 kbps) than supported by LIN or SAEJ2602 specifications. This allows the TLIN1028S-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

9.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor (1 kΩ) and a series diode to V_{SUP} must be added when the device is used for master node applications as per the LIN specification.

图 23 shows a master node configuration and how the voltage levels are defined

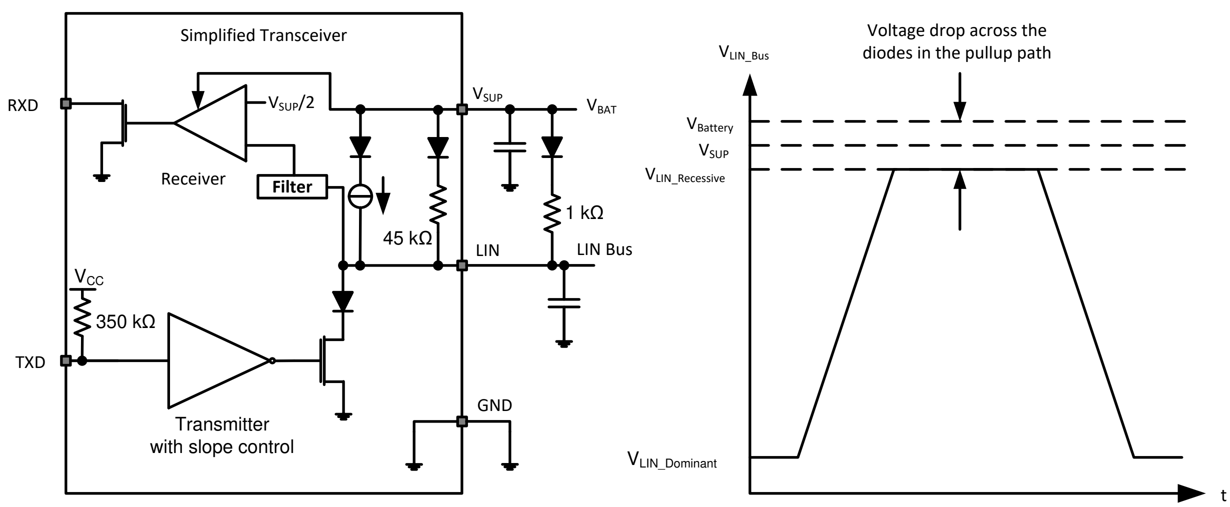


图 23. Master Node Configuration with Voltage Levels

9.3.2 TXD (Transmit Input and Output)

TXD is the interface to the node processors's LIN protocol controller that is used to control the state of the LIN output. When TXD is low, the LIN output is dominant (near ground). When TXD is high, the LIN output is recessive (near V_{SUP}). See 图 23. The TXD input structure is compatible with processors with 3.3 V and 5 V_I and V_O. TXD has an internal pull-up resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state time-out timer.

Feature Description (接下页)

9.3.3 RXD (Receive Output)

RXD is the interface to the processors LIN protocol controller, which reports the state of the LIN bus voltage. LIN recessive (near V_{SUP}) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3 V and 5 $V_{I/O}$ processors. If the processors RXD pin does not have an integrated pull-up, an external pull-up resistor to the processors I and O supply voltage is required. In standby mode, the RXD pin is driven low to indicate a wake up request from the LIN bus from sleep mode. When going from normal mode to standby mode the RXD pin is released and pulled up to the voltage rail the external pull-up resistor is connected.

9.3.4 V_{SUP} (Supply Voltage)

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse battery-blocking diode.

The V_{SUP} pin is a high-voltage-tolerant pin. Decoupling capacitor with a value of 100 nF is recommended to be connected close to this pin to better the transient performance. If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied). When V_{SUP} drops low enough the regulated output drops out of regulation. The LIN bus works with a V_{SUP} as low as 5.5 V, but at a lower voltage, the performance is indeterminate and not ensured. If V_{SUP} voltage level drops enough, it triggers the UV_{SUP}, and if it keeps dropping, at some point it passes the POR threshold.

9.3.5 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.6 EN (Enable Input)

EN controls the operational modes of the device. When EN is high, the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low, the device is put into sleep mode and there are no transmission paths available. EN has an internal pull-down resistor to ensure the device remains in low power mode even if EN is left floating. EN should be held low until V_{SUP} reaches the expected system voltage level.

9.3.7 nRST (Reset Output)

The V_{CC} pin is monitored for under voltage events. This pin is internally pulled up to V_{CC} and when an undervoltage event takes place, this pin is pulled low. The pin returns to V_{CC} once the voltage on V_{CC} exceeds the under voltage threshold. nRST is only dependent upon UV_{CC} and not dependent upon the operational mode. If UV_{CC} takes place for longer than $t_{DET(UVCC)}$ nRST is pulled low. If a thermal shutdown event takes place, this pin is pulled to ground.

9.3.8 V_{CC} (Supply Output)

The V_{CC} terminal can provide 5 V or 3.3 V with up to 70 mA to power up external devices when using high-k boards and thermal management best practices.

9.3.9 Protection Features

The device has several protection features that are described as follows.

Feature Description (接下页)

9.3.9.1 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state time-out timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than t_{TXD_DTO}, the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the t_{TXD_DTO} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-up to ensure the device fails to a known recessive state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of stated request on EN), the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on.

9.3.9.2 Bus Stuck Dominant System Fault: False Wake Up Lockout

The device contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current use. 图 24 and 图 25 show the behavior of this protection.

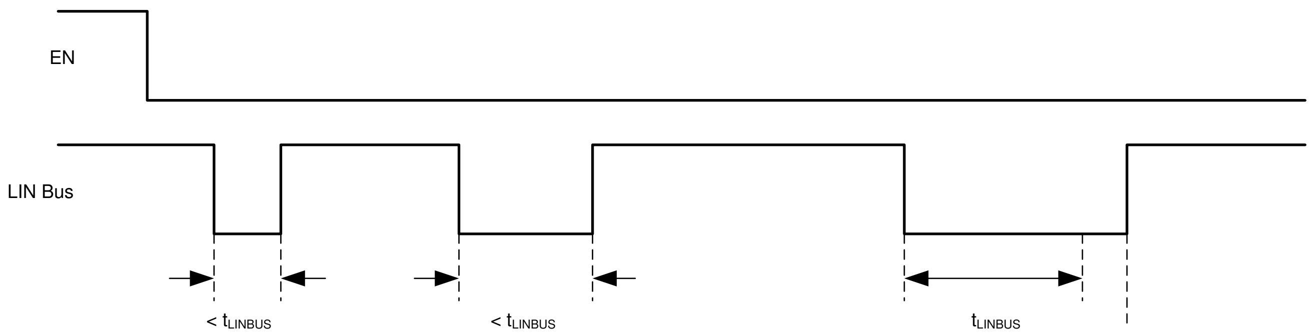


图 24. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wakeup

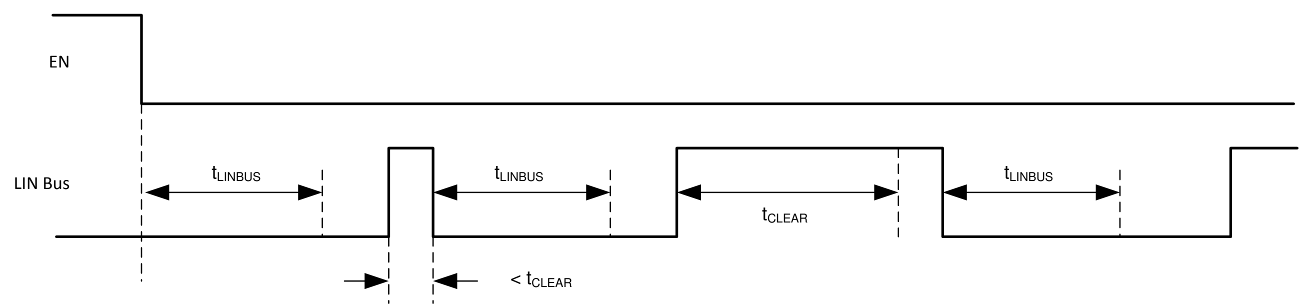


图 25. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wakeup

9.3.9.3 Thermal Shutdown

The LIN transmitter is protected by current limiting circuit; however, if the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state and turns off the V_{CC} regulator. The nRST pin is pulled to ground during a TSD event. Once the over-temperature fault condition has been removed and the virtual junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled. During this fault the device enters a TSD off mode. Once the junction temperature cools, the device enters standby mode as per the state diagram.

9.3.9.4 Under Voltage on V_{SUP}

The device contains a power-on reset circuit to avoid false bus messages during under voltage conditions when V_{SUP} is less than UV_{SUP}.

Feature Description (接下页)

9.3.9.5 Unpowered Device and LIN Bus

In automotive applications, some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remain powered by the battery. The device has extremely low unpowered leakage current from the bus, so an unpowered node does not affect the network or load it down.

9.4 Device Functional Modes

The TLIN1028S-Q1 has three functional modes of operation, normal, sleep, and standby. The next sections describes these modes as well as how the device moves between the different modes. 图 26 graphically shows the relationship while 表 1 shows the state of pins.

表 1. Operating Modes

Mode	EN	RXD	LIN BUS Termination	Transmitter	nRST	Comment
Sleep	Low	Floating	Weak Current pull-up	Off	Ground	nRST is internally connected to the LDO output which in sleep mode is pulled to ground
Standby Init	Low	Floating	45 kΩ (typical)	Off	Ramping	nRST is internally connected to the LDO output which in standby init mode is pulled low until VCC raises beyond UV_{CC} threshold.
Standby from SLP	Low	Low	45 kΩ (typical)	Off	V_{CC}	Wake up event detected, waiting on processors to set EN nRST comes on to V_{CC} once thresholds are met.
Standby from Norm	Low	High	45 kΩ (typical)	Off	V_{CC}	LDO is on and RXD is high
Normal	High	LIN Bus Data	45 kΩ (typical)	On	V_{CC}	LIN transmission up to 20 kbps
TSD Off	NA	Floating	45 kΩ (typical)	Off	Ground	nRST is pulled low as the LDO is turned off which means UV_{CC} threshold has been met.

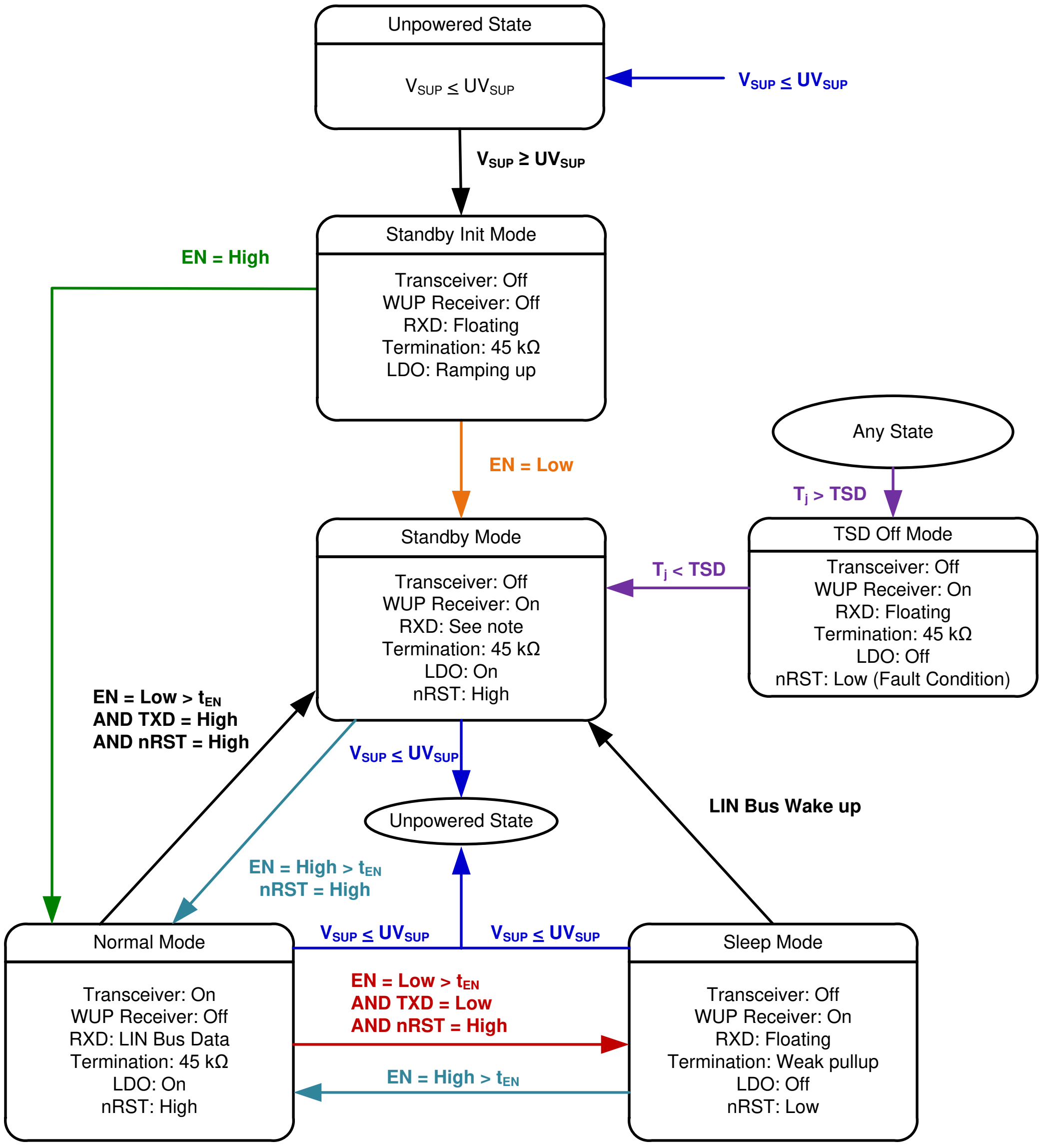


图 26. Operating State Diagram

注

- RXD is latched low due to a wake event from sleep mode once entering standby mode
- RXD is high when entering standby mode from other modes and is not latch low for a wake event

---

9.4.1 Normal Mode

If the EN pin is high after the device enters standby init mode it enters normal mode. If EN is low, it enters standby mode. In normal operational mode, the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a digital high and a dominant signal on the LIN bus is a digital low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high while the device is in sleep or standby mode for > t_{EN}. Once EN has been high for t_{EN} the device enters normal mode after t_{MODE_CHANGE} and $t_{NOMINIT}$ times.

9.4.2 Sleep Mode

Sleep Mode is the power saving mode for the TLIN1028S-Q1. Even with extremely low current consumption in this mode, the device can still wake up from the LIN bus through a wake-up signal or if EN is set high for > . The wake-up events must be active for the respective time periods (t_{LINBUS}).

While the device is in sleep mode, the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input and LIN wake up receiver are active.

9.4.3 Standby Mode

Standby mode is entered either by a wake up event through LIN bus while the device is in sleep mode or by the EN pin from normal or standby init modes. From normal mode EN must be low for > t_{EN} and TXD and nRST are high. RXD pin in standby mode is dependent upon how standby mode was entered. If entered from normal mode or power up, RXD is high. If entered from sleep mode, RXD is pulled low to indicate a wake event.

During power up, if EN is low the device goes into standby mode, and if EN is high, the device goes into normal mode. EN has an internal pull-down resistor ensuring EN is pulled low if the pin is left floating in the system.

9.4.4 Wake Up Events

There are ways to wake up from sleep mode:

- Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on the LIN bus where the dominant state is held for the t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake up event eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Local wake up through EN being set high for longer than .

9.4.4.1 Wake Up Request (RXD)

When the TLIN1028S-Q1 encounters a wake up event from the LIN bus, RXD goes low and the device transitions to standby mode until EN is reasserted high and the device enters normal mode. Once the device enters normal mode, the RXD pin releases the wake up request signal and the RXD pin then reflects the receiver output from the LIN bus.

9.4.5 Mode Transitions

When the device is transitioning between modes, the device needs the time t_{MODE_CHANGE} and t_{NOMINT} to allow the change to fully propagate from the EN pin through the device into the new state.

9.4.6 Voltage Regulator

The device has an integrated high-voltage LDO that operates over a 5.5 V to 28 V input voltage range for both 3.3 V and 5 V V_{CC}. The device has an output current capability of 70 mA and support fixed output voltages of 3.3 V (TLIN10283S-Q1) or 5 V (TLIN10285S-Q1). It features thermal shutdown and short-circuit protection to prevent damage during over-temperature and over-current conditions

9.4.6.1 V_{CC}

The V_{CC} pin is the regulated output based on the required voltage. The regulated voltage accuracy is ± 2%. The output is current limited. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UV_{SUP} threshold, the regulator shuts down until the input voltage returns above the UV_{SUPR} level. The device monitors situations where V_{CC} may drop below the UV_{CC} level thus causing the nRST pin to be pulled low.

9.4.6.2 Output Capacitance Selection

For stable operation over the full temperature range and with load currents up to 70 mA on V_{CC} a certain capacitance is expected and depends upon the minimum load current. To support no load to full load a value of 10 µF and ESR smaller than 2 Ω is needed. For 500 µA to full load an 1 µF capacitance can be used. The low ESR recommendation is to improve the load transient performance.

9.4.6.3 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (IL) and power switch resistor. This tracking allows for a smaller input capacitance and can possibly eliminate the need for a boost converter during cold-crank conditions.

9.4.6.4 Power Supply Recommendation

The device is designed to operate from an input-voltage supply range between 5.5 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device. The recommended minimum capacitance at the pin is 100 nF . The max voltage range is for the LIN functionality. Exceeding 24V for the LDO reduces the effective current sourcing capability due to thermal considerations.

10 Application and Implementation

注

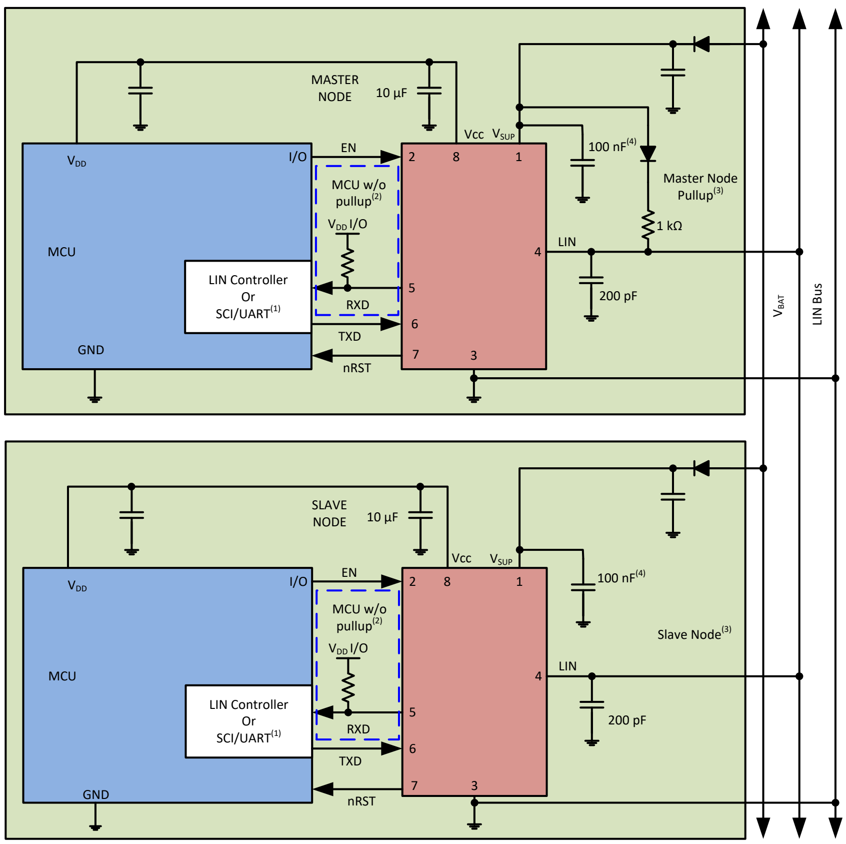
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TLIN1028S-Q1 can be used as both a slave device and a master device in a LIN network. The device comes with the ability to support a remote wake up requests. It can provide the power to the local processor.

10.2 Typical Application

The device comes with an integrated 45 kΩ pull-up resistor and series diode for slave applications. For master applications, an external 1 kΩ pull-up resistor with series blocking diode can be used. 图 27



(1) If RXD on MCU or LIN slave has internal pullup; no external pullup resistor is needed.
(2) If RXD on MCU or LIN slave does not have an internal pullup requires external pullup resistor.
(3) Master node applications require and external 1 kΩ pullup resistor and serial diode.
(4) Decoupling capacitor values are system dependent but usually have 100 nF, 1 µF and ≥10 µF

图 27. Typical LIN Bus

Typical Application (接下页)

10.2.1 Design Requirements

10.2.1.1 Normal Mode Application Note

When using the TLIN1028S-Q1 in systems which are monitoring the RXD pin for a wake up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake up request until t_{MODE_CHANGE}. This is shown in when transitioning to normal mode there is an initialization period shown as $t_{NOMINIT}$.

10.2.1.2 TXD Dominant State Timeout Application Note

The maximum dominant TXD time allowed by the TXD dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for master and slave applications; thus, there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

10.2.1.3 Brownout

图 35 and show the behavior of the LIN, nRST and V_{CC} pins during a brownout condition. For the TLIN10283S-Q1, V_{SUP} down to ~ 2.24 V has results as shown. For the TLIN10285S-Q1, V_{SUP} down to ~ 2.63 V has results as shown. When V_{SUP} drops below these levels the signals are indeterminate.

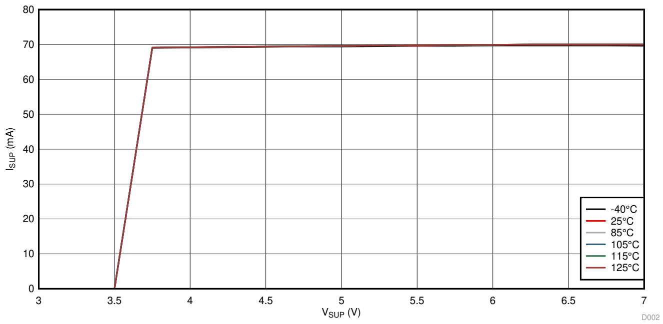
10.2.2 Detailed Design Procedures

RXD on processors or LIN slave has internal pull-up; no external pull-up resistor is need. RXD on processors or LIN slave without internal pull-up requires external pull-up resistor. Master node applications require and external 1 kΩ pull-up resistor and serial diode.

Typical Application (接下页)

10.2.3 Application Curves

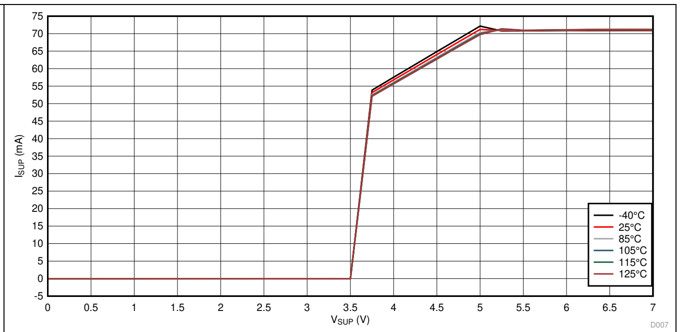
Characteristic curves below show the LDO performance ramping between 0 V and up to 7 V.



Package = D V_{CC} = 3.3 V   Temperature = Ambient

I_{CC} = 70 mA

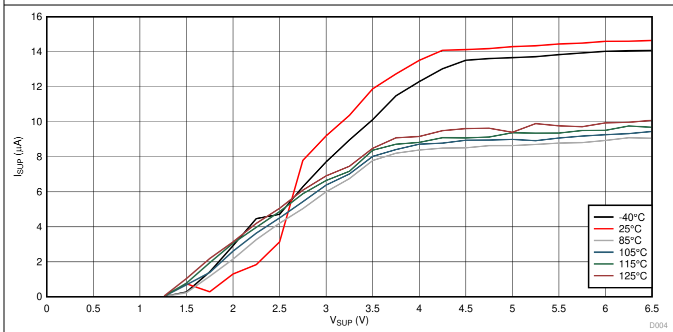
图 28. I_{SUP} vs V_{SUP} vs Temperature



Package = D V_{CC} = 5 V   Temperature = Ambient

I_{CC} = 70 mA

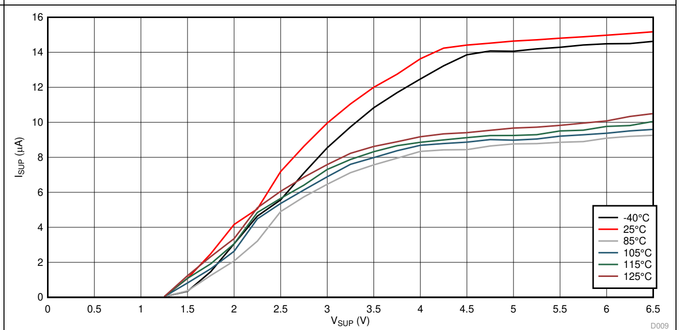
图 29. I_{SUP} vs V_{SUP} vs Temperature



Package = D   3.3 V V_{CC} = Off   Temperature = Ambient

Mode = Sleep

图 30. I_{SUP} vs V_{SUP} vs Temperature Ramp-down



Package = D   5 V V_{CC} = Off   Temperature = Ambient

Mode = Sleep

图 31. I_{SUP} vs V_{SUP} vs Temperature Ramp-down

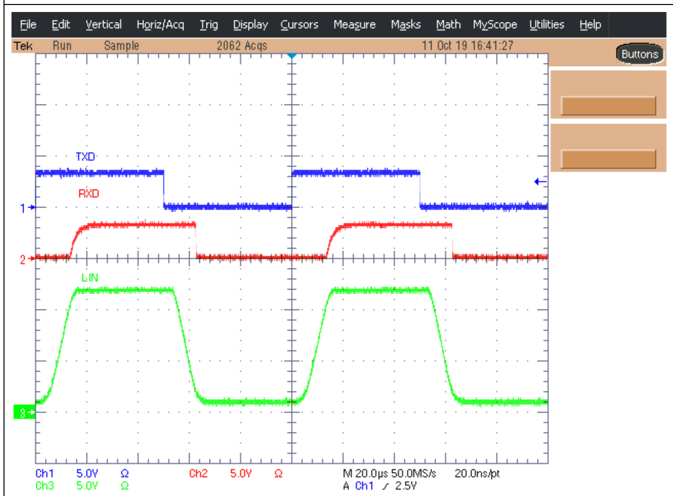


图 32. LIN Bus Performance

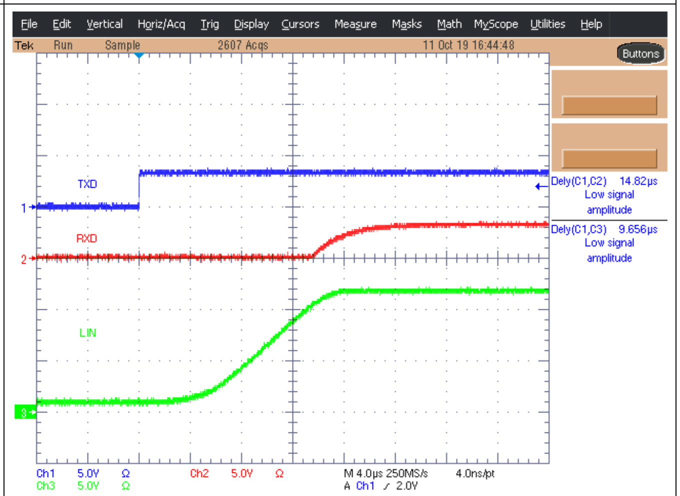


图 33. Dominant to Recessive Propagation Delay

Typical Application（接下页）

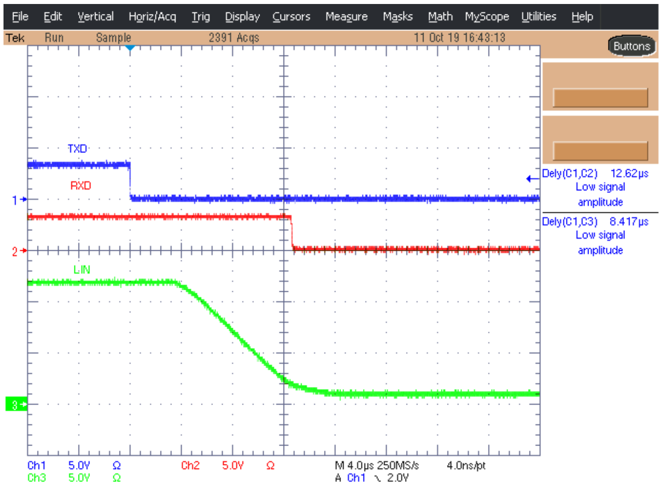


图 34. Recessive to Dominant Propagation Delay

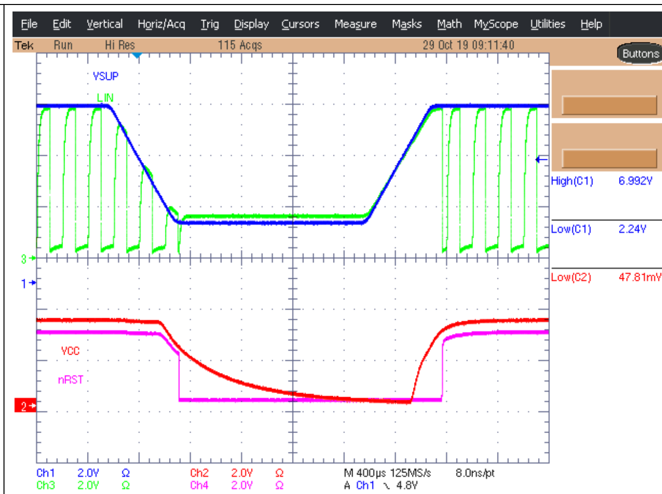


图 35. TLIN10283S-Q1 Brownout

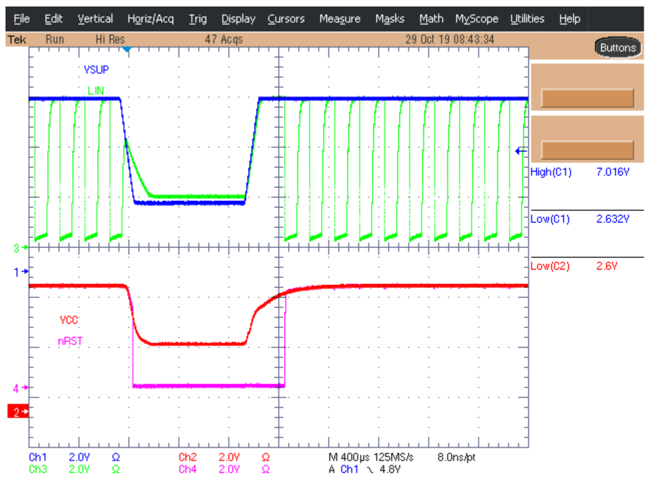


图 36. TLIN10285S-Q1 Brownout

11 Power Supply Recommendations

The TLIN1028S-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 5.5 V to 28 V . A 100 nF decoupling capacitor should be placed as close to the V_{SUP} pin of the device as possible.

12 Layout

PCB design should start with understanding that frequency bandwidth from approximately 3 MHz to 3 GHz is needed thus high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

12.1 Layout Guidelines

- **Pin 1 (V_{SUP}):** This is the supply pin for the device. A 100 nF decoupling capacitor should be placed as close to the device as possible.
- **Pin 2 (EN):** EN is an input pin that is used to place the device in a low power sleep mode. If this feature is not used, the pin should be pulled high to the regulated voltage supply of the microprocessor through a series resistor, values between 1 kΩ and 10 kΩ. Additionally, a series resistor may be placed on the pin to limit current on the digital lines in the event of an over voltage fault.
- **Pin 3 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 4 (LIN):** This pin connects to the LIN bus. For slave applications, a 200 pF capacitor to ground is implemented. For master applications, an additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin. See 图 27
- **Pin 5 (RXD):** The pin is an open drain output and requires and external pull-up resistor in the range of 1 kΩ to 10 kΩ to function properly. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external pull-up resistor should be placed on RXD. If RXD is connected to the V_{CC} pin a higher pull-up resistor value can be used to reduce standby current.
- **Pin 6 (TXD):** The TXD pin is the transmit input signal to the device from the processors. A series resistor can be placed to limit the input current to the device in the event of an over voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 7 (nRST):** This pin connects to the processors as a reset out.
- **Pin 8 (V_{CC}):** Output source, either 3.3 V or 5 V depending upon the version of the device.

注

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

12.2 Layout Example

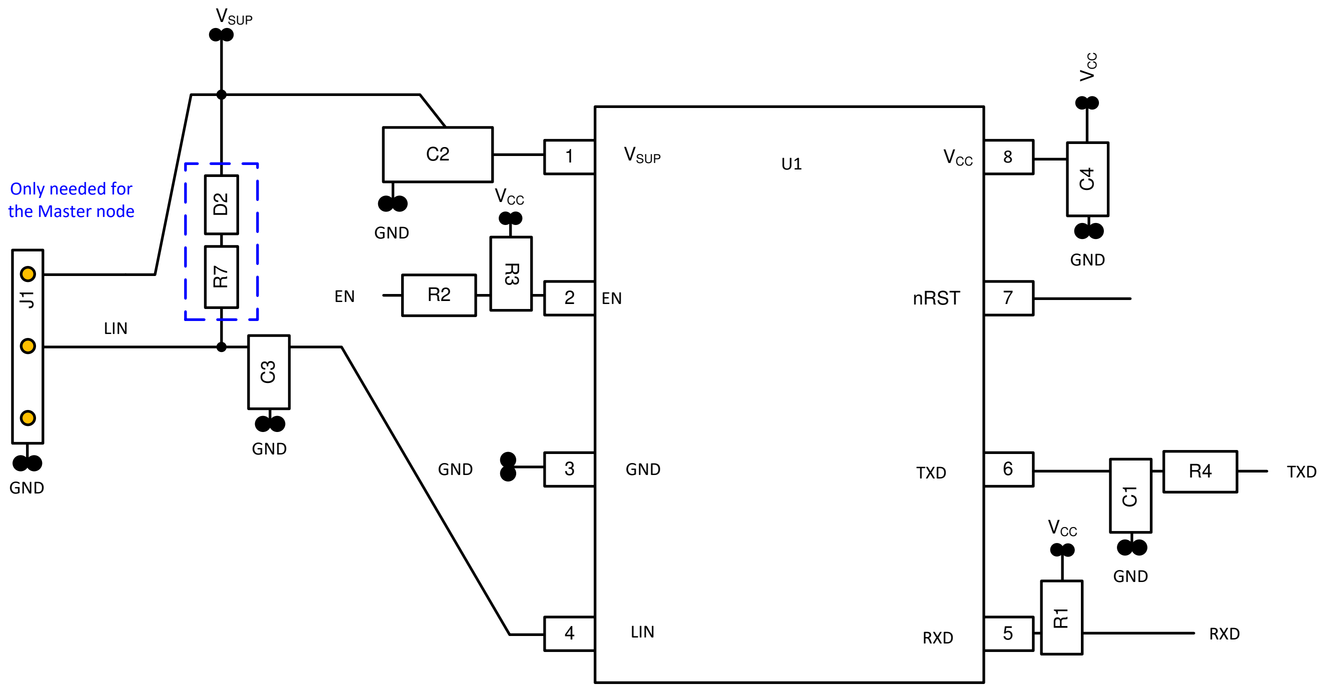


图 37. Layout Example

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

请参阅如下相关文档：

LIN 标准：

- ISO/DIS 17987-1.2：道路车辆 - 局域互联网络 (LIN) - 第 1 部分：一般信息和用例定义
- ISO/DIS 17987-4.2：道路车辆 - 局域互联网络 (LIN) - 第 4 部分：电气物理层规格 (EPL) 12V/24V
- SAE J2602-1：车用 LIN 网络 应用
- LIN2.0、LIN2.1、LIN2.2 和 LIN2.2A 规格

EMC 要求：

- SAE J2962-2：TBD
- CAN、LIN、FR V1.3 的硬件要求：德国对 LIN 的 OEM 要求
- ISO 10605：道路车辆 - 静电放电引起的电干扰的试验方法
- ISO 11452-4:2011：道路车辆 - 窄带辐射电磁能量的电子干扰组件试验方法 - 第 4 部分：线束激励方法
- ISO 7637-1:2015：道路车辆 - 传导和耦合造成的电干扰 - 第 1 部分：定义和一般描述
- ISO 7637-3：道路车辆 - 由传导和耦合引起的电干扰 - 第 3 部分：通过电容耦合和电感耦合经由非电源线线路的瞬间电传输
- IEC 62132-4:2006：集成电路 - 150kHz - 1GHz 电磁抗扰度的测量 - 第 4 部分：直接射频功率注入法
- IEC 61967-4
- CISPR25

符合性测试要求：

- ISO/DIS 17987-7.2：道路车辆 - 局域互联网络 (LIN) - 第 7 部分：电气物理层 (EPL) 符合性测试规格
- SAE J2602-2：车用 LIN 网络 网络 符合性测试

TLINx441 LDO 性能，SLLA427

13.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 商标

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13.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLIN10283SDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL083	Samples
TLIN10285SDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL085	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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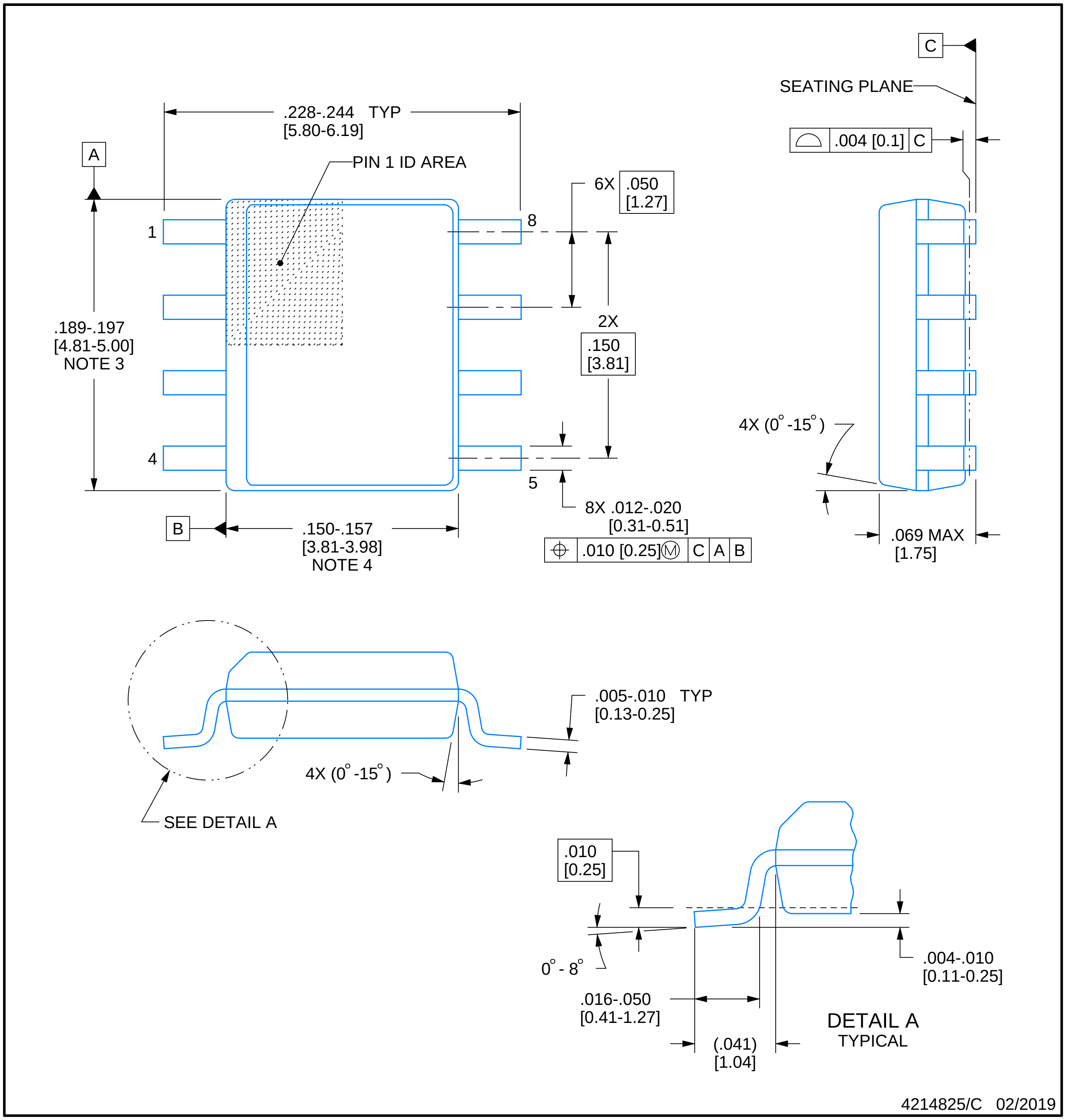
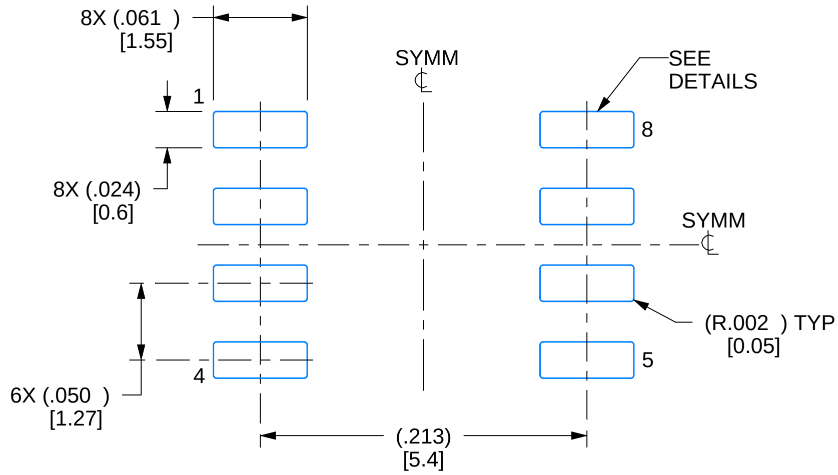
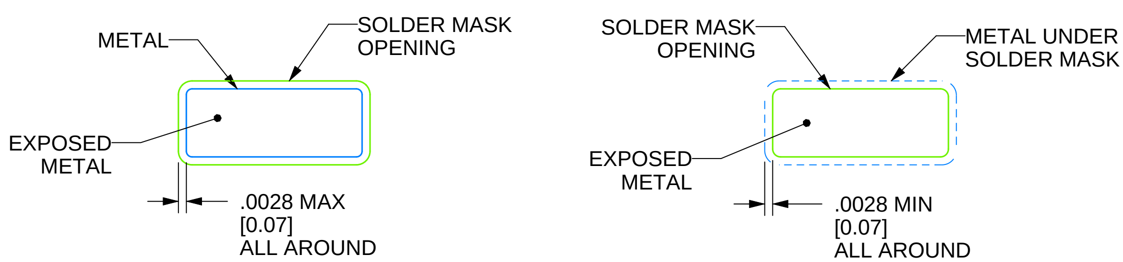


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

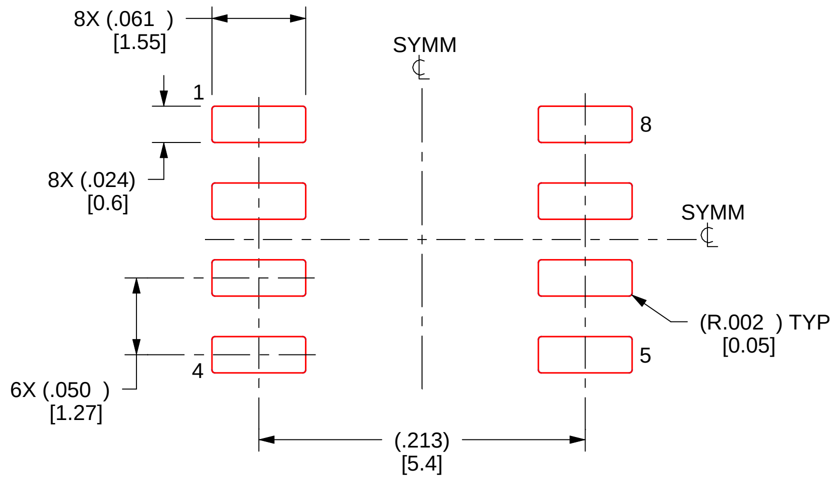
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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