

# UCC5350-Q1 Single-Channel Isolated Gate Driver for SiC/IGBT and Automotive Applications

## 1 Features

- 5-kV<sub>RMS</sub> and 3-kV<sub>RMS</sub> single-channel isolated gate driver
- AEC-Q100 qualified for automotive applications
  - Temperature grade 1
  - HBM ESD classification level H2
  - CDM ESD classification level C6
- $\pm 5$ -A minimum peak current drive strength
- 3-V to 15-V input supply voltage
- Up to 33-V driver supply voltage
- 100-V/ns minimum CMTI
- Negative 5-V handling capability on input pins
- 100-ns (maximum) propagation delay and <25ns part-to-part skew
- 12-V UVLO
- 8-pin DWV (8.5mm creepage) and D (4-mm creepage) packages
- Isolation barrier life > 40 Years
- Safety-related certifications:
  - 7000-V<sub>PK</sub> isolation DWV and 4242-V<sub>PK</sub> isolation D per DIN V VDE V 0884-11:2017-01 and DIN EN 61010-1 (planned)
  - 5000-V<sub>RMS</sub> DWV and 3000-V<sub>RMS</sub> D isolation rating for 1 minute per UL 1577 (planned)
  - CQC certification per GB4943.1-2011 D and DWV (planned)
- CMOS inputs
- Operating junction temperature: –40°C to +150°C

## 2 Applications

- On-board charger
- Traction inverter for EVs
- DC charging stations
- HVAC
- Heaters

## 3 Description

The UCC5350-Q1 is a single-channel, isolated gate driver with 5-A source and 5-A sink minimum peak current designed to drive MOSFETs, IGBTs, and SiC MOSFETs. The UCC5350-Q1 has a CLAMP pin to connect the transistor gate to an internal clamp to prevent false turn-on caused by Miller current.

The UCC5350-Q1 is available in a 4 mm SOIC-8 (D) or 8.5 mm wide body SOIC-8 (DWV) package and can support isolation voltage up to 3-kV<sub>RMS</sub> and 5-kV<sub>RMS</sub>, respectively. The input side is isolated from the output side with SiO<sub>2</sub> capacitive isolation technology with longer than 40 years isolation barrier lifetime. The UCC5350-Q1 is a good fit for driving IGBTs or MOSFETs in applications such as high-voltage traction inverters and on-board chargers.

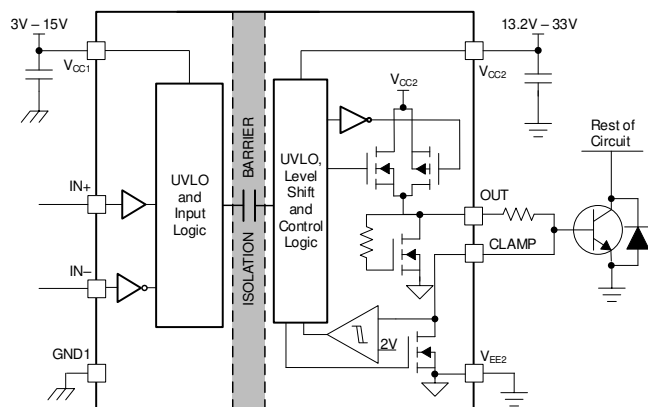
Compared to an optocoupler, the UCC5350-Q1 has lower part-to-part skew, lower propagation delay, higher operating temperature, and higher CMTI.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC5350-Q1	DWV SOIC-8	7.5 mm x 5.85 mm
	D SOIC-8	3.91 mm x 4.9 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Functional Block Diagram



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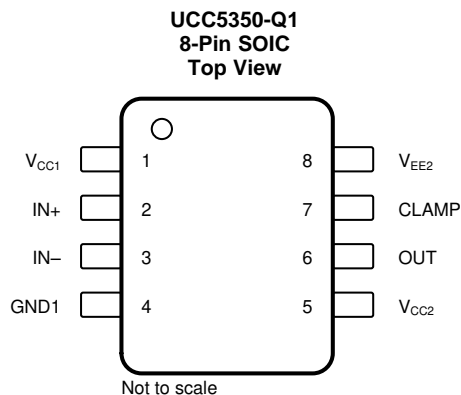
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2020) to Revision B	Page
• Changed marketing status from Advance Information to initial release.	1

## 5 Pin Configuration and Function



**Pin Functions**

PIN		TYPE	DESCRIPTION
NAME	NO.		
CLAMP	7	I	Active Miller-clamp input used to prevent false turn-on of the power switches.
GND1	4	G	Input ground. All signals on the input side are referenced to this ground.
IN+	2	I	Noninverting gate-drive voltage-control input. The IN+ pin has a CMOS input threshold. This pin is pulled low internally if left open. Use <a href="#">Table 4</a> to understand the input and output logic of these devices.
IN–	3	I	Inverting gate-drive voltage control input. The IN– pin has a CMOS input threshold. This pin is pulled high internally if left open. Use <a href="#">Table 4</a> to understand the input and output logic of these devices.
OUT	6	O	Gate-drive output
V <sub>CC1</sub>	1	P	Input supply voltage. Connect a locally decoupled capacitor to GND1. Use a low-ESR or ESL capacitor located as close to the device as possible.
V <sub>CC2</sub>	5	P	Positive output supply rail. Connect a locally decoupled capacitor to V <sub>EE2</sub> . Use a low-ESR or ESL capacitor located as close to the device as possible.
V <sub>EE2</sub>	8	G	Ground pin. Connect to MOSFET source or IGBT emitter. Connect a locally decoupled capacitor from V <sub>CC2</sub> to V <sub>EE2</sub> . Use a low-ESR or ESL capacitor located as close to the device as possible.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input bias pin supply voltage	$V_{CC1} - \text{GND1}$	GND1 – 0.3	18	V
Driver bias supply	$V_{CC2} - V_{EE2}$	–0.3	35	V
Output signal voltage	$V_{OUT} - V_{EE2}$ , $V_{CLAMP} - V_{EE2}$	$V_{EE2} - 0.3$	$V_{CC2} + 0.3$	V
Input signal voltage	$V_{IN+} - \text{GND1}$ , $V_{IN-} - \text{GND1}$	GND1 – 5	$V_{CC1} + 0.3$	V
Junction temperature, $T_J$ <sup>(2)</sup>		–40	150	°C
Storage temperature, $T_{stg}$		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) To maintain the recommended operating conditions for  $T_J$ , see the [Thermal Information](#).

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000
		Charged-device model (CDM), per AEC Q100-011	±1500

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CC1}$	Supply voltage, input side	3		15	V
$V_{CC2}$	Positive supply voltage output side ( $V_{CC2} - V_{EE2}$ )	13.2		33	V
$T_J$	Junction Temperature	–40		150	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		UCC5350-Q1		UNIT
		D (SOIC)	DWV (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.5	119.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.1	64.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	65.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	18.3	37.6	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	50.7	63.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D Package						
P <sub>D</sub>	Maximum power dissipation on input and output	V <sub>CC1</sub> = 15 V, V <sub>CC2</sub> = 15 V, f = 2.1-MHz, 50% duty cycle, square wave, 2.2-nF load			1.14	W
P <sub>D1</sub>	Maximum input power dissipation				0.05	W
P <sub>D2</sub>	Maximum output power dissipation				1.09	W
DWV Package						
P <sub>D</sub>	Maximum power dissipation on input and output	V <sub>CC1</sub> = 15 V, V <sub>CC2</sub> = 15 V, f = 1.9-MHz, 50% duty cycle, square wave, 2.2-nF load			1.04	W
P <sub>D1</sub>	Maximum input power dissipation				0.05	W
P <sub>D2</sub>	Maximum output power dissipation				0.99	W

## 6.6 Insulation Specifications for D Package

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			D	
CLR	External Clearance <sup>(1)</sup>	Shortest pin-to-pin distance through air	$\geq 4$	mm
CPG	External Creepage <sup>(1)</sup>	Shortest pin-to-pin distance across the package surface	$\geq 4$	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	$> 21$	$\mu\text{m}$
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	$> 600$	V
	Material Group	According to IEC 60664-1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage $\leq 150 \text{ V}_{\text{RMS}}$	I-IV	
		Rated mains voltage $\leq 300 \text{ V}_{\text{RMS}}$	I-III	
<b>DIN V VDE 0884-11: 2017-01<sup>(2)</sup></b>				
$V_{\text{IORM}}$	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	990	$V_{\text{PK}}$
$V_{\text{IOWM}}$	Maximum isolation working voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDb) test	700	$V_{\text{RMS}}$
$V_{\text{IOTM}}$	Maximum transient isolation voltage	$V_{\text{TEST}} = V_{\text{IOTM}}$ , $t = 60 \text{ s}$ (qualification); $V_{\text{TEST}} = 1.2 \times V_{\text{IOTM}}$ , $t = 1 \text{ s}$ (100% production)	4242	$V_{\text{PK}}$
$V_{\text{IOSM}}$	Maximum surge isolation voltage <sup>(3)</sup>	Test method per IEC 62368-1, 1.2/50- $\mu\text{s}$ waveform, $V_{\text{TEST}} = 1.3 \times V_{\text{IOSM}}$ (qualification)	4242	$V_{\text{PK}}$
$q_{\text{pd}}$	Apparent charge <sup>(4)</sup>	Method a: After I/O safety test subgroup 2/3, $V_{\text{ini}} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60 \text{ s}$ $V_{\text{pd(m)}} = 1.2 \times V_{\text{IORM}}$ , $t_{\text{m}} = 10 \text{ s}$	$\leq 5$	pC
		Method a: After environmental tests subgroup 1, $V_{\text{ini}} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60 \text{ s}$ ; $V_{\text{pd(m)}} = 1.2 \times V_{\text{IORM}}$ , $t_{\text{m}} = 10 \text{ s}$	$\leq 5$	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{\text{ini}} = 1.2 \times V_{\text{IOTM}}$ , $t_{\text{ini}} = 1 \text{ s}$ ; $V_{\text{pd(m)}} = 1.5 \times V_{\text{IORM}}$ , $t_{\text{m}} = 1 \text{ s}$	$\leq 5$	
$C_{\text{IO}}$	Barrier capacitance, input to output <sup>(5)</sup>	$V_{\text{IO}} = 0.4 \times \sin(2\pi ft)$ , $f = 1 \text{ MHz}$	1.2	pF
$R_{\text{IO}}$	Isolation resistance, input to output <sup>(5)</sup>	$V_{\text{IO}} = 500 \text{ V}$ , $T_{\text{A}} = 25^{\circ}\text{C}$	$> 10^{12}$	$\Omega$
		$V_{\text{IO}} = 500 \text{ V}$ , $100^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$	$> 10^{11}$	
		$V_{\text{IO}} = 500 \text{ V}$ at $T_{\text{S}} = 150^{\circ}\text{C}$	$> 10^9$	
	Pollution degree		2	
	Climatic category		40/125/21	
<b>UL 1577</b>				
$V_{\text{ISO}}$	Withstand isolation voltage	$V_{\text{TEST}} = V_{\text{ISO}}$ , $t = 60 \text{ s}$ (qualification); $V_{\text{TEST}} = 1.2 \times V_{\text{ISO}}$ , $t = 1 \text{ s}$ (100% production)	3000	$V_{\text{RMS}}$

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-pin device.

## 6.7 Insulation Specifications for DWV Package

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DWV	
CLR	External Clearance <sup>(1)</sup>	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External Creepage <sup>(1)</sup>	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303–11); IEC 60112	> 600	V
Material Group		According to IEC 60664–1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 600 <sub>VRMS</sub>	I-III	
		Rated mains voltage ≤ 1000 <sub>VRMS</sub>	I-II	
DIN V VDE 0884–11: 2017–01 <sup>(2)</sup>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum isolation working voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDb) test	1500	V <sub>RMS</sub>
		DC Voltage	2121	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification) ; V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production)	7000	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	Test method per IEC 62368-1, 1.2/50-μs waveform, V <sub>TEST</sub> = 1.6 × V <sub>IOSM</sub> (qualification)	8000	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(4)</sup>	Method a: After I/O safety test subgroup 2/3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), V <sub>ini</sub> = 1.2 × V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s; V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> , t <sub>m</sub> = 1 s	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.4 × sin (2πft), f = 1 MHz	1.2	pF
R <sub>IO</sub>	Isolation resistance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	
Pollution degree			2	
Climatic category			40/125/21	
UL 1577				
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60 s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> , t = 1 s (100% production)	5000	V <sub>RMS</sub>

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-pin device.

## 6.8 Safety-Related Certifications For D Package

VDE	UL	CQC
Certified according to DIN V VDE V 0884–11:2017–01 and DIN EN 61010-1 (VDE 0411-1):2011-07	Planned Component Recognition	Plan to certify according to GB 4943.1–2011
Basic Insulation Maximum Transient Isolation Overvoltage, 4242 V <sub>PK</sub> ; Maximum Repetitive Peak Voltage, 990 V <sub>PK</sub> ; Maximum Surge Isolation Voltage, 4242 V <sub>PK</sub>	Single protection, 3000 V <sub>RMS</sub>	Basic Insulation, Altitude ≤ 5000m, Tropical Climate, 700 V <sub>RMS</sub> Maximum Working Voltage
Certification Planned	Certification Planned	Certification Planned

## 6.9 Safety-Related Certifications For DWV Package

VDE	UL	CQC
Plan to certify according to DIN V VDE V 0884–11:2017–01 and DIN EN 61010-1	Planned Component Recognition	Plan to certify according to GB 4943.1–2011
Reinforced Insulation Maximum Transient Isolation Overvoltage, 7000 V <sub>PK</sub> ; Maximum Repetitive Peak Isolation Voltage, 2121 V <sub>PK</sub> ; Maximum Surge Isolation Voltage, 8000 V <sub>PK</sub>	Single protection, 5000 V <sub>RMS</sub>	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate
Certification planned	Certification planned	Certification planned

## 6.10 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>D PACKAGE</b>					
I <sub>S</sub> Safety output supply current	R <sub>θJA</sub> = 109.5°C/W, V <sub>CC2</sub> = 15 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 2</a>			73	mA
	R <sub>θJA</sub> = 109.5°C/W, V <sub>CC2</sub> = 30 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 2</a>			36	
P <sub>S</sub> Safety output supply power	R <sub>θJA</sub> = 109.5°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 4</a>	Input side		0.05	W
		Output side		1.09	
		Total		1.14	
T <sub>S</sub> Maximum safety temperature <sup>(1)</sup>				150	°C
<b>DWV PACKAGE</b>					
I <sub>S</sub> Safety input, output, or supply current	R <sub>θJA</sub> = 119.8°C/W, V <sub>I</sub> = 15 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 1</a>	Output side		66	mA
	R <sub>θJA</sub> = 119.8°C/W, V <sub>I</sub> = 30 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 1</a>	Output side		33	
P <sub>S</sub> Safety input, output, or total power	R <sub>θJA</sub> = 119.8°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 3</a>	Input side		0.05	W
		Output side		0.99	
		Total		1.04	
T <sub>S</sub> Maximum safety temperature <sup>(1)</sup>				150	°C

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$$T_J = T_A + R_{\theta JA} \times P, \text{ where } P \text{ is the power dissipated in the device.}$$

$$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S, \text{ where } T_{J(max)} \text{ is the maximum allowed junction temperature.}$$

$$P_S = I_S \times V_I, \text{ where } V_I \text{ is the maximum input voltage.}$$



## 6.11 Electrical Characteristics

$V_{CC1} = 3.3\text{ V}$  or  $5\text{ V}$ ,  $0.1\text{-}\mu\text{F}$  capacitor from  $V_{CC1}$  to GND1,  $V_{CC2} = 15\text{ V}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_L = 100\text{-pF}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I <sub>VCC1</sub>	Input supply quiescent current			1.67	2.4	mA
I <sub>VCC2</sub>	Output supply quiescent current			1.1	1.8	mA
SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V <sub>IT+(UVLO1)</sub>	VCC1 Positive-going UVLO threshold voltage			2.6	2.8	V
V <sub>IT– (UVLO1)</sub>	VCC1 Negative-going UVLO threshold voltage		2.4	2.5		V
V <sub>hys(UVLO1)</sub>	VCC1 UVLO threshold hysteresis			0.1		V
OUTPUT SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V <sub>IT+(UVLO2)</sub>	VCC2 Positive-going UVLO threshold voltage			12	13	V
V <sub>IT–(UVLO2)</sub>	VCC2 Negative-going UVLO threshold voltage		10.3	11		V
V <sub>hys(UVLO2)</sub>	VCC2 UVLO threshold voltage hysteresis			1		V
LOGIC I/O						
V <sub>IT+(IN)</sub>	Positive-going input threshold voltage (IN+, IN–)			0.55 × V <sub>CC1</sub>	0.7 × V <sub>CC1</sub>	V
V <sub>IT–(IN)</sub>	Negative-going input threshold voltage (IN+, IN–)		0.3 × V <sub>CC1</sub>	0.45 × V <sub>CC1</sub>		V
V <sub>hys(IN)</sub>	Input hysteresis voltage (IN+, IN–)			0.1 × V <sub>CC1</sub>		V
I <sub>IH</sub>	High-level input leakage at IN+	IN+ = V <sub>CC1</sub>		40	240	μA
I <sub>IL</sub>	Low-level input leakage at IN–	IN– = GND1	–240	–40		μA
		IN– = GND1 – 5 V	–310	–80		
GATE DRIVER STAGE						
V <sub>OH</sub>	High-level output voltage (OUT)	I <sub>OUT</sub> = –20 mA		100	240	mV
V <sub>OL</sub>	Low level output voltage (OUT)	IN+ = low, IN– = high; I <sub>O</sub> = 20 mA		5	7	mV
I <sub>OH</sub>	Peak source current	IN+ = high, IN– = low		5	10	A
I <sub>OL</sub>	Peak sink current	IN+ = low, IN– = high		5	10	A
Active Miller Clamp						
V <sub>CLAMP</sub>	Low-level clamp voltage	I <sub>CLAMP</sub> = 20mA		7	10	mV
I <sub>CLAMP</sub>	Clamp low-level current	V <sub>CLAMP</sub> = V <sub>EE2</sub> + 15 V	5	10		A
I <sub>CLAMP(L)</sub>	Clamp low-level current for low output voltage	V <sub>CLAMP</sub> = V <sub>EE2</sub> + 2 V	5	10		A
V <sub>CLAMP-TH</sub>	Clamp threshold voltage			2.1	2.3	V
SHORT CIRCUIT CLAMPING						
V <sub>CLP-OUT</sub>	Clamping voltage (V <sub>OUT</sub> – V <sub>CC2</sub> )	IN+ = high, IN– = low, t <sub>CLAMP</sub> = 10 μs, I <sub>OUT</sub> = 500 mA		1	1.3	V
V <sub>CLP-OUT</sub>	Clamping voltage ( V <sub>EE2</sub> – V <sub>OUT</sub> )	IN+ = low, IN– = high, t <sub>CLAMP</sub> = 10 μs, I <sub>OUT</sub> = –500 mA		1.5		V
		IN+ = low, IN– = high, I <sub>OUT</sub> = –20 mA		0.9	1	
ACTIVE PULLDOWN						
V <sub>OUTSD</sub>	Active pulldown voltage on OUT	I <sub>OUT</sub> = 0.1 × I <sub>OUT(typ)</sub> , V <sub>CC2</sub> = open		1.8	2.5	V

## 6.12 Switching Characteristics

$V_{CC1}$  = 3.3 V or 5 V, 0.1- $\mu$ F capacitor from  $V_{CC1}$  to GND1,  $V_{CC2}$  = 15 V, 1- $\mu$ F capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $T_J$  =  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	Output-signal rise time		10	26	ns
$t_f$	Output-signal fall time		10	22	ns
$t_{PLH}$	Propagation delay, high		65	100	ns
$t_{PHL}$	Propagation delay, low		65	100	ns
$t_{UVLO1\_rec}$	UVLO recovery delay of $V_{CC1}$		30		$\mu$ s
$t_{UVLO2\_rec}$	UVLO recovery delay of $V_{CC2}$		50		$\mu$ s
$t_{PWD}$	Pulse width distortion $ t_{PHL} - t_{PLH} $		1	20	ns
$t_{sk(pp)}$	Part-to-part skew		1	25	ns
CMTI	Common-mode transient immunity	PWM is tied to GND or $V_{CC1}$ , $V_{CM}$ = 1200 V	100	120	kV/ $\mu$ s

## 6.13 Insulation Characteristics Curves

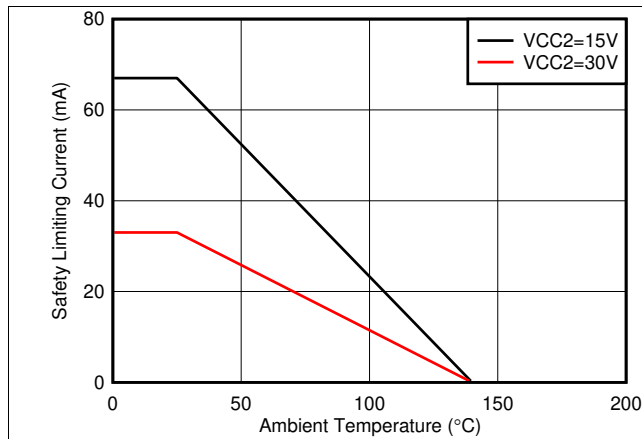


Figure 1. Thermal Derating Curve for Limiting Current per VDE for DWV Package

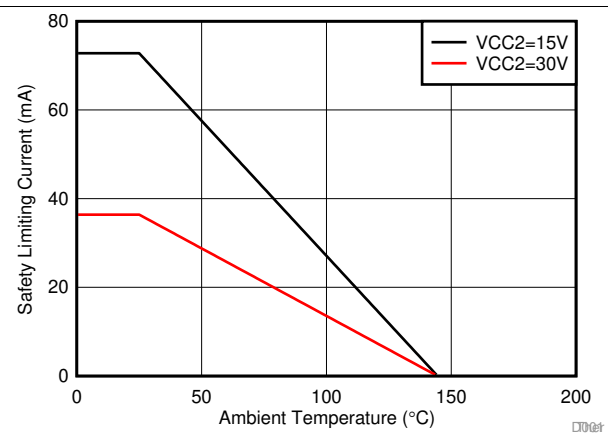


Figure 2. Thermal Derating Curve for Limiting Current per VDE for D Package

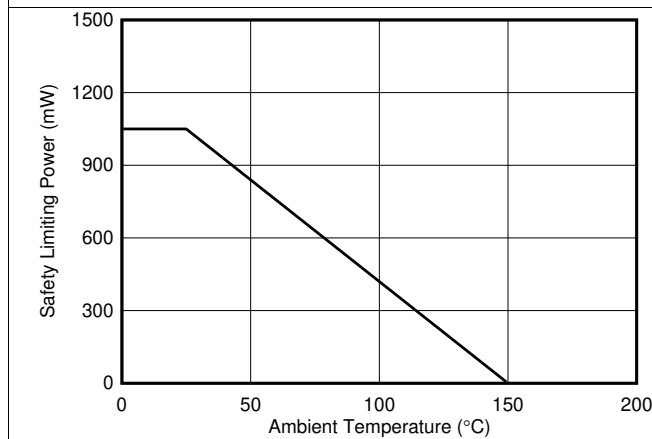


Figure 3. Thermal Derating Curve for Limiting Power per VDE for DWV Package

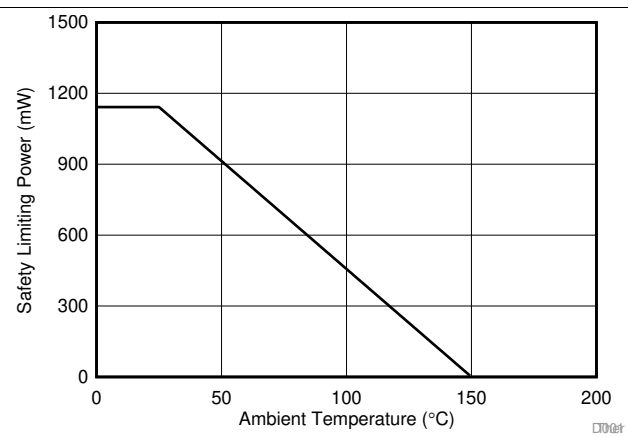
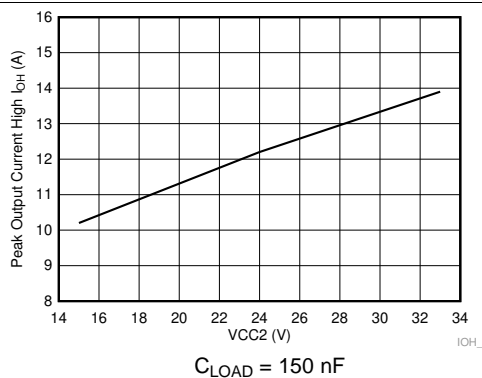


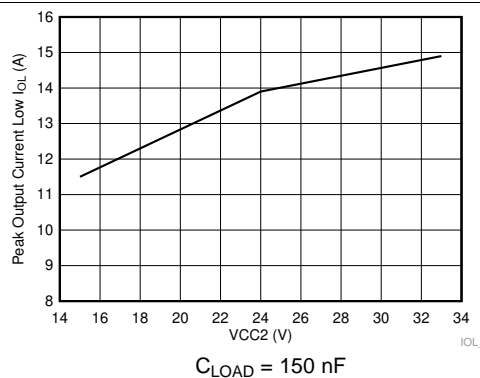
Figure 4. Thermal Derating Curve for Limiting Power per VDE for D Package

## 6.14 Typical Characteristics

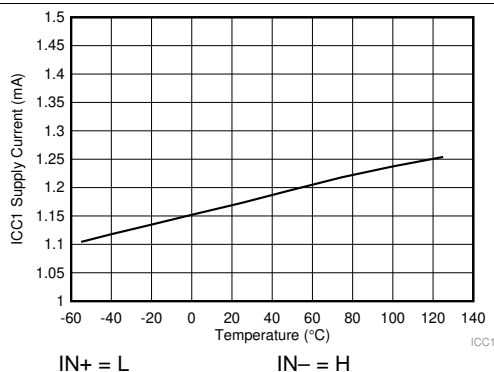
$V_{CC1} = 3.3\text{ V}$  or  $5\text{ V}$ ,  $0.1\text{-}\mu\text{F}$  capacitor from  $V_{CC1}$  to  $\text{GND1}$ ,  $V_{CC2} = 15\text{ V}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_{\text{LOAD}} = 1\text{ nF}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , (unless otherwise noted)



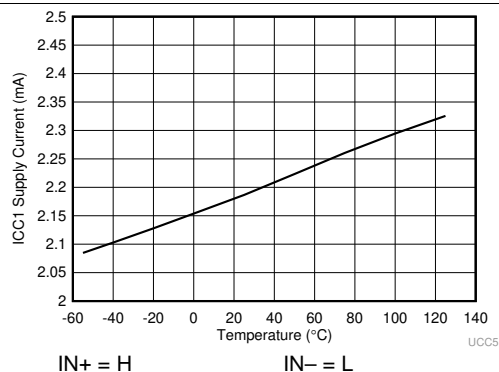
**Figure 5. Output-High Drive Current vs Output Voltage**



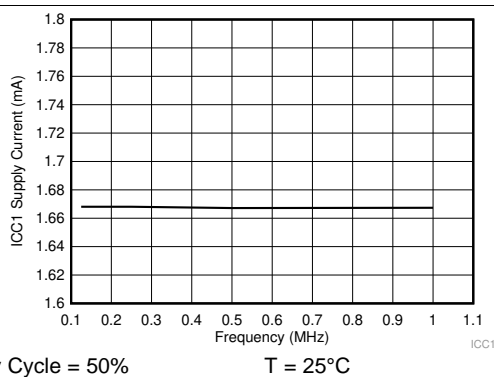
**Figure 6. Output-Low Drive Current vs Output Voltage**



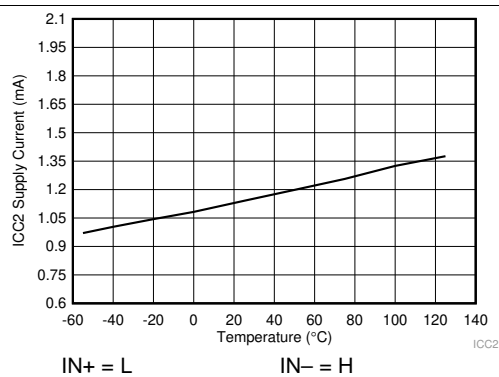
**Figure 7. I<sub>CC1</sub> Supply Current vs Temperature**



**Figure 8. I<sub>CC1</sub> Supply Current vs Temperature**



**Figure 9. I<sub>CC1</sub> Supply Current vs Input Frequency**



**Figure 10. I<sub>CC2</sub> Supply Current vs Temperature**

## Typical Characteristics (continued)

$V_{CC1} = 3.3\text{ V}$  or  $5\text{ V}$ ,  $0.1\text{-}\mu\text{F}$  capacitor from  $V_{CC1}$  to GND1,  $V_{CC2} = 15\text{ V}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_{LOAD} = 1\text{ nF}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , (unless otherwise noted)

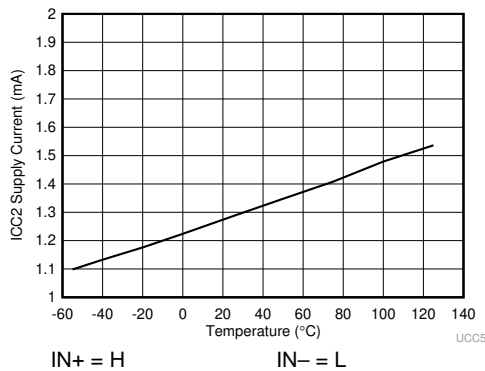


Figure 11.  $I_{CC2}$  Supply Current vs Temperature

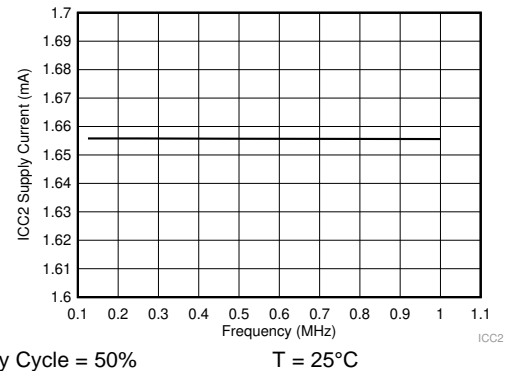


Figure 12.  $I_{CC2}$  Supply Current vs Input Frequency

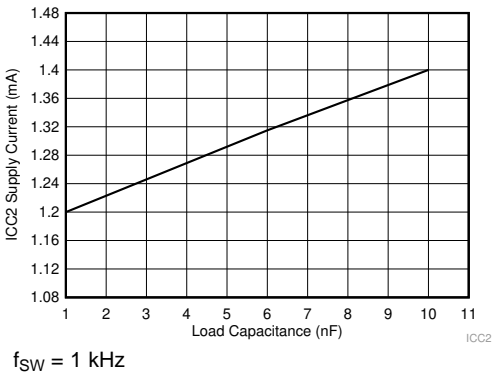


Figure 13.  $I_{CC2}$  Supply Current vs Load Capacitance

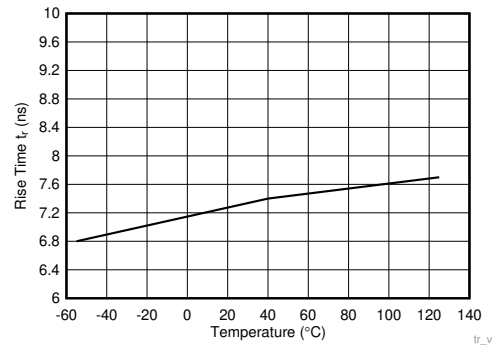


Figure 14. Rise Time vs Temperature

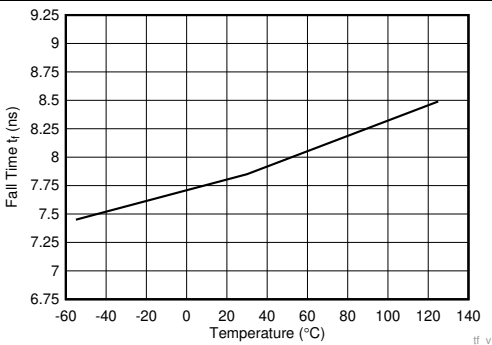


Figure 15. Fall Time vs Temperature

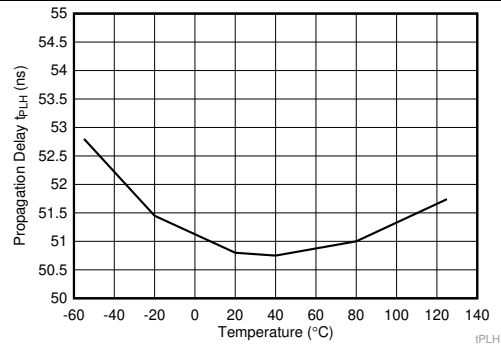
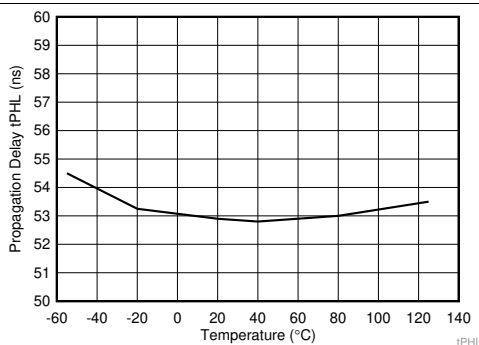


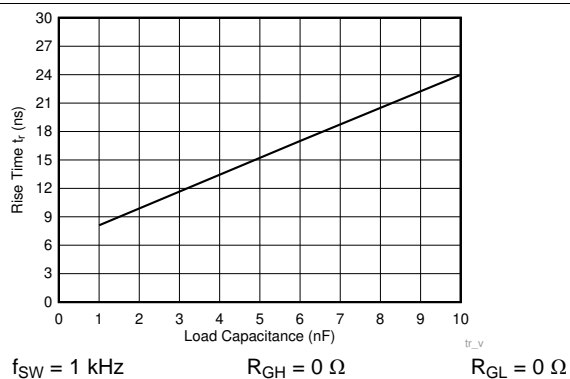
Figure 16. Propagation Delay  $t_{PLH}$  vs Temperature

## Typical Characteristics (continued)

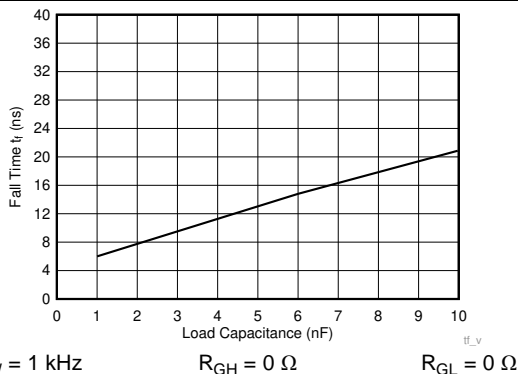
$V_{CC1} = 3.3\text{ V}$  or  $5\text{ V}$ ,  $0.1\text{-}\mu\text{F}$  capacitor from  $V_{CC1}$  to GND1,  $V_{CC2} = 15\text{ V}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_{LOAD} = 1\text{ nF}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , (unless otherwise noted)



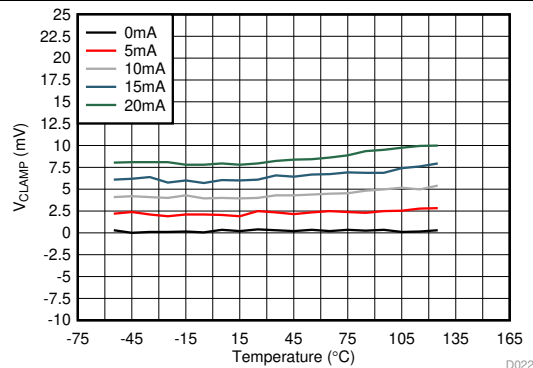
**Figure 17. Propagation Delay  $t_{PHL}$  vs Temperature**



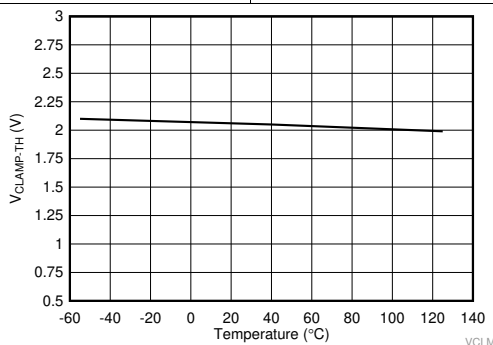
**Figure 18. Rise Time vs Load Capacitance**



**Figure 19. Fall Time vs Load Capacitance**



**Figure 20.  $V_{CLAMP}$  vs Temperature**

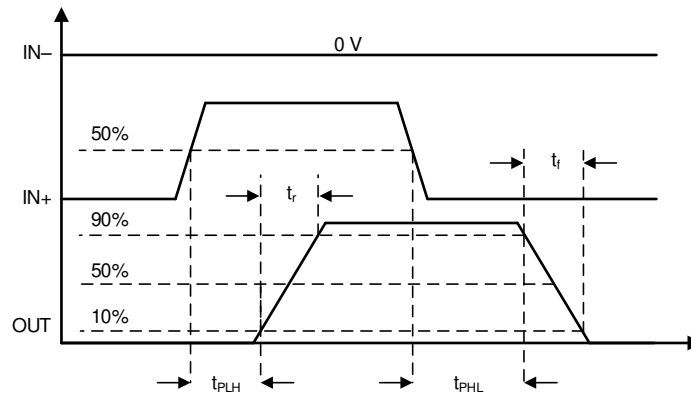


**Figure 21.  $V_{CLAMP-TH}$  vs Temperature**

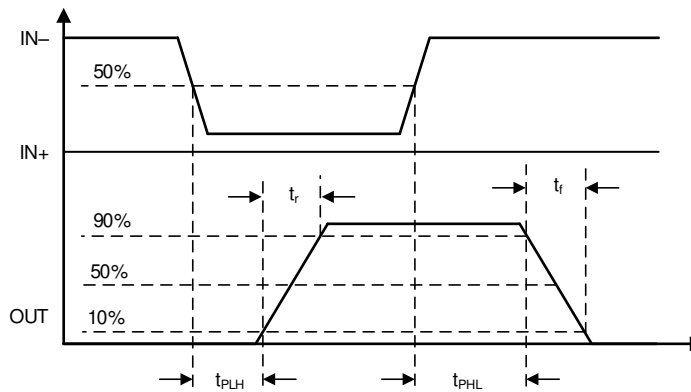
## 7 Parameter Measurement Information

### 7.1 Propagation Delay, Inverting, and Noninverting Configuration

Figure 22 shows the propagation delay for noninverting configurations. Figure 23 shows the propagation delay with the inverting configuration. These figures also demonstrate the method used to measure the rise ( $t_r$ ) and fall ( $t_f$ ) times.



**Figure 22. Propagation Delay, Noninverting Configuration**

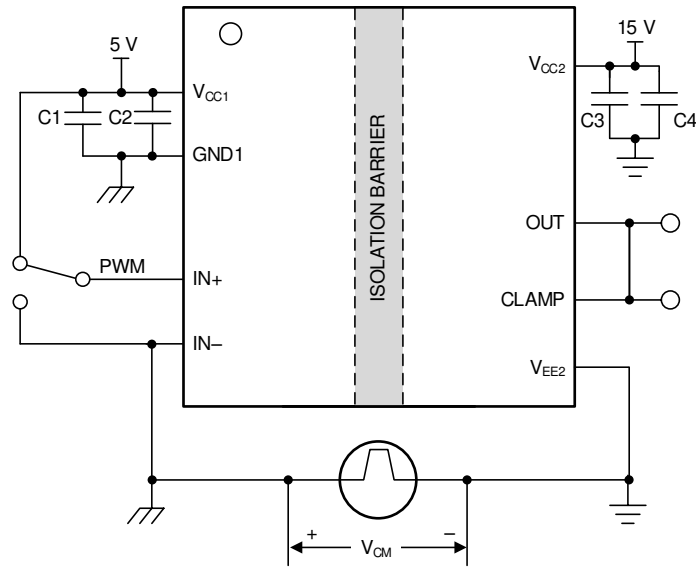


**Figure 23. Propagation Delay, Inverting Configuration**

## Propagation Delay, Inverting, and Noninverting Configuration (continued)

### 7.1.1 CMTI Testing

Figure 24 is a simplified diagram of the CMTI testing configuration.



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**Figure 24. CMTI Test Circuit**

## 8 Detailed Description

### 8.1 Overview

The isolation inside the UCC5350-Q1 is implemented with high-voltage SiO<sub>2</sub>-based capacitors. The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier (see Figure 26). The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The UCC5350-Q1 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 25, shows a functional block diagram of a typical channel. Figure 26 shows a conceptual detail of how the OOK scheme works.

Figure 25 shows how the input signal passes through the capacitive isolation barrier through modulation (OOK) and signal conditioning.

### 8.2 Functional Block Diagram

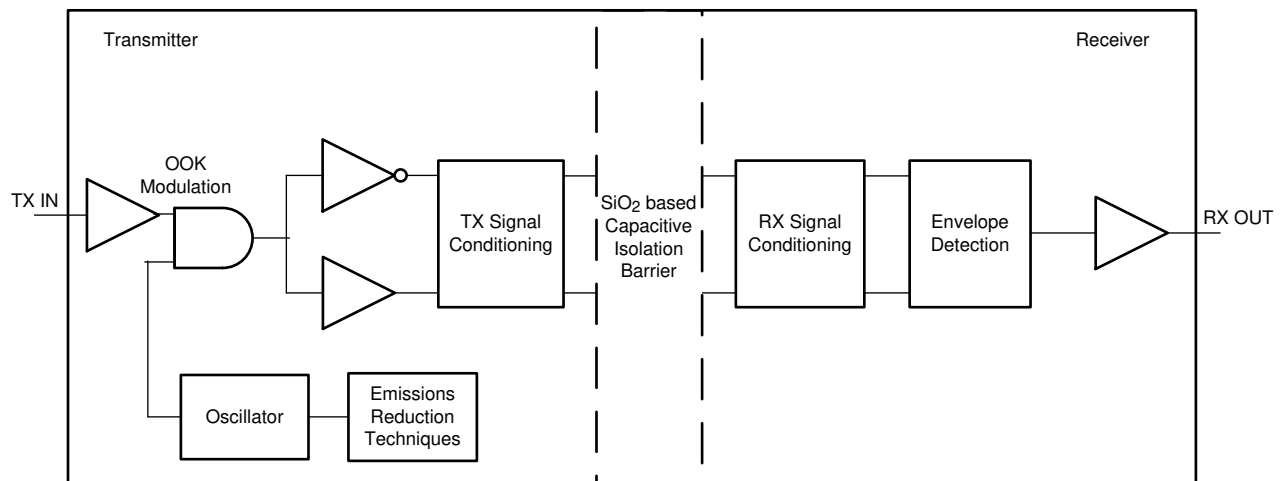


Figure 25. Conceptual Block Diagram of a Capacitive Data Channel

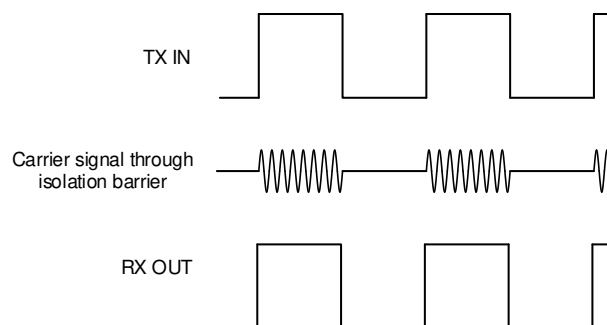


Figure 26. On-Off Keying (OOK) Based Modulation Scheme



## Functional Block Diagram (continued)

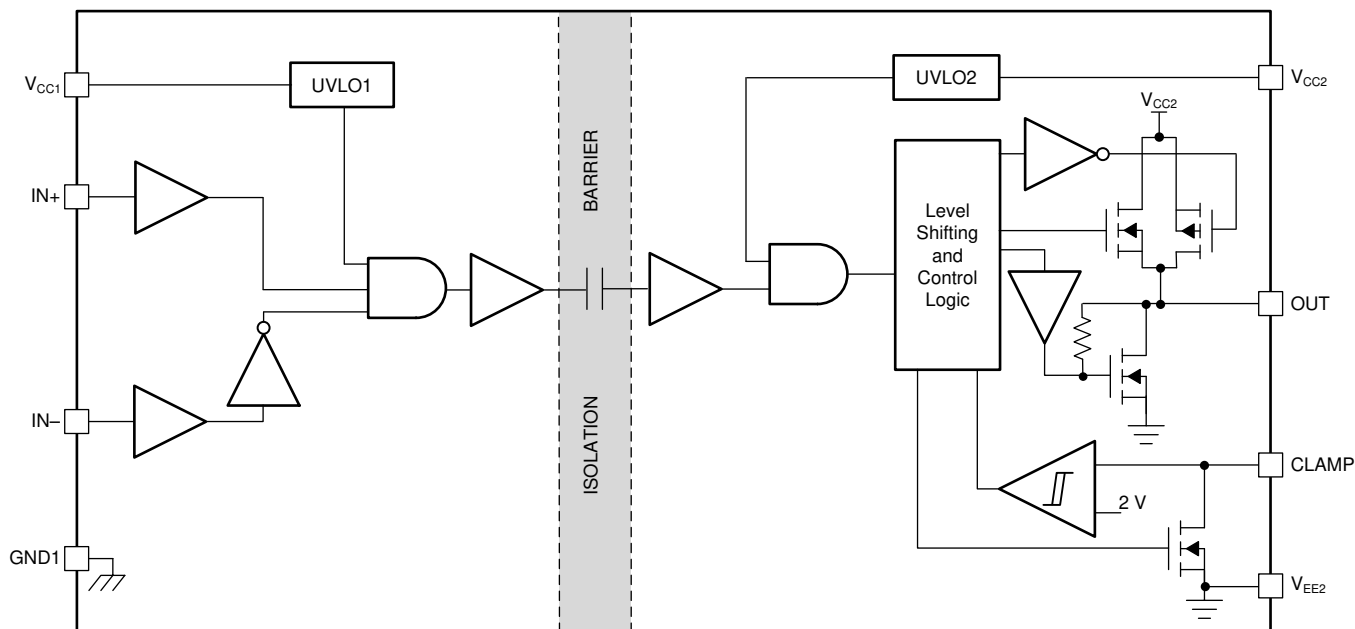


Figure 27. Functional Block Diagram

## 8.3 Feature Description

### 8.3.1 Power Supply

The  $V_{CC1}$  input power supply supports a wide voltage range from 3 V to 15 V and the  $V_{CC2}$  output supply supports a voltage range from 13.2 V to 33 V.

For operation with unipolar supply, the  $V_{CC2}$  supply is connected to 15 V with respect to  $V_{EE2}$  for IGBTs, and 20 V for SiC MOSFETs. The  $V_{EE2}$  supply is connected to 0 V. In this use case, the Miller clamp helps to prevent a false turn-on of the power switch without a negative voltage rail. The Miller clamping function is implemented by adding a low impedance path between the gate of the power device and the  $V_{EE2}$  supply. Miller current sinks through the clamp pin, which clamps the gate voltage to be lower than the turn-on threshold value for the gate.

### 8.3.2 Input Stage

The input pins (IN+ and IN-) of the UCC5350-Q1 are based on CMOS-compatible input-threshold logic that is completely isolated from the  $V_{CC2}$  supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V microcontrollers), because the UCC5350-Q1 has a typical high threshold ( $V_{IT+(IN)}$ ) of  $0.55 \times V_{CC1}$  and a typical low threshold of  $0.45 \times V_{CC1}$ . A wide hysteresis ( $V_{hys(IN)}$ ) of  $0.1 \times V_{CC1}$  makes for good noise immunity and stable operation. If either of the inputs are left open, 128 k $\Omega$  of internal pull-down resistance forces the IN+ pin low and 128 k $\Omega$  of internal resistance pulls IN- high. However, TI still recommends grounding an input or tying to  $V_{CC1}$  if it is not being used for improved noise immunity.

Because the input side of the UCC5350-Q1 is isolated from the output driver, the input signal amplitude can be larger or smaller than  $V_{CC2}$  provided that it does not exceed the recommended limit. This feature allows greater flexibility when integrating the gate-driver with control signal sources and allows the user to choose the most efficient  $V_{CC2}$  for any gate. However, the amplitude of any signal applied to IN+ or IN- must never be at a voltage higher than  $V_{CC1}$ .

## Feature Description (continued)

### 8.3.3 Output Stage

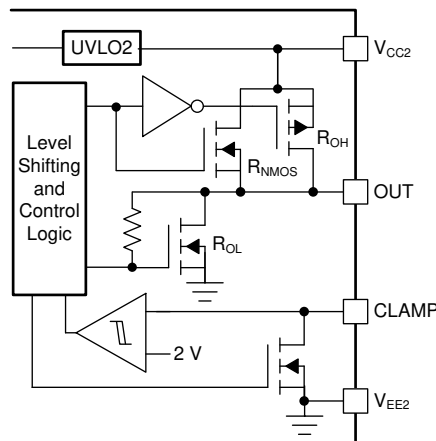
The output stage of the UCC5350-Q1 feature a pull-up structure that delivers the highest peak-source current when it is most needed which is during the Miller plateau region of the power-switch turn-on transition (when the power-switch drain or collector voltage experiences  $dV/dt$ ). The output stage pull-up structure features a P-channel MOSFET and an additional pull-up N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, which enables fast turn-on. Fast turn-on is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. Table 1 lists the typical internal resistance values of the pull-up and pull-down structure.

**Table 1. UCC5350-Q1 On-Resistance**

DEVICE OPTION	$R_{NMOS}$	$R_{OH}$	$R_{OL}$	$R_{CLAMP}$	UNIT
UCC5350-Q1	1.54	12	0.26	0.26	$\Omega$

The  $R_{OH}$  parameter is a DC measurement and is representative of the on-resistance of the P-channel device only. This parameter is only for the P-channel device, because the pull-up N-channel device is held in the OFF state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore, the effective resistance of the UCC5350-Q1 pull-up stage during this brief turn-on phase is much lower than what is represented by the  $R_{OH}$  parameter, which yields a faster turn-on. The turn-on-phase output resistance is the parallel combination  $R_{OH} \parallel R_{NMOS}$ .

The pull-down structure in the UCC5350-Q1 is simply composed of an N-channel MOSFET. The output of the UCC5350-Q1 is capable of delivering, or sinking, 5-A peak current pulses. The output voltage swing between  $V_{CC2}$  and  $V_{EE2}$  provides rail-to-rail operation because of the MOS-out stage which delivers very low dropout.



**Figure 28. Output Stage**

### 8.3.4 Protection Features

#### 8.3.4.1 Undervoltage Lockout (UVLO)

UVLO functions are implemented for both the  $V_{CC1}$  and  $V_{CC2}$  supplies between the  $V_{CC1}$  and GND1, and  $V_{CC2}$  and  $V_{EE2}$  pins to prevent an underdriven condition on IGBTs and MOSFETs. When  $V_{CC}$  is lower than  $V_{IT+ (UVLO)}$  at device start-up or lower than  $V_{IT- (UVLO)}$  after start-up, the voltage-supply UVLO feature holds the effected output low, regardless of the input pins (IN+ and IN-) as shown in Table 2. The  $V_{CC}$  UVLO protection has a hysteresis feature ( $V_{hys (UVLO)}$ ). This hysteresis prevents chatter when the power supply produces ground noise; this allows the device to permit small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly. Figure 29 shows the UVLO functions.

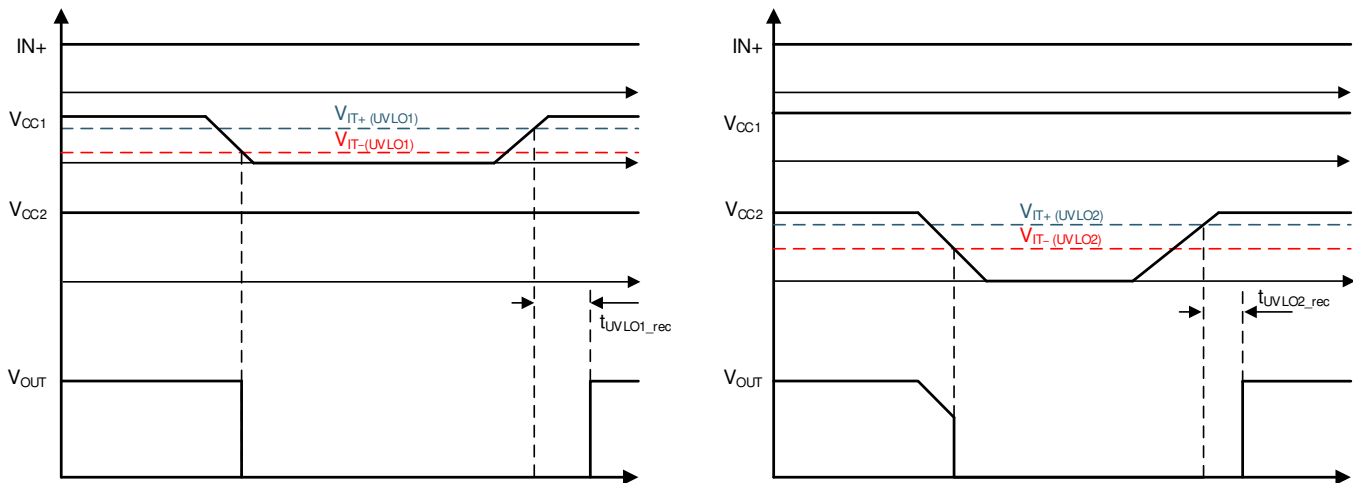
**Table 2. UCC5350-Q1  $V_{CC1}$  UVLO Logic**

CONDITION	INPUTS		OUTPUT
	IN+	IN–	OUT
$V_{CC1} - GND1 < V_{IT+(UVLO1)}$ during device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L
$V_{CC1} - GND1 < V_{IT-(UVLO1)}$ after device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L

**Table 3. UCC5350-Q1  $V_{CC2}$  UVLO Logic**

CONDITION	INPUTS		OUTPUT
	IN+	IN–	OUT
$V_{CC2} - V_{EE2} < V_{IT+(UVLO2)}$ during device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L
$V_{CC2} - V_{EE2} < V_{IT-(UVLO2)}$ after device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L

When  $V_{CC1}$  or  $V_{CC2}$  drops below the UVLO1 or UVLO2 threshold, a delay,  $t_{UVLO1\_rec}$  or  $t_{UVLO2\_rec}$ , occurs on the output when the supply voltage rises above  $V_{IT+(UVLO)}$  or  $V_{IT+(UVLO2)}$  again. Figure 29 shows this delay.



**Figure 29. UVLO Functions**

### 8.3.4.2 Active Pulldown

The active pull-down function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the  $V_{CC2}$  supply. This feature prevents false IGBT and MOSFET turn-on on the OUT and CLAMP pins by clamping the output to approximately 2 V.

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs. In this condition, the upper PMOS is resistively held off by a pull-up resistor while the lower NMOS gate is tied to the driver output through a 500-k $\Omega$  resistor. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, which is approximately 1.5 V when no bias power is available.

### 8.3.4.3 Short-Circuit Clamping

The short-circuit clamping function is used to clamp voltages at the driver output and pull the active Miller clamp pins slightly higher than the  $V_{CC2}$  voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the  $V_{CC2}$  pin inside the driver. The internal diodes can conduct up to 500-mA current for a duration of 10  $\mu$ s and a continuous current of 20 mA. Use external Schottky diodes to improve current conduction capability as needed.

### 8.3.4.4 Active Miller Clamp

The active Miller-clamp function is used to prevent false turn-on of the power switches caused by Miller current in applications where a unipolar power supply is used. The active Miller-clamp function is implemented by adding a low impedance path between the power-switch gate terminal and ground ( $V_{EE2}$ ) to sink the Miller current. With the Miller-clamp function, the power-switch gate voltage is clamped to less than 2 V during the off state. [Figure 31](#) shows a typical application circuit of this function.

## 8.4 Device Functional Modes

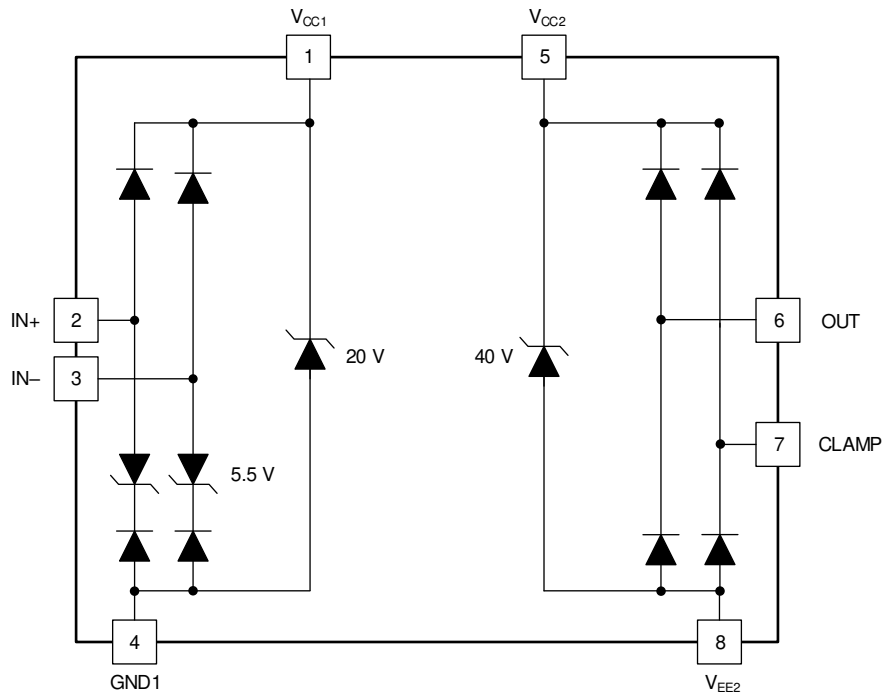
[Table 4](#) lists the functional modes for the UCC5350-Q1 assuming  $V_{CC1}$  and  $V_{CC2}$  are in the recommended range.

**Table 4. Function Table**

IN+	IN–	OUT
Low	X	Low
X	High	Low
High	Low	High

### 8.4.1 ESD Structure

Figure 30 shows the multiple diodes involved in the ESD protection components of the UCC5350-Q1. This provides pictorial representation of the absolute maximum rating for the device.



**Figure 30. ESD Structure**

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

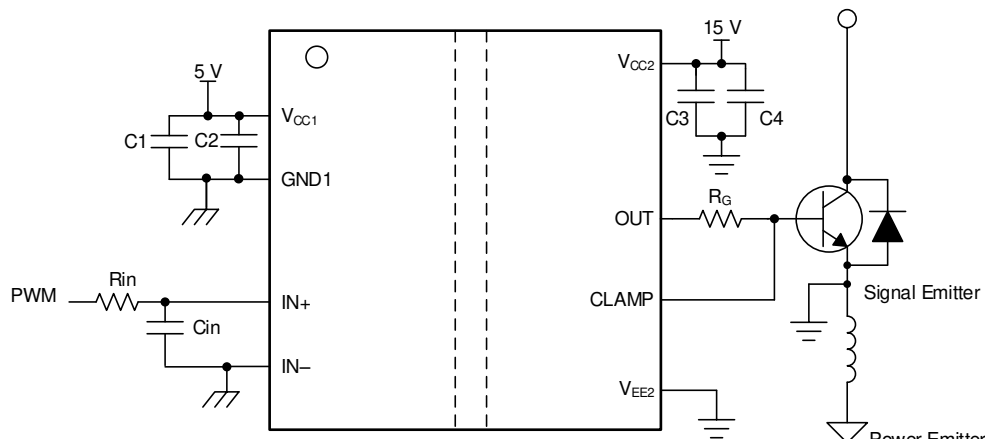
### 9.1 Application Information

The UCC5350-Q1 is a simple, isolated gate driver for power semiconductor devices, such as MOSFETs, IGBTs, or SiC MOSFETs. The family of devices is intended for use in applications such as motor control, solar inverters, switched-mode power supplies, and industrial inverters.

The UCC5350-Q1 has active Miller clamping, which can be used to prevent false turn-on of the power transistors induced by the Miller current. The device comes in an 8-pin D and 8-pin DWV package and has creepage, or clearance, of 4 mm and 8.5 mm, respectively, which is suitable for applications where basic or reinforced isolation is required. The UCC5350-Q1 offers a 5-A minimum drive current.

### 9.2 Typical Application

The circuit in [Figure 31](#) show a typical application for driving IGBTs.



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**Figure 31. Typical Application Circuit for UCC5350-Q1**

#### 9.2.1 Design Requirements

[Table 5](#) lists the recommended conditions to observe the input and output of the UCC5350-Q1 gate driver with the IN– pin tied to the GND1 pin.

**Table 5. UCC5350-Q1 Design Requirements**

PARAMETER	VALUE	UNIT
V <sub>CC1</sub>	3.3	V
V <sub>CC2</sub> – V <sub>EE2</sub>	18	V
IN+	3.3	V
IN–	GND1	-
Switching frequency	150	kHz
Gate Charge of Power Device	126	nC

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Designing IN+ and IN– Input Filter

TI recommends that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input filter,  $R_{IN}$ - $C_{IN}$ , can be used to filter out the ringing introduced by nonideal layout or long PCB traces.

Such a filter should use an  $R_{IN}$  resistor with a value from 0  $\Omega$  to 100  $\Omega$  and a  $C_{IN}$  capacitor with a value from 10 pF to 1000 pF. In the example, the selected value for  $R_{IN}$  is 51  $\Omega$  and  $C_{IN}$  is 33 pF, with a corner frequency of approximately 100 MHz.

When selecting these components, pay attention to the trade-off between good noise immunity and propagation delay.

### 9.2.2.2 Gate-Driver Output Resistor

The external gate-driver resistors,  $R_{G(ON)}$  and  $R_{G(OFF)}$  are used to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage or high current switching dv/dt, di/dt, and body-diode reverse recovery
3. Fine-tune gate drive strength, specifically peak sink and source current to optimize the switching loss
4. Reduce electromagnetic interference (EMI)

The output stage has a pull-up structure consisting of a P-channel MOSFET and an N-channel MOSFET in parallel. The combined typical peak source current is 10 A for UCC5350-Q1. Use Equation 1 to estimate the peak source current.

$$I_{OH} = \frac{V_{CC2} - V_{EE2}}{R_{NMOS} \parallel R_{OH} + R_{ON} + R_{GFET\_Int}}$$

where

- $R_{ON}$  is the external turn-on resistance, which is 2.2  $\Omega$  in this example.
- $R_{GFET\_Int}$  is the power transistor internal gate resistance, found in the power transistor data sheet. We will assume 1.8  $\Omega$  for our example.
- $I_{OH}$  is the typical peak source current which is the minimum value between 10 A, the gate-driver peak source current, and the calculated value based on the gate-drive loop resistance.

(1)

In this example, the peak source current is approximately 3.36 A as calculated in Equation 2.

$$I_{OH} = \frac{V_{CC2} - V_{EE2}}{R_{NMOS} \parallel R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{18 \text{ V}}{1.54 \Omega \parallel 12 \Omega + 2.2 \Omega + 1.8 \Omega} \approx 3.36 \text{ A}$$

(2)

Similarly, use Equation 3 to calculate the peak sink current.

$$I_{OL} = \frac{V_{CC2} - V_{EE2}}{R_{OL} + R_{OFF} + R_{GFET\_Int}}$$

where

- $R_{OFF}$  is the external turn-off resistance, which is 2.2  $\Omega$  in this example.
- $I_{OL}$  is the typical peak sink current which is the minimum value between 10 A, the gate-driver peak sink current, and the calculated value based on the gate-drive loop resistance.

(3)

In this example, the peak sink current is the minimum value between Equation 4 and 10 A.

$$I_{OL} = \frac{V_{CC2} - V_{EE2}}{R_{OL} + R_{OFF} + R_{GFET\_Int}} = \frac{18 \text{ V}}{0.26 \Omega + 2.2 \Omega + 1.8 \Omega} \approx 4.23 \text{ A}$$

(4)

### NOTE

The estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate-driver loop can slow down the peak gate-drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends that the gate-driver loop should be minimized. Conversely, the peak source and sink current is dominated by loop parasitics when the load capacitance ( $C_{ISS}$ ) of the power transistor is very small (typically less than 1 nF) because the rising and falling time is too small and close to the parasitic ringing period.

#### 9.2.2.3 Estimate Gate-Driver Power Loss

The total loss,  $P_G$ , in the gate-driver subsystem includes the power losses ( $P_{GD}$ ) of the UCC5350-Q1 device and the power losses in the peripheral circuitry, such as the external gate-drive resistor.

The  $P_{GD}$  value is the key power loss which determines the thermal safety-related limits of the UCC5350-Q1 device, and it can be estimated by calculating losses from several components.

The first component is the static power loss,  $P_{GDQ}$ , which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. The  $P_{GDQ}$  parameter is measured on the bench with no load connected to the OUT pins at a given  $V_{CC1}$ ,  $V_{CC2}$ , switching frequency, and ambient temperature. In this example,  $V_{CC1}$  is 3.3V and  $V_{CC2}$  is 18 V. The current on each power supply, with PWM switching from 0 V to 3.3 V at 150 kHz, is measured to be  $I_{CC1} = 1.67$  mA and  $I_{CC2} = 1.11$  mA. Therefore, use Equation 5 to calculate  $P_{GDQ}$ .

$$P_{GDQ} = V_{CC1} \times I_{CC1} + (V_{CC2} - V_{EE2}) \times I_{CC2} \approx 23.31 \text{ mW} \quad (5)$$

The second component is the switching operation loss,  $P_{GDO}$ , with a given load capacitance which the driver charges and discharges the load during each switching cycle. Use Equation 6 to calculate the total dynamic loss from load switching,  $P_{GSW}$ .

$$P_{GSW} = (V_{CC2} - V_{EE2}) \times Q_G \times f_{SW}$$

where

- $Q_G$  is the gate charge of the power transistor at  $V_{CC2}$ . (6)

So, for this example application the total dynamic loss from load switching is approximately 340 mW as calculated in Equation 7.

$$P_{GSW} = 18 \text{ V} \times 126 \text{ nC} \times 150 \text{ kHz} = 340 \text{ mW} \quad (7)$$

$Q_G$  represents the total gate charge of the power transistor, and is subject to change with different testing conditions. The UCC5350-Q1 gate-driver loss on the output stage,  $P_{GDO}$ , is part of  $P_{GSW}$ .  $P_{GDO}$  is equal to  $P_{GSW}$  if the external gate-driver resistance and power-transistor internal resistance are 0  $\Omega$ , and all the gate driver-loss will be dissipated inside the UCC5350-Q1. If an external turn-on and turn-off resistance exists, the total loss is distributed between the gate driver pull-up/down resistance, external gate resistance, and power-transistor internal resistance. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 10 A, however, it will be non-linear if the source/sink current is saturated. The gate driver loss will be estimated in the case in which it is not saturated as given in Equation 8.

$$P_{GDO} = \frac{P_{GSW}}{2} \left( \frac{R_{OH} \parallel R_{NMOS}}{R_{OH} \parallel R_{NMOS} + R_{ON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{GFET\_Int}} \right) \quad (8)$$

In this design example UCC5350-Q1, all the predicted source and sink currents are less than 10 A, therefore, use Equation 9 to estimate the gate-driver loss.

$$P_{GDO} = \frac{340 \text{ mW}}{2} \left( \frac{12 \Omega \parallel 1.54 \Omega}{12 \Omega \parallel 1.54 \Omega + 2.2 \Omega + 1.8 \Omega} + \frac{0.26 \Omega}{0.26 \Omega + 2.2 \Omega + 1.8 \Omega} \right) \approx 53.66 \text{ mW} \quad (9)$$

Use Equation 10 to calculate the total gate-driver loss dissipated in the UCC5350-Q1 gate driver,  $P_{GD}$ .

$$P_{GD} = P_{GDQ} + P_{GDO} = 25.31 \text{ mW} + 53.66 \text{ mW} = 78.97 \text{ mW} \quad (10)$$



### 9.2.2.4 Estimating Junction Temperature

Use Equation 11 to estimate the junction temperature ( $T_J$ ) of the UCC5350-Q1 family.

$$T_J = T_C + \Psi_{JT} \times P_{GD}$$

where

- $T_C$  is the UCC5350-Q1 case-top temperature measured with a thermocouple or some other instrument.
- $\Psi_{JT}$  is the junction-to-top characterization parameter from the Thermal Information table. (11)

Using the junction-to-top characterization parameter ( $\Psi_{JT}$ ) instead of the junction-to-case thermal resistance ( $R_{\theta JC}$ ) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). The  $R_{\theta JC}$  resistance can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heat sink is applied to an IC package. In all other cases, use of  $R_{\theta JC}$  will inaccurately estimate the true junction temperature. The  $\Psi_{JT}$  parameter is experimentally derived by assuming that the dominant energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimations can be made accurately to within a few degrees Celsius.

### 9.2.3 Selecting $V_{CC1}$ and $V_{CC2}$ Capacitors

Bypass capacitors for the  $V_{CC1}$  and  $V_{CC2}$  supplies are essential for achieving reliable performance. TI recommends choosing low-ESR and low-ESL, surface-mount, multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients, and capacitance tolerances.

#### NOTE

DC bias on some MLCCs will impact the actual capacitance value. For example, a 25-V, 1- $\mu$ F X7R capacitor is measured to be only 500 nF when a DC bias of 15- $V_{DC}$  is applied.

#### 9.2.3.1 Selecting a $V_{CC1}$ Capacitor

A bypass capacitor connected to the  $V_{CC1}$  pin supports the transient current required for the primary logic and the total current consumption, which is only a few milliamperes. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power-supply output is located a relatively long distance from the  $V_{CC1}$  pin, a tantalum or electrolytic capacitor with a value greater than 1  $\mu$ F should be placed in parallel with the MLCC.

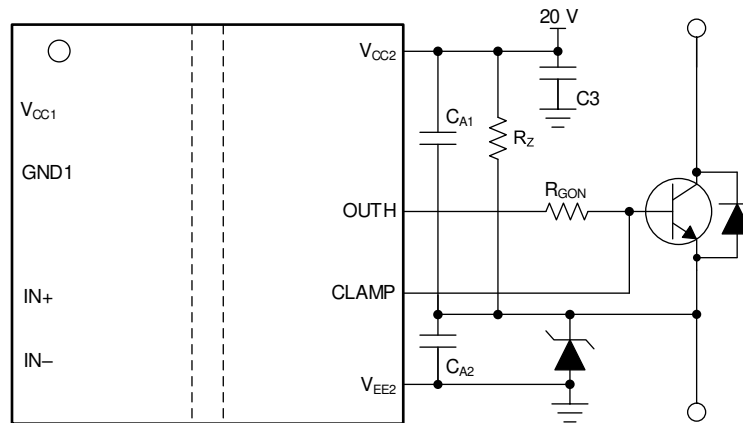
#### 9.2.3.2 Selecting a $V_{CC2}$ Capacitor

A 50-V, 10- $\mu$ F MLCC and a 50-V, 0.22- $\mu$ F MLCC are selected for the  $V_{CC2}$  capacitor. If the bias power supply output is located a relatively long distance from the  $V_{CC2}$  pin, a tantalum or electrolytic capacitor with a value greater than 10  $\mu$ F should be used in parallel with  $V_{CC2}$ .

#### 9.2.3.3 Application Circuits With Output Stage Negative Bias

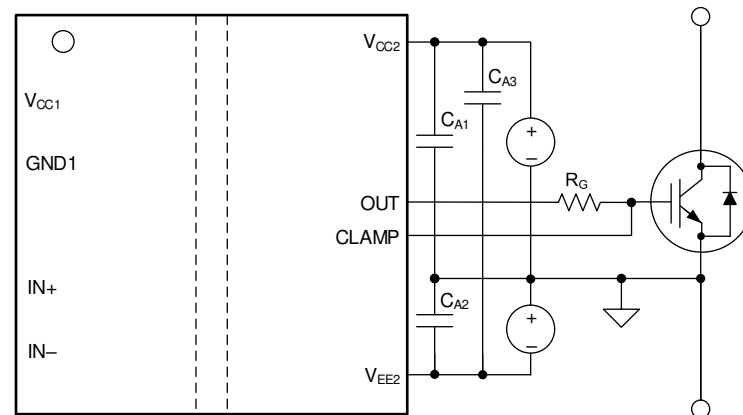
When parasitic inductances are introduced by nonideal PCB layout and long package leads (such as TO-220 and TO-247 type packages), ringing in the gate-source drive voltage of the power transistor could occur during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, unintended turn-on and shoot-through could occur. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. A few examples of implementing negative gate-drive bias follow.

Figure 32 shows the first example with negative bias turn-off on the output using a Zener diode on the isolated power-supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply is equal to 20 V, the turn-off voltage is -5.1 V and the turn-on voltage is 20 V - 5.1 V  $\approx$  15 V.



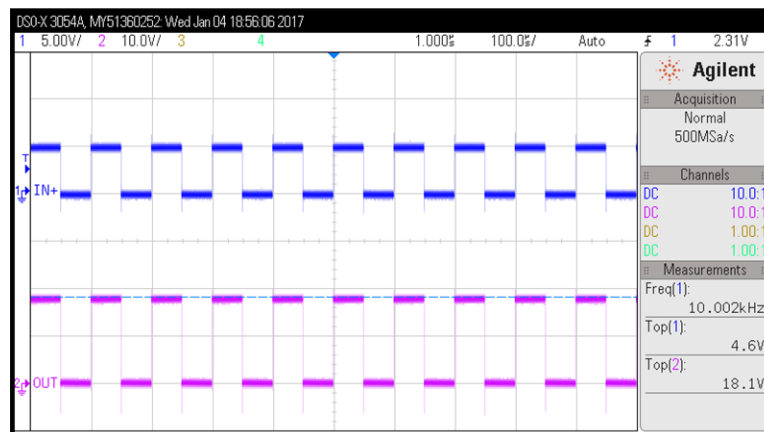
**Figure 32. Negative Bias With Zener Diode on Iso-Bias Power-Supply Output**

Figure 33 shows another example which uses two supplies (or single-input, double-output power supply). The power supply across  $V_{CC2}$  and the emitter determines the positive drive output voltage and the power supply across  $V_{EE2}$  and the emitter determines the negative turn-off voltage. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.



**Figure 33. Negative Bias With Two Iso-Bias Power Supplies**

## 9.2.4 Application Curve



$$V_{CC2} = 20 \text{ V} \quad V_{EE2} = \text{GND} \quad f_{\text{SW}} = 10 \text{ kHz}$$

**Figure 34. PWM Input And Gate Voltage Waveform**

## 10 Power Supply Recommendations

The recommended input supply voltage ( $V_{CC1}$ ) for the UCC5350-Q1 device is from 3 V to 15 V. The lower limit of the range of output bias-supply voltage ( $V_{CC2}$ ) is determined by the internal UVLO protection feature of the device. The  $V_{CC1}$  and  $V_{CC2}$  voltages should not fall below their respective UVLO thresholds for normal operation, or else the gate-driver outputs can become clamped low for more than 50  $\mu$ s by the UVLO protection feature. For more information on UVLO, see the [Undervoltage Lockout \(UVLO\)](#) section. The higher limit of the  $V_{CC2}$  range depends on the maximum gate voltage of the power device that is driven by the UCC5350-Q1 device, and should not exceed the recommended maximum  $V_{CC2}$  of 33 V. A local bypass capacitor should be placed between the  $V_{CC2}$  and  $V_{EE2}$  pins, with a value of 220-nF to 10- $\mu$ F for device biasing. TI recommends placing an additional 100-nF capacitor in parallel with the device biasing capacitor for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended. Similarly, a bypass capacitor should also be placed between the  $V_{CC1}$  and GND1 pins. Given the small amount of current drawn by the logic circuitry within the input side of the UCC5350-Q1 device, this bypass capacitor has a minimum recommended value of 100 nF.

If only a single, primary-side power supply is available in an application, isolated power can be generated for the secondary side with the help of a transformer driver such as Texas Instruments' [SN6501](#) or [SN6505A](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501 Transformer Driver for Isolated Power Supplies data sheet](#) and [SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies data sheet](#).

## 11 Layout

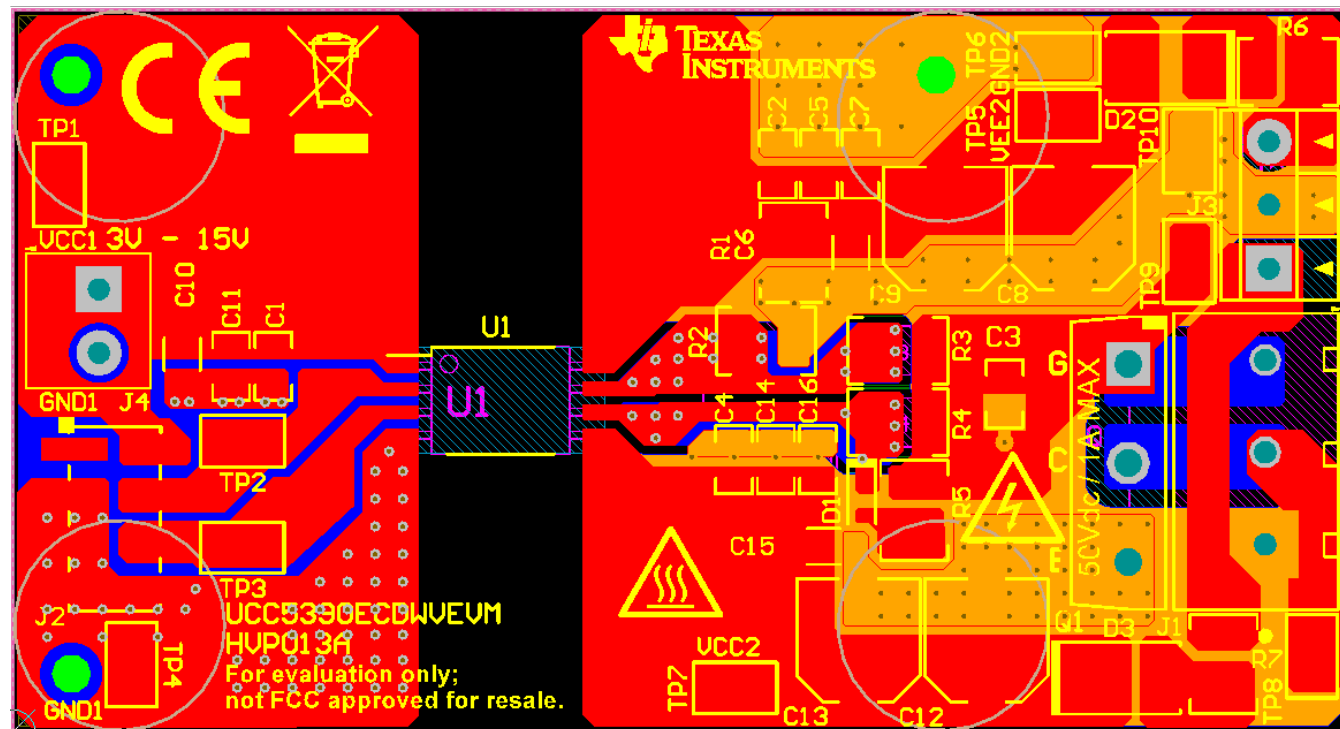
### 11.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the UCC5350-Q1. Some key guidelines are:

- Component placement:
  - Low-ESR and low-ESL capacitors must be connected close to the device between the  $V_{CC1}$  and GND1 pins and between the  $V_{CC2}$  and  $V_{EE2}$  pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - To avoid large negative transients on the  $V_{EE2}$  pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- Grounding considerations:
  - Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.
- Thermal considerations:
  - A large amount of power may be dissipated by the UCC5350-Q1 if the driving voltage is high, the load is heavy, or the switching frequency is high (for more information, see the [Estimate Gate-Driver Power Loss](#) section). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance ( $\theta_{JB}$ ).
  - Increasing the PCB copper connecting to the  $V_{CC2}$  and  $V_{EE2}$  pins is recommended, with priority on maximizing the connection to  $V_{EE2}$ . However, the previously mentioned high-voltage PCB considerations must be maintained.
  - If the system has multiple layers, TI also recommends connecting the  $V_{CC2}$  and  $V_{EE2}$  pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

## 11.2 Layout Example

Figure 35 shows a PCB layout example with the signals and key components labeled. The UCC5390ECDWV evaluation module (EVM) is given as an example, available in the same DWV package as the UCC5350-Q1. The UCC5390EC has a split emitter versus Miller clamp so although the layout is not exactly the same, general guidelines and practices still apply. The evaluation board can be configured for the Miller clamp version, as well, as described in the *UCC5390ECDWV Isolated Gate Driver Evaluation Module User's Guide*.



- (1) No PCB traces or copper are located between the primary and secondary side, which ensures isolation performance.

Figure 35. Layout Example

## Layout Example (continued)

Figure 36 and Figure 37 show the top and bottom layer traces and copper.

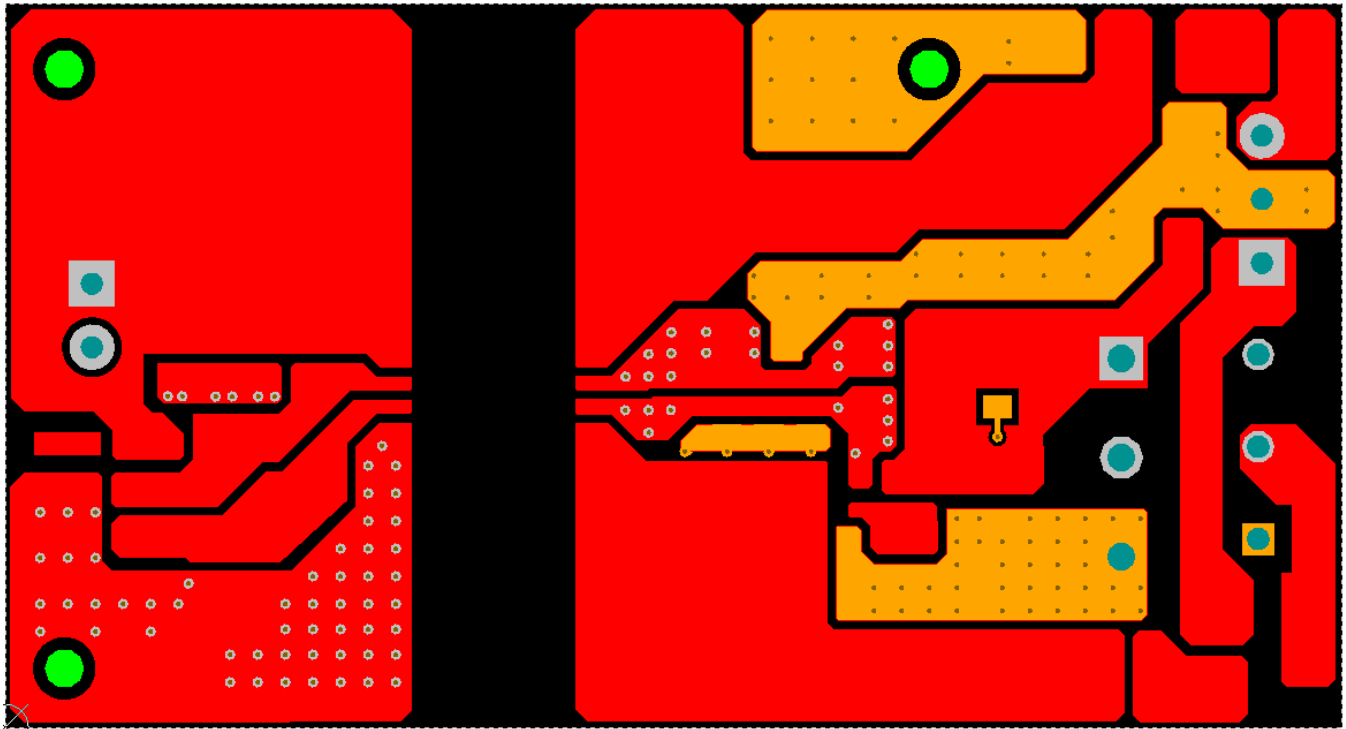


Figure 36. Top-Layer Traces and Copper

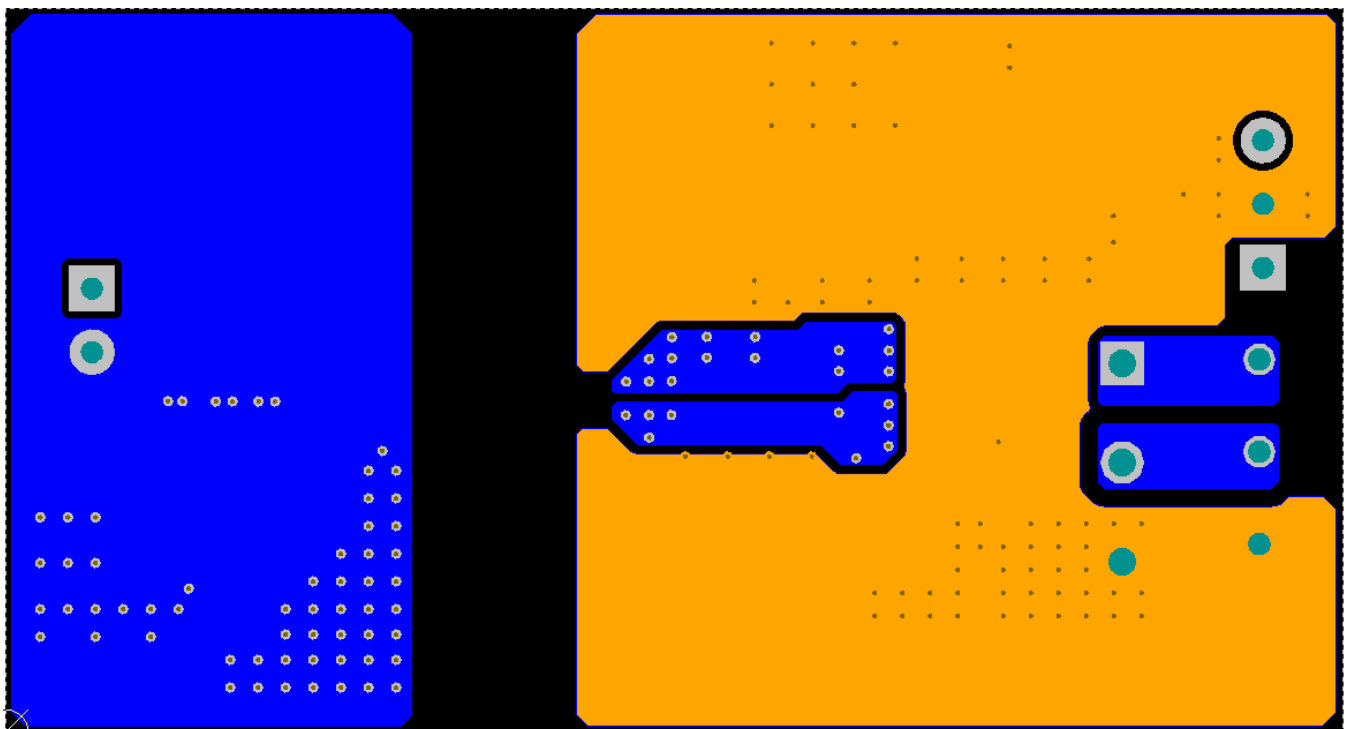


Figure 37. Bottom-Layer Traces and Copper (Flipped)

## Layout Example (continued)

Figure 38 shows the 3D layout of the top view of the PCB.

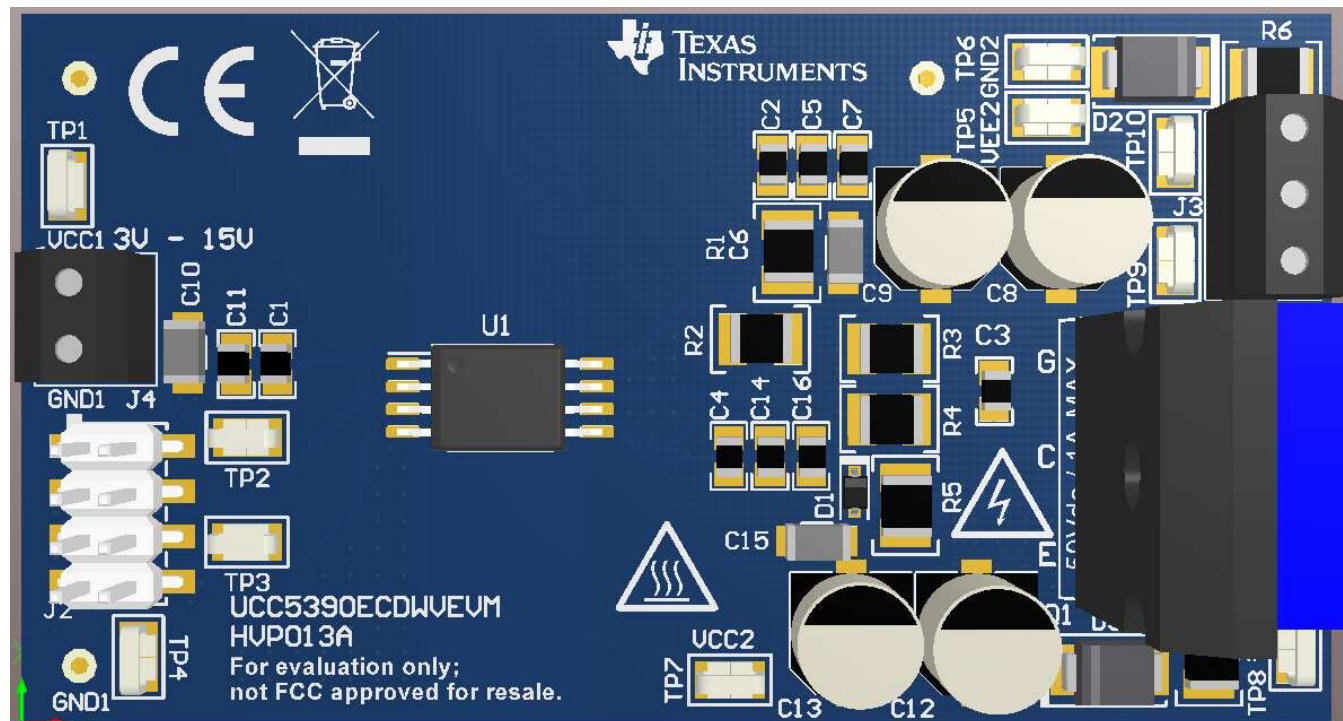


Figure 38. 3-D PCB View

## 11.3 PCB Material

Use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

Figure 39 shows the recommended layer stack.

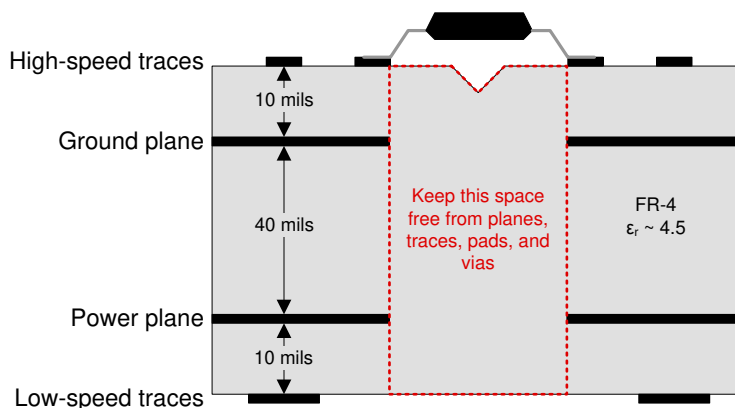


Figure 39. Recommended Layer Stack

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [Isolation Glossary](#)
- Texas Instruments, [SN6501 Transformer Driver for Isolated Power Supplies data sheet](#)
- Texas Instruments, [SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies data sheet](#)
- Texas Instruments, [UCC5390ECDWV Isolated Gate Driver Evaluation Module user's guide](#)
- Texas Instruments, [UCC53x0xD Evaluation Module user's guide](#)

### 12.2 Certifications

UL Online Certifications Directory, ["FPPT2.E181974 Nonoptical Isolating Devices - Component" Certificate Number: 20170718-E181974](#),

### 12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

### 12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.5 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC5350MCQDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5350Q	<a href="#">Samples</a>
UCC5350MCQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5350Q	<a href="#">Samples</a>
UCC5350MCQDWVQ1	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	5350MCQ	<a href="#">Samples</a>
UCC5350MCQDWVRQ1	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	5350MCQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF UCC5350-Q1 :**

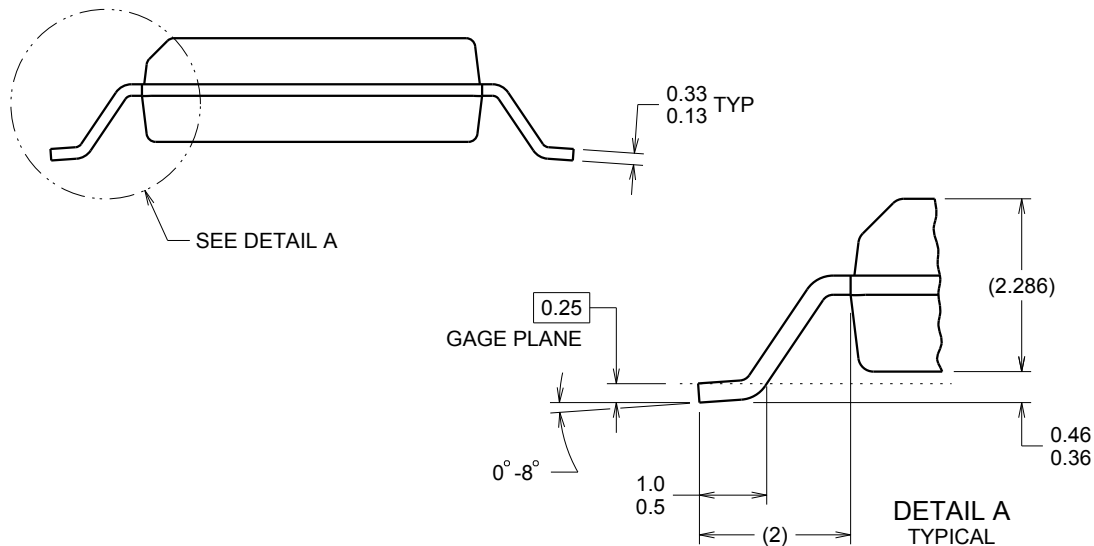
- Catalog: [UCC5350](#)

NOTE: Qualified Version Definitions:

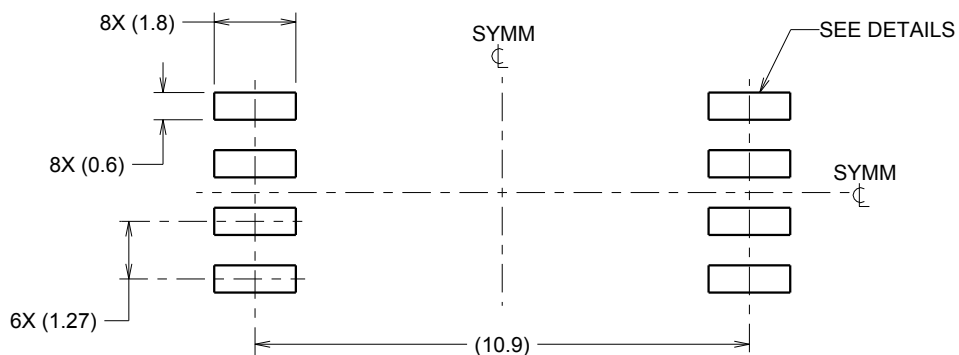
- Catalog - TI's standard catalog product

SOIC - 2.8 mm max height

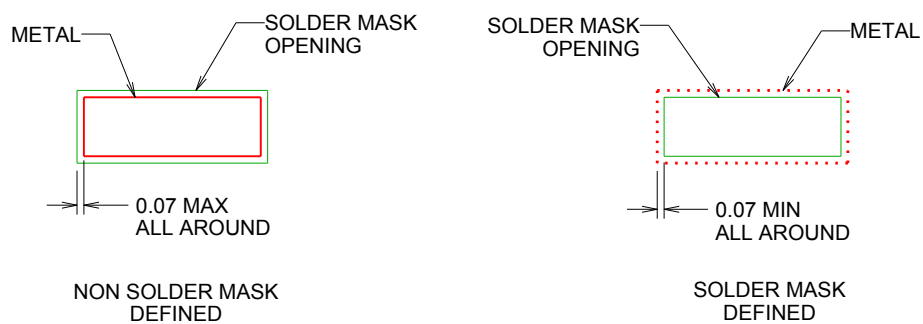
PIN 1 ID AREA  
 11.5 ± 0.25 TYP  
 5.95  
 5.75  
 NOTE 3  
 1  
 4  
 8  
 5  
 6X 1.27  
 2X 3.81  
 8X 0.51  
 0.31  
 7.6  
 7.4  
 NOTE 4  
 A  
 B  
 SEATING PLANE  
 0.1 C  
 2.8 MAX  
 C  
 A  
 B



1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



**LAND PATTERN EXAMPLE**  
9.1 mm NOMINAL CLEARANCE/CREEPAGE  
SCALE:6X

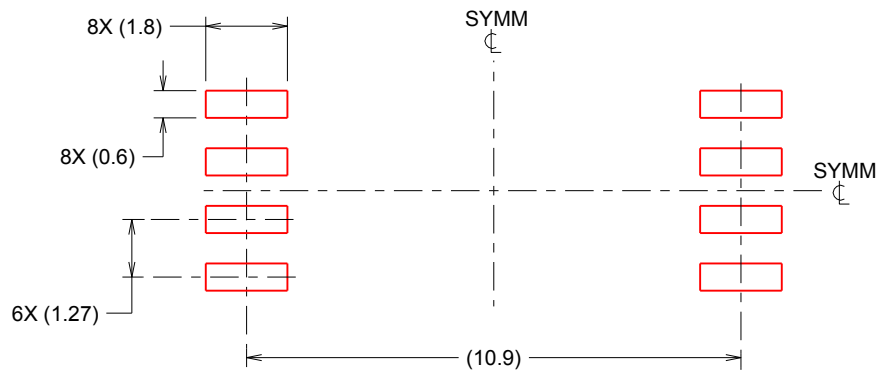


**SOLDER MASK DETAILS**

4218796/A 09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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