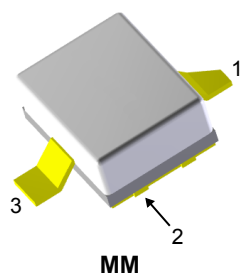


10 W, 28 V, HF to 1.6 GHz RF Power LDMOS transistor



Pin connection	
Pin	Connection
1	Drain
2	Source (bottom side)
3	Gate

Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
ST16010	930 MHz	28 V	10 W	23 dB	58%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internally input matched for ease of use
- Large positive and negative gate-source voltage range for improved class C operation
- In compliance with the european directive 2002/95/EC

Applications

- Telecom and wideband communication
- Industrial, scientific and medical
- Avionics

Description

The **ST16010** is a 10 W, 28 V LDMOS transistor designed for wideband radio, Avionics and ISM applications at frequencies up to 1.6 GHz.



Product status link
ST16010

Product summary	
Order code	ST16010
Marking	ST16010
Package	MM
Packing	Tape and reel 13"
Base / Bulk qty	300/300

1 Electrical ratings

Table 1. Absolute maximum ratings ($T_C = 25\text{ °C}$)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	90	V
V_{GS}	Gate-source voltage	-6 to 10	V
V_{DD}	Drain voltage operating voltage	32	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}^{(1)}$	Thermal resistance, junction-to-case	3	°C/W

1. $T_C = 85\text{ °C}$, $T_J = 200\text{ °C}$, DC test

Table 3. ESD protection

Symbol	Parameter	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	1B
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS-002-2014)	C3

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified).

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	90			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 75\text{ V}$			1	μA
I_{GSS}	Gate-body leakage current	$V_{GS} = -6/10\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 10\text{ V}$, $I_D = 50\text{ }\mu\text{A}$	1.5		2.5	V
$V_{GS(Q)}$	Gate quiescent voltage	$V_{DS} = 1\text{ V}$, $I_{DS} = 100\text{ mA}$	2.0		5.0	V
$I_{DS(on)}$	Static drain-source on-current	$V_{GS} = 10\text{ V}$, $V_{DS} = 100\text{ mV}$			2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 100\text{ mV}$			1	Ω
$V_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 1\text{ V}$, $I_D = 100\text{ mA}$			250	mV
C_{iss}	Common source input capacitance	$V_{GS} = 0\text{ V}$, $V_{DD} = 28\text{ V}$, $f = 1\text{ MHz}$		15		pF
C_{oss}	Common source output capacitance			5.7		
C_{rss}	Common source feedback capacitance			0.4		

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	$f = 930\text{ MHz}$ 1dB compression	-	10		W
G_{PS}	Power gain		-	23		dB
η_D	Drain efficiency		-	58		%
VSWR	Load mismatch	@ $P_{OUT} = 10\text{ W}$ all phases	-		20:1	

Note: $V_{DD} = 28\text{ V}$, $I_{DQ} = 100\text{ mA}$, pulsed CW, pulse width=10 μs , duty cycle = 10%

2.1 Typical performance

Figure 1. Power gain and efficiency versus output power
($f = 930\text{MHz}$, $V_{DD} = 28\text{V}$, $I_{DQ} = 0.1\text{A}$)



Figure 2. Typical capacitance characteristics

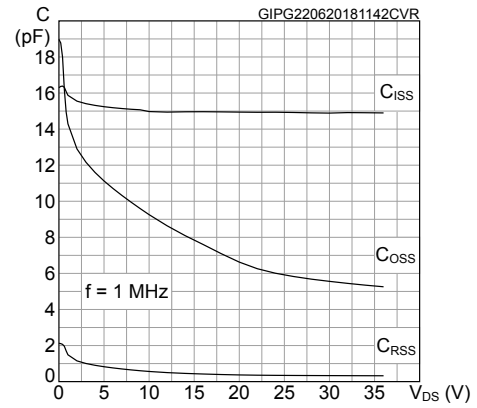


Figure 3. Typical transfer characteristics

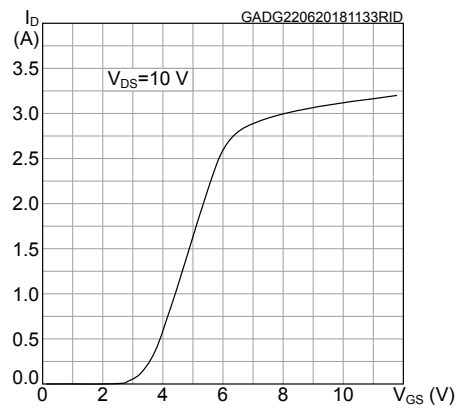


Figure 4. Gain and efficiency versus frequency @ $P_{OUT} = 10\text{ W}$ (broadband, 30 - 512 MHz)

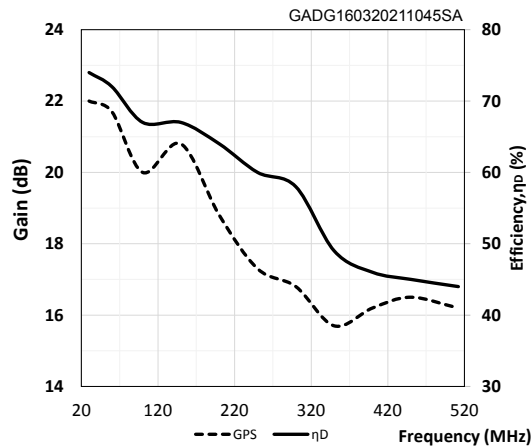
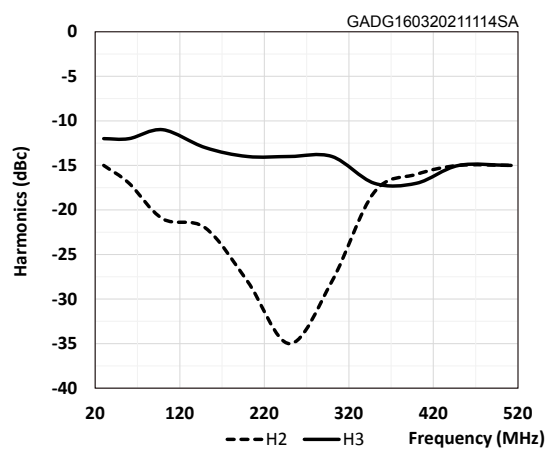


Figure 5. Harmonics versus frequency @ $P_{OUT}=10$ W (broadband, 30 - 512 MHz)



3 Test circuits

Figure 6. Test circuit photo (f=930 MHz)

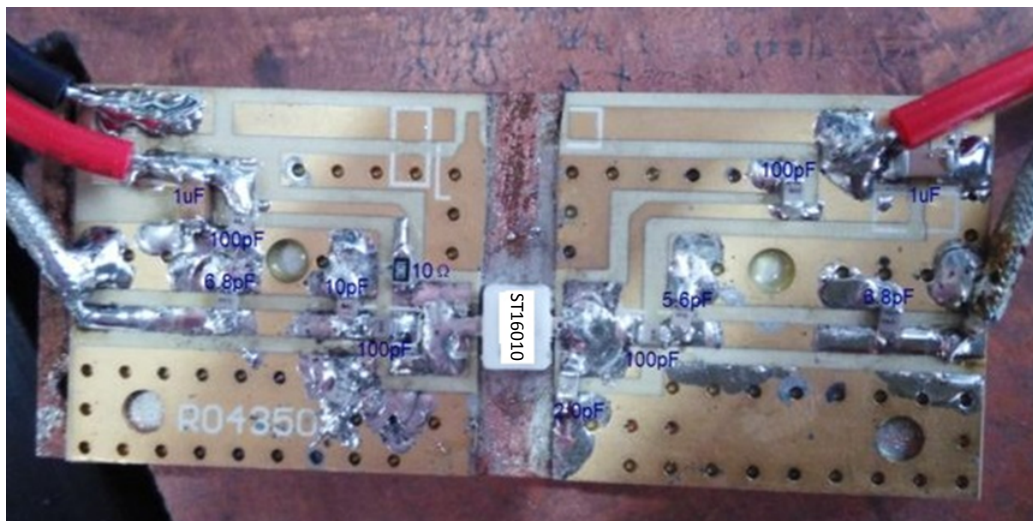
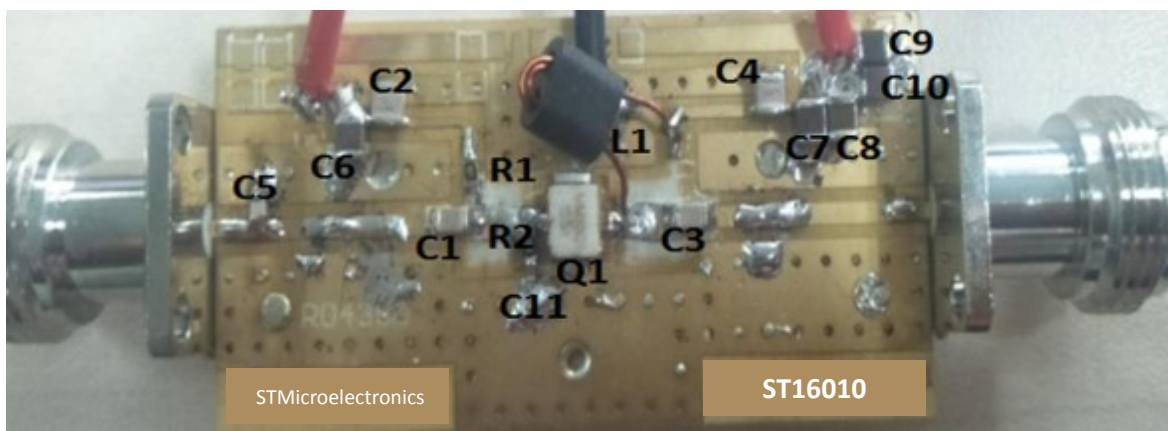


Figure 7. Test circuit photo (broadband, 30 - 512 MHz)



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Table 6. Component list (broadband, 30 - 512 MHz)

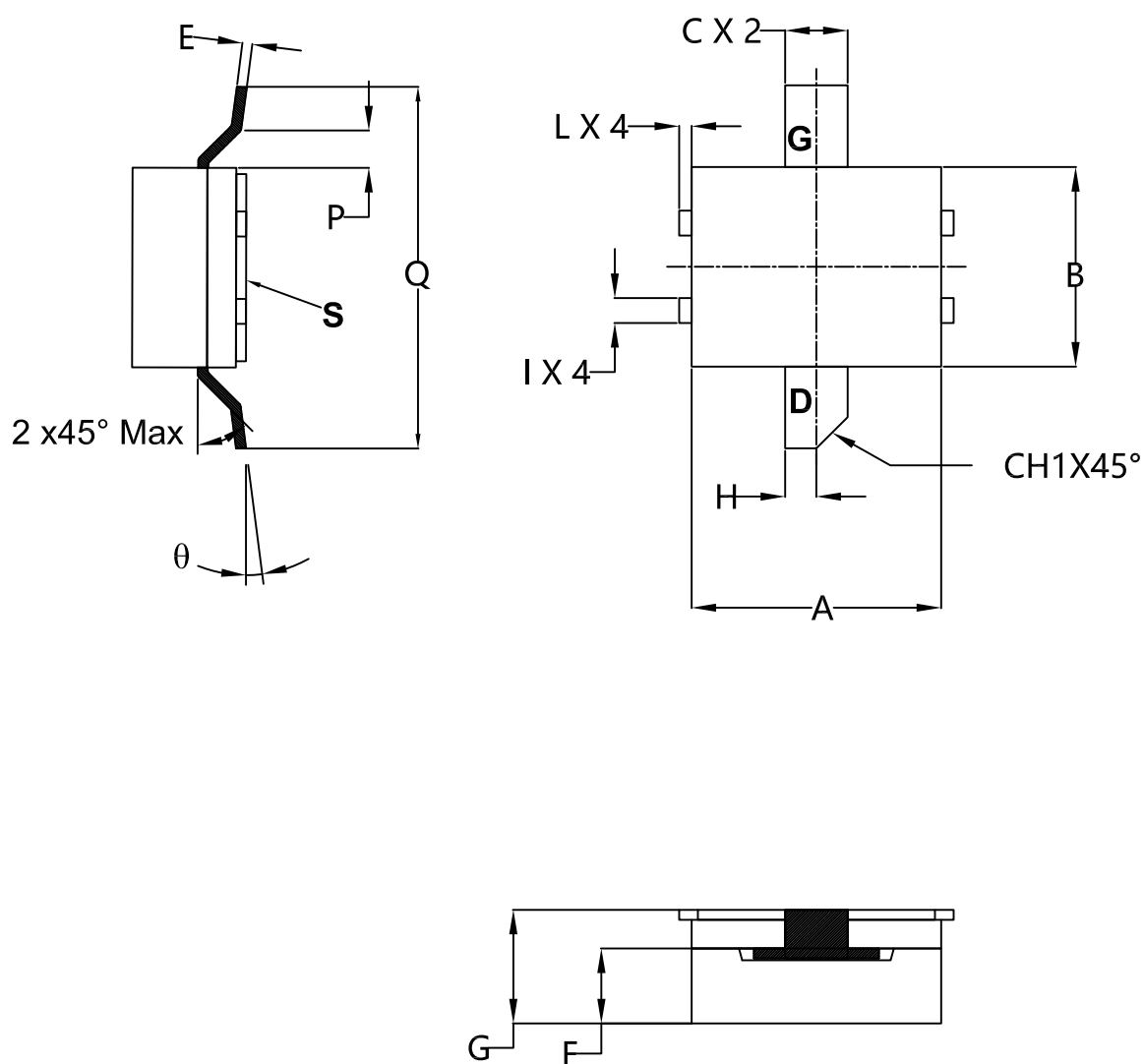
Reference	Value	Size	Reference
C1, C2, C3, C4	470 pF	1210	DLC70B
C5	8.2 pF	0805	DLC75D
C6, C7, C8, C9, C10	10 μ F	1210	50 V ceramic multilayer capacitor
R1	560 Ω	0805	Chip resistor
R2	30 Ω	0805	Chip resistor
Q1	ST16010		Package : MM
PCB	0.762 mm (0.030") thick, $\epsilon_r = 3.48$, Rogers RO4350B		

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 MM package information

Figure 8. MM package outline



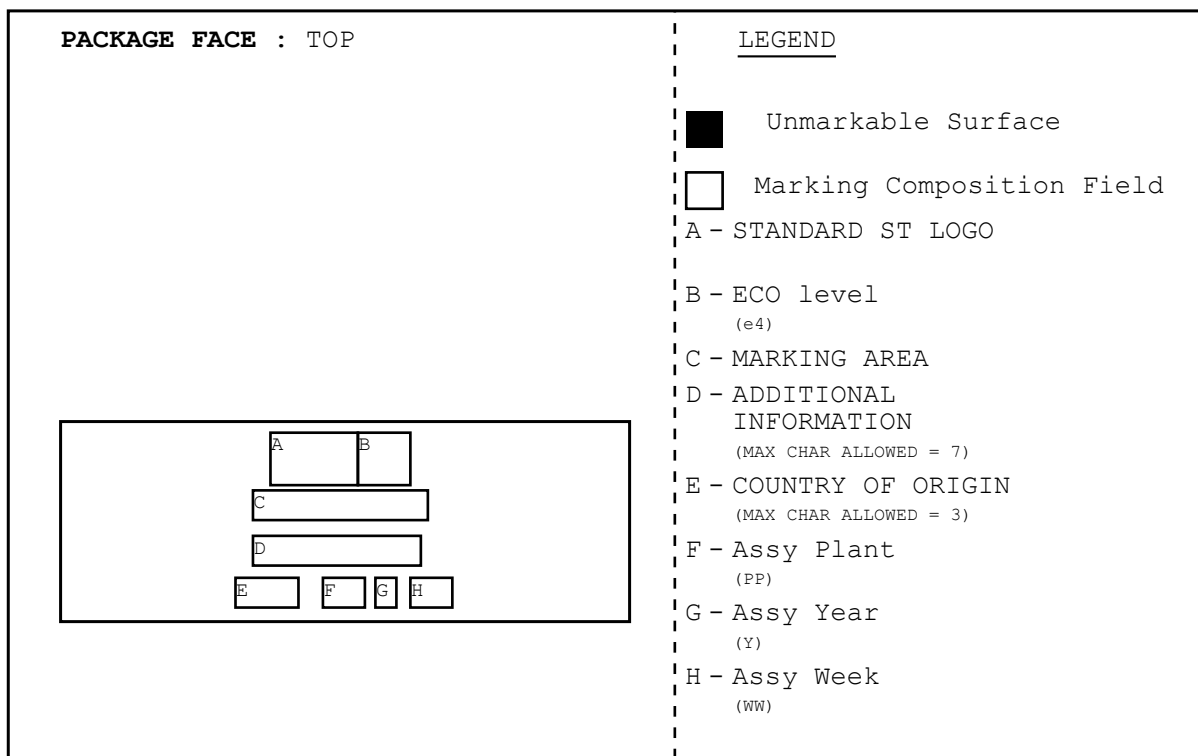
00418518_2

Table 7. MM package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.95	5.08	5.21
B	3.93	4.06	4.19
C	1.14	1.27	1.40
E	0.18	0.20	0.23
F	1.39	1.52	1.65
G	2.16		2.46
H	0.51	0.64	0.77
I	0.38	0.51	0.64
L			0.25
P	0.63	0.76	0.89
Q	7.23	7.36	7.49
CH1		0.64	
Θ	0°		7°

5 Marking information

Figure 9. Marking composition



GADG040220211644GT

Revision history

Table 8. Document revision history

Date	Version	Changes
22-Jun-2018	1	Initial release.
11-Oct-2018	2	Updated features in cover page.
13-May-2021	3	Modified silhouette, features table in cover page. Added pin connection table in cover page. Modified Table 1. Absolute maximum ratings ($T_C = 25\text{ }^{\circ}\text{C}$), Table 2. Thermal data, Table 3. ESD protection, Table 4. Static, Table 5. Dynamic. Added Figure 4. Gain and efficiency versus frequency @ $P_{OUT} = 10\text{ W}$ (broadband, 30 - 512 MHz) and Figure 5. Harmonics versus frequency @ $P_{OUT} = 10\text{ W}$ (broadband, 30 - 512 MHz). Modified Section 3 Test circuits. Added Section 5 Marking information.

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