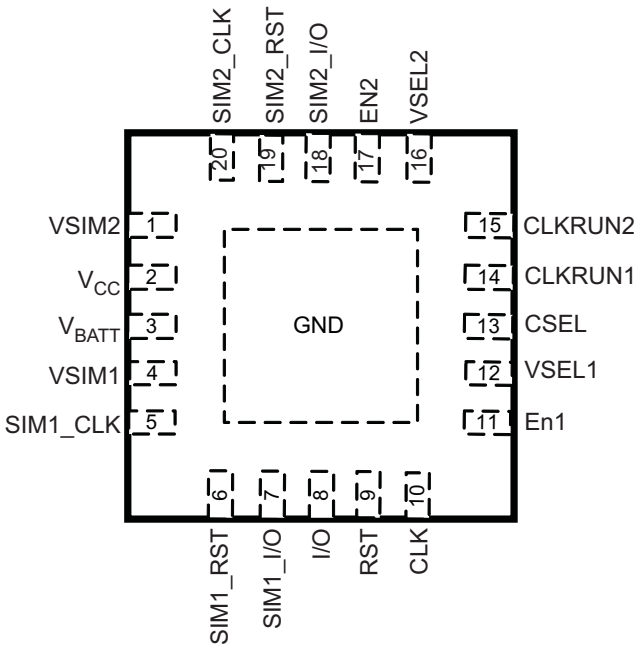
具有电平转换器和专用双LDO的双SIM卡电源

查询样品: TXS4558

特性

- 电平转换器
  - V_{CC}的电压范围 **1.65 V** 至 **3.3 V**
  - V_{BATT}的电压范围 **2.3 V** 至 **5.5 V**
- 低压降 **(LDO)** 稳压器
  - **50-mA LDO** 调节器具有可用的
  - **1.8-V** 或者 **2.95-V** 可选输出电压
  - 超低压降**:** 在**100 mV (**最大值**)** 电压下 **50 mA**
- 通过**GPIO** 接口与基带处理器实现控制和通信
- 用于 **SIM1** 和 **SIM2** 卡的分离时钟停止模式
- **ESD** 保护等级超过 **JESD 22** 标准的要求
  - **2000-V** 人体模式 **(A114-B)**
  - **500-V** 充电设备模式（**C101**）
  - **8kV HBM** 用于 **SIM** 引脚
- 封装
  - **20-**引脚 **QFN (3 mm x 3 mm)**

RUK 封装
（顶视图）



NOTE: 裸露的中心散热焊盘必须电接地。

说明

TXS4558 是一款完整的双电源待机智能身份模块 (SIM) 卡解决方案，用于将无线基带处理器与两个单独的 SIM 用户卡相连，以存储移动手机应用程序的数据。 这是一款定制器件，用于把单个 SIM/UICC 接口扩展至能够支持两个 SIM/UICC （通用集成芯片卡）。

该器件不但符合 ISO / IEC 智能卡接口要求，而且还支持 GSM 与 3G 移动标准。 它包含能够支持 Class B (2.95 V) 与 Class C (1.8 V) 接口的高速电平转换器、低压降 (LDO) 稳压器，可在 2.95 V Class B 与 1.8 V Class C 接口之间选择输出电压。 简单GPIO输入用于在两个SIM卡之间进行交换并使其进入不同模式。 电压电平转换器具有两个电源电压引脚。 VCC 负责设定用于基带接口的基准，并可采用 1.65V 至 3.3V 的工作电压。 VSIM1 和 VSIM2 被设置为
1.8V 或 2.95V，各由一个独立的内部 LDO 稳压器供电。 集成型 LDO 可接受 2.3V 至 5.5V 的输入电池电压，并向B侧电路及外部 Class B 或 Class C SIM 卡输出高达 50mA 的电流。

此外，TXS4558 还根据 SIM 卡的 ISO 7816-3 规范为 SIM 卡引脚整合了关断定序功能。 该器件不但可为 SIM 引脚提供 8 kV HBM 保护，而且还可为所有其它引脚提供标准 2kV HBM 保护。

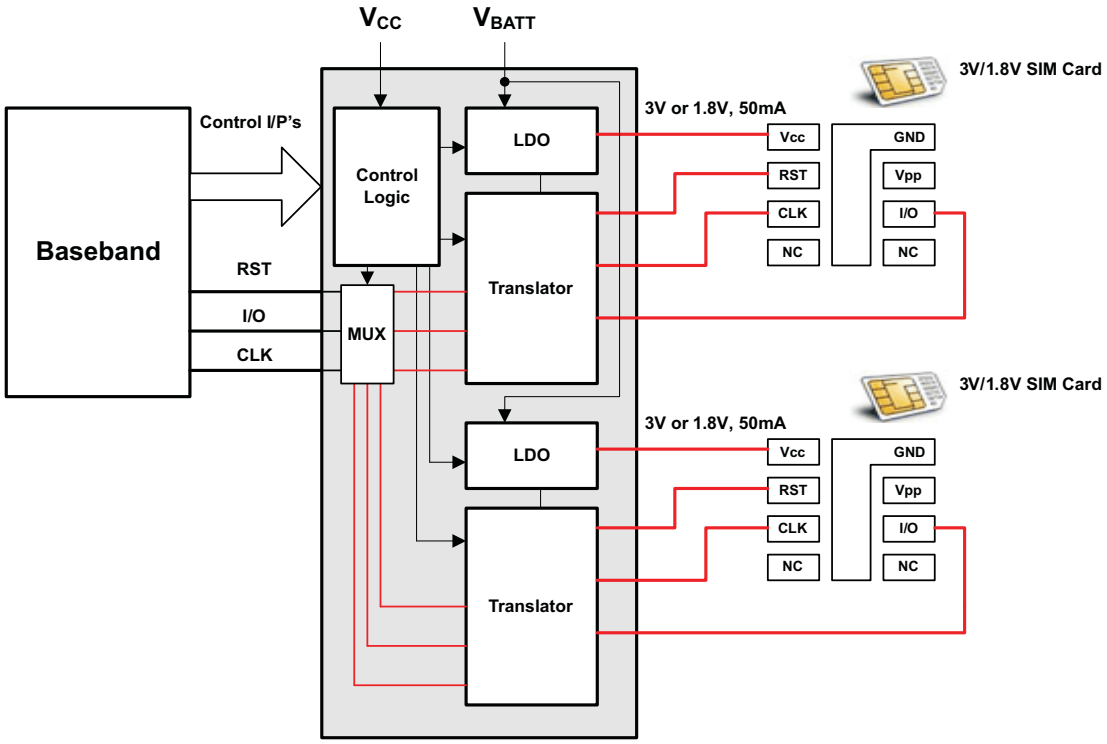
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RUK	Tape and reel	TXS4558RUKR	ZTG

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

INTERFACING THE SIM CARD



PIN FUNCTIONS(1)

NO.	NAME	TYPE(2)	POWER DOMAIN	DESCRIPTION
1	VSIM2	O	V_{BATT}	1.8 V/2.95 V supply voltage to SIM2
2	V_{CC}	P	—	1.8-V power supply for device operation and I/O buffers toward baseband
3	V_{BATT}	P	—	Battery power supply
4	VSIM1	O	VBATT	1.8 V/2.95 V supply voltage to SIM1
5	SIM1CLK	O	VSIM1	SIM1 clock
6	SIM1RST	O	VSIM1	SIM1 reset
7	SIM1I/O	I/O	VSIM1	SIM1 data
8	I/O	I/O	V_{CC}	UICC/SIM data
9	RST	I	V_{CC}	UICC/SIM reset from baseband
10	CLK	I	V_{CC}	UICC/SIM clock
11	EN1	I	V_{CC}	Enable pin for SIM1 interface
12	VSEL1	I	V_{CC}	Select pin for 1.8V or 2.95V LDO1 output
13	CSEL	I	V_{CC}	Channel select between SIM1 or SIM2

(1) Thermal Pad must be electrically connected to Ground Plane.
(2) G = Ground, I = Input, O = Output, P = Power

PIN FUNCTIONS(1) (continued)

NO.	NAME	TYPE(2)	POWER DOMAIN	DESCRIPTION
14	CLKRUN1	I	V_{CC}	Select pin for SIM1 Clock stop mode
15	CLKRUN2	I	V_{CC}	Select pin for SIM2 Clock stop mode
16	VSEL2	I	V_{CC}	Select pin for 1.8V or 2.95V LDO2 output
17	EN2	I	V_{CC}	Enable pin for SIM2 interface
18	SIM2I/O	I/O	VSIM2	SIM2 data
19	SIM2RST	O	VSIM2	SIM2 reset
20	SIM2CLK	O	VSIM2	SIM2 clock

TRUTH TABLE

CSEL	VSEL1	VSEL2	SELECTED CARD	VSIM1	VSIM2
0	0	0	1	1.8 V	1.8 V
0	0	1	1	1.8 V	2.95 V
0	1	0	1	2.95 V	1.8 V
0	1	1	1	2.95 V	2.95 V
1	0	0	2	1.8 V	1.8 V
1	0	1	2	1.8 V	2.95 V
1	1	0	2	2.95 V	1.8 V
1	1	1	2	2.95 V	2.95 V

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
LEVEL TRANSLATOR					
VCC	Supply voltage range		–0.3	4.0	V
V_I	Input voltage range	VCC-port	–0.5	4.6	V
		VSIMx-port	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state	VCC-port	–0.5	4.6	V
		VSIMx-port	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state	VCC-port	–0.5	4.6	V
		VSIMx-port	–0.5	4.6	
		Control inputs	–0.5	4.6	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current		±50		mA
	Continuous current through VCCA or GND		±100		mA
T_{stg}	Storage temperature range		–65	150	°C
LDO					
V_{BAT}	Input voltage range		–0.3	6	V
V_{OUT}	Output voltage range		–0.3	6	V
T_J	Junction temperature range		–55	150	°C
T_{stg}	Storage temperature range		–55	150	°C
	ESD rating (host side)	Human-Body Model (HBM)		2	kV
		Charged-Device Model (CDM)		500	V

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
LEVEL TRANSLATOR					
VCC	Supply voltage		1.7	3.3	V
V_{IH}	High-level input voltage	Applies to pins: EN1, EN2,RST, CLK, I/O, CLKRUN1, CLKRUN2, VSEL1, VSEL2, CSEL	VCC × 0.7	3.3	V
V_{IL}	Low-level input voltage		0	VCC × 0.3	V
Δt/Δv	Input transition rise or fall rate			5	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS — LEVEL TRANSLATOR

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VCC	VSIM1	VSIM2	MIN	TYP(1)	MAX	UNIT
V_{OH}	SIM1_RST	I_{OH} = –100 µA, Push-Pull	1.7 V to 3.3 V	1.8 V / 2.95 V, (Supplied by LDO)	1.8 V / 2.95 V, (Supplied by LDO)	VSIM1 × 0.8			V
	SIM1_CLK					VSIM1 × 0.8			
	SIM1_I/O	I_{OH} = –10 µA, Open-Drain				VSIM1 × 0.8			
	SIM2_RST	I_{OH} = –100 µA, Push-Pull				VSIM2 × 0.8			
	SIM2_CLK					VSIM2 × 0.8			
	SIM2_I/O	I_{OH} = –10 µA, Open-Drain				VSIM2 × 0.8			
	I/O	I_{OH} = –10 µA, Open-Drain				VCC × 0.8			
V_{OL}	SIM1_RST	I_{OL} = 1 mA, Push-Pull	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)			VSIM1 × 0.2	V
	SIM1_CLK							VSIM1 × 0.2	
	SIM1_I/O	I_{OL} = 1 mA, Open-Drain						0.3	
	SIM2_RST	I_{OL} = 1 mA, Push-Pull						VSIM2 × 0.2	
	SIM2_CLK							VSIM2 × 0.2	
	SIM2_I/O	I_{OL} = 1 mA, Open-Drain						0.3	
	I/O	I_{OL} = 1 mA, Open-Drain						0.3	
I_I	Control inputs	V_I = EN1,EN2, CLKRUN1, CSEL, CLKRUN2, VSEL1, VSEL2,	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)			±1	µA
$I_{CC\ I/O}$		V_I = V_{CCI}, I_O = 0	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)			±5	µA
C_{io}	SIM_I/O port						8		pF
	VSIMx port						8		
C_i	Control inputs	V_I = VCC or GND					4		pF

(1) All typical values are at T_A = 25°C.

LDO ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
VBAT	Input voltage			2.3		5.5	V
$V_{SIM1,2}$	Output voltage	Class-B Mode , 0 mA < $I_{SIM1,2}$ < 50 mA		2.85	2.95	3.05	V
		Class-C Mode , 0 mA < $I_{SIM1,2}$ < 50 mA		1.7	1.8	1.9	
V_{DO}	Dropout voltage	I_{OUT} = 50 mA				100	mV
I_{VBAT}	Operating current	V_{SIM1} = 2.95 V, V_{SIM2} = 0, ISIM1 = 0 µA			40	50	µA
		V_{SIM1} = 1.8 V, V_{SIM2} = 0, I_{SIM1} = 0 µA			40	50	
I_{SHDN}	Shutdown current (IGND)	V_{ENx} ≤ 0.4 V, (VSIMx + V_{DO}) ≤ VBAT ≤ 5.5 V, T_J = 85°C				1	µA
$I_{OUT(SC)}$	Short-circuit current	R_L = 0 Ω			145		mA
C_{OUT}	Output Capacitor				1		µF
PSRR	Power-supply rejection ratio	V_{BAT} = 3.15 V, $V_{SIM1,2}$ = 1.8 V or 2.95 V, C_{OUT} = 1 µF, I_{OUT} = 10 mA	f = 1 kHz	50			dB
			f = 10 kHz	40			
T_{STR}	$V_{SIM1,2}$ Start-up time	$V_{SIM1,2}$ = 1.8 V or 3 V, I_{OUT} = 50 mA, C_{OUT} = 1 µF				400	µS
T_J	Operating junction temperature			–40		125	°C

(1) All typical values are at T_A = 25°C.

GENERAL ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{I/OPU}$	I/O pull-up		16	20	24	kΩ
R_{SIMPU}	SIM_I/O pull-up	SIM enabled and selected with CSEL	7.4	8.0	8.7	kΩ
R_{SIMPD}	SIM_I/O pull-down	Active pull-downs are connected to the VSIM regulator output to the SIM_CLK, SIM_RST, SIM_I/O when EN = 0			2	kΩ

SWITCHING CHARACTERISTICS – VSIMx = 1.8 V or 2.95 V Supplied by Internal LDO

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VCC = 1.8 V ± 0.15 V		UNIT
			MIN	MAX	
t_{rA}	I/O	C_L = 50 pF		1	µs
t_{rB}	SIMx_RST			1	µs
	SIMx_CLK			50	ns
	SIMx_I/O			100	ns
f_{max}	SIMx_CLK			25	MHz
Duty Cycle	SIMx_CLK		40%	60%	

OPERATING CHARACTERISTICS

T_A = 25°C, V_{SIMx} = 1.8 V

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}(1)	Class C (CLK, RST)	VCC-port input, VSIMx-port output	C_L = 0 f = 5 MHz t_r = t_f = 1 ns	12.7	pF
	Class B (CLK, RST)	VCC-port input, VSIMx-port output		15.4	
	CLASS C (IO)	VCC-port input, VSIMx-port output		10.8	pF
	CLASS B (IO)	VCC-port input, VSIMx-port output		20.3	

(1) Power dissipation capacitance per transceiver

PIN FUNCTION

PIN NAME	PIN NUMBER	PIN FUNCTION
VCC	2	Power supply and voltage reference for device operation and I/O buffers toward baseband.
VBATT	3	This is the battery power supply for the TXS4558.
VSIM1, VSIM2	1,4	1.8 V/2.95 V supply voltage for the respective SIM1 and SIM2. These outputs are activated through the EN1 and EN2 pins and set to be 1.8V or 2.95V through VSEL1 and VSEL2.
SIMCLK, SIM2CLK	5, 20	These are voltage level shifted CLK signals for connection to SIM1 and SIM2. Functionality while the corresponding SIM is not selected via CSEL is controlled by CLKRUN1 and CLKRUN2 control pins.
SIM1RST, SIM2RST	6, 19	These are voltage level shifted RST signals for connection to SIM1 and SIM2. Their output level when de-selected is latched at the last state.
SIM1IO, SIM2IO	7, 18	These are voltage level shifted IO signals for connection to SIM1 and SIM2. These are bi-directional data signals.
IO	8	Microcontroller side data IO pin. The IO pin provides the bidirectional communication path to the SIM cards. The SIMxIO communicating with IO is selected by CSEL.
RST	9	Microcontroller side reset RST pin input. RST provides signals directly to the selected SIM SIMxRST. When a SIM interface is deselected with CSEL, the last RST value is held at the SIMxRST.
CLK	10	The CLK pin supplies the clock signal to the cards. It is level shifted and transmitted directly to the SIMxCLK pin of the selected card. If CLKRUNx is HIGH, the clock signal will be transmitted to the SIMxCLK pin, regardless of whether that card is selected.
EN1, EN2	11, 17	EN1 and EN2 enable and disable the power supply to SIM1 and SIM2, and the corresponding interface.
VSEL1, VSEL2	12, 16	These pins set the VSIM1 and VSIM2 voltages and the corresponding interface IO voltages. When VSELx is low, VSIMx is 1.8V. When VSELx is high, VSIMx is 2.95V.
CSEL	13	CSEL selects which SIM is activated and communicates with the baseband. When CSEL is low, SIM1 is active. When CSEL is high, SIM2 is active.
CLKRUN1, CLKRUN2	14, 15	The CLKRUN1 and CLKRUN2 control the functionality of the SIM1CLK and SIM2CLK pins when their corresponding SIM cards are deselected using CSEL. When CLKRUNx is high, the CLK signal is transmitted to the corresponding SIMxCLK, even when the card is deselected with CSEL. When CLKRUNx is low, the SIMxCLK signal is brought low when the corresponding SIM is deselected with CSEL.
Exposed Center Pad	21	This center pad must be connected to ground.

OPERATION

Clock Run Mode

SIMS have varying requirements for the SIM CLK. Using CLKRUN, the user can decide if the SIMxCLK pin continuously transmits the CLK signal, or is brought low when the SIM is deselected with CSEL. If CLKRUNx is LOW, the SIMxCLK is brought LOW two clock cycles after the SIMx is deselected with CSEL. If SIMxCLK is high, the CLK transmits to the SIMxCLK, even if the SIMx is deselected with CSEL.

CSEL

When a channel is deselected using the CSEL pin, the SIMxRST state is latched, the SIMxIO becomes high impedance and SIMxCLK function is dependent on CLKRUNx.

Operation Activation/Deactivation

When the EN1, EN2 pin is brought high, the device performs the activation sequence for the corresponding SIM interface. Each SIM interface is activated independently based on its EN IO.

Activation Sequence

1. The device holds SIMxIO, SIMxCLK and SIMxRST low.
2. VSIMx is activated and powered.
3. The device waits for the VSIMx output to reach the correct voltage. Once this voltage is reached, SIMxIO, and SIMxRST are enabled.
4. The SIMxCLK is activated on the 2nd rising edge after the SIMxIO is enabled.

When the ENx pin is brought low, the device performs the deactivation sequence for the corresponding SIM interface. Deactivation Sequence,

Deactivation Sequence

1. SIMxRST is deactivated and set low.
2. Two clock cycles after EN is brought LOW, the SIMxCLK is disabled and brought LOW. If the CLK is not active, SIMxCLK is disabled and brought low approximately 9us after ENx is brought low.
3. Approximately 9us after the ENx is brought LOW, SIMxIO is disabled and set LOW.
4. After SIMxIO is brought LOW, the VSIMx is deactivated and unpowered.

APPLICATION INFORMATION

The LDO's included on the TXS4558 achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR at very low headroom (V_{BAT} – $V_{SIM1/2}$). The TXS4558 provides fixed regulation at 1.8V or 2.95V. Low noise, GPIO enable and low ground pin current make it ideal for portable applications. The device offers current limit and thermal protection, and is fully specified from –40°C to 125°C.

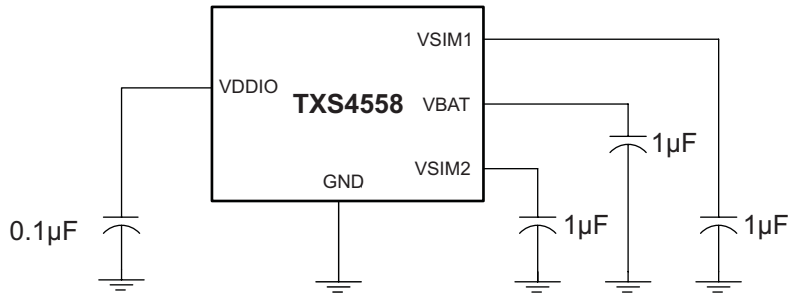


Figure 1. Typical Application Circuit for TXS4558

Input and Output Capacitor Requirements

It is good analog design practice to connect a 1.0 µF low equivalent series resistance (ESR) capacitor across the input supply (VBAT) near the regulator. Also, a 0.1µF is required for the logic core supply (VCC).

This capacitor will counteract reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. The LDO's are designed to be stable with standard ceramic capacitors of values 1.0 µF or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be <1.0 Ω.

Output Noise

In most LDO's, the bandgap is the dominant noise source. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for VIN and VOUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Curent Limit

The TXS4558 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TXS4558 has a built-in body diode that conducts current when the voltage at VSIM1/2 exceeds the voltage at VBAT. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

Dropout Voltage

The TXS4558 uses a PMOS pass transistor to achieve low dropout. When (V_{BAT} – $V_{SIM1/2}$) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} will approximately scale with output current because the PMOS device behaves like a resistor in dropout.

Startup

The TXS4558 uses a quick-start circuit which allows the combination of very low output noise and fast start-up times.

Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

Minimum Load

The TXS4558 is stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TXS4558 employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TXS4558 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the TXS4558 into thermal shutdown will degrade device reliability.

TYPICAL CHARACTERISTICS

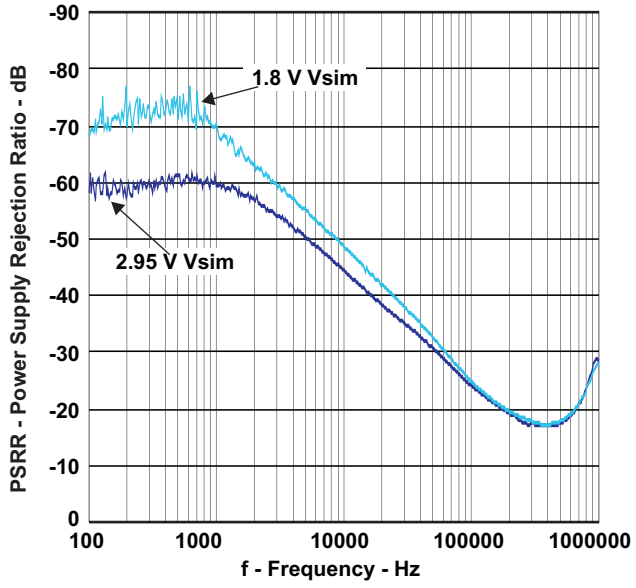


Figure 2. PSRR

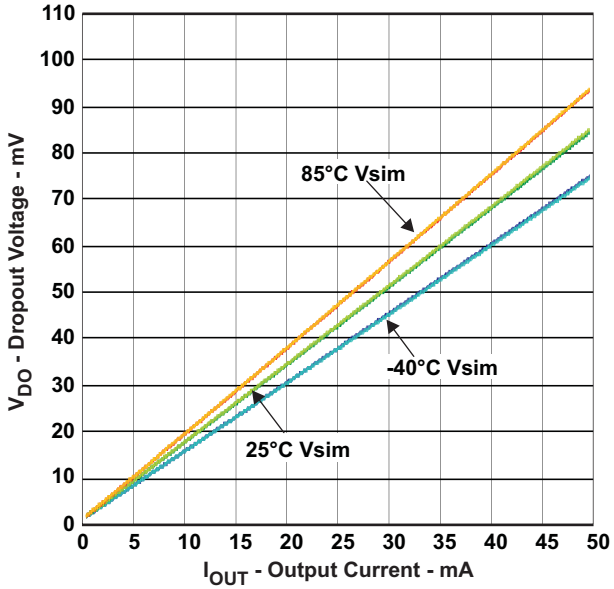


Figure 3. Dropout Voltage vs Output Current

TYPICAL CHARACTERISTICS (continued)

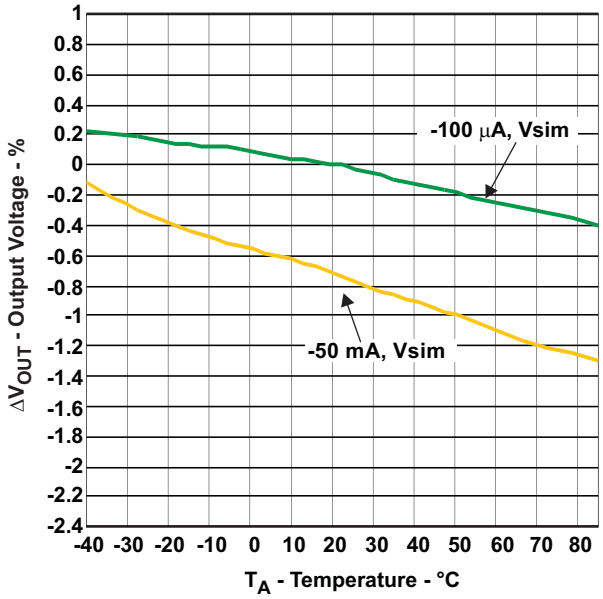


Figure 4. Output Voltage vs Temperature, Class-B/C

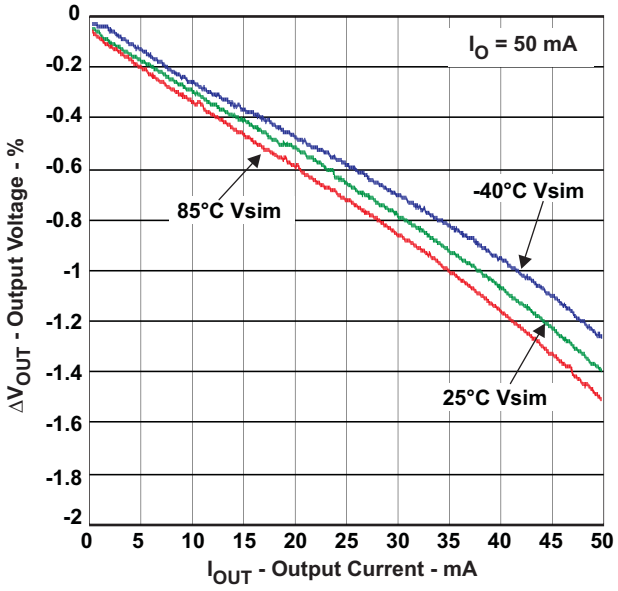


Figure 5. Load Regulation, Iout = 50 mA, Class-C

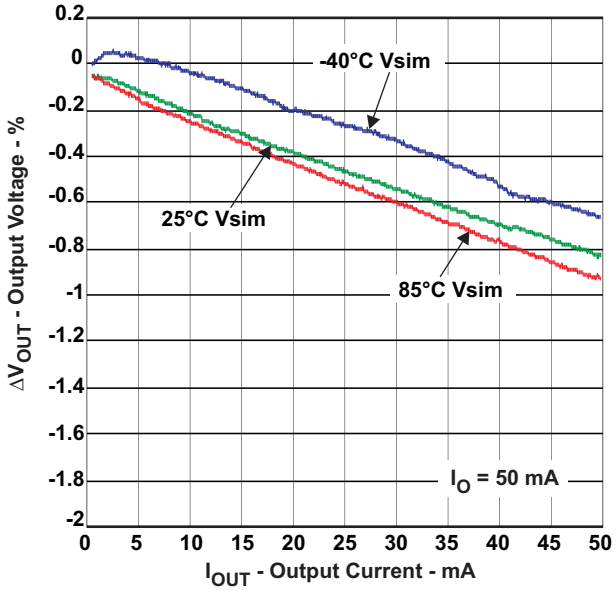


Figure 6. Load Regulation, Iout = 50 mA, Class-B

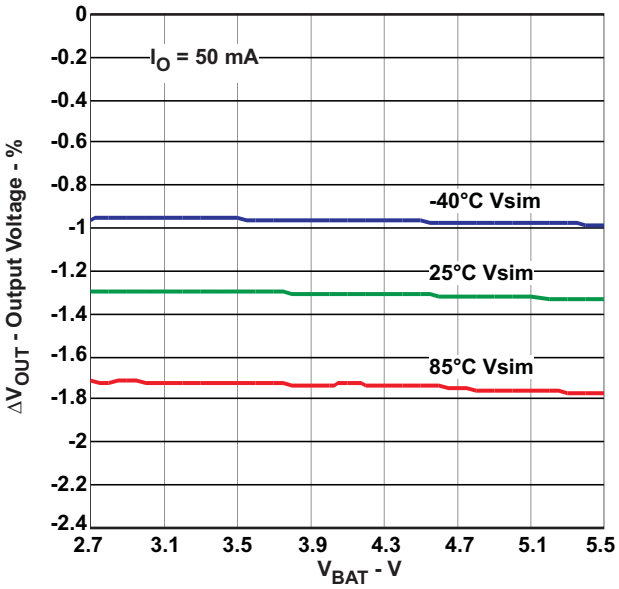


Figure 7. Line Regulation, Iout = 50 mA, Class-C

TYPICAL CHARACTERISTICS (continued)

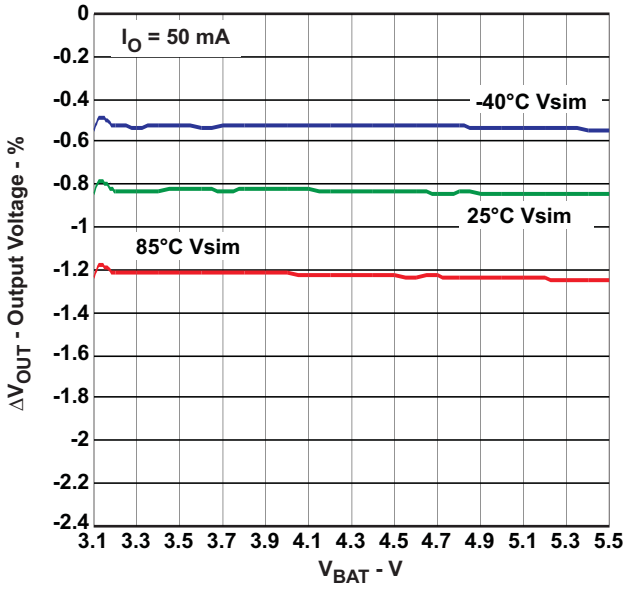


Figure 8. Line Regulation, Iout = 50 mA, Class-B

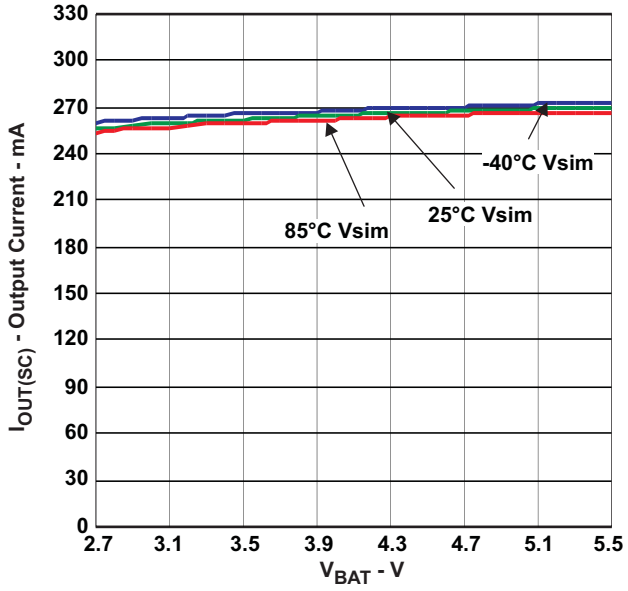


Figure 9. Current Limit vs Input Voltage, Class-B/C

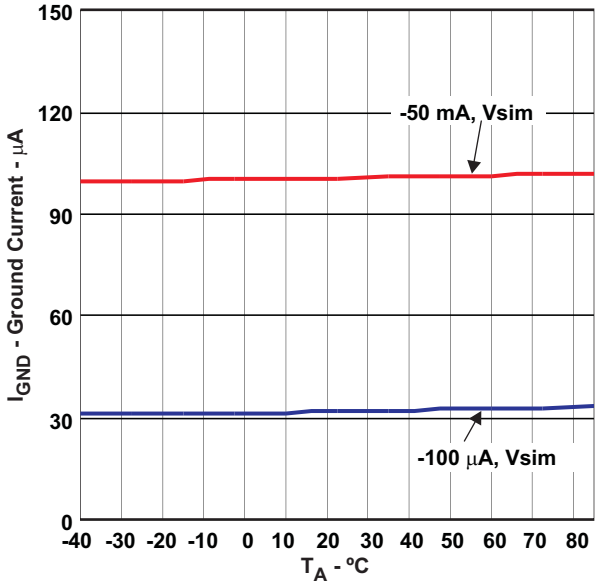


Figure 10. Ground Current vs Temperature, Class-C

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS4558RUKR	ACTIVE	WQFN	RUK	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

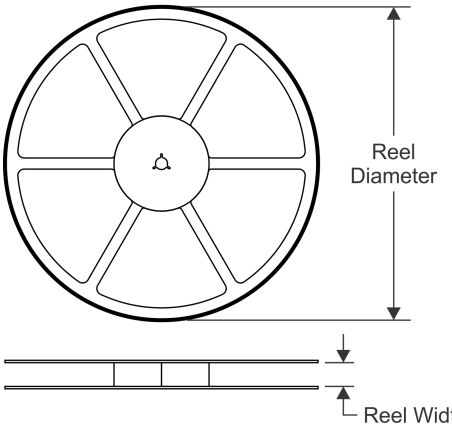
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

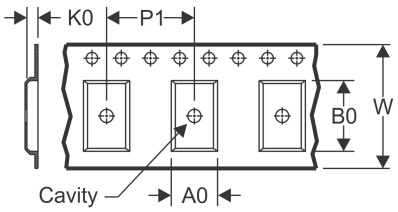
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

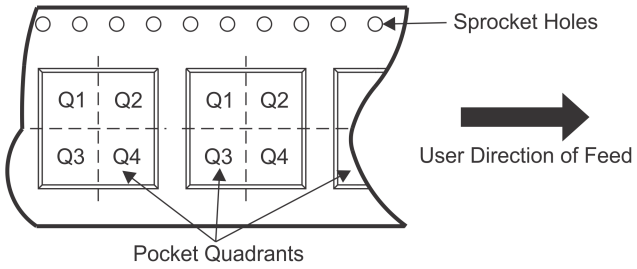


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

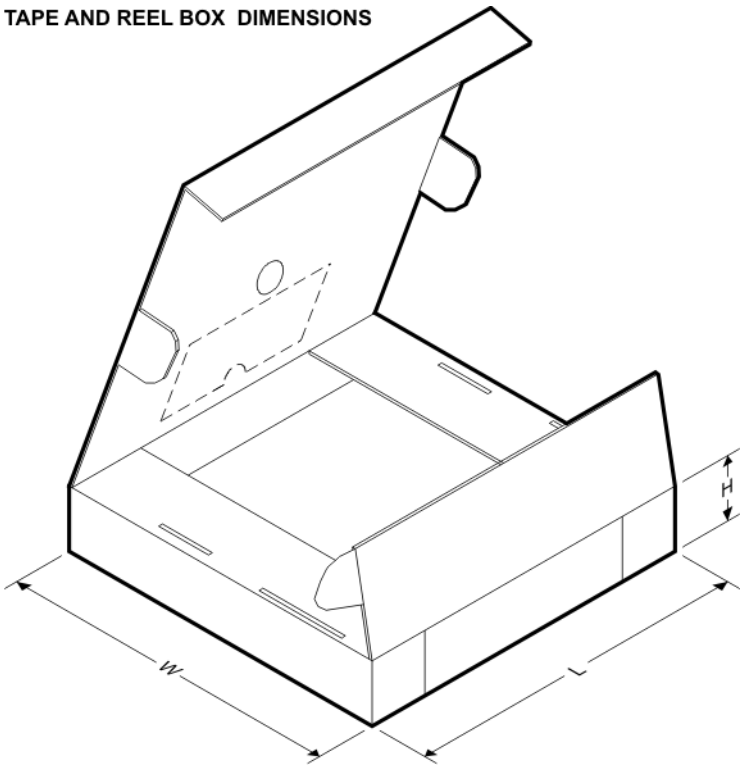
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS4558RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

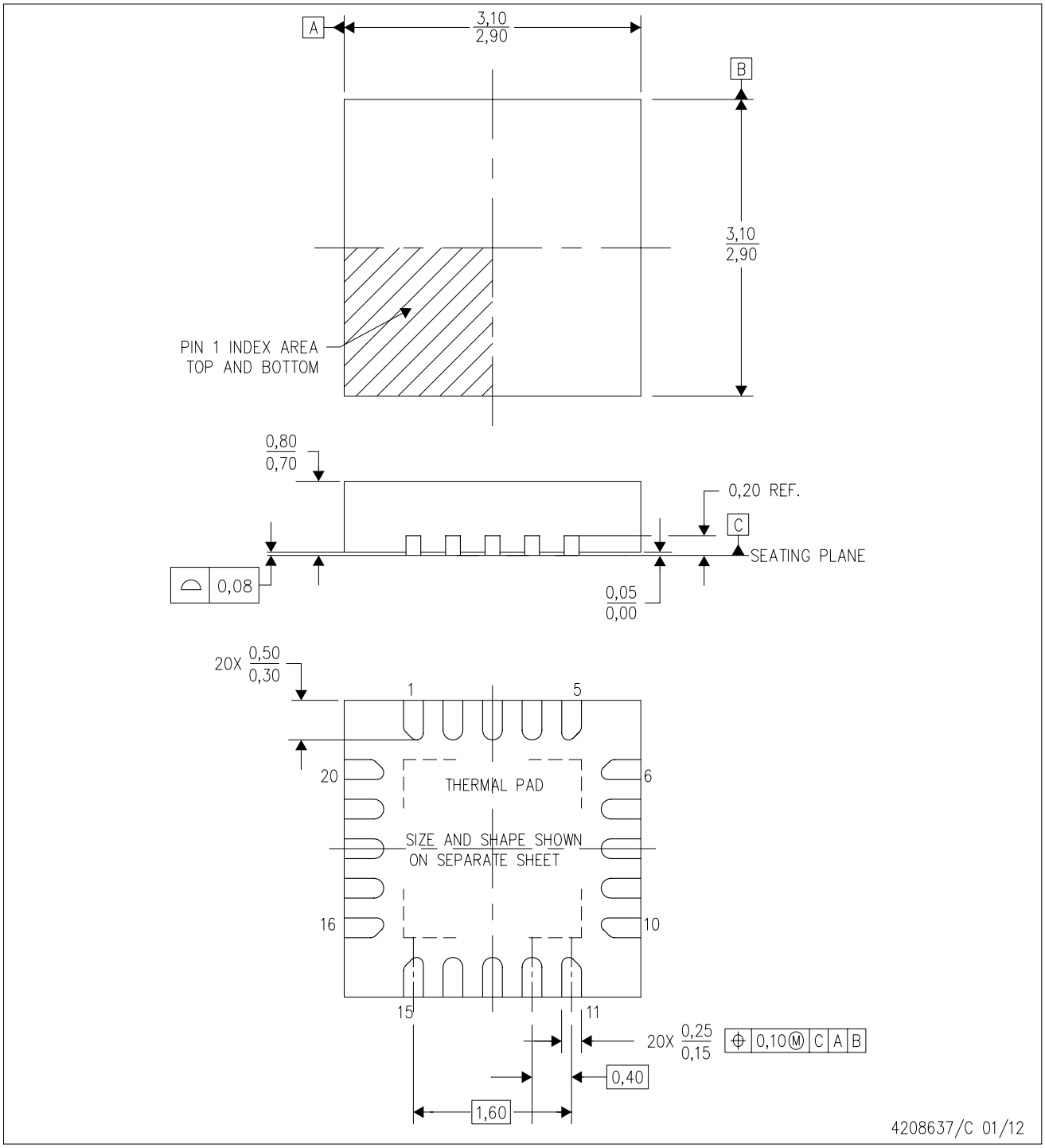
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS4558RUKR	WQFN	RUK	20	3000	367.0	367.0	35.0

RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

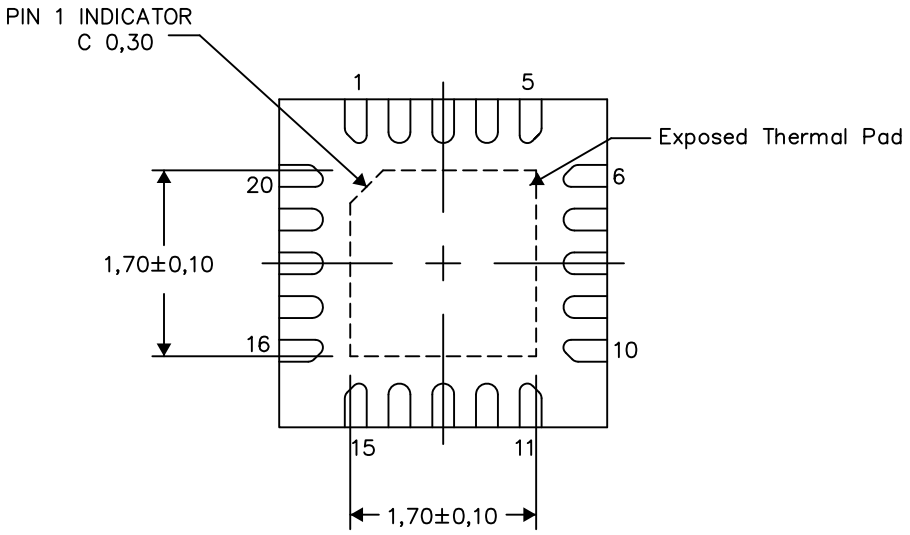
RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



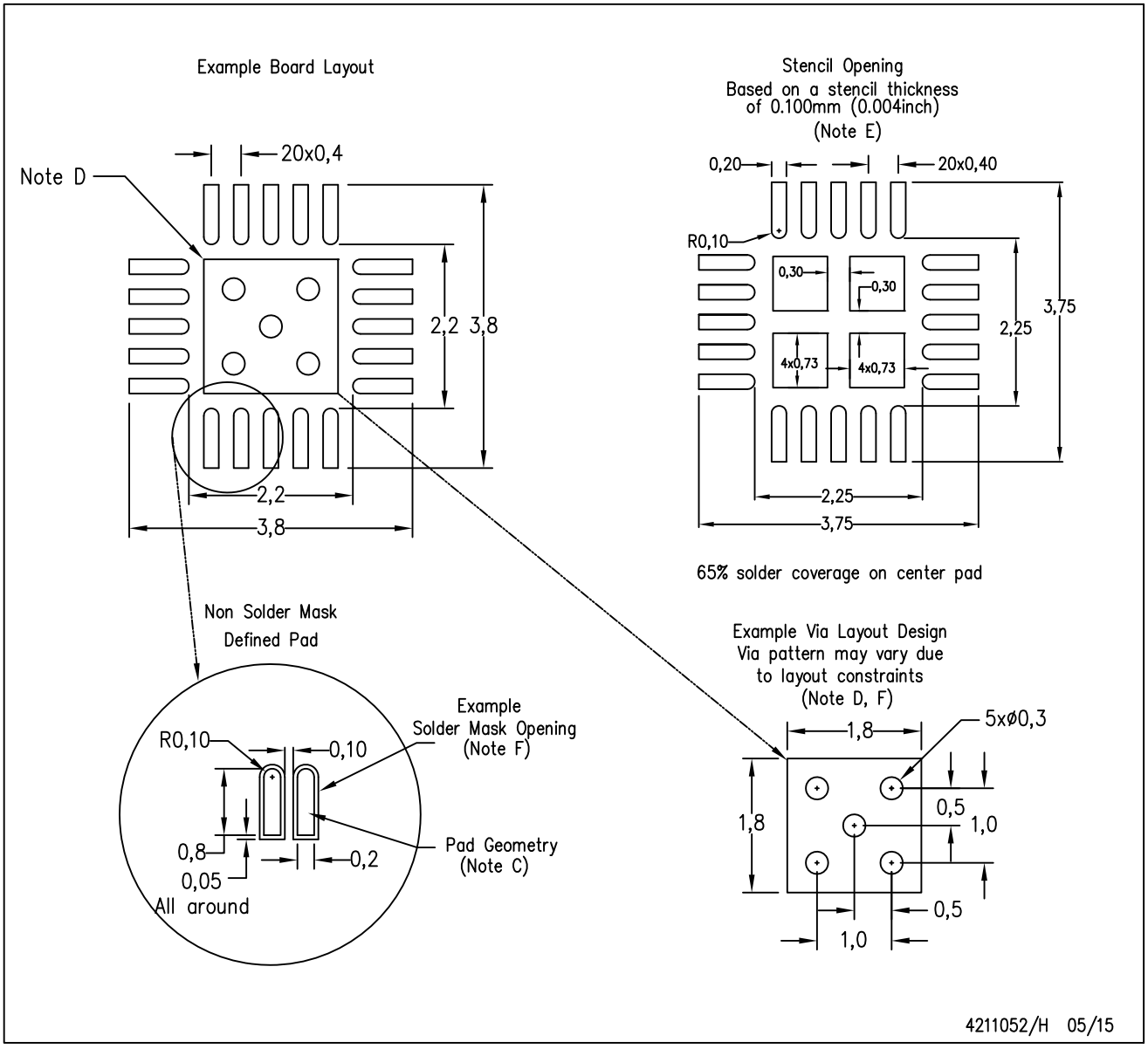
Bottom View

Exposed Thermal Pad Dimensions

4209762/I 05/15

NOTE: All linear dimensions are in millimeters

RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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