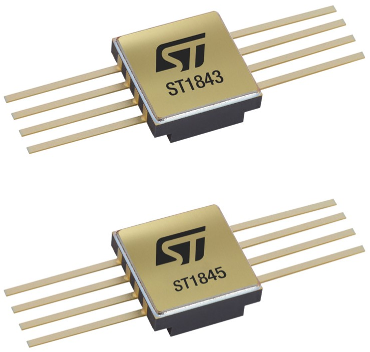
ST1843, ST1845

Datasheet

Rad-hard current mode PWM controller



FLAT-8 metallic lid floating

Features

- Oscillator frequency guaranteed at 250 kHz
- Trimmed oscillator for precise frequency control
- Current mode operation to 500 kHz automatic feed forward compensation
- Latching PWM for cycle-by-cycle current limiting
- Internally trimmed reference with undervoltage lockout
- High current totem pole output
- Undervoltage lockout with hysteresis
- Low start-up (<0.5 mA) and operating current
- Ceramic hermetic package Flat-8 metallic lid floating
- ST1843 50 krad (Si)
- ST1845 100 krad (Si)
- SEL free @ 120 MeV/cm2/mg at 125 °C
- ESCC qualified as 9108/020 and 9108/021

Description

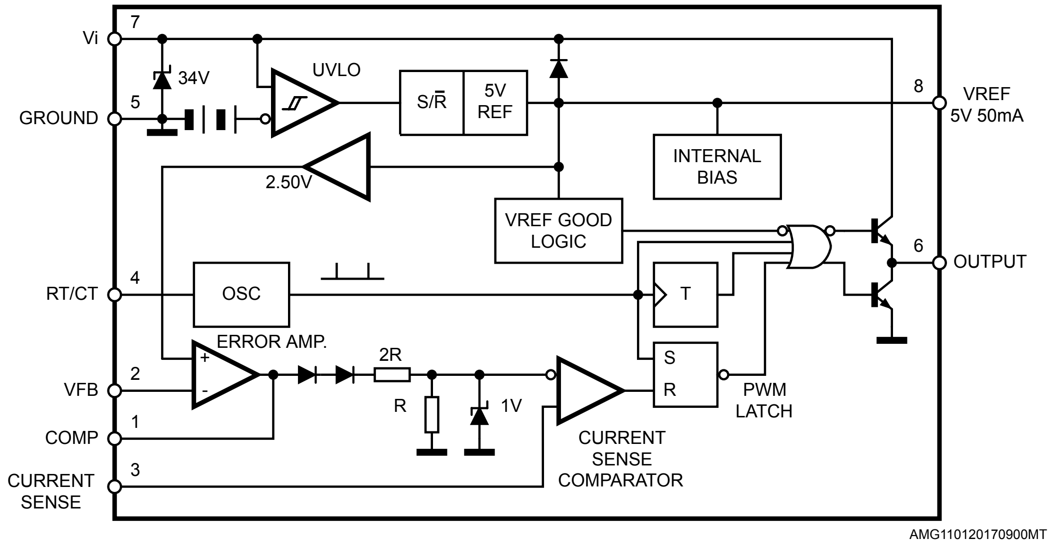
The ST1843 and ST1845 ICs are rad-hard current mode PWM controllers providing an industry standard solution for the implementation of off-line or DC to DC fixed-frequency current mode control schemes with a minimal external part count.

Its radiation hardness, hermetic packaging and its ESCC qualification make it an ideal choice for aerospace and other harsh environments.

Product status link
ST1843, ST1845

1 Block diagram

Figure 1. Block diagram (toggle flip-flop used in the ST1845 only)



2 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_i	Supply voltage (low impedance source)	30	V
	Supply voltage (Ii < 30 mA)	Self-limiting	
I_O	Output current	±1	A
E_O	Output energy (capacitive load)	5	µJ
	Analog inputs (pins 2, 3)	-0.3 to 5.5	V
	Error amplifier output sink current	10	mA
P_{tot}	Power dissipation at $T_A \leq 25$ °C	800	mW
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Junction operating temperature	-55 to 150	°C

Note: All voltages are with respect to pin 5, all currents are positive into the specified terminal.

3 Thermal data

Table 2. Thermal data

Symbol	Description	Flat-8	Unit
R_{thj-a}	Thermal resistance junction-ambient conditions: 2s2p board as per std Jedec spec. JESD51-7 board size: 76.2x114.5x1.6 mm outer layers: 20% Cu inner layers: 90% Cu natural convection, T_{AMB} = 25 °C. 100 µm air- gap between package and board filled in with glue (k = 1 W/m°K)	47.7	°C/W
Rthj-c top	Package top case (lid cap side) in contact with a cold plate (infinite heat sink like) as per std Jedec spec JESD51-12	20.4	
Rthj-b	Ring cold plate as per std Jedec spec JESD51-8	34.7	

4 Pin connection

Figure 2. Pin connection

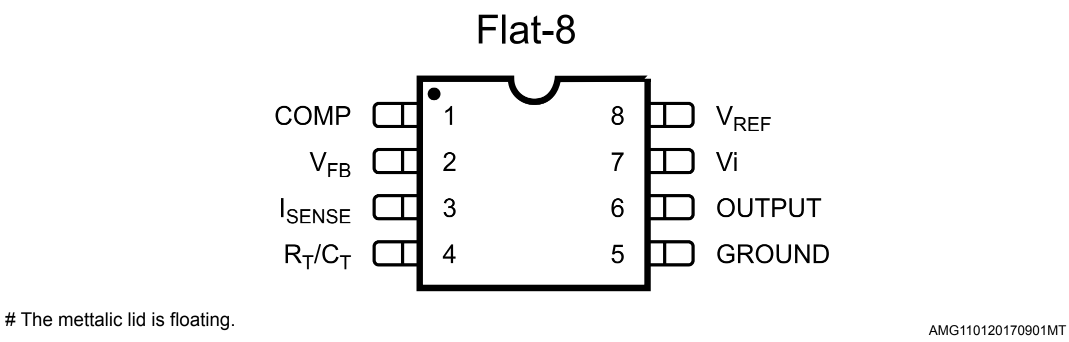


Table 3. Pin functions

No	Function	Description
1	COMP	This pin is the error amplifier output and is made available for loop compensation.
2	V_{FB}	This is the inverting input of the error amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor RT to Vref and capacitor CT to ground. Operation to 500 kHz is possible.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1 A are sourced and sunk by this pin.
7	V_i	This pin is the positive supply of the control IC.
8	V_{ref}	This is the reference output. It provides charging current for capacitor CT through resistor RT.

5 Electrical characteristics

Maximum package power dissipation limits must be respected; low duty cycle pulse techniques are used during test maintain T_J as close to T_A as possible.

Unless otherwise stated, these specifications apply for -T_A = 22 ±3 °C, V_i = 15 V, adjust V_i above the start threshold before setting at 15 V; R_T = 10 kΩ; C_T = 3.3 nF.

Table 4. Electrical characteristics

Symbol	MIL-STD-883 test method	Parameter	Test conditions	Values		Unit
				Min.	Max.	
Reference section						
V_{REF}		Output voltage	I_O = 1 mA	4.95	5.05	V
ΔV_{REF_LINE}		Line regulation	12 V ≤ V_i ≤ 25 V		0.02	V
ΔV_{REF_LOAD}		Load regulation for ST1843	1 mA ≤ I_O ≤ 20 mA		19	mV
		Load regulation for ST1845			25	
I_{SC}	3011	Output short-circuit		-0.18	-0.03	A
Oscillator section						
f_{OSC}		Frequency for the ST1843	1 mA ≤ I_O ≤ 20 mA	49	55	kHz
		Frequency for the ST1845		24.5	27.5	
$\Delta f_{OSC}/\Delta V$		Frequency change with voltage	12 V ≤ V_I ≤ 25 V	-	1	%
I_{dischg}		Discharge current for the ST1843	1 mA ≤ I_O ≤ 20 mA; V_{OSC} = 2 V	8.1	8.8	mA
		Discharge current for the ST1845		8.3		
Error amp section						
V_{FB}		Input voltage	V_{PIN1} = 2.5 V	2.45	2.55	V
I_b	4001	Input bias current	V_{FB} = 5 V	-1		μA
A_{VOL}		A_{VOL}	2 V ≤ V_O ≤ 4 V	65		dB
PSRR	4003	Power supply rejec. ratio for the ST1843	12 V ≤ V_i ≤ 25 V	67		dB
		Power supply rejec. ratio for the ST1845		68		
I_{o_sink}		Output sink current	V_{PIN2} = 2.7 V; V_{PIN1} = 1.1 V	6		mA
I_{o_source}		Output source current	V_{PIN2} = 2.2 V; V_{PIN1} = 5 V		-1	mA
V_{OH}		V_{OUT} high for the ST1843	V_{PIN2} = 2.3 V; R_L = 15 kΩ to GND	6.2		V
		V_{OUT} high for the ST1845		5.4		
V_{OL}		V_{OUT} low	V_{PIN2} = 2.7 V; R_L = 15 kΩ to pin 8 (V_{REF})		0.95	V
Current sense section						

Symbol	MIL-STD-883 test method	Parameter	Test conditions	Values		Unit
				Min.	Max.	
G_V	4004	Gain	R_T = 10 kΩ; C_T = 3.3 nF[(1)(2)]	2.85	3.15	V/V
V_3		Maximum input signal	V_{PIN1} = 5 V[(1)]	0.9	1.05	V
SVR		Supply voltage rejection for the ST1843	12 V ≤ V_i ≤ 25 V	74		dB
		Supply voltage rejection for the ST1845		72		
I_b	4001	Input bias current			-10	µA
D_O	3003	Delay to output			300	ns
Output section						
V_{OL1}	3007	Output low level for the ST1843	I_{SINK} = 20 mA		0.26	V
		Output low level for the ST1845			0.18	
V_{OL2}		Output low level	I_{SINK} = 200 mA		2.2	V
V_{OH1}	3006	Output high level	I_{SOURCE} = 20 mA	13		V
V_{OH2}			I_{SOURCE} = 200 mA	12		V
V_{OLS}		UVLO saturation	V_I = 6 V; I_{SINK} = 1 mA		1.1	V
t_r	3004	Rise time	C_L = 1 nF		150	ns
t_f		Fall time			150	ns
Undervoltage lock-out section						
V_{TH}		Start threshold		7.8	9	V
V_{MIN}		Min. operating voltage after turn-on for the ST1843		7	8.2	V
		Min. operating voltage after turn-on for the ST1845			8	
DC_{MAX}		Max. duty cycle for the ST1843		94	100	%
		Max. duty cycle for the ST1845		47	50	%
DC_{MIN}		Min. duty cycle			0	%
Total standby current						
I_{st}		Start-up current			0.5	mA
I_i	3005	Operating supply current	V_{PIN2} = V_{PIN3} = 0 V		17	mA
V_{iz}		Zener voltage	I_i = 25 mA	30		V

1. *Parameter measured at trip point of latch with V_{PIN2} = 0.*
2. *Gain defined as:*

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}};\ 0 \leq \Delta V_{PIN3} \leq 0.8\,V$$

6 Radiation

The technology of the STMicroelectronics rad-hard current mode PWM controller is resistant to radioactive environments.

The product radiation hardness assurance is supported by a total ionisation dose (TID) tested at low dose rate and a single effect event (SEE) characterization.

6.1 Total dose radiation (TID) testing

The ST184x are qualified, tested and characterized in full compliance with the ESCC22900 “Low Rate” window: 36 to 360 rad/h.

A characterization in total ionizing dose has been done at very low dose rate, i.e. 36 rad/h, on each device type on 5 parts biased and 5 parts unbiased.

Each wafer lot is tested at low dose rate, in the worst bias case condition, based on the results obtained during the initial qualification.

Both pre-irradiation and post-irradiation performance has been tested using the same circuitry and test conditions. A direct comparison can be done (T_{amb}= 22±3 °C unless otherwise specified).

The following parameters were measured:

- Before irradiation
- After irradiation at final dose
- After 24 hrs at room temperature
- After 168 hrs at 100 °C anneal

Table 5. **Total dose performance**

Feature	Conditions	Max. value	Unit
Total-ionization dose immunity	ST1843 low dose rate. Compliance with electrical measurements for total dose radiation testing	50	krad(Si)
	ST1845 low dose rate. Compliance with electrical measurements for total dose radiation testing	100	

Unless otherwise stated, these specifications apply for -T_A = 22 ±3 °C, V_i = 15 V, adjust V_i above the start threshold before setting at 15 V; R_T = 10 kΩ; C_T = 3.3 nF

Table 6. Post radiation electrical characteristics

Symbol	Parameter	Test conditions	Values		Unit
			Min.	Max.	
Reference section					
V_{REF}	Output voltage for the ST1843	I_O = 1 mA	4.85	5.15	V
	Output voltage for the ST1845			5.15	
ΔV_{REF_LINE}	Line regulation	12 V ≤ V_i ≤ 25 V		0.02	V
ΔV_{REF_LOAD}	Load regulation	1 mA ≤ I_o ≤ 20 mA		0.025	V
I_{SC}	Output short-circuit current		-0.18	-0.03	A
Oscillator section					
F_{OSC}(1)	Frequency		49	65	kHz
ΔF_{OSC} / ΔV	Frequency change with voltage	12 V ≤ V_i ≤ 25 V	-1	1	%
IDISCHG	Discharge current	V_{OSC} = 2 V	0.0078	0.0088	A
Error amp section					
V_2	Input voltage for the ST1843	VPIN1 = 5 V	2.45	2.6	V
	Input voltage for the ST1845		2.45	2.55	
I_b	Input bias current the ST1843	V_{FB} = 5 V	-2.75		µA
	Input bias current ST1845		-2.8		
AVOL	AVOL for the ST1843	2 V ≤ V_o ≤ 4 V	60		dB
	AVOL for the ST1845		62		
PSRR	Power supply rejection ratio	12 V ≤ V_i ≤ 25 V	60		dB
IO_SINK	Output sink current	VPIN2 = 2.7 V; VPIN1 = 1.1 V	2		mA
IO_SOURCE	Output source current	VPIN2 = 2.3 V; VPIN1 = 5 V		-0.5	mA
V_{OH}	VOUT high	VPIN2 = 2.3 V; RL = 15 K to GND	5		V
V_{OL}	VOUT low	VPIN2 = 2.3 V; R_L = 15 kΩ to pin		1.1	V
Current sense section					
G_V	Gain		2.85	3.15	V/V
V3	Maximum input signal	VPIN1 = 2.3 V	0.9	1.1	V
SVR	Supply voltage rejection	12 V ≤ V_i ≤ 25 V	60		dB
I_b	Input bias current ST1843		-50		µA
	Input bias current ST1845		-45		
D_O	Delay to output			300	ns
Output section					
V_{OL1}	Output low level	I_{SINK} = 20 mA		0.4	V
V_{OL2}	Output low level	I_{SINK} = 200 mA		2.2	V
V_{OH1}	Output high level	I_{SOURCE} = 20 mA	13		V
V_{OH2}	Output high level	I_{SOURCE} = 200 mA	12		V
V_{OLS}	UVLO saturation	I_{SINK} = 1 mA		1.1	V
T_R	Rise time	C_L = 1 nF		180	ns
T_F	Fall time	C_L = 1 nF		180	ns

Symbol	Parameter	Test conditions	Values		Unit
			Min.	Max.	
Undervoltage lock-out section					
V_{TH}	Start threshold for the ST1843		7.8	9.5	V
	Start threshold for the ST1845		7.8	10.5	
V_{MIN}	Min. operating voltage after turn-on for the ST1843		7	8.6	V
	Min. operating voltage after turn-on for the ST1845		7	9	
DCMAX	Max. duty cycle for the ST1843		94	100	%
	Max. duty cycle for the ST1845		47	50	
DCMIN	Min. duty cycle			0	%
Total standby current					
I_{ST}	Start-up current	V_i = 6.5 V		0.5	mA
I_i	Operating supply current	VPIN2 = VPIN3 = 0 V		17	mA
Viz	Zener voltage	I_i = 25 mA	30		V

1. *For the ST1845 the limits applies to the internal frequency of the device before the output divider by 2. The limits for the external frequency are divide by 2 ,i.e. 24.5 kHz min and 32.5 kHz max.*

6.2 Single event effect

A Single event effect characterization has been performed on the qualification lots only. They have been performed according to single event effects test method ESCC basic specification number 25100. SEE tests have been characterized in RADEF (FI). The single event effect (SEE) relevant to power integrated circuits are characterized, i.e. the single event latch-up (SEL) and single event transient (SET).

The accept/reject criteria are:

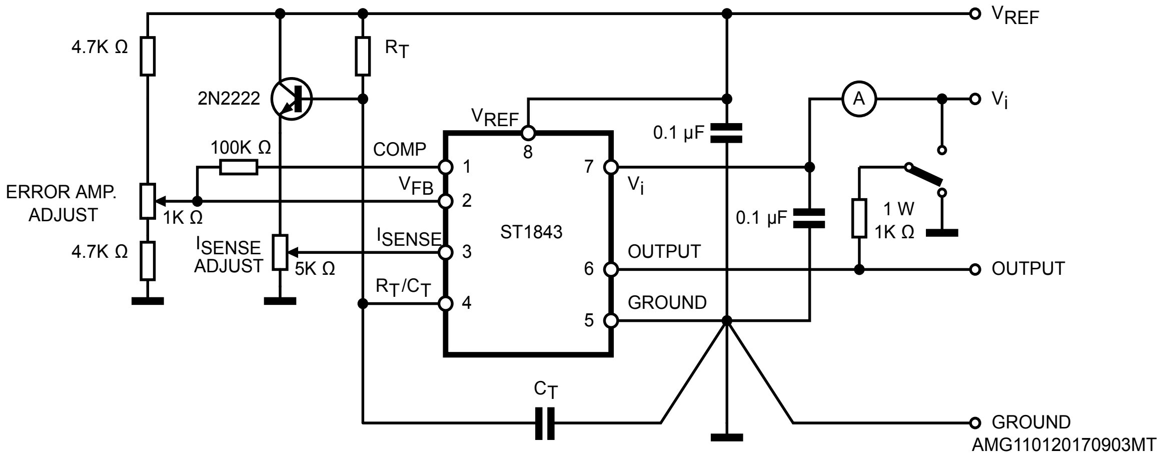
- SEL: the device is biased during irradiation. Ambient temperature for the SEL test is 125 °C. The test is stopped as soon as a SEL occurs or when the consumption is above the nominal current level or when the overall fluency on the component reaches $1e^{7}$ cm².
- SET: the device is biased during irradiation. Ambient temperature for the SET test is 25 °C. A SET is recorded when an event occurs on the output. The run is stopped when the overall fluency on the component reaches $1e^{6}$ cm²

Table 7. Radiation hardness assurance summary

Feature	Parameter	Conditions	Value	Unit
SEL immunity	Linear energy transfer (LET)	Range ≥ 40 µm, V_{IN} = 30 V, T_A = +125 °C. No destructive events	120	MeV.cm²/mg
SET performance	Linear energy transfer threshold (LETth)	V_{IN} = 15 V f^{osc} = 80 kHz and 200 kHz	1.5	MeV.cm²/mg
	ST1843 saturated cross-section		1.15 $e\text{-}^{2}$	cm²
	ST1845 saturated cross-section		7.20 e^{-3}	cm²

7 Test circuit

Figure 3. **Open loop test circuit**



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5 kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 4. **Timing resistor vs oscillator frequency**

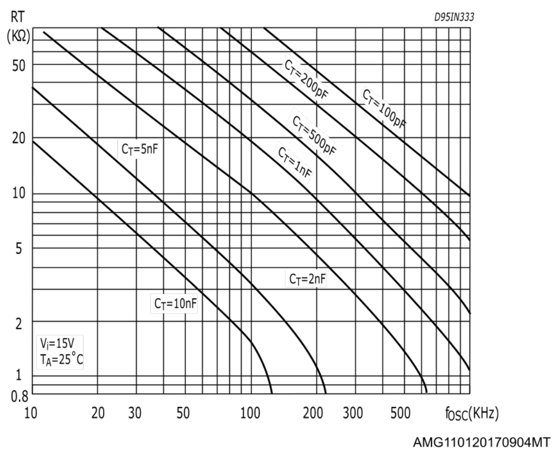


Figure 5. **Output dead-time vs oscillator frequency**

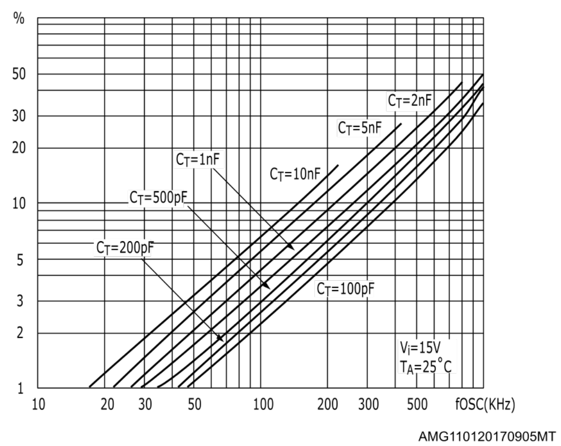


Figure 6. Oscillator discharge current vs temperature

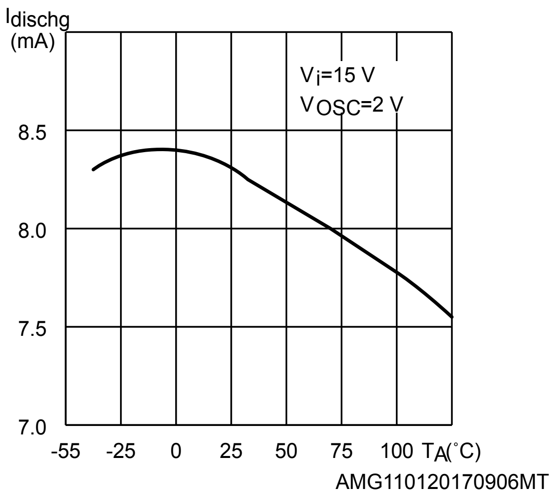


Figure 7. Maximum output duty cycle vs timing resistor

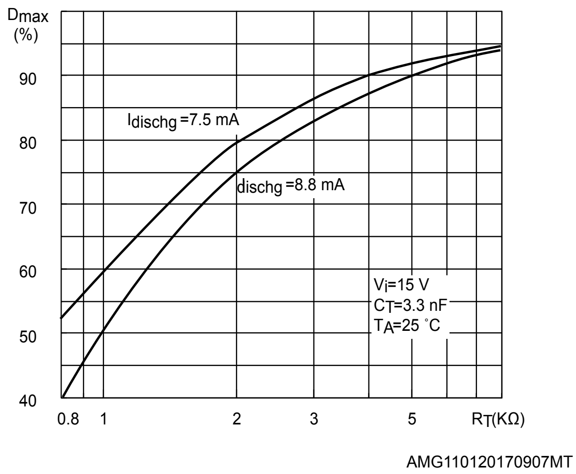


Figure 8. Error amp open-loop gain and phase vs frequency

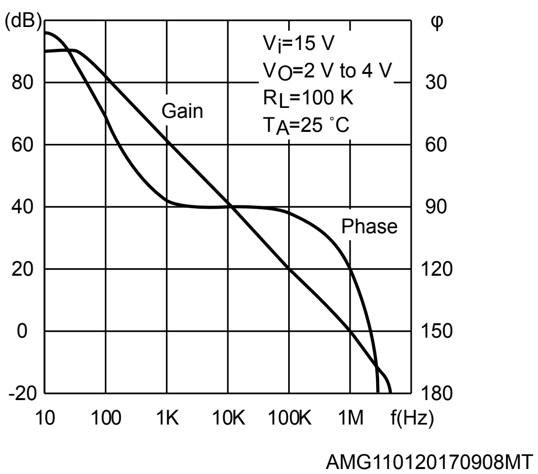


Figure 9. Current sense input threshold vs error amp output voltage

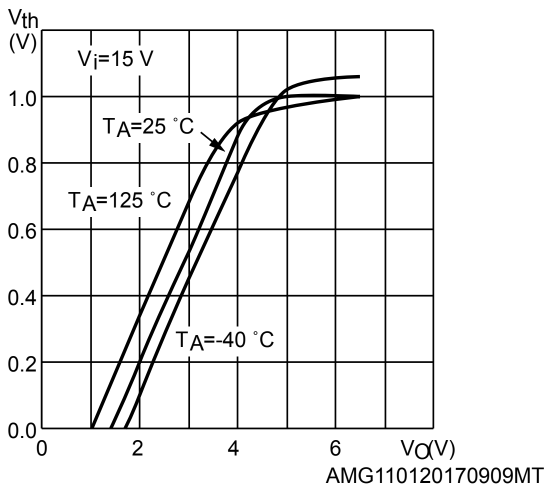


Figure 10. Reference voltage change vs source current

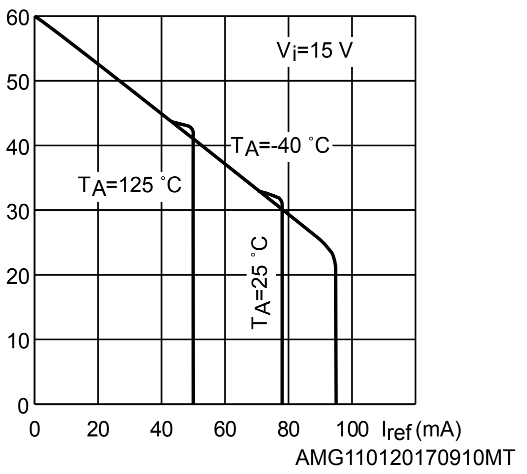


Figure 11. Reference short-circuit current vs temperature

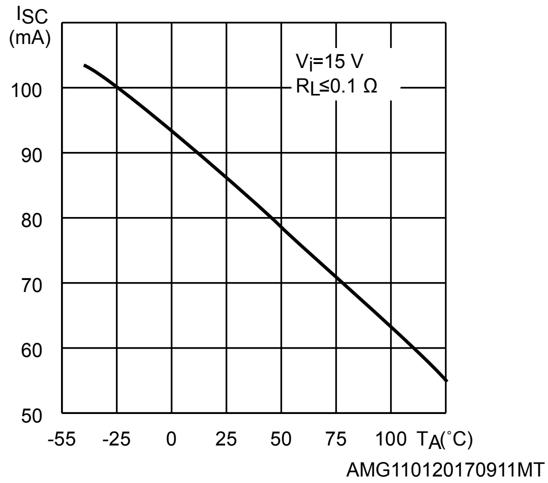


Figure 12. Output saturation voltage vs load current

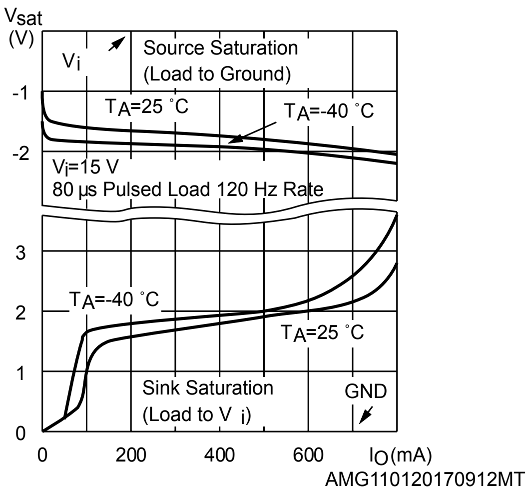


Figure 13. Supply current vs supply voltage

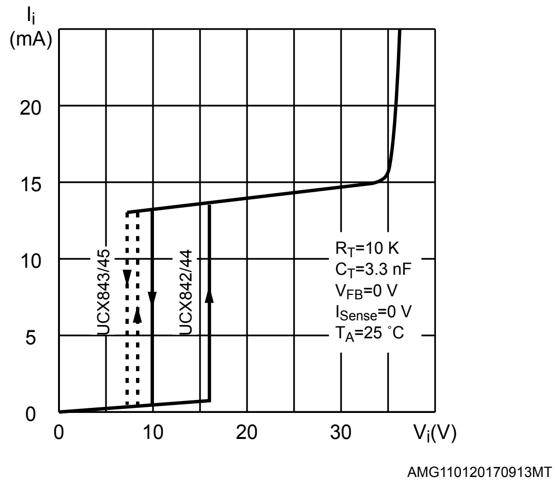


Figure 14. Output waveform

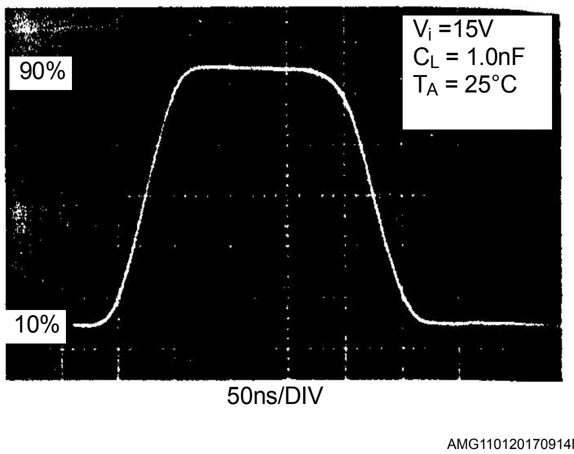


Figure 15. Output cross conduction

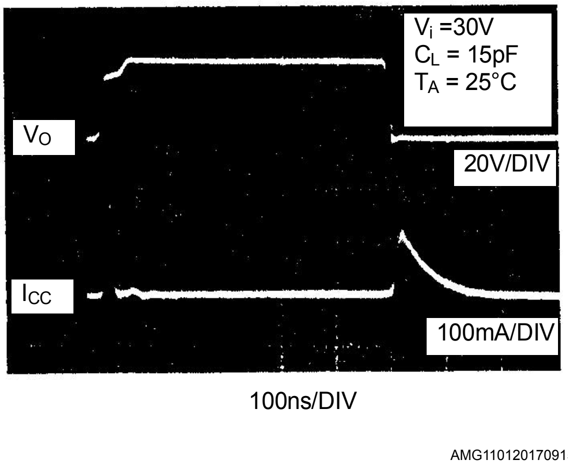


Figure 16. Oscillator and output waveforms

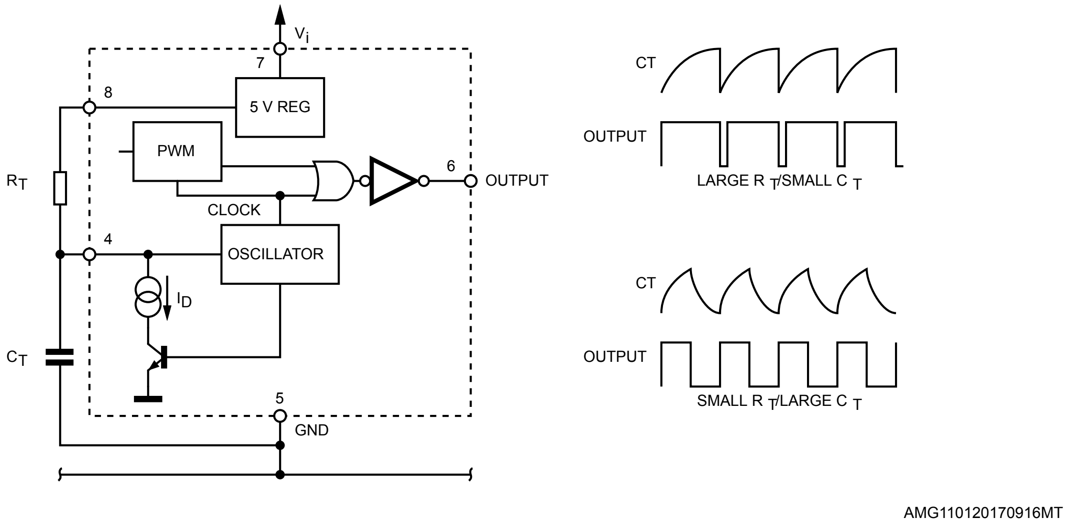


Figure 17. Error amp configuration

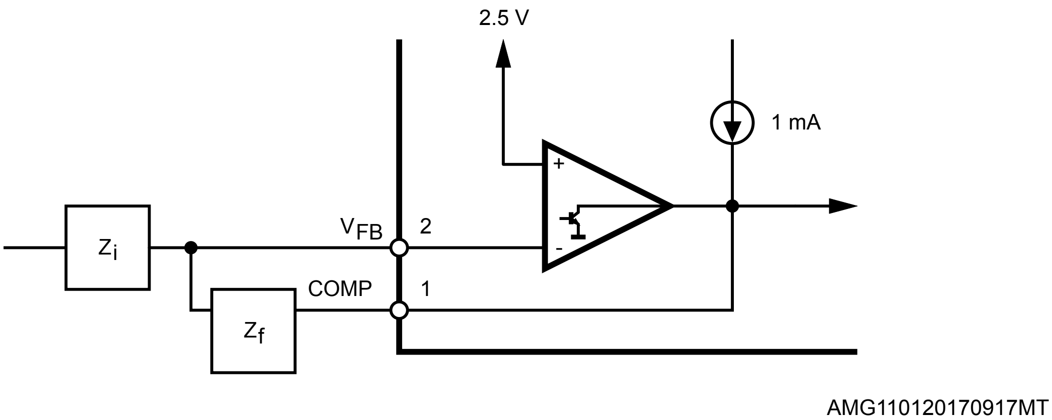
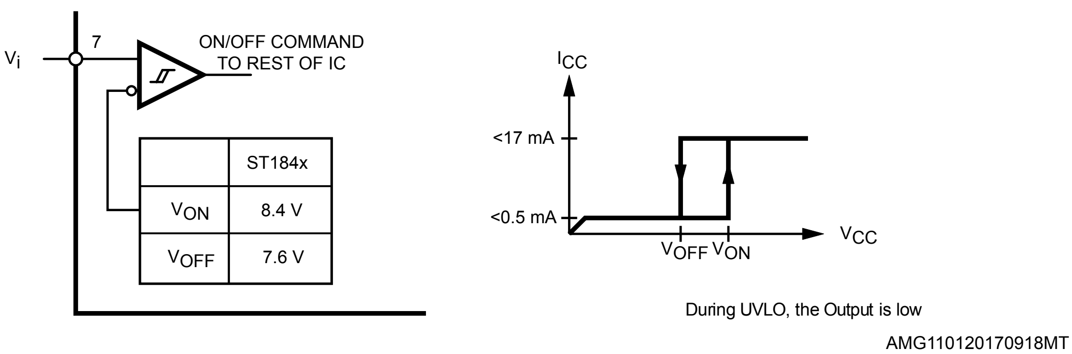
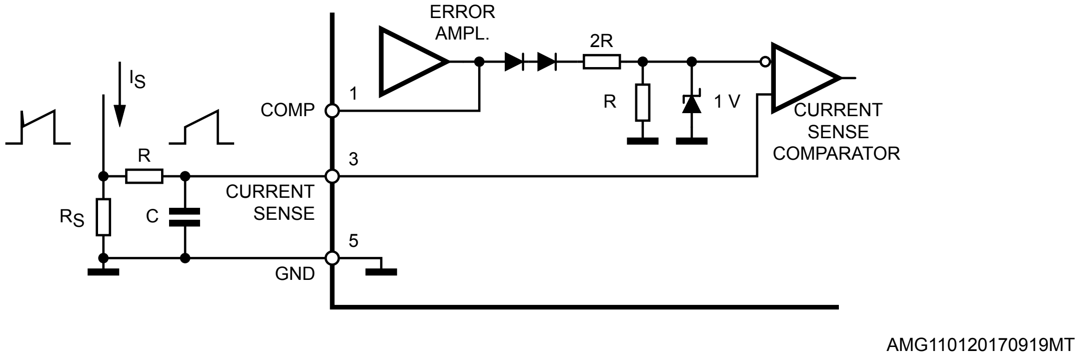


Figure 18. Undervoltage lockout



	ST184x
V_{ON}	8.4 V
V_{OFF}	7.6 V

Figure 19. Current sense circuit



Peak current (is) is determined by the formula:

$$I_{Smax} \approx \frac{1.0\ V}{R_S} \quad (1)$$

A small RC filter may be required to suppress switch transients.

Figure 20. Slope compensation techniques

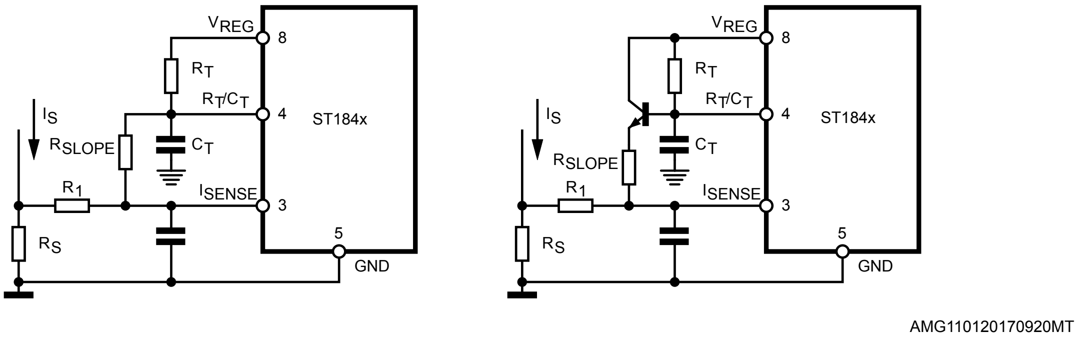


Figure 21. Isolated MOSFET drive and current transformer sensing

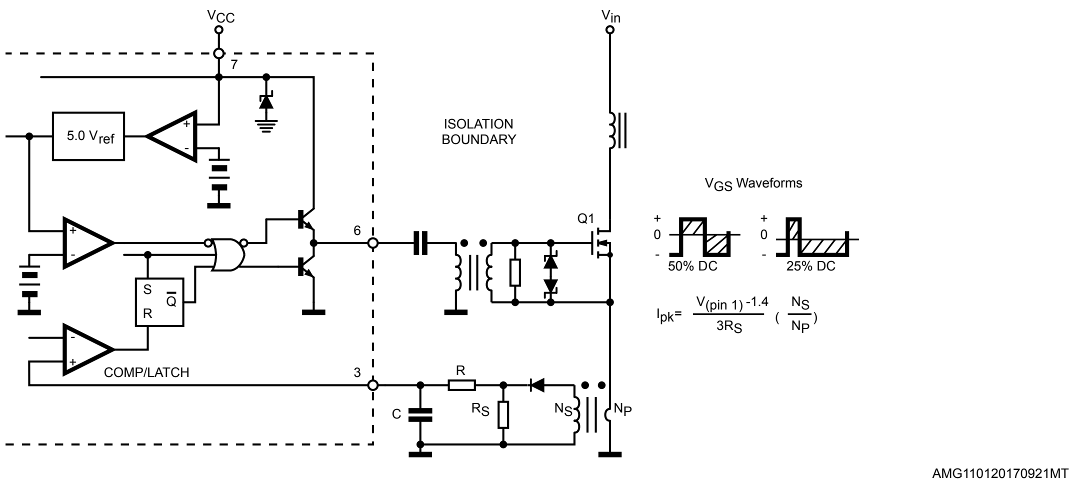
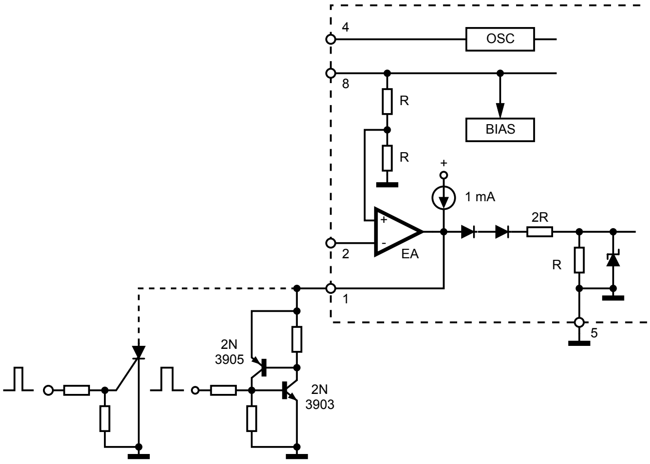


Figure 22. Latched shutdown



SCR must be selected for a holding current of less than 0.5 mA at $T_{A(min)}$.
The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 K.

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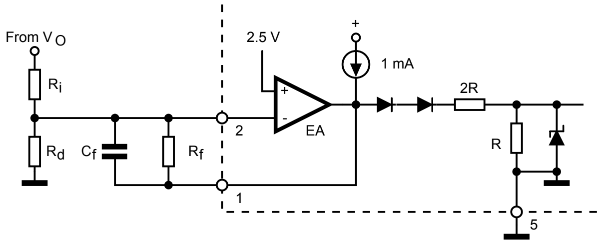
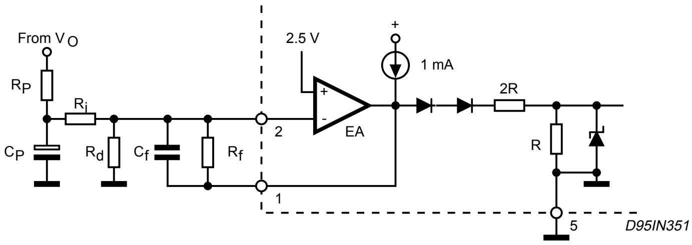
Figure 23. Error amplifier compensation



for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

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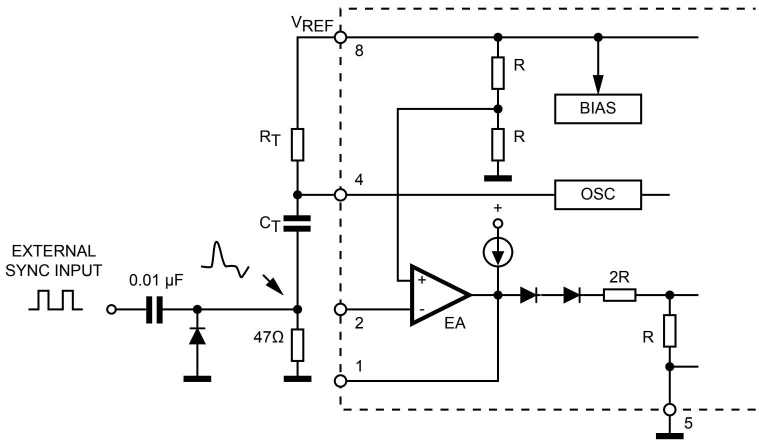
Figure 24. External clock synchronization



The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

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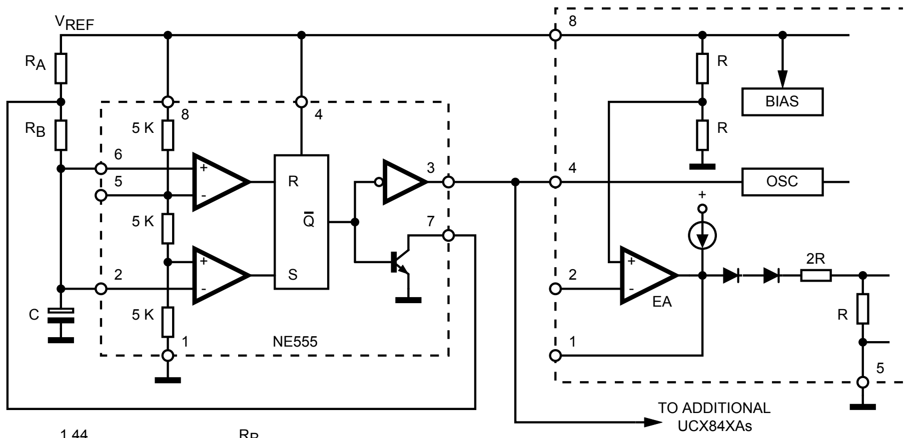
Figure 25. External duty cycle clamp and multi unit synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

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Figure 26. **Soft-start circuit**

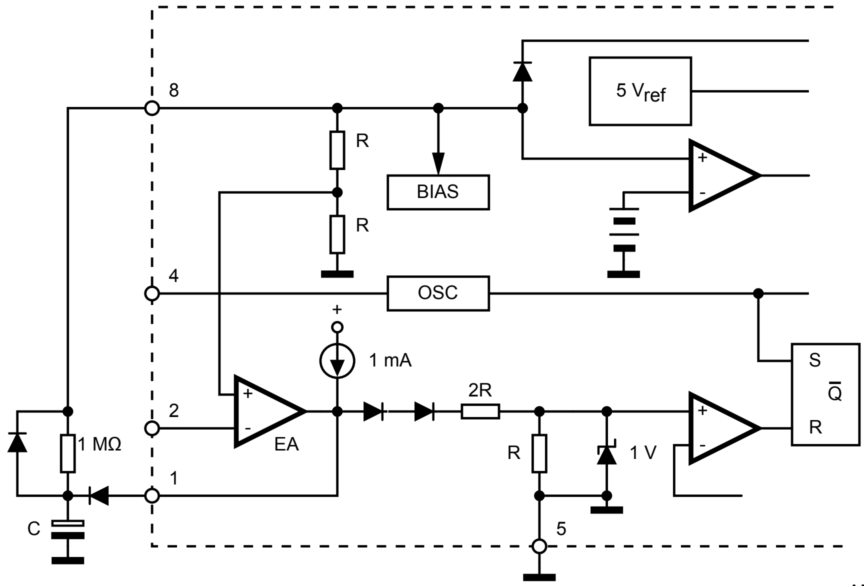

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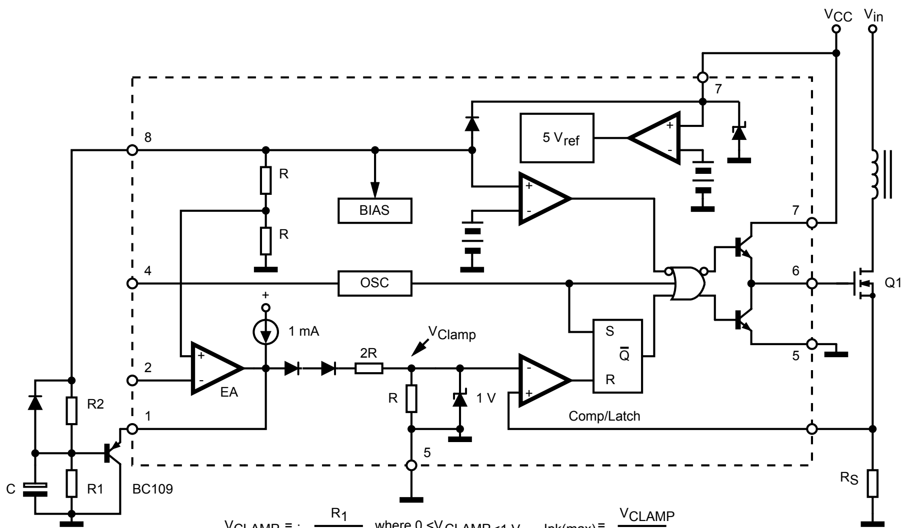
Figure 27. **Soft-start and error amplifier output duty cycle clamp**



$V_{CLAMP} = \frac{R_1}{R_1 + R_2}$ where $0 < V_{CLAMP} < 1$ V $\quad Ipk(max) = \frac{V_{CLAMP}}{R_S}$

AMG110120170927MT

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 Flat-8 package information

Figure 28. Flat-8 package outline

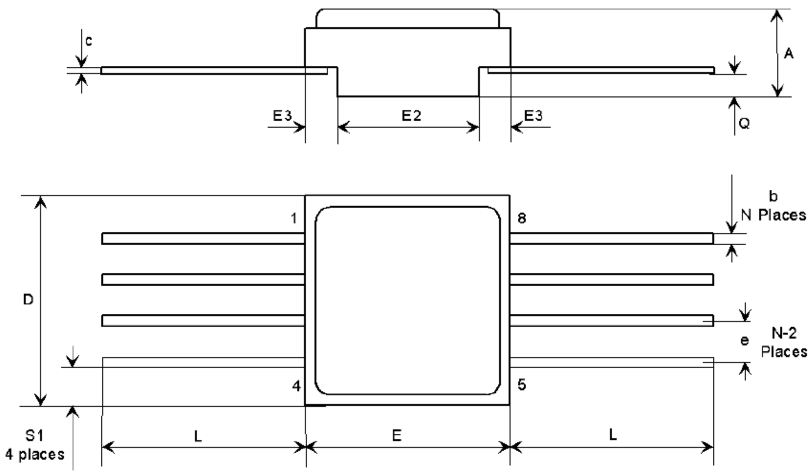


Table 8. Flat-8 mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.24	2.44	2.64	0.088	0.096	0.104
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.13	0.16	0.004	0.005	0.006
D	6.35	6.48	6.61	0.250	0.255	0.260
E	6.35	6.48	6.61	0.250	0.255	0.260
E2	4.32	4.45	4.58	0.170	0.175	0.180
E3	0.88	1.01	1.14	0.035	0.040	0.045
e		1.27			0.050	
L	6.51	-	7.38	0.256	-	0.291
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.92	1.12	1.32	0.036	0.044	0.052
N	08			08		

9 Ordering information

Table 9. Order codes

Order code	Detailed specification	Quality level	Radiation level	Duty cycle max.	Package	Mass (g)	Lead finish	Marking(1)	Packing
ST1843K1	-	Engineering model	-	100%	Flat-8	0.45	Gold	ST1843K1	Strip pack
ST1843FKG	9108/020/01F	ESCC	50 krad(si)	100%	Flat-8	0.45	Gold	9108/020/01F	Strip pack
ST1843FKT	9108/020/02F	ESCC	50 krad(si)	100%	Flat-8	0.45	Solder dip	9108/020/02F	Strip pack
ST1845K1	-	Engineering model	-	50%	Flat-8	0.45	Gold	ST1845K1	Strip pack
ST1845RKG	9108/021/01R	ESCC	100 krad(si)	50%	Flat-8	0.45	Gold	9108/021/01R	Strip pack
ST1845RKT	9108/021/02R	ESCC	100 krad(si)	50%	Flat-8	0.45	Solder dip	9108/021/02R	Strip pack

1. *Specific marking only. Complete marking includes in addition the following: ST logo, ESCC logo, date code and country of origin.*

Note: Contact ST Sales office for information about specific conditions for products in die form, other quality levels and tape and reel packing.

9.1 Other information

9.1.1 Traceability information

The date code information is structured as described in the table below:

Table 10. Date codes

Model	Datecode(1)
EM	3yywwN
ESCC	yywwN

1. *yy = year, ww = week number, N = lot index in the week*

9.1.2 Documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The documentation is provided on printed paper in a dedicated envelop.

Table 11. **Default documentation provided with the parts**

Quality level	Documentation(1)
Engineering model	Certificate of conformance including: • Customer name • Customer purchase order number • ST sales order number and item • ST part number • Quantity delivered • Date code • Reference datasheet • Reference to the TN1180 on engineering models • ST Rennes assembly lot ID
ESCC flight	Certificate of conformance including: • Customer name • Customer purchase order number • ST sales order number and item • ST part number • Quantity delivered • Date code • Serial numbers • Reference of the applicable ESCC qualification maintenance lot • Reference to the ESCC detail specification • ST Rennes assembly lot ID Radiation verification test report(2)

1. *Default documentation only. Contact STMicroelectronics sales office for optional documentation.*
2. *Report of the ESCC22900 test supporting the delivered parts*

Revision history

Table 12. **Document revision history**

Date	Revision	Changes
12-Sep-2011	1	First revision
21-Mar-2017	2	Updated the features, the description and Table 1: "Device summary" in cover page. Updated Table 2: "Absolute maximum ratings", Figure 2: "Pin connection", Table 5: "Electrical characteristics ", Figure 3: "Unbias conditions", Table 7: "Electrical parameter during irradiation testing", Section 6.1.3: "Heavy Ions" and Table 10: "Order codes". Added Section 9.1: "Other information". Minor text changes.
04-Aug-2017	3	Updated Table 5: "Electrical characteristics ", Figure 3: "Unbias conditions", Figure 19: "Undervoltage lockout" and Figure 21: "Slope compensation techniques". Minor text changes.
24-Apr-2019	4	Updated Table 5. Total dose performance and Table 9. Order codes.
19-May-2020	5	Updated the cover page. Updated Table 2. Thermal data, Table 4. Electrical characteristics , Table 5. Total dose performance, Table 1, Table 9. Order codes and Table 11. Default documentation provided with the parts.
11-Jun-2020	6	Updated package silhouette on the cover page.

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