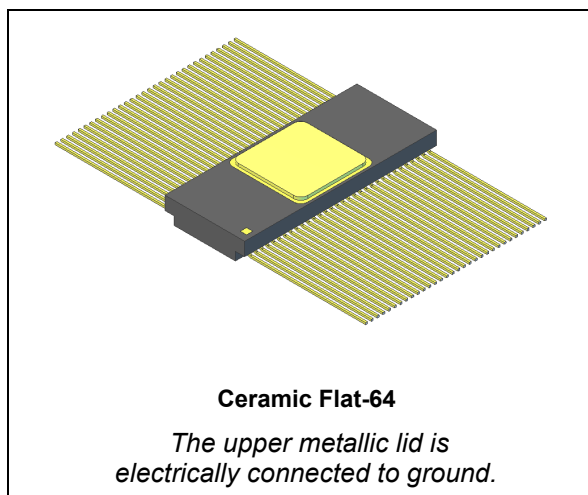


## Rad-hard, dual 4x4 crosspoint switch LVDS

Datasheet - production data



### Features

- LVDS input/output
- Multiple configuration: Mux, repeater and splitter
- ANSI TIA/EIA-644 compliant
- 400 Mbps LVDS (200 MHz)
- 200 MHz clock channel
- Cold spare on all pins
- Fail-safe function
- 3.3 V operating power supply
- 4.8 V absolute rating
- Hermetic package
- Power consumption: 220 mW at 3.3 V

- Large input common mode: -4 V to +5 V
- Guaranteed up to 300 krad TID
- SEL immune up to 135 MeV.cm<sup>2</sup>/mg
- SET/SEU immune up to 22 MeV.cm<sup>2</sup>/mg

### Description

The RHFLVDS2281 is an 8-channel, 4x4 crosspoint switch base, on low voltage differential signaling (LVDS) for low-power and high-speed communications. The two 4x4 multiplexers allow connection from any of the four inputs to any of the four outputs.

Packaged and qualified for use in aerospace environments in a low-power, fast-transmission standard, the RHFLVDS2281 operates at 3.3 V power supply (3.6 V max. operating and 4.8 V AMR) and a common mode of -4 V to +5 V. The LVDS outputs operate over a controlled impedance of 100-ohm transmission media that may be printed circuit board traces, back planes, or cables.

The circuit features an internal fail-safe function to ensure a known state in case of an input short circuit or a floating input.

All pins have cold spare buffers to ensure they are in high impedance when  $V_{CC}$  is tied to GND. The RHFLVDS2281 can operate over a wide temperature range of -55 °C to +125 °C and it is housed in an hermetic Ceramic Flat-64 package.

Table 1. Device summary

| Reference       | SMD pin      | Quality level     | Package         | Lead finish | Mass   | EPPL <sup>(1)</sup> | Temp. range      |
|-----------------|--------------|-------------------|-----------------|-------------|--------|---------------------|------------------|
| RHFLVDS2281K1   | -            | Engineering model | Ceramic Flat-64 | Gold        | 1.94 g | -                   | -55 °C to 125 °C |
| RHFLVDS2281K01V | 5962F1423401 | QML-V flight      |                 |             |        | Target              |                  |

1. EPPL = ESA preferred part list

## Contents

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# 1 Functional description

Table 2. Mux truth table

| SL1 | SL2 | SL3 | SL4 | OUT1 | OUT2 | OUT3 | OUT4 | Mode              |
|-----|-----|-----|-----|------|------|------|------|-------------------|
| 0   | 0   | 0   | 0   | IN1  | IN1  | IN3  | IN3  | Splitter          |
| 0   | 0   | 0   | 1   | IN1  | IN1  | IN3  | IN4  | Splitter/repeater |
| 0   | 0   | 1   | 0   | IN1  | IN1  | IN1  | IN1  | Splitter          |
| 0   | 0   | 1   | 1   | IN1  | IN1  | IN4  | IN4  |                   |
| 0   | 1   | 0   | 0   | IN1  | IN2  | IN3  | IN3  | Splitter/repeater |
| 0   | 1   | 0   | 1   | IN1  | IN2  | IN3  | IN4  | Repeater          |
| 0   | 1   | 1   | 0   | IN1  | IN2  | IN4  | IN3  | Repeater/switch   |
| 0   | 1   | 1   | 1   | IN1  | IN2  | IN4  | IN4  | Splitter/repeater |
| 1   | 0   | 0   | 0   | IN2  | IN2  | IN2  | IN2  | Splitter          |
| 1   | 0   | 0   | 1   | IN2  | IN1  | IN3  | IN4  | Switch/repeater   |
| 1   | 0   | 1   | 0   | IN2  | IN1  | IN4  | IN3  | Switch            |
| 1   | 0   | 1   | 1   | IN3  | IN3  | IN3  | IN3  | Splitter          |
| 1   | 1   | 0   | 0   | IN2  | IN2  | IN3  | IN3  |                   |
| 1   | 1   | 0   | 1   | IN2  | IN2  | IN3  | IN4  | Splitter/repeater |
| 1   | 1   | 1   | 0   | IN4  | IN4  | IN4  | IN4  | Splitter          |
| 1   | 1   | 1   | 1   | IN2  | IN2  | IN4  | IN4  |                   |

- Note:
- 1 A floating SL pin is equivalent to a low logic level
  - 2 Channels 5, 6, 7, and 8 behave like channels 1, 2, 3 and 4 respectively (see also [Figure 2](#))

Table 3. Enable (EN) truth table

| EN                                  | Inputs                                     | Outputs |      |
|-------------------------------------|--|---------|------|
|                                     | (IN+) - (IN-)                              | OUT+    | OUT- |
| L                                   | X  | Z       | Z    |
| H or floating<br>(internal pull-up) | $V_{id} \geq 0.1 \text{ V}$                | H       | L    |
|                                     | $V_{id} \leq -0.1 \text{ V}$               | L       | H    |
|                                     | $-0.1 \text{ V} < V_{id} < +0.1 \text{ V}$ | Unknown |      |
|                                     | Full fail-safe open/short or terminated    | H       | L    |

Note:  $V_{id} = (VIN+) - (VIN-)$ , L = low level, H = high level, X = don't care, Z = high impedance

## 2 Internal schematic and pin configuration

Figure 1. Internal schematic

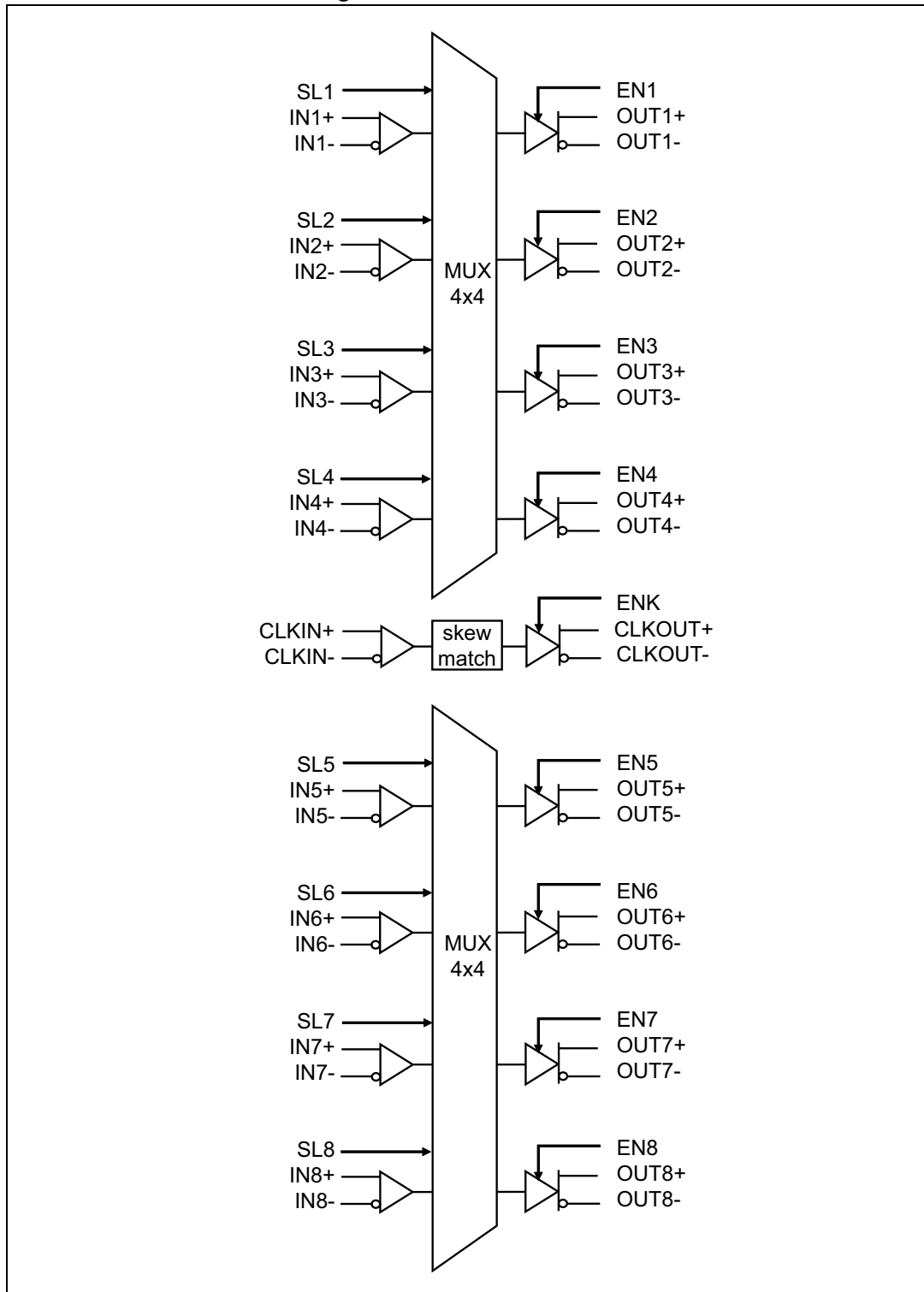
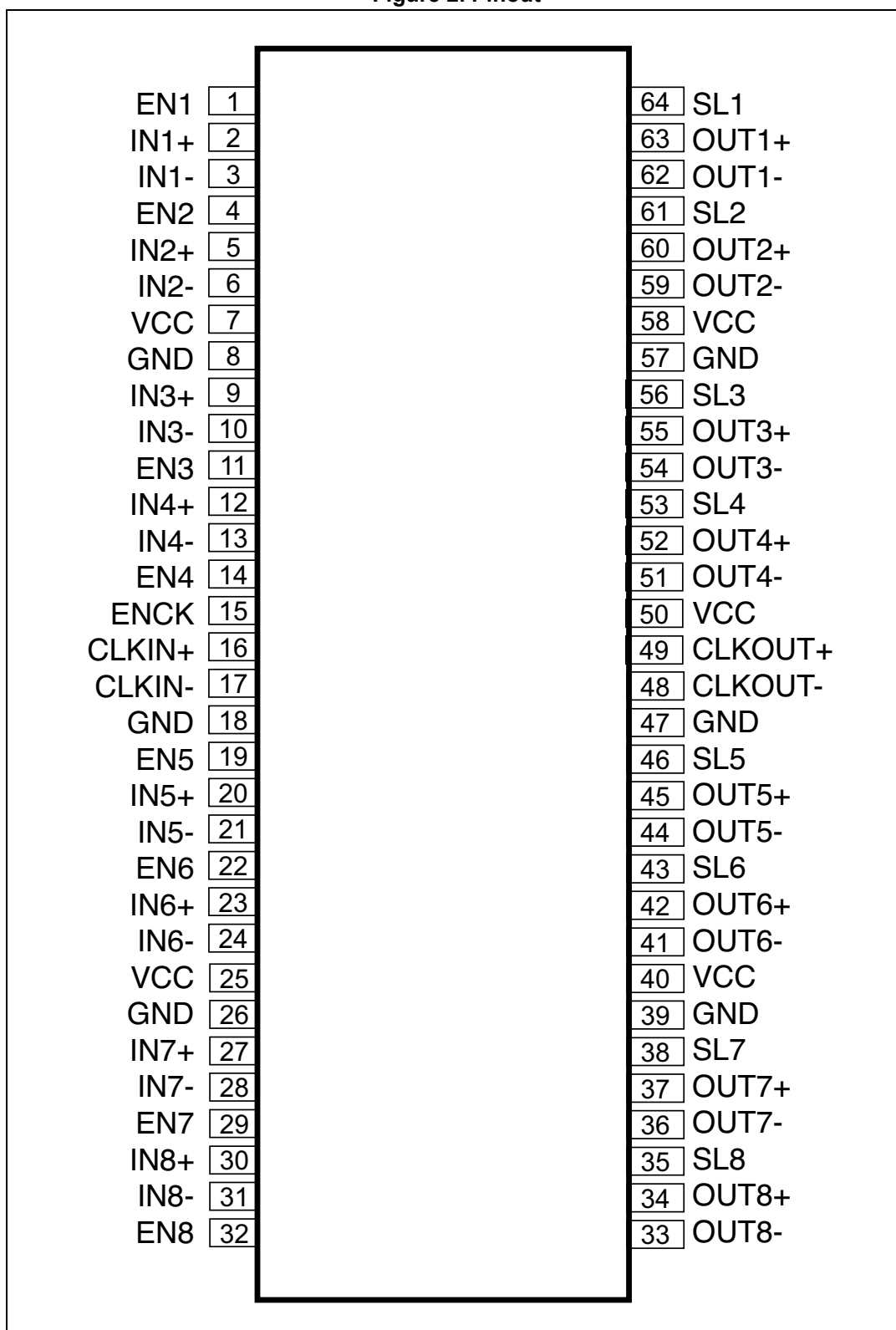


Figure 2. Pinout



1. Power supplies are not internally separated. All Vcc pins must be connected to the same potential.

### 3 Maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

**Table 4. Absolute maximum ratings**

| Symbol     | Parameter   | Value        | Unit |
|------------|---|--------------|------|
| $V_{CC}$   | Supply voltage <sup>(1)</sup>   | 4.8          | V    |
| $V_i$      | TTL inputs (operating or cold-spares)   | -0.3 to +4.8 |      |
| $V_{OUT}$  | LVDS outputs (operating or coldspare)   | -0.3 to +4.8 |      |
| $V_{CM}$   | LVDS common mode (operating or cold-spares)   | -5 to +6     |      |
| $T_{stg}$  | Storage temperature range   | -65 to +150  | °C   |
| $T_j$      | Maximum junction temperature  | +150         |      |
| $R_{thjc}$ | Thermal resistance junction to case <sup>(2)</sup>  | 20           | °C/W |
| ESD        | HBM: Human body model<br>– All pins excepted LVDS inputs and outputs<br>– LVDS inputs and outputs vs. GND | 2<br>8       | kV   |
|            | CDM: Charge device model  | 500          | V    |

1. All voltages, except the differential I/O bus voltage, are with respect to the network ground terminal.
2. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.

**Table 5. Operating conditions**

| Symbol   | Parameter                 | Min. | Typ. | Max. | Unit |
|----------|---------------------------|------|------|------|------|
| $V_{CC}$ | Supply voltage            | 3    | 3.3  | 3.6  | V    |
| $V_{CM}$ | Static common mode        | - 4  |      | + 5  |      |
| $T_A$    | Ambient temperature range | -55  |      | +125 | °C   |

## 4 Electrical characteristics

### Total dose (MIL-STD-883 TM 1019)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHFLVDS2281 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, between 50 and 300 rad/s only (full CMOS technology).

All parameters provided in [Table 7: Electrical characteristics table](#) apply to both pre- and post-irradiation, as follows:

- All test are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

### Heavy ions

The behavior of the product when submitted to heavy ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

**Table 6. Radiations**

| Type       | Characteristics   | Value | Unit                    |
|------------|---|-------|-------------------------|
| TID        | High-dose rate (50 - 300 rad/sec)                                 | 300   | krad                    |
| Heavy ions | SEL immunity up to:<br>(with a particle angle of 60 °, at 125 °C) | 135   | MeV.cm <sup>2</sup> /mg |
|            | SEL immunity up to:<br>(with a particle angle of 0 °, at 125 °C)  | 67    |                         |
|            | SET/SEU immunity up to:<br>(at 25 °C)                             | 22    |                         |

In [Table 7](#) below,  $V_{CC} = 3\text{ V}$  to  $3.6\text{ V}$ , capa-load (CL) =  $10\text{ pF}$ , typical values are at  $T_{amb} = +25\text{ }^{\circ}\text{C}$ , min. and max values are at  $T_{amb} = -55\text{ }^{\circ}\text{C}$  and  $+125\text{ }^{\circ}\text{C}$  unless otherwise specified.

Table 7. Electrical characteristics table

| Symbol                          | Parameter   | Test conditions  | Min.  | Typ. | Max.            | Unit  |
|---------------------------------|---|--|-------|------|-----------------|-------|
| Whole circuit                   |   |  |       |      |                 |       |
| I <sub>CCL</sub>                | Total enabled supply current, drivers and receivers enabled, not switching          | V <sub>ID</sub> = 400 mV and load = 100 W on all channels  |       | 67   | 80              | mA    |
| I <sub>CCZ</sub>                | Total disabled supply current, loaded or not loaded, drivers and receivers disabled | V <sub>ID</sub> = 400 mV<br>EN and ENCK = GND              |       |      | 20              |       |
| Digital inputs EN, ENCK, and SL |   |  |       |      |                 |       |
| V <sub>IH</sub>                 | Input voltage high  |  | 2     |      | V <sub>CC</sub> | V     |
| V <sub>IL</sub>                 | Input voltage low   |  | GND   |      | 0.8             |       |
| I <sub>IH</sub>                 | High level input current  | V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = V <sub>CC</sub> | -10   |      | 10              | μA    |
| I <sub>IL</sub>                 | Low level input current   | V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = 0               | -10   |      | 10              |       |
| I <sub>OFF</sub>                | TTL inputs power off leakage current  | V <sub>CC</sub> = 0 V,<br>EN and SL = 3.6 V                | -10   |      | 10              |       |
| LVDS inputs                     |   |  |       |      |                 |       |
| V <sub>TL</sub>                 | Differential input low threshold  | V <sub>CM</sub> = 1.2 V                                    |       |      | -100            | mV    |
|                                 |   | -4 V < V <sub>CM</sub> < +5 V                              |       |      | -130            |       |
| V <sub>TH</sub>                 | Differential input high threshold   | V <sub>CM</sub> = 1.2 V                                    | +100  |      |                 |       |
|                                 |   | -4 V < V <sub>CM</sub> < +5 V                              | +130  |      |                 |       |
| V <sub>CL</sub>                 | TTL input clamp voltage   | I <sub>CL</sub> = 18 mA                                    |       |      | 1.5             | V     |
| V <sub>CMR</sub>                | Common mode voltage range   | V <sub>ID</sub> = 200 mVp-p                                | - 4   |      | +5              |       |
| V <sub>CMREJ</sub>              | Common mode rejection <sup>(1)</sup>  | F = 10 MHz   |       |      | 300             | mVp-p |
| I <sub>ID</sub>                 | Differential input current  | V <sub>ID</sub> = 400 mVp-p                                | -10   |      | 10              | μA    |
| I <sub>ICM</sub>                | Common mode input current   | V <sub>IC</sub> = - 4 V to + 5 V                           | -70   |      | 70              |       |
| I <sub>OFFIN</sub>              | LVDS input power-off leakage current <sup>(2)</sup>                                 | V <sub>CC</sub> = 0 V, V <sub>IN</sub> = -4 V to 5 V       | -60   |      | 60              |       |
| C <sub>IN</sub>                 | Input capacitance   |  |       | 3    |                 | pF    |
| LVDS outputs                    |   |  |       |      |                 |       |
| V <sub>OH</sub>                 | Output voltage high   |  |       |      | 1.65            | V     |
| V <sub>OL</sub>                 | Output voltage low  |  | 0.925 |      |                 |       |
| V <sub>OD</sub>                 | Differential output voltage   |  | 250   |      | 400             | mV    |
| DV <sub>OD</sub>                | Change of magnitude of V <sub>OD</sub> for complementary output states              |  |       |      | 10              |       |
| V <sub>OS</sub>                 | Offset voltage  |  | 1.125 |      | 1.45            | V     |



Table 7. Electrical characteristics table (continued)

| Symbol                   | Parameter   | Test conditions   | Min. | Typ. | Max. | Unit |
|--------------------------|---|---|------|------|------|------|
| DV <sub>OS</sub>         | Change of magnitude of V <sub>OS</sub> for complementary output states      |   |      |      | 25   | mV   |
| I <sub>OS</sub>          | Output short-circuit current  | V <sub>ID</sub> = -400 mV and V <sub>OUT-</sub> = 0 V<br>V <sub>ID</sub> = +400 mV and V <sub>OUT+</sub> = 0 V                  | -9   |      |      | mA   |
| I <sub>OZ</sub>          | High impedance output current   | Disabled, V <sub>OUT</sub> = 3.6 V or 0V  | -10  |      | 10   | μA   |
| I <sub>OFFOUT</sub>      | LVDS outputs power-off leakage current                                      | V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 3.6 V   | -50  |      | +50  |      |
| T <sub>S</sub>           | Input to SL setup time <sup>(3)</sup>                                       | Refer to <a href="#">Figure 5</a>   | 1.6  |      |      | ns   |
| T <sub>H</sub>           | Input to SL Hold time <sup>(3)</sup>  |   | 1.5  |      |      |      |
| T <sub>Sw</sub>          | SL to Switched output <sup>(3)</sup>  |   |      |      | 5    |      |
| t <sub>PHLD</sub>        | Propagation delay time, high to low   | V <sub>ID</sub> = 200 mVp-p, input pulse from 1.1 V to 1.3 V, V <sub>CM</sub> =1.2 V<br>Load: refer to <a href="#">Figure 3</a> | 1.5  |      | 4    |      |
| t <sub>PLHD</sub>        | Propagation delay time, low to high   |   | 1.5  |      | 4    |      |
| t <sub>SK1</sub>         | Channel to channel skew <sup>(3)(4)</sup>                                   | V <sub>ID</sub> = 200 mVp-p<br>Load: refer to <a href="#">Figure 6</a>  |      |      | 0.6  |      |
| t <sub>SK2</sub>         | Chip to chip skew <sup>(3)(5)</sup>   |   |      |      | 0.7  |      |
| t <sub>SKD</sub>         | Differential skew <sup>(6)</sup><br>(t <sub>PHLD</sub> -t <sub>PLHD</sub> ) |   |      |      | 0.6  |      |
| t <sub>r</sub>           | Output signal rise time   | Refer to <a href="#">Figure 4</a>   |      | 0.9  |      |      |
| t <sub>f</sub>           | Output signal fall time   |   |      | 0.9  |      |      |
| t <sub>PLZ</sub>         | Propagation delay time, low level to high impedance output                  | Refer to <a href="#">Figure 6</a>   |      |      | 2.8  |      |
| t <sub>PHZ</sub>         | Propagation delay time, high level to high impedance output                 |   |      |      | 2.8  |      |
| t <sub>PZH</sub>         | Propagation delay time, high impedance to high level output                 |   |      |      | 2.5  |      |
| t <sub>PZL</sub>         | Propagation delay time, high impedance to low level output                  |   |      |      | 2.5  |      |
| Fail-safe and cold-spore |   |   |      |      |      |      |
| t <sub>D1</sub>          | Fail-safe to active time  |   |      | 1    |      | μs   |
| t <sub>D2</sub>          | Active to fail-safe time  |   |      | 1    |      |      |

1. Guaranteed by characterization on bench.
2. All pins are floating except pin under test and V<sub>CC</sub>.
3. Guaranteed by design.
4. t<sub>SK1</sub> is the maximum delay time difference between drivers on the same device (with all inputs connected together).
5. t<sub>SK2</sub> is the maximum delay time difference between outputs of all devices when they operate with the same supply voltage, at the same temperature.
6. t<sub>SKD</sub> is the maximum delay time difference between t<sub>PHLD</sub> and t<sub>PLHD</sub> (see [Figure 4](#)).

**Cold sparing**

The RHFLVDS2281 features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V ( $V_{CC} = \text{GND}$ ) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices to be kept powered off so that they can be switched on only when required. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between the I/Os and  $V_{CC}$ . ESD protection is ensured through a non-conventional dedicated structure.

**Fail-safe**

In many applications, inputs need a fail-safe function to avoid an uncertain output state when the inputs are not connected properly. In case of an LVDS input short circuit or floating inputs, the LVDS outputs remain in stable logic-high state.

## 5 Test circuit

Figure 3. Voltage and current definition

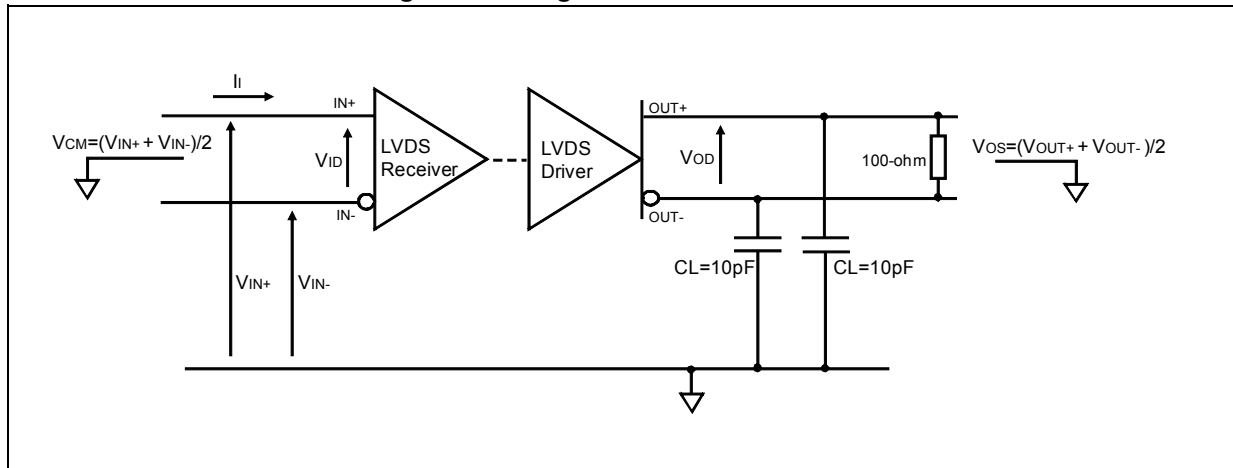
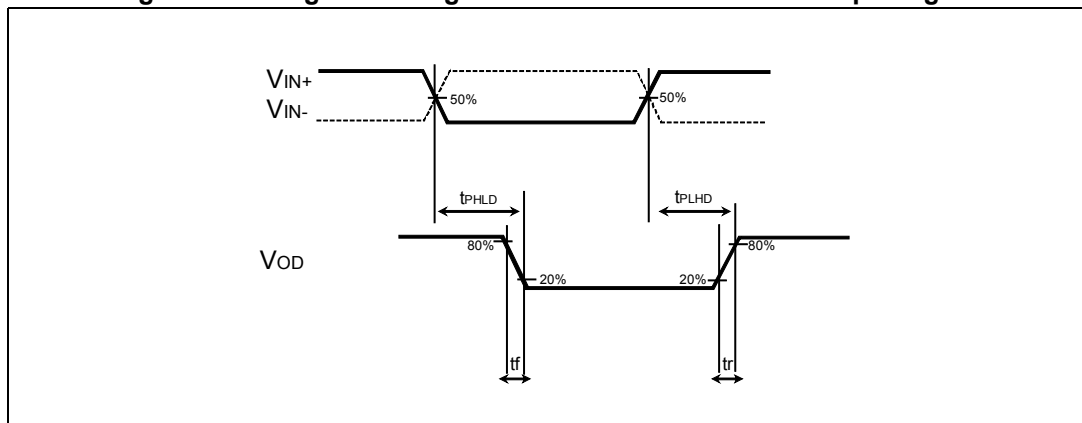


Figure 4. Timing and voltage definitions for differential output signal



1. All input pulses are supplied by a generator with the following characteristics:  $t_r$  or  $t_f \leq 1\text{ ns}$ ,  $f = 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ , and duty cycle = 50%.
2. The product is guaranteed with  $C_L = 10\text{ pF}$ .

Figure 5. MUX switch timings

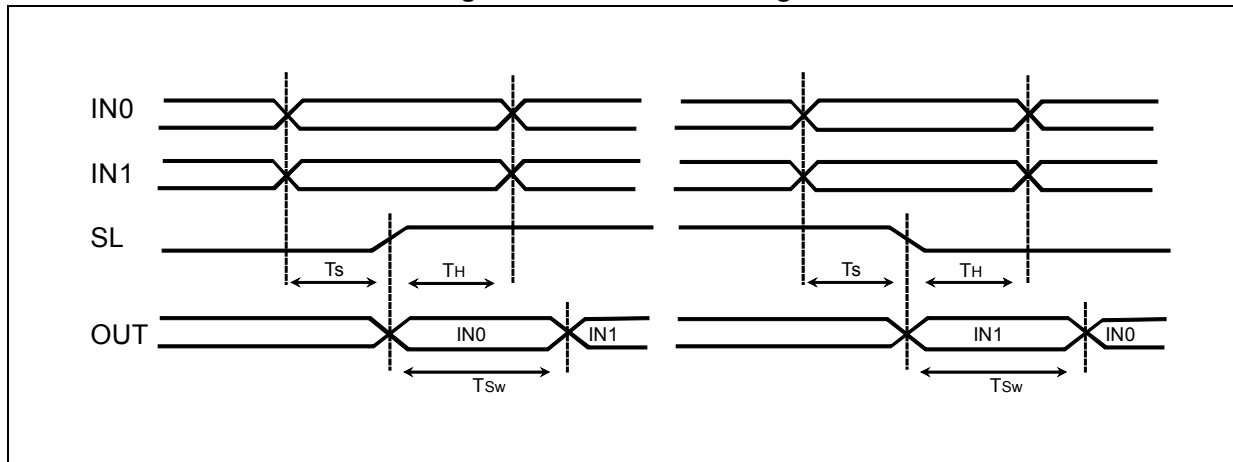
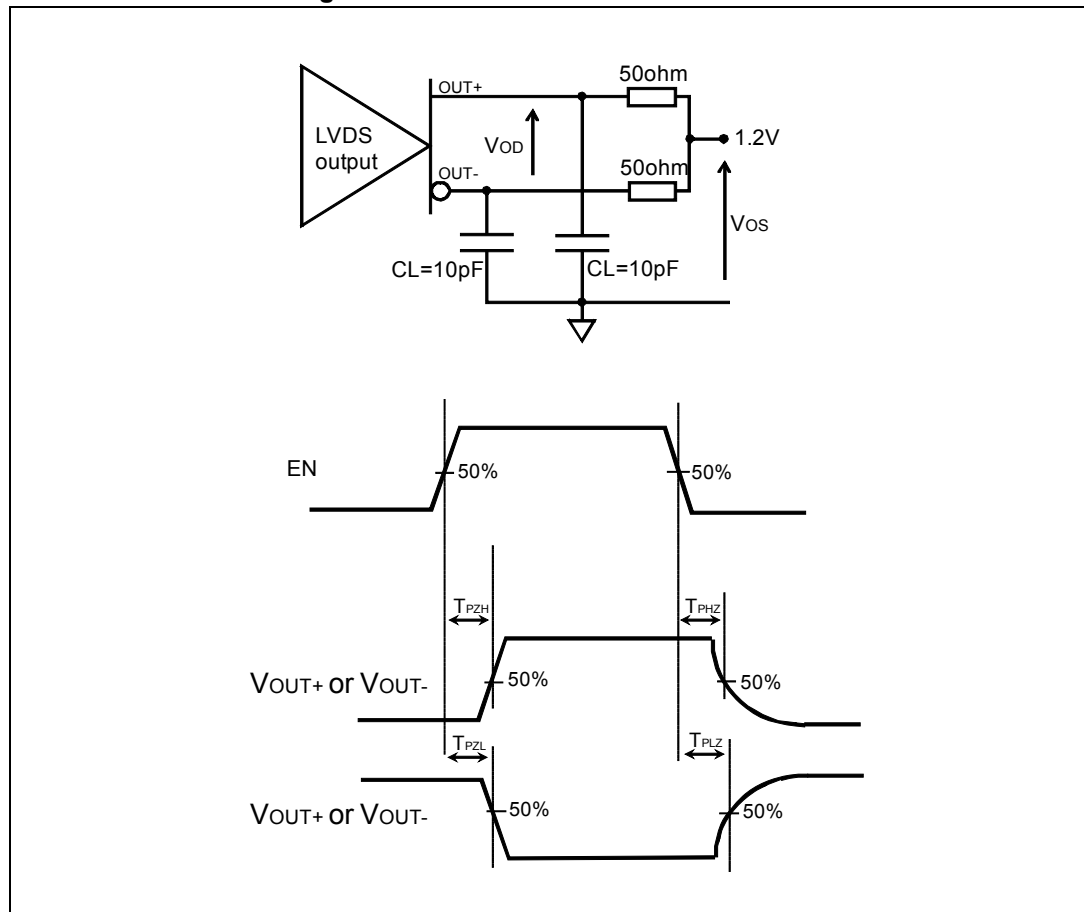


Figure 6. Enable and disable waveforms



1. All input pulses are supplied by a generator with the following characteristics on EN:  
 $t_r$  or  $t_f \leq 1$  ns,  $F = 500$  kHz, pulse width = 500 ns.

## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.



## 7 Ordering information

Table 9. Order codes

| Order code      | Description       | Temp. range      | Package         | Marking <sup>(1)</sup> | Packing    |
|-----------------|-------------------|------------------|-----------------|------------------------|------------|
| RHFLVDS2281K1   | Engineering model | -55 °C to 125 °C | Ceramic Flat-64 | RHFLVDS2281K1          | Strip pack |
| RHFLVDS2281K01V | QML-V flight      |                  |                 | 5962F1423401VXC        |            |

1. Specific marking only. Complete marking includes the following:
- SMD pin (on QML-V flight only)
  - ST logo
  - Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)
  - QML logo (Q or V)
  - Country of origin (FR = France).

*Note:* Contact your ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.

## 8 Shipping information

### Date code

The date code is structured as follows:

- Engineering model: EM xyywwz
- QML flight model: FM yywwz

Where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

## 9 Revision history

**Table 10. Document revision history**

| Date        | Revision | Changes          |
|-------------|----------|------------------|
| 04-Mar-2015 | 1        | Initial release. |



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