

FEATURES

- Member of the Texas Instruments Widebus™ Family
- DOC™ (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC}

- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

DESCRIPTION

A Dynamic Output Control (DOC™) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

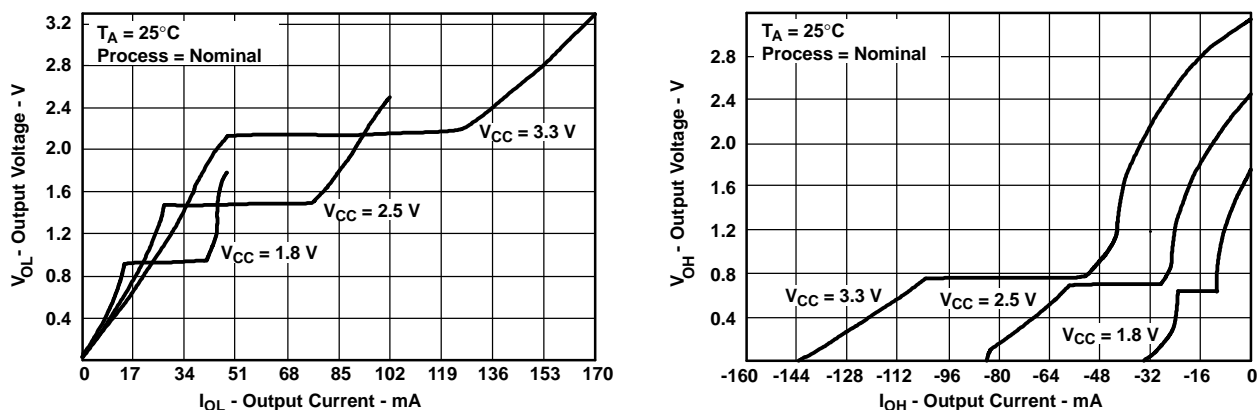


Figure 1. Output Voltage vs Output Current

This 16-bit universal bus driver is operational at 1.2-V to 3.6-V V_{CC} , but is designed specifically for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (\overline{LE}) input is low. When \overline{LE} is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If \overline{LE} is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



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SN74AVC16334

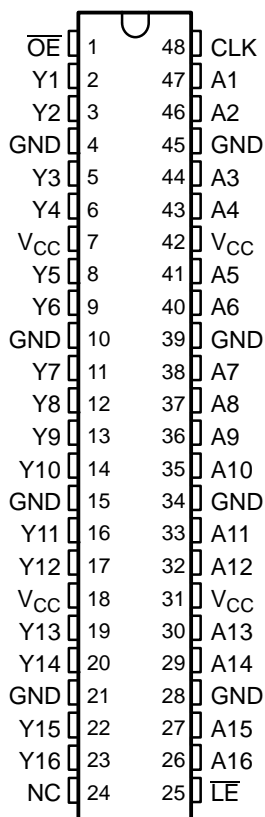
16-BIT UNIVERSAL BUS DRIVER

WITH 3-STATE OUTPUTS

SCES154I–DECEMBER 1998–REVISED MAY 2005

TERMINAL ASSIGNMENTS

DGG OR DGV PACKAGE
(TOP VIEW)



NC - No internal connection

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74AVC16334DGGR	AVC16334
	TVSOP – DGV	Tape and reel	SN74AVC16334DGVR	CVA334

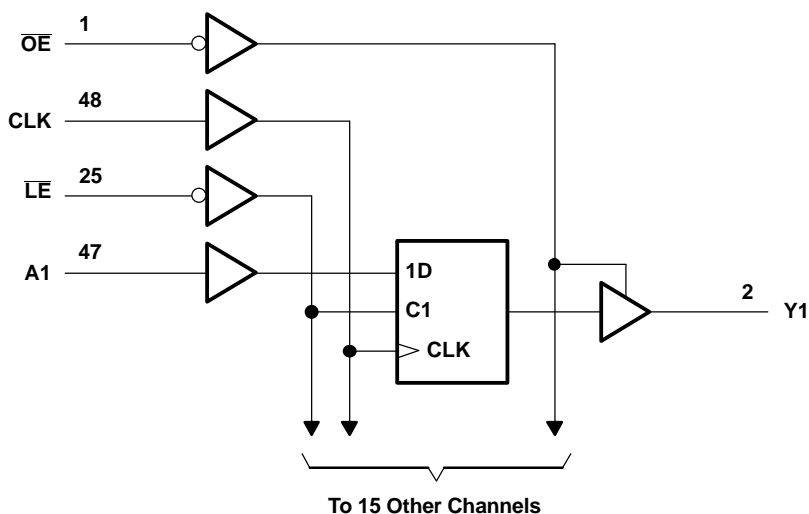
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(EACH UNIVERSAL BUS DRIVER)

INPUTS				OUTPUT Y
\overline{OE}	\overline{LE}	CLK	A	
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	\uparrow	L	L
L	H	\uparrow	H	H
L	H	L or H	X	$Y_0^{(1)}$

(1) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	4.6	V
V_I	Input voltage range ⁽²⁾	–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	4.6	V
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		–50 mA
I_{OK}	Output clamp current	$V_O < 0$		–50 mA
I_O	Continuous output current			± 50 mA
	Continuous current through each V_{CC} or GND			± 100 mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package		70 °C/W
		DGV package		58 °C/W
T_{stg}	Storage temperature range	–65	150	°C

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
- The package thermal impedance is calculated in accordance with JESD 51-7.

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WITH 3-STATE OUTPUTS

SCES154I–DECEMBER 1998–REVISED MAY 2005

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.4	3.6	V
		Data retention only	1.2		
V_{IH}	High-level input voltage	$V_{CC} = 1.2\text{ V}$	V_{CC}		V
		$V_{CC} = 1.4\text{ V to }1.6\text{ V}$	$0.65 \times V_{CC}$		
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$		
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	2		
V_{IL}	Low-level input voltage	$V_{CC} = 1.2\text{ V}$		GND	V
		$V_{CC} = 1.4\text{ V to }1.6\text{ V}$		$0.35 \times V_{CC}$	
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$		$0.35 \times V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		0.7	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		0.8	
V_I	Input voltage		0	3.6	V
V_O	Output voltage	Active state	0	V_{CC}	V
		3-state	0	3.6	
I_{OHS}	Static high-level output current ⁽²⁾	$V_{CC} = 1.4\text{ V to }1.6\text{ V}$		–2	mA
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$		–4	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		–8	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		–12	
I_{OLS}	Static low-level output current ⁽²⁾	$V_{CC} = 1.4\text{ V to }1.6\text{ V}$		2	mA
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$		4	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		8	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.4\text{ V to }3.6\text{ V}$		5	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Dynamic drive capability is equivalent to standard outputs with I_{OH} and I_{OL} of $\pm 24\text{ mA}$ at 3.3-V V_{CC} . See Figure 1 for V_{OL} vs I_{OL} and V_{OH} vs I_{OH} characteristics. Refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{OH}	I _{OHS} = −100 μA		1.4 V to 3.6 V		V _{CC} − 0.2			V	
	I _{OHS} = −2 mA,	V _{IH} = 0.91 V	1.4 V		1.05				
	I _{OHS} = −4 mA,	V _{IH} = 1.07 V	1.65 V		1.2				
	I _{OHS} = −8 mA,	V _{IH} = 1.7 V	2.3 V		1.75				
	I _{OHS} = −12 mA,	V _{IH} = 2 V	3 V		2.3				
V _{OL}	I _{OLS} = 100 μA		1.4 V to 3.6 V				0.2	V	
	I _{OLS} = 2 mA,	V _{IL} = 0.49 V	1.4 V				0.4		
	I _{OLS} = 4 mA,	V _{IL} = 0.57 V	1.65 V				0.45		
	I _{OLS} = 8 mA,	V _{IL} = 0.7 V	2.3 V				0.55		
	I _{OLS} = 12 mA,	V _{IL} = 0.8 V	3 V				0.7		
I _I		V _I = V _{CC} or GND		3.6 V				±2.5	μA
I _{off}		V _I or V _O = 3.6 V		0				±10	μA
I _{OZ}		V _O = V _{CC} or GND		3.6 V				±10	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0		3.6 V				40	μA
C _i	CLK input	V _I = V _{CC} or GND		2.5 V		4		pF	
				3.3 V		4			
	Control inputs	V _I = V _{CC} or GND		2.5 V		4			
				3.3 V		4			
	Data inputs	V _I = V _{CC} or GND		2.5 V		2.5			
				3.3 V		2.5			
C _O	Outputs	V _O = V _{CC} or GND		2.5 V		6.5		pF	
				3.3 V		6.5			

(1) Typical values are measured at T_A = 25°C.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#) through [Figure 5](#))

			V _{CC} = 1.2 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency						150		150		150		MHz
t _w	Pulse duration	LE low					3.3		3.3		3.3		ns
		CLK high or low					3.3		3.3		3.3		
t _{su}	Setup time	Data before CLK↑		1	0.8	0.7	0.7	0.7	0.7			ns	
		Data before LE↑	CLK high	1.5	1.4	0.9	0.9	0.9	0.9				
			CLK low	2.7	1.6	1.2	1	1					
t _h	Hold time	Data after CLK↑		1.3	1.1	0.9	0.8	0.7				ns	
t _h	Hold time	Data after LE↑	CLK high	2.2	1.9	1.7	1.5	1.5				ns	
			CLK low	2.4	1.8	1.6	1.4	1.3		ns			

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16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

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Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2 through Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.2 V	V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}						150		150		150		MHz
t _{pd}	A	Y	5.3	1.2	6.2	1.5	4.9	1	3.2	0.9	2.5	ns
	$\overline{\text{LE}}$		7	2.2	9.7	1.8	7.5	1.5	4.9	0.8	4	
	CLK		6	1.9	7.8	1.6	6	1.1	3.7	1	3.1	
t _{en}	$\overline{\text{OE}}$	Y	7.9	2.4	10.2	1.6	8.8	1.5	6.7	1	6.2	ns
t _{dis}	$\overline{\text{OE}}$	Y	7.7	2.1	10.3	1.5	8.4	1.2	5.3	1	5.3	ns

Switching Characteristics⁽¹⁾

T_A = 0°C to 85°C, C_L = 0 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t _{pd}	A	Y	0.6	1.3	ns
	CLK		0.7	1.5	

(1) Texas Instruments SPICE simulation data

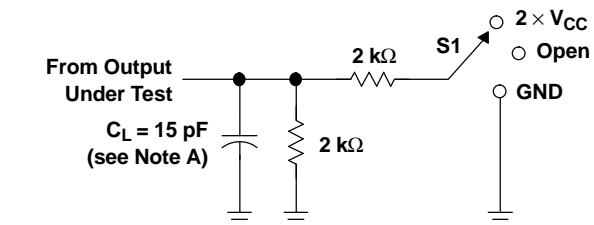
Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	C _L = 0, f = 10 MHz	45	48	52	pF
	Outputs disabled		23	25	28	

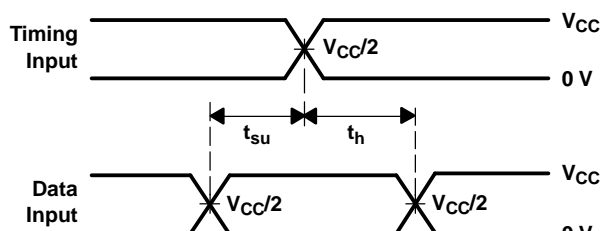
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.2\text{ V}$ AND $1.5\text{ V} \pm 0.1\text{ V}$

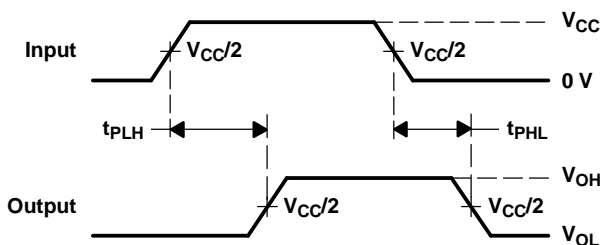


LOAD CIRCUIT

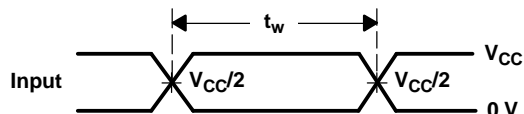
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



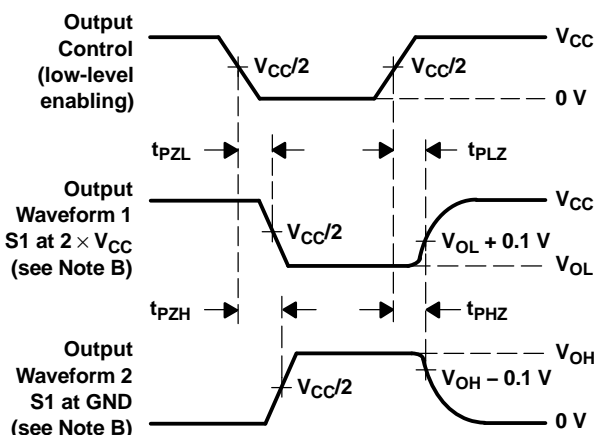
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



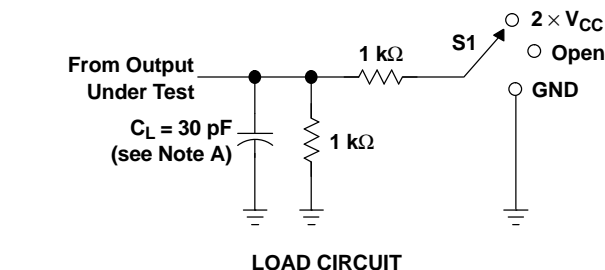
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

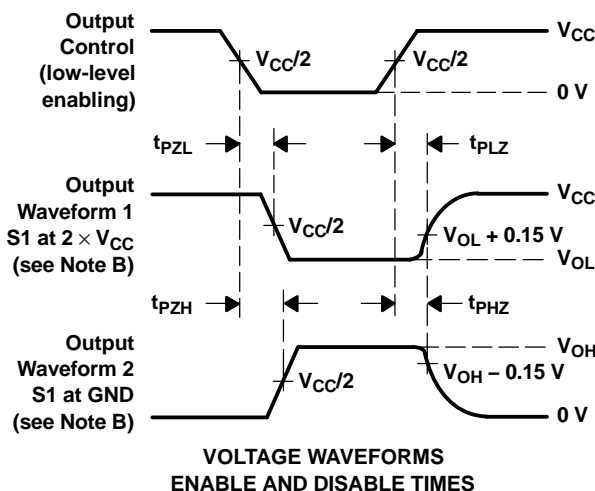
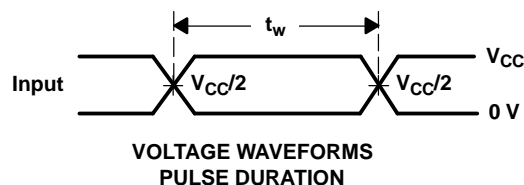
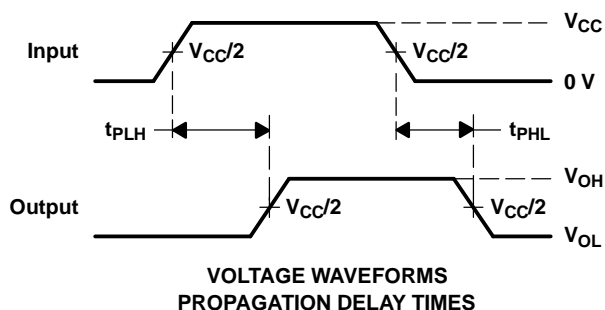
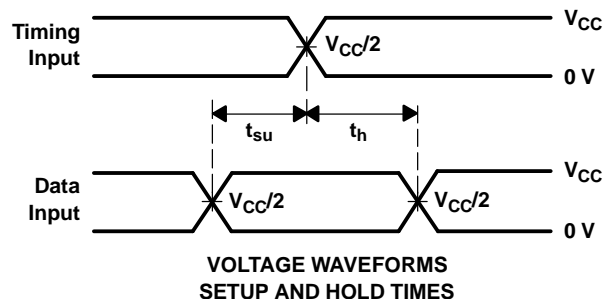
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

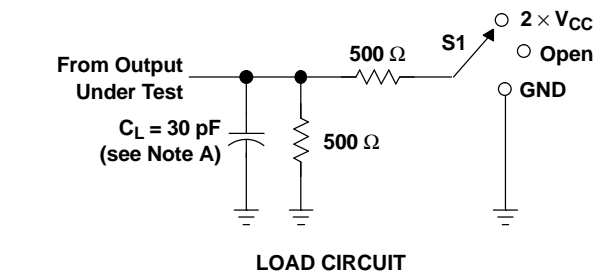


- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

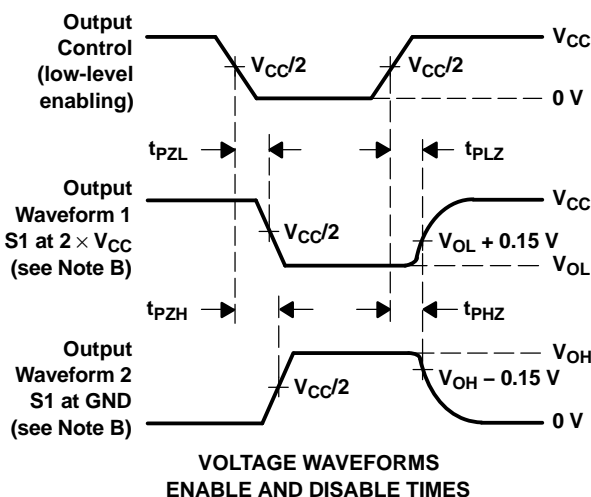
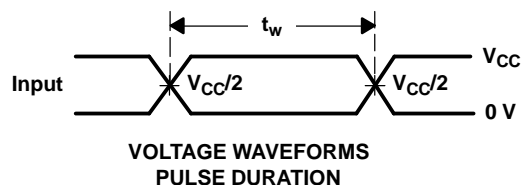
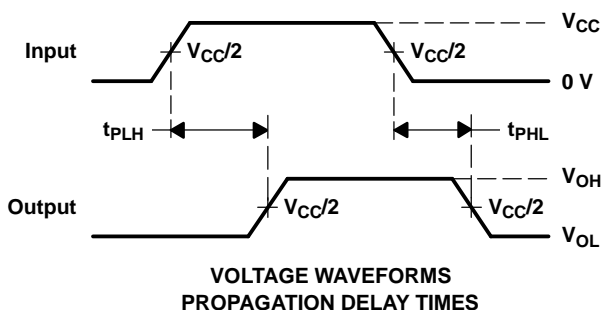
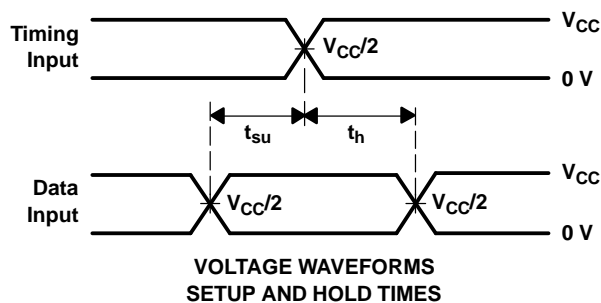
Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHZ}	GND

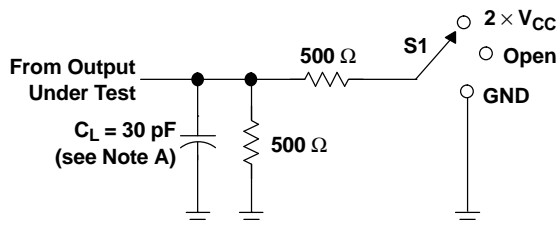


- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 4. Load Circuit and Voltage Waveforms

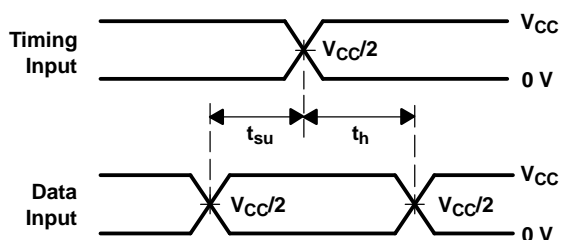
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$$

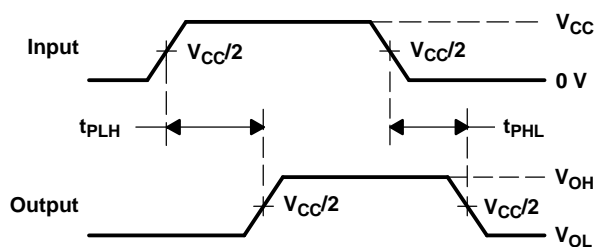


LOAD CIRCUIT

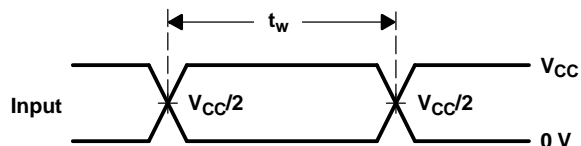
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



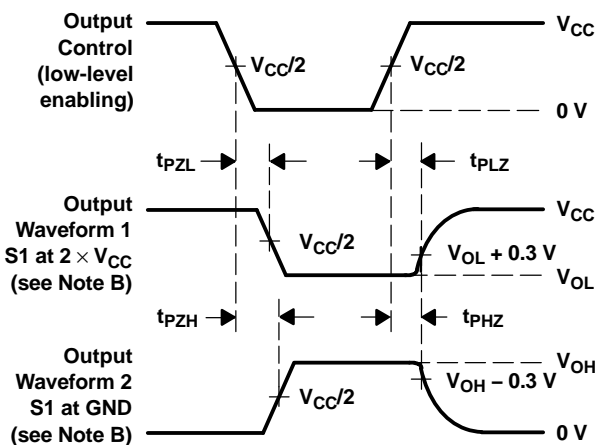
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 5. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AVC16334DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC16334	Samples
SN74AVC16334DGVR	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVA334	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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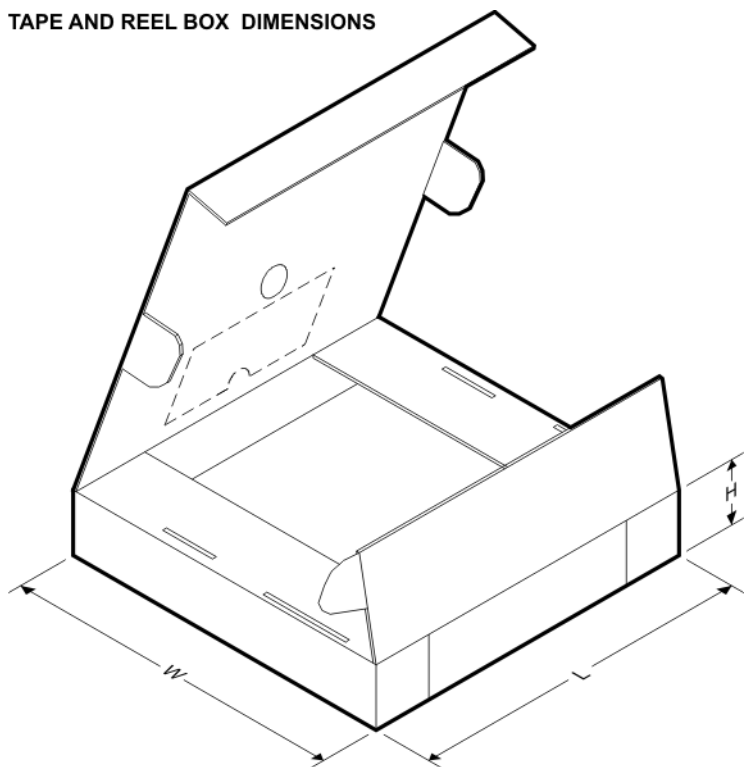
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC16334DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AVC16334DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



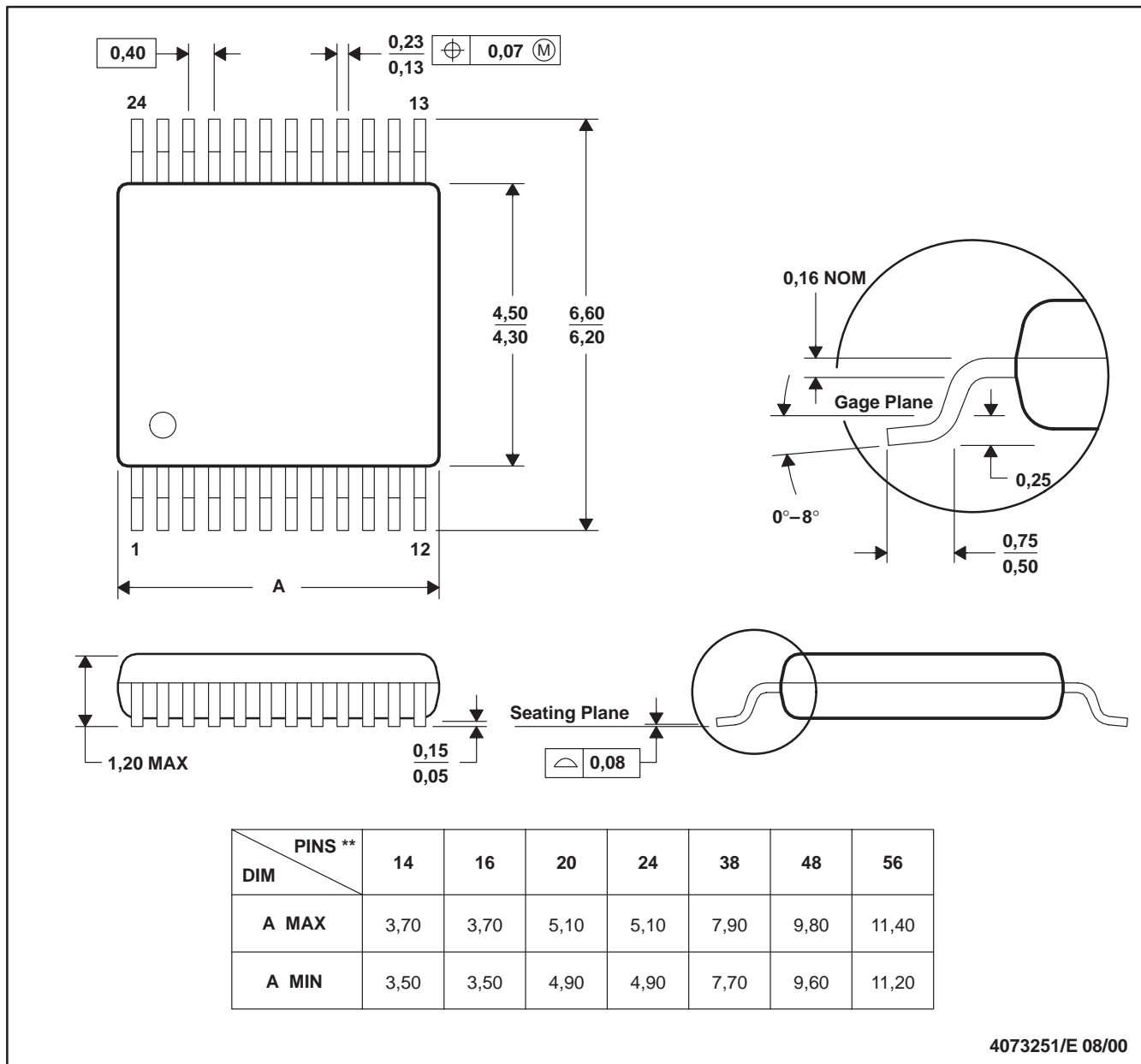
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC16334DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74AVC16334DGVR	TVSOP	DGV	48	2000	853.0	449.0	35.0

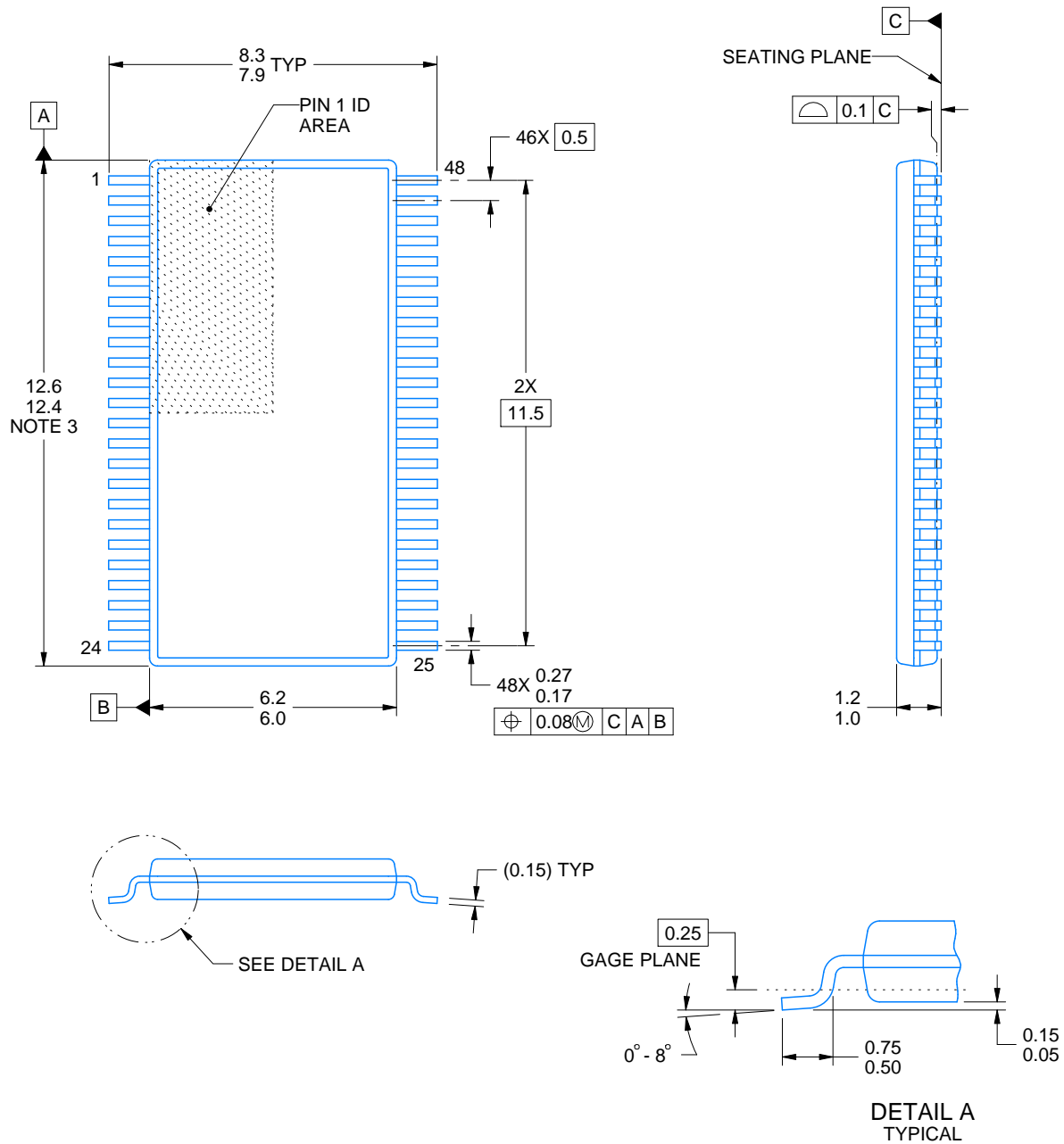
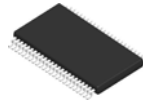
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



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NOTES:

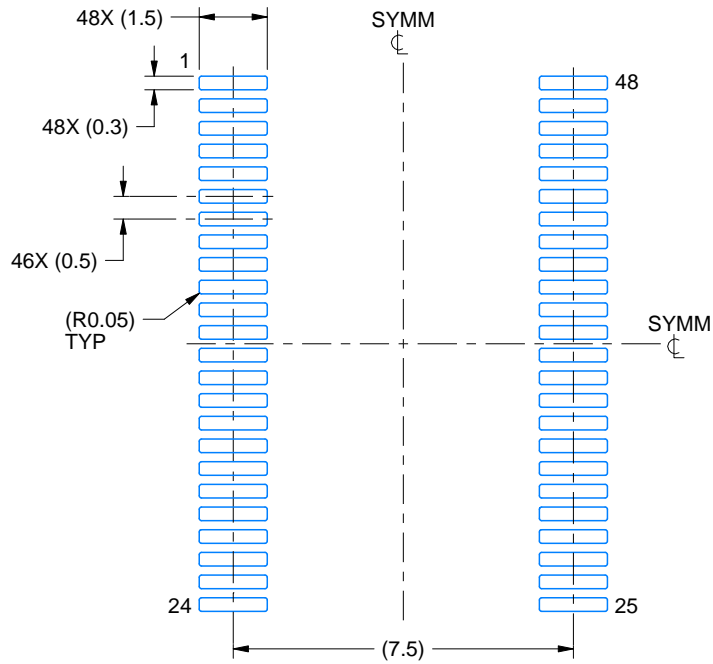
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

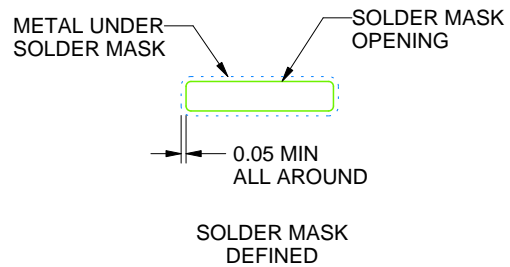
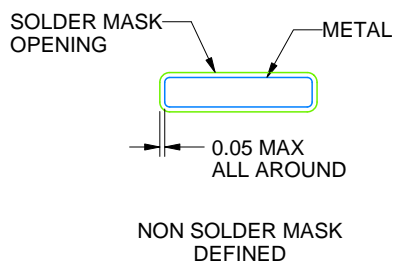
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

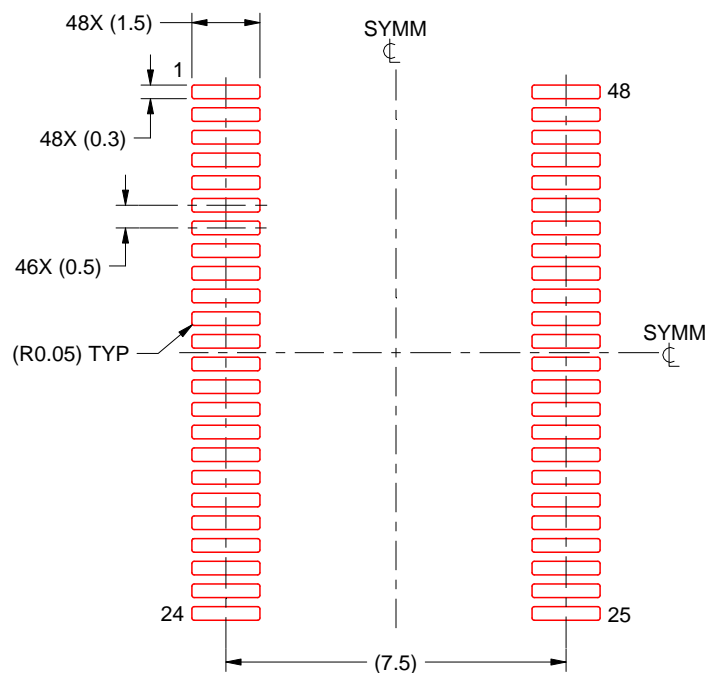
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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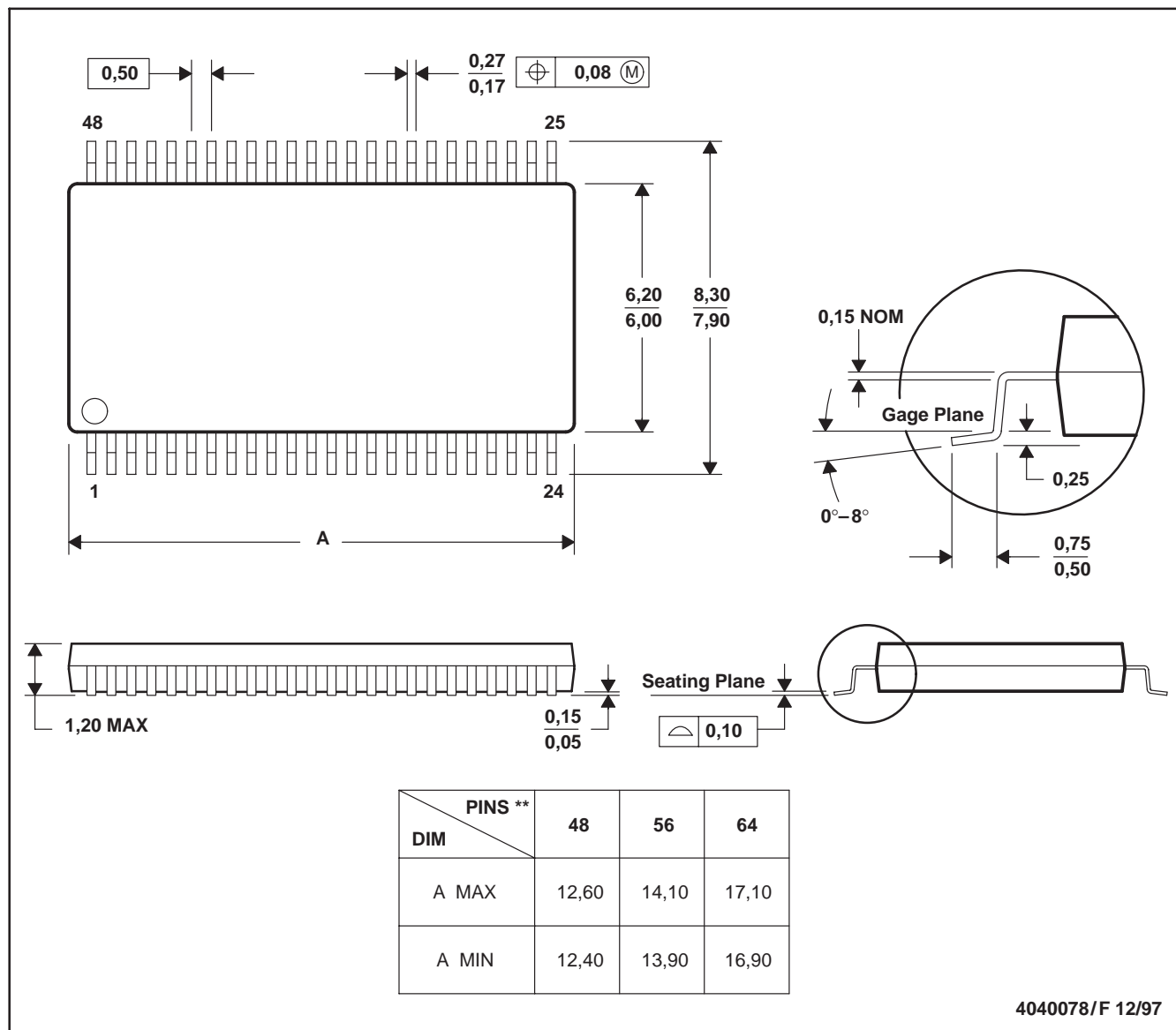
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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