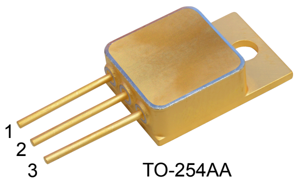
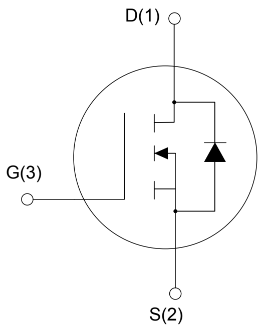
STRH100N6

Datasheet

Rad-Hard N-channel, 60 V, 40 A Power MOSFET



TO-254AA



SC30150

Product status link
STRH100N6

Features

V_{DS}	I_D	$R_{DS(on)}$ typ.	Q_g
60 V	40 A	12 mΩ	134.4 nC

- Fast switching
- 100% avalanche tested
- Hermetic package
- 50 krad TID
- SEE radiation hardened

Description

This N-channel Power MOSFET is developed with STMicroelectronics unique STripFET process.

It has been specifically designed for satellite application able to sustain high TID and immunity to heavy ion effects. It is qualified as per 5205/022 ESCC specification.

Product summary

Product summary							
Part numbers	ESCC part number	Quality level	Package	Lead finish	Mass	Temp. range	EPPL
STRH100N6HY1		Engineering model	TO-254AA	Gold	10 g	-55 to 150 °C	
STRH100N6HYG	5205/022/01	ESCC flight					Yes
STRH100N6HYT	5205/022/02			Solder dip			Yes

Note: Contact ST sales office for information about the specific conditions for product in die form and for other packages.

1 Electrical ratings

T_C= 25 °C unless otherwise specified

Table 1. Absolute maximum ratings (pre-irradiation)

Symbol	Parameter	Value	Unit
V_{DS} (1)	Drain-source voltage (V_{GS} = 0)	60	V
V_{GS} (2)	Gate-source voltage	±20	V
I_D (3)	Drain current (continuous) at T_{case} = 25 °C	40	A
	Drain current (continuous) at T_{case} = 100 °C	25	A
I_{DM} (4)	Drain current (pulsed)	320	A
P_{TOT} (3)	Total power dissipation at T_{case} = 25 °C	176	W
dv/dt (5)	Peak diode recovery voltage slope	2.5	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Max. operating junction temperature range	150	°C

1. *This rating is guaranteed at T_J > 25 °C (see Figure 9. Normalized $V_{(BR)DSS}$ vs temperature).*
2. *This value is guaranteed over the full range of temperature.*
3. *Rated according to the $R_{thj-case}$ + R_{thc-s}*
4. *Pulse width limited by safe operating area.*
5. *I_{SD} ≤ 40 A, di/dt ≤ 600 A/µs, V_{DD} = 80 %$V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	0.50	°C/W
R_{thc-s}	Thermal resistance case-sink typ.	0.21	°C/W

Table 3. **Avalanche characteristics**

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	40	A
E_{AS} (1)	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 40 V)	954	mJ
E_{AS}	Single pulse avalanche energy (starting T_j = 110 °C, I_D = I_{AR}, V_{DD} = 40 V)	280	mJ
E_{AR}	Repetitive pulse avalanche energy (V_{DD} = 40 V, I_{AR} = 40 A, f = 10 KHz, T_J = 25 °C, duty cycle = 50%)	40	mJ
	Repetitive pulse avalanche energy (V_{DD} = 40 V, I_{AR} = 40 A, f = 100 KHz, T_J = 25 °C, duty cycle = 10%)	24	mJ
	Repetitive pulse avalanche energy (V_{DD} = 40 V, I_{AR} = 40 A, f = 100 KHz, T_J = 110 °C, duty cycle = 10%)	7.7	

1. *Maximum rating value.*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4. Pre-irradiation on/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 48 V			10	µA
		V_{GS} = 0 V, V_{DS} = 48 V, T_C = 125 °C			100	
I_{GSS}	Gate body leakage current	V_{GS} = 20 V			100	nA
		V_{GS} = -20 V	-100			
		V_{GS} = 20 V, T_C = 125 °C			200	
		V_{GS} = -20 V, T_C = 125 °C	-200			
$V_{(BR)DSS}$(1)	Drain-to-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	60			V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA, T_C = -55 °C	2.2		5.0	V
		V_{DS} = V_{GS}, I_D = 1 mA	2.0		4.5	
		V_{DS} = V_{GS}, I_D = 1 mA, T_C = 125 °C	1.5		3.7	
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 12 V, I_D = 40 A		12	13.5	mΩ
		V_{GS} = 12 V, I_D = 40 A, T_C = 125 °C			24	

1. *This rating is guaranteed at T_J > 25 °C (see Figure 9).*

Table 5. Pre-irradiation dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	3900	4895	5900	pF
C_{oss} (1)	Output capacitance		860	1080	1300	pF
C_{rss}	Reverse transfer capacitance		300	407	470	pF
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 40 A, V_{GS} = 0 to 12 V	100	134.4	160	nC
Q_{gs}	Gate-to-source charge		18	24	30	nC
Q_{gd}	Gate-to-drain (“Miller”) charge		29	46.5	51	nC
R_G(2)	Gate input resistance	f = 1 MHz Gate DC bias = 0, test signal level = 20 mV, open drain		2.0		Ω

1. *This value is guaranteed over the full range of temperature.*
2. *Not tested, guaranteed by process.*

Table 6. **Pre-irradation switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 12 V	16	28	40	ns
t_r	Rise time		60	115	260	ns
$t_{d(off)}$	Turn-off delay time		50	86	120	ns
t_f	Fall time		60	69	160	ns

Table 7. **Pre-irradation source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				40	A
I_{SDM} (1)	Source-drain current (pulsed)				160	A
V_{SD} (2)	Forward on voltage	I_{SD} = 40 A, V_{GS} = 0 V		1.1	1.5	V
		I_{SD} = 40 A, V_{GS} = 0 V, T_C = 125 °C			1.275	
t_{rr} (3)	Reverse recovery time	I_{SD} = 40 A, di/dt = 100 A/µs, V_{DD} = 48 V	320	400	480	ns
Q_{rr} (3)	Reverse recovery charge			4.7		µC
I_{RRM} (3)	Reverse recovery current			24.6		A
t_{rr} (3)	Reverse recovery time	I_{SD} = 40 A, di/dt = 100 A/µs, V_{DD} = 48 V, T_J = 150 °C		462.5		ns
Q_{rr} (3)	Reverse recovery charge			6.5		µC
I_{RRM} (3)	Reverse recovery current			28.3		A

1. *Pulse width limited by safe operating area*
2. *Pulsed: pulse duration ≤ 680 µs, duty cycle ≤ 2%*
3. *Not tested, guaranteed by process.*

Note: *Refer to Figure 15. Source drain diode*

3 Radiation characteristics

The technology of STMicroelectronics Rad-Hard Power MOSFETs is extremely resistant to radiative environments. Every manufacturing lot is tested for total ionizing dose (irradiation done according to the ESCC 22900 specification, window 1.) using the TO-3 package. Both pre-irradiation and post-irradiation performance are tested and specified using the same circuitry and test conditions in order to provide a direct comparison.

(T_{amb} = 22 ± 3 °C unless otherwise specified).

3.1 Total dose radiation (TID) testing

One bias conditions using the TO-254AA package:

- V_{GS} bias: + 15 V applied and V_{DS} = 0 V during irradiation

The following parameters are measured (see Table 8 , Table 9 and Table 10):

- Before irradiation
- After irradiation
- After 24 hrs at room temperature
- after 168 hrs at 100 °C anneal

Table 8. Post-irradiation on/off states at T_J = 25 °C, (Co60 γ rays 50 K Rad(Si))

Symbol	Parameter	Test conditions	Drift values Δ	Unit
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	80% $V_{(BR)DSS}$	+10	µA
I_{GSS}	Gate body leakage current	V_{GS} = 20 V	1.5	nA
		V_{GS} = -20 V	-1.5	
$V_{(BR)DSS}$	Drain-to-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	-15%	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	-60% / + 25%	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 40 A	±15%	Ω

Table 9. Dynamic post-irradiation at T_J= 25 °C, (Co60 γ rays 50 K Rad(Si))

Symbol	Parameter	Test conditions	Drift values Δ	Unit
Q_g	Total gate charge	V_{DS} = 30 V, I_G = 1 mA, V_{GS} = 12 V, I_{DS} = 40 A	-5% / +50%	nC
Q_{gs}	Gate-to-source charge		±35%	
Q_{gd}	Gate-to-drain charge		-5% / +110%	

Table 10. **Source drain diode post-irradiation at T_J= 25 °C, (Co60 γ rays 50 K Rad(Si))**

Symbol	Parameter	Test conditions	Drift values Δ	Unit
V_{DS}(1)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 40 A	±5%	V

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3.2 Single event effect SOA

The technology of the STMicroelectronics Rad-Hard Power MOSFETs is extremely resistant to heavy ion environment for single event effect (irradiation per MIL-STD-750E, method 1080 bias circuit in Figure 2. Single event effect, bias circuit) SEB and SEGR tests have been performed with a fluence of 3e+5 ions/cm².

The accept/reject criteria are :

- SEB (test):
  drain voltage checked, trigger level is set to V_{DS} = - 2 V. Stop condition: as soon as a SEB occurs or if the fluence reaches 3e+5 ions/cm².
- SEGR test:
  the gate current is monitored every 100 ms. A gate stress is performed before and after irradiation. Stop condition: as soon as the gate current reaches 1 mA (during irradiation or during PIGS test) or if the fluence reaches 3e+5 ions/cm².

The results are:

- SEB immune at 60 MeV/mg/cm^2
- SEGR immune at 60 MeV/mg/cm^2 within the safe operating area (SOA) given in Table 11. Single event effect (SEE), safe operating area (SOA) and Figure 1. Single event effect, SOA.

Table 11. **Single event effect (SEE), safe operating area (SOA)**

Ion	Let (Mev/(mg/cm^2)	Energy (MeV)	Range (µm)	V_{DS} (V)				
				at V_{GS}=0 V	at V_{GS}=-2 V	at V_{GS}=-5 V	at V_{GS}=-10 V	at V_{GS}=-20 V
Kr	32	768	94	60	48	39	27	15
Xe	60	1217	89	30	30			

Figure 1. Single event effect, SOA

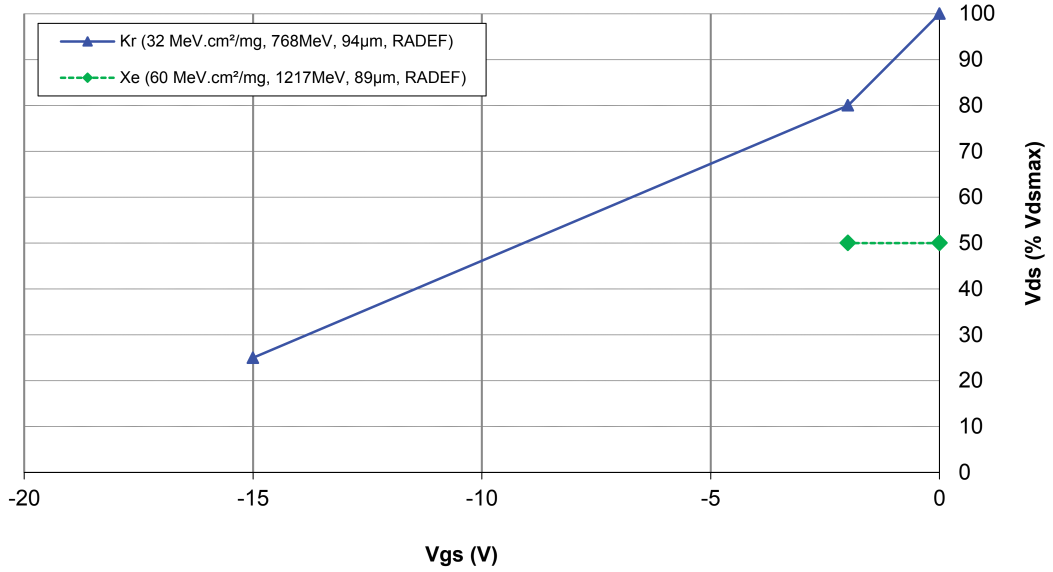
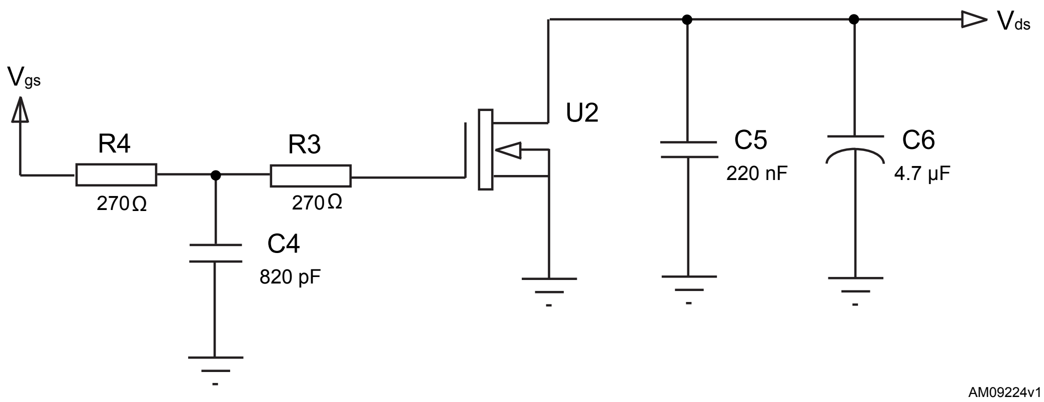


Figure 2. Single event effect, bias circuit



Note: Bias condition during radiation refer to Table 11. Single event effect (SEE), safe operating area (SOA).

4 Electrical characteristics (curves)

Figure 3. Safe operating area

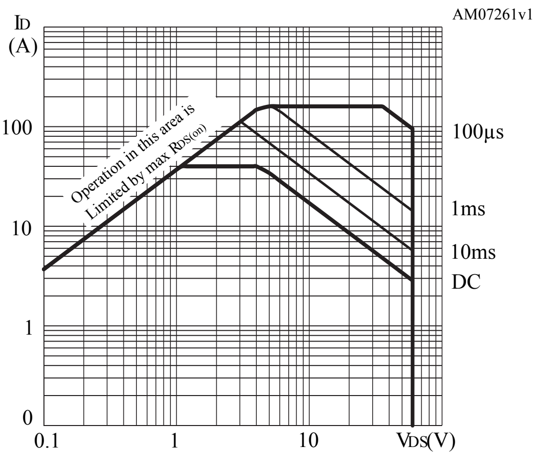


Figure 4. Thermal impedance

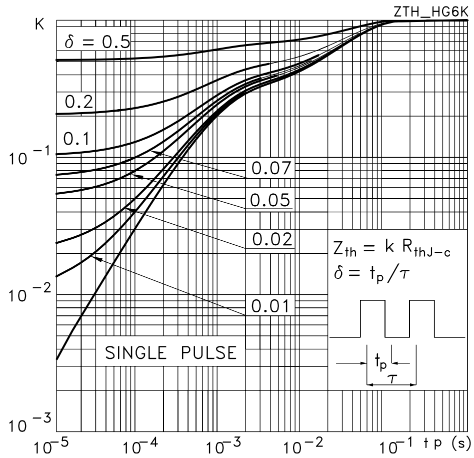


Figure 5. Output characteristics

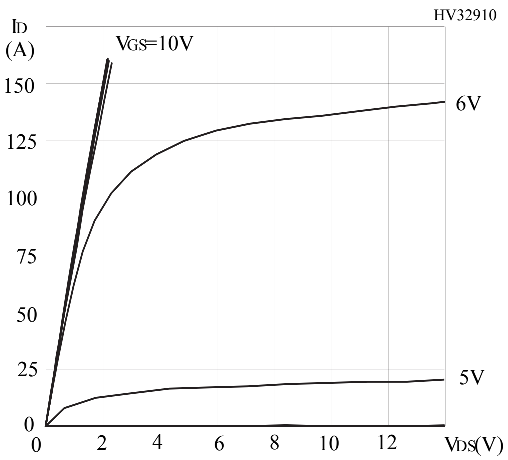


Figure 6. Transfer characteristics

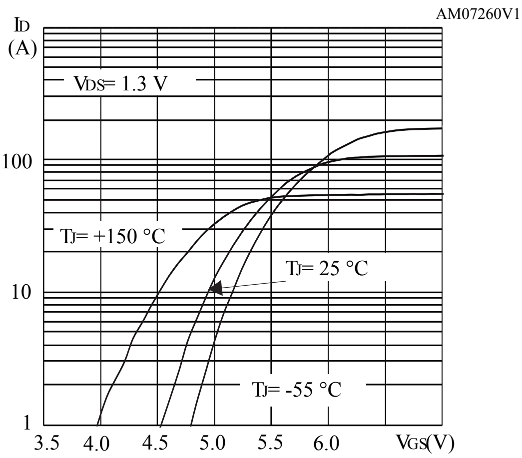


Figure 7. Gate charge vs gate-source voltage

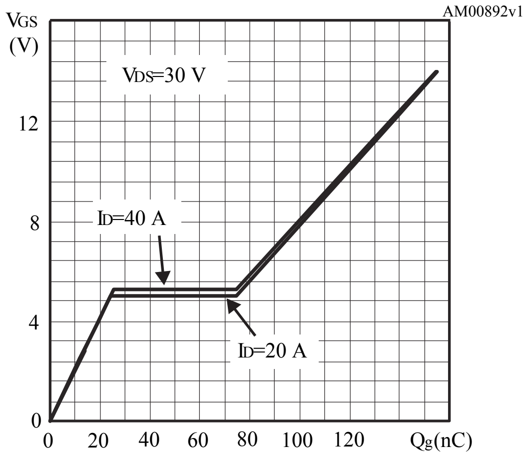


Figure 8. Capacitance variations

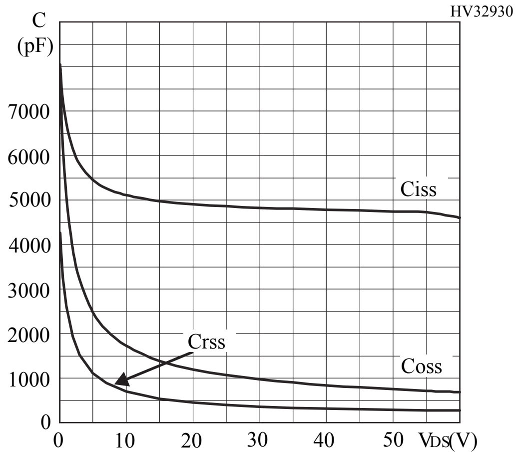


Figure 9. Normalized $V_{(BR)DSS}$ vs temperature

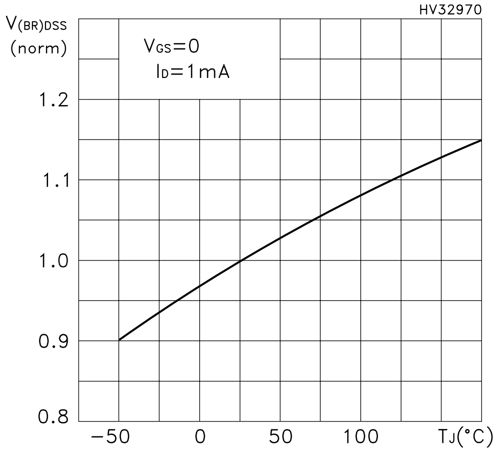


Figure 10. Static drain-source on-resistance

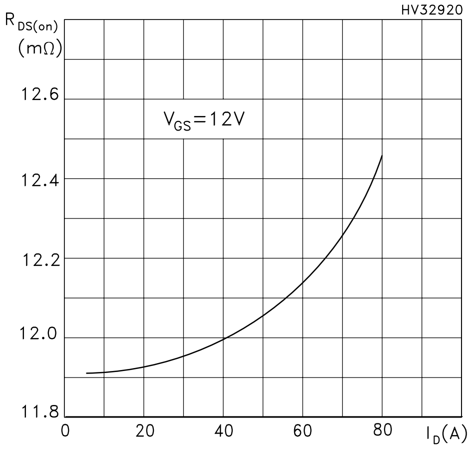


Figure 11. Normalized gate threshold voltage vs temperature

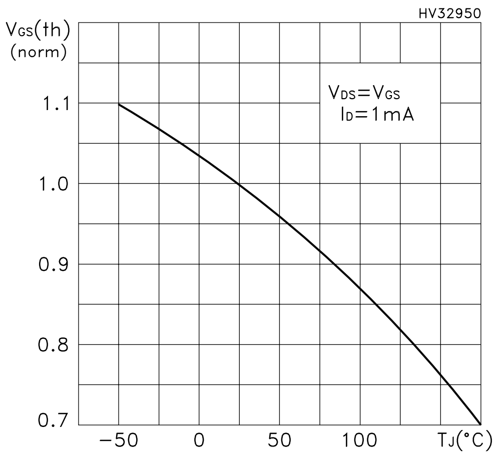


Figure 12. Normalized on-resistance vs temperature

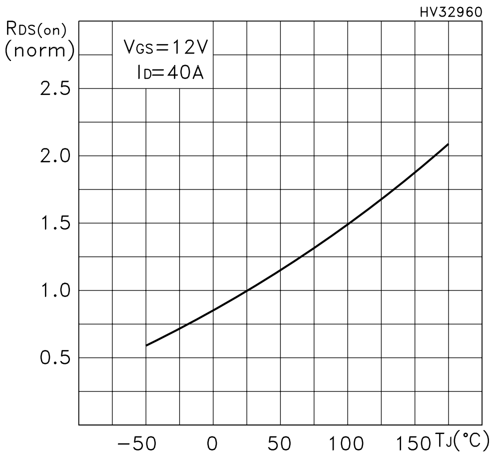
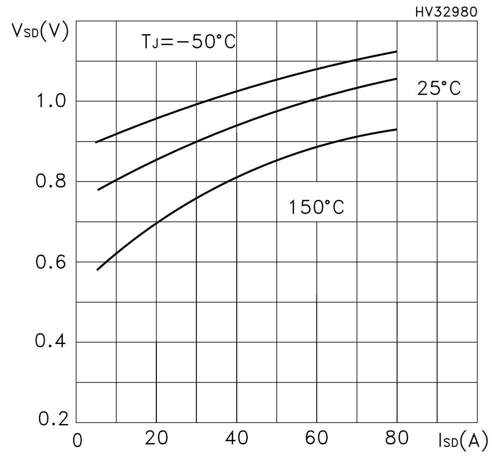
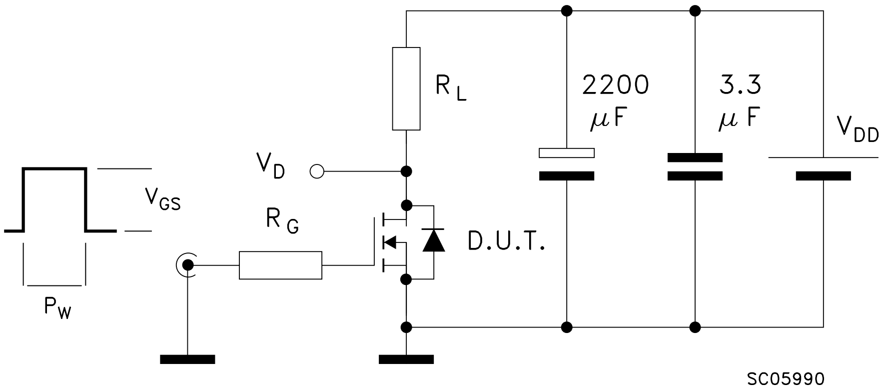


Figure 13. Source drain-diode forward characteristics



5 Test circuits

Figure 14. **Switching times test circuit for resistive load**



Note: Max driver V_{GS} slope = 1V/ns (no DUT)

Figure 15. **Source drain diode**

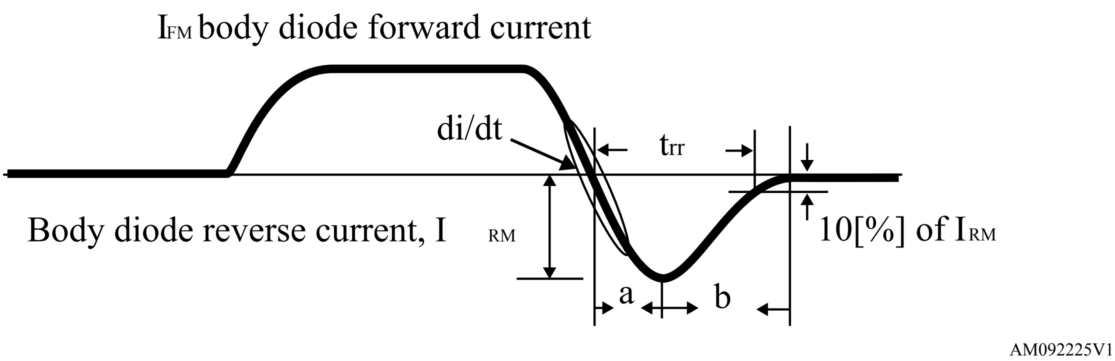
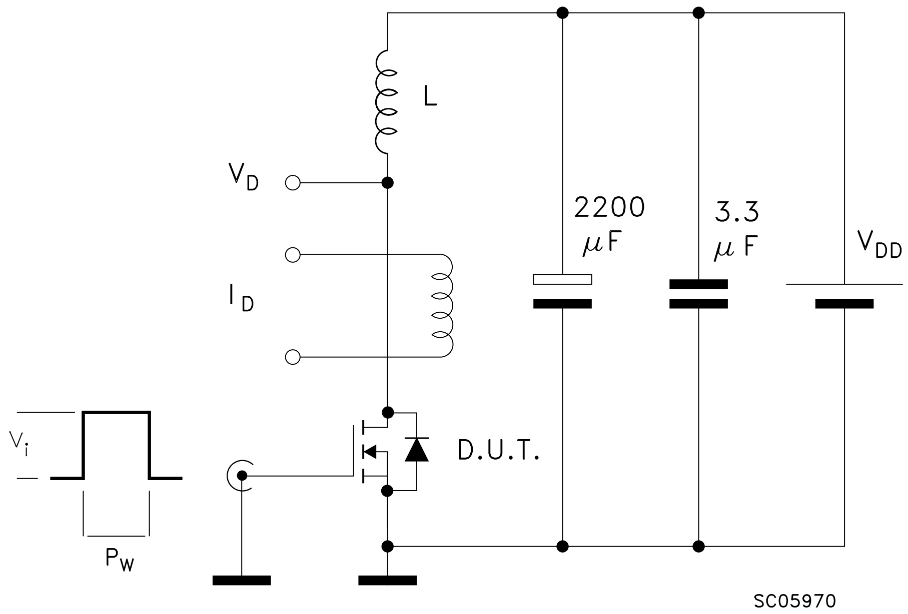


Figure 16. **Unclamped inductive load test circuit (single pulse and repetitive)**

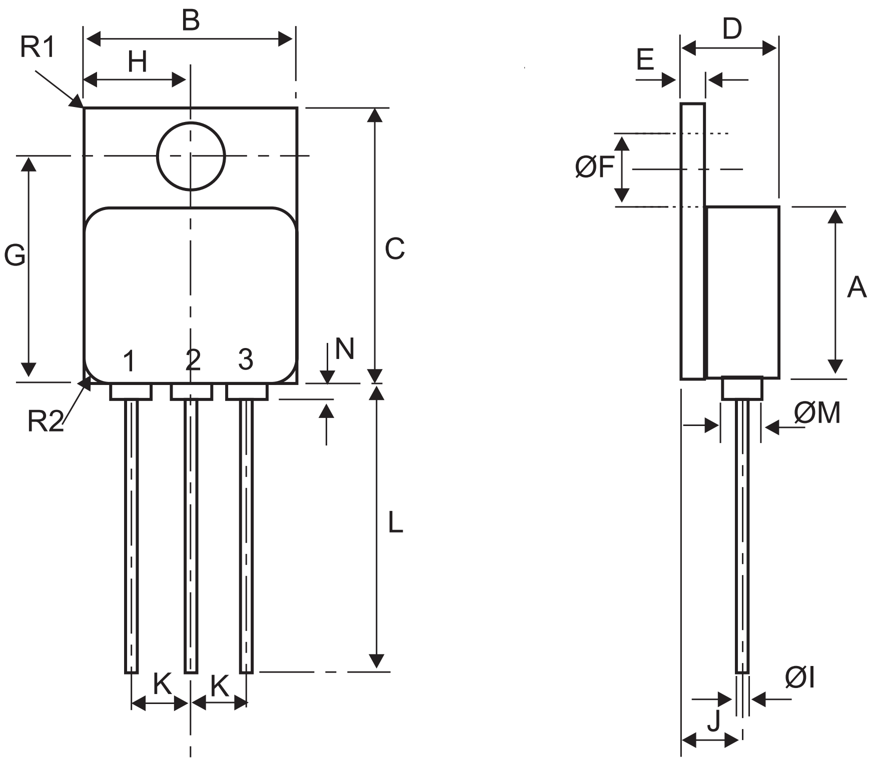


6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 TO-254AA package information

Figure 17. TO-254AA package outline



The TO-254-AA is a metallic package. It is not connected to any pin nor to the inside die.

0005824 rev13

Table 12. **TO-254AA package mechanical data**

Symbols	Dimensions (mm)			Dimension (inches)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	13.59		13.84	0.535		0.545
B	13.59		13.84	0.535		0.545
C	20.07		20.32	0.790		0.800
D	6.30		6.70	0.248		0.264
E	1.00		1.35	0.039		0.054
ØF	3.50		3.90	0.137		0.154
G	16.89		17.40	0.665		0.685
H		6.86			0.270	
ØI	0.89	1.14	2.00	0.035	0.045	0.079
J		3.81			0.150	
K		3.81			0.150	
L	12.95		14.50	0.510		0.571
ØM		3.05			0.120	
N			0.71			0.028
R1			1.00			0.039
R2		1.65			0.065	

7 Order codes

Table 13. Ordering information

Order codes	ESCC part number	Quality level	EPPL	Package	Lead finish	Marking	Packing
STRH100N6HY1		Engineer model		TO-254AA	Gold	STRH100N6HY1 + BeO	Strip pack
STRH100N6HYG	5205/022/01	ESCC flight	Yes			520502201F + BeO	
STRH100N6HYT	5205/022/02		Yes		Solder dip	520502202F + BeO	

For specific marking only the complete structure is:

- ST Logo
- ESA Logo
- Date code (date of sealing of the package) : YYWWA
  - YY: year
  - WW: week number
  - A: week index
- ESCC part number (as mentioned in the table)
- Warning signs (e.g. BeO)
- Country of origin: FR (France)
- Part serial number within in the assembly lot

Contact ST sales office for information about the specific conditions for products in die form and for other packages.

8 Other information

8.1 Date code

The date code for “ESCC flight” is structured as follows: yywwz where:

- yy: last two digits of year
- ww: week digits
- z: lot index in the week

8.2 Documentation

The table below provide a summary of the documentation provided with each type of products.

Table 14. **Default documentation provided with the parts**

Quality level	Radiation level	Documentation
Engineering model	-	-
ESCC flight	50Krad	Certificate of conformance. Radiation verification test report

Revision history

Table 15. Document revision history

Date	Version	Changes
04-Jan-2011	1	First release.
27-Jul-2011	2	Updated order codes in Table 1: Device summary and Table 14: Ordering information. Minor text changes.
09-Nov-2011	3	Updated dynamic values on Table 6: Pre-irradation dynamic and Table 7: Pre-irradation switching times.
27-Feb-2013	4	Corrected ID value on: – Features – Table 2: Absolute maximum ratings (pre-irradiation) – Table 5: Pre-irradation on/off states – Table 6: Pre-irradation dynamic – Table 8: Pre-irradation source drain diode – Table 9: Post-irradiation on/off states at T_J = 25 °C, (Co60 g rays 70 K Rad(Si)) – Table 10: Dynamic post-irradiation at T_J = 25 °C, (Co60 g rays 70 K Rad(Si)) – Table 11: Source drain diode post-irradiation at T_J = 25 °C, (Co60 g rays 70 K Rad(Si))
02-Jul-2013	5	Updated Table 1: Device summary and Table 14: Ordering information. Added Chapter 7.1: Other information.
16-Dec-2013	6	Modified: Description Minor text changes
16-Dec-2015	7	Updated features in cover page. Updated Table 5, Table 8, Table 9, Table 10, Table 11 and Table 15.
31-Mar-2016	8	Updated Table 8: Pre-irradation source drain diode. Minor text changes.
21-Dec-2016	9	Updated Table 7: Pre-irradation switching times and Table 8: Pre-irradation source drain diode. Minor text changes.
20-Mar-2019	10	Updated Table 13. Ordering information. Minor text changes.