- **Member of the Texas Instruments Widebus™ Family**
- **DOC™ (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation**
- **Dynamic Drive Capability Is Equivalent to Standard Outputs With $I_{OH}$ and $I_{OL}$ of ±24 mA at 2.5-V $V_{CC}$**
- **Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

## description

A Dynamic Output Control (DOC™) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical $V_{OL}$ vs $I_{OL}$ and $V_{OH}$ vs $I_{OH}$ curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to TI application reports *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

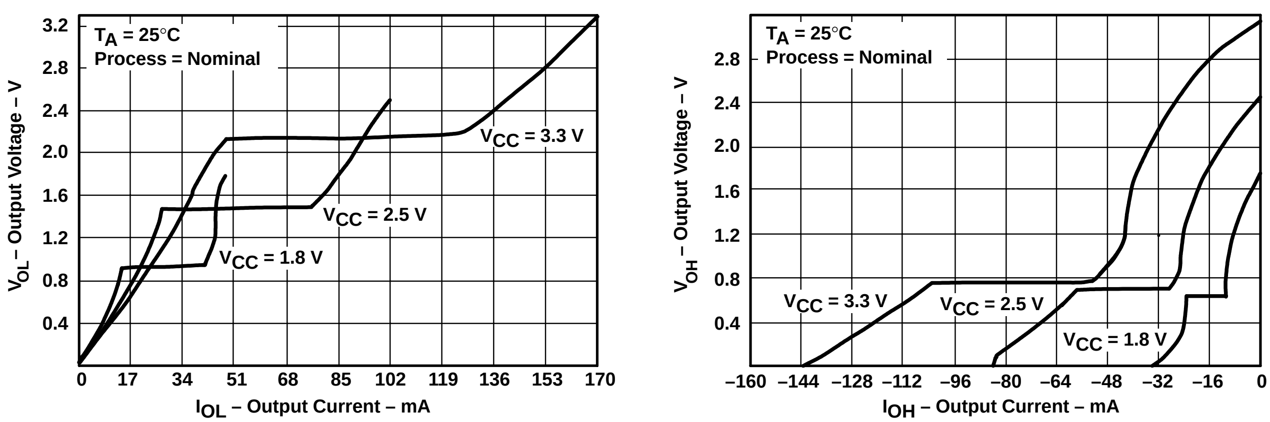



**Figure 1. Output Voltage vs Output Current**

This 18-bit universal bus driver is operational at 1.2-V to 3.6-V $V_{CC}$, but is designed specifically for 1.65-V to 3.6-V $V_{CC}$ operation.

Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## terminal assignments

**DGG OR DGV PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| NC | 1 | 56 | GND |
| NC | 2 | 55 | NC |
| Y1 | 3 | 54 | A1 |
| GND | 4 | 53 | GND |
| Y2 | 5 | 52 | A2 |
| Y3 | 6 | 51 | A3 |
| $V_{CC}$ | 7 | 50 | $V_{CC}$ |
| Y4 | 8 | 49 | A4 |
| Y5 | 9 | 48 | A5 |
| Y6 | 10 | 47 | A6 |
| GND | 11 | 46 | GND |
| Y7 | 12 | 45 | A7 |
| Y8 | 13 | 44 | A8 |
| Y9 | 14 | 43 | A9 |
| Y10 | 15 | 42 | A10 |
| Y11 | 16 | 41 | A11 |
| Y12 | 17 | 40 | A12 |
| GND | 18 | 39 | GND |
| Y13 | 19 | 38 | A13 |
| Y14 | 20 | 37 | A14 |
| Y15 | 21 | 36 | A15 |
| $V_{CC}$ | 22 | 35 | $V_{CC}$ |
| Y16 | 23 | 34 | A16 |
| Y17 | 24 | 33 | A17 |
| GND | 25 | 32 | GND |
| Y18 | 26 | 31 | A18 |
| $\overline{OE}$ | 27 | 30 | CLK |
| LE | 28 | 29 | GND |

NC – No internal connection

### ORDERING INFORMATION

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | TSSOP – DGG | Tape and reel | SN74AVC16835DGGR | AVC16835 |
| | TVSOP – DGV | Tape and reel | SN74AVC16835DGVR | CVA835 |

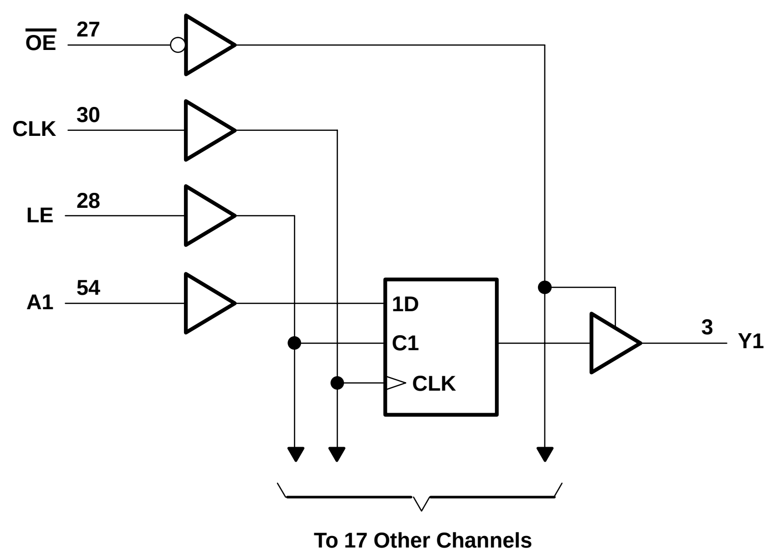
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each universal bus driver)**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OE}$ | LE | CLK | A | Y |
| H | X | X | X | Z |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | ↑ | L | L |
| L | L | ↑ | H | H |
| L | L | L or H | X | $Y_0$† |

† Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes low

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . . . . . . –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) . . . . . . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$
(see Note 1) . . . . . . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, $V_O$
(see Notes 1 and 2) . . . . . . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . . . . . . –50 mA
Continuous output current, $I_O$ . . . . . . . . . . ±50 mA
Continuous current through each $V_{CC}$ or GND . . . . . . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package . . . . . . . . . . 64°C/W
DGV package . . . . . . . . . . 48°C/W
Storage temperature range, $T_{stg}$ . . . . . . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.4 | 3.6 | V |
| | | Data retention only | 1.2 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.2 V | $V_{CC}$ | | V |
| | | $V_{CC}$ = 1.4 V to 1.6 V | $0.65 \times V_{CC}$ | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | $0.65 \times V_{CC}$ | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.2 V | | GND | V |
| | | $V_{CC}$ = 1.4 V to 1.6 V | | $0.35 \times V_{CC}$ | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | $0.35 \times V_{CC}$ | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 3.6 | V |
| $V_O$ | Output voltage | Active state | 0 | $V_{CC}$ | V |
| | | 3-state | 0 | 3.6 | |
| $I_{OHS}$ | Static high-level output current† | $V_{CC}$ = 1.4 V to 1.6 V | | –2 | mA |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | –4 | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | –8 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | –12 | |
| $I_{OLS}$ | Static low-level output current† | $V_{CC}$ = 1.4 V to 1.6 V | | 2 | mA |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | 4 | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 8 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 1.4 V to 3.6 V | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

† Dynamic drive capability is equivalent to standard outputs with $I_{OH}$ and $I_{OL}$ of ±24 mA at 2.5-V $V_{CC}$. See Figure 1 for $V_{OL}$ vs $I_{OL}$ and $V_{OH}$ vs $I_{OH}$ characteristics. Refer to TI application reports ***AVC Logic Family Technology and Applications***, literature number **SCEA006**, and ***Dynamic Output Control (DOC™) Circuitry Technology and Applications***, literature number **SCEA009**.

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OHS}$ = –100 µA, | | 1.4 V to 3.6 V | $V_{CC}$–0.2 | | | V |
| | | $I_{OHS}$ = –2 mA, | $V_{IH}$ = 0.91 V | 1.4 V | 1.05 | | | |
| | | $I_{OHS}$ = –4 mA, | $V_{IH}$ = 1.07 V | 1.65 V | 1.2 | | | |
| | | $I_{OHS}$ = –8 mA, | $V_{IH}$ = 1.7 V | 2.3 V | 1.75 | | | |
| | | $I_{OHS}$ = –12 mA, | $V_{IH}$ = 2 V | 3 V | 2.3 | | | |
| $V_{OL}$ | | $I_{OLS}$ = 100 µA | | 1.4 V to 3.6 V | | | 0.2 | V |
| | | $I_{OLS}$ = 2 mA, | $V_{IL}$ = 0.49 V | 1.4 V | | | 0.4 | |
| | | $I_{OLS}$ = 4 mA, | $V_{IL}$ = 0.57 V | 1.65 V | | | 0.45 | |
| | | $I_{OLS}$ = 8 mA, | $V_{IL}$ = 0.7 V | 2.3 V | | | 0.55 | |
| | | $I_{OLS}$ = 12 mA, | $V_{IL}$ = 0.8 V | 3 V | | | 0.7 | |
| $I_I$ | | $V_I$ = $V_{CC}$ or GND | | 3.6 V | | | ±2.5 | µA |
| $I_{off}$ | | $V_I$ or $V_O$ = 3.6 V | | 0 | | | ±10 | µA |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND, | $\overline{OE}$ = $V_{CC}$ | 3.6 V | | | ±10 | µA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 3.6 V | | | 40 | µA |
| $C_i$ | CLK input | $V_I$ = $V_{CC}$ or GND | | 2.5 V | | 4 | | pF |
| | | | | 3.3 V | | 4 | | |
| | Control inputs | $V_I$ = $V_{CC}$ or GND | | 2.5 V | | 4 | | |
| | | | | 3.3 V | | 4 | | |
| | Data inputs | $V_I$ = $V_{CC}$ or GND | | 2.5 V | | 2.5 | | |
| | | | | 3.3 V | | 2.5 | | |
| $C_o$ | Outputs | $V_O$ = $V_{CC}$ or GND | | 2.5 V | | 6.5 | | pF |
| | | | | 3.3 V | | 6.5 | | |

† Typical values are measured at $T_A$ = 25°C.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 5)

| | | | | $V_{CC}$ = 1.2 V | | $V_{CC}$ = 1.5 V ± 0.1 V | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | | | | | | 150 | | 150 | | 150 | MHz |
| $t_w$ | Pulse duration | LE high | | | | | | 3.3 | | 3.3 | | 3.3 | | ns |
| | | CLK high or low | | | | | | 3.3 | | 3.3 | | 3.3 | | |
| $t_{su}$ | Setup time | Data before CLK↑ | | 1 | | 0.9 | | 0.7 | | 0.7 | | 0.7 | | ns |
| | | Data before LE↓ | CLK high | 1.7 | | 1.6 | | 1.2 | | 0.8 | | 0.8 | | |
| | | | CLK low | 2 | | 0.9 | | 0.7 | | 0.5 | | 0.5 | | |
| $t_h$ | Hold time | Data after CLK↑ | | 1.5 | | 1.3 | | 1 | | 0.9 | | 1.3 | | ns |
| | | Data after LE↓ | CLK high | 3.2 | | 2.4 | | 2 | | 1.7 | | 1.6 | | |
| | | | CLK low | 2.8 | | 2.1 | | 1.7 | | 1.5 | | 1.4 | | |

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 5)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.2 V | $V_{CC}$ = 1.5 V ± 0.1 V | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | | | | 150 | | 150 | | 150 | | MHz |
| $t_{pd}$ | A | Y | 4.5 | 1.2 | 6.2 | 1.3 | 5.5 | 1 | 3.1 | 0.9 | 2.5 | ns |
| | LE | | 6.2 | 1.6 | 9.4 | 1.3 | 7.2 | 1.1 | 4.7 | 0.9 | 3.8 | |
| | CLK | | 5.2 | 1.6 | 7.8 | 1.5 | 6 | 1 | 3.7 | 0.8 | 3.1 | |
| $t_{en}$ | $\overline{OE}$ | Y | 7.1 | 2.4 | 10.2 | 2.2 | 8.8 | 1.5 | 6.7 | 1.2 | 6.2 | ns |
| $t_{dis}$ | $\overline{OE}$ | Y | 6.9 | 2.2 | 10.3 | 2 | 8.4 | 1.2 | 5.3 | 1.1 | 5.3 | ns |

## switching characteristics, $T_A$ = 0°C to 85°C, $C_L$ = 0 pF†

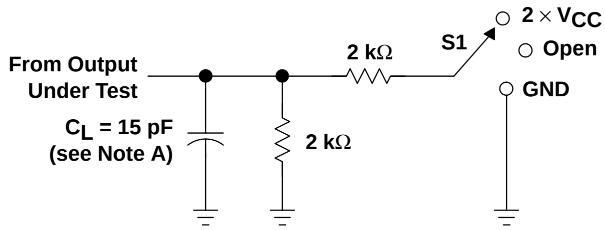
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 3.3 V ± 0.15 V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{pd}$ | A | Y | 0.6 | 1.3 | ns |
| | CLK | | 0.7 | 1.5 | |

† Texas Instruments SPICE simulation data

## operating characteristics, $T_A$ = 25°C

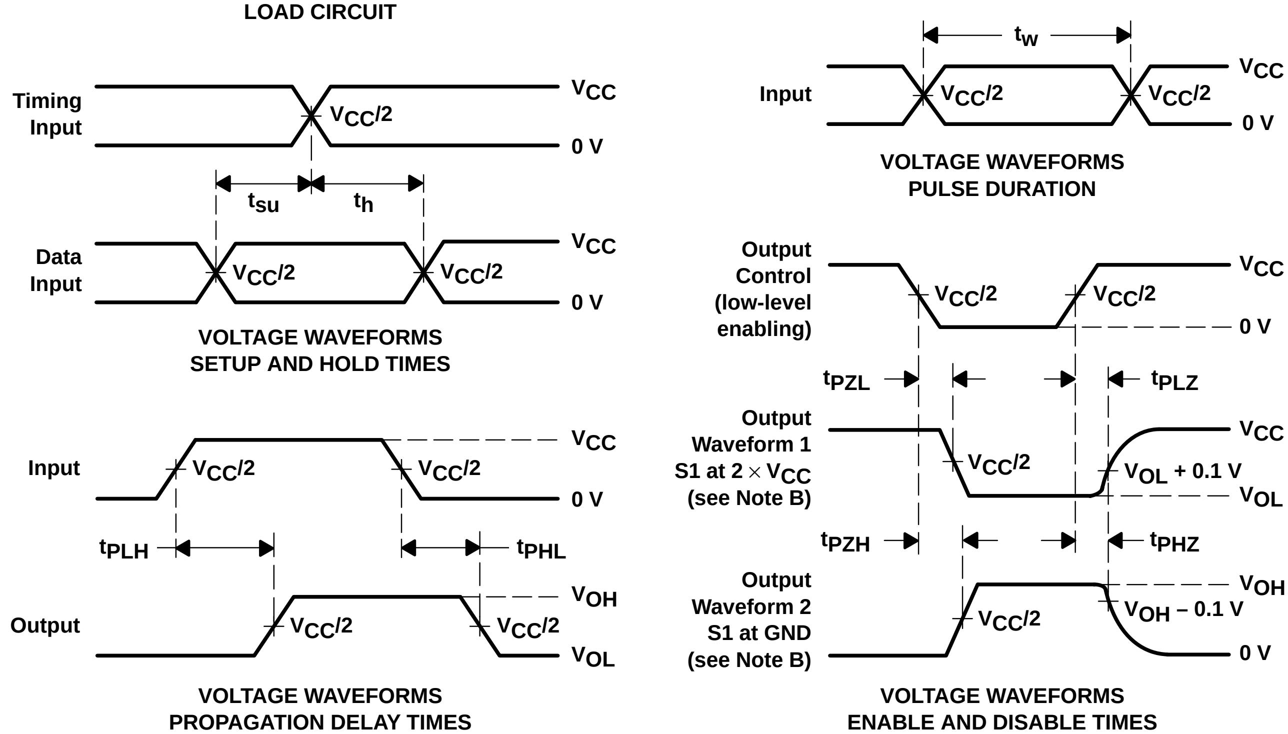
| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 0, f = 10 MHz | 45 | 48 | 52 | pF |
| | | Outputs disabled | | 23 | 25 | 28 | |

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 1.2 V AND 1.5 V ± 0.1 V




LOAD CIRCUIT

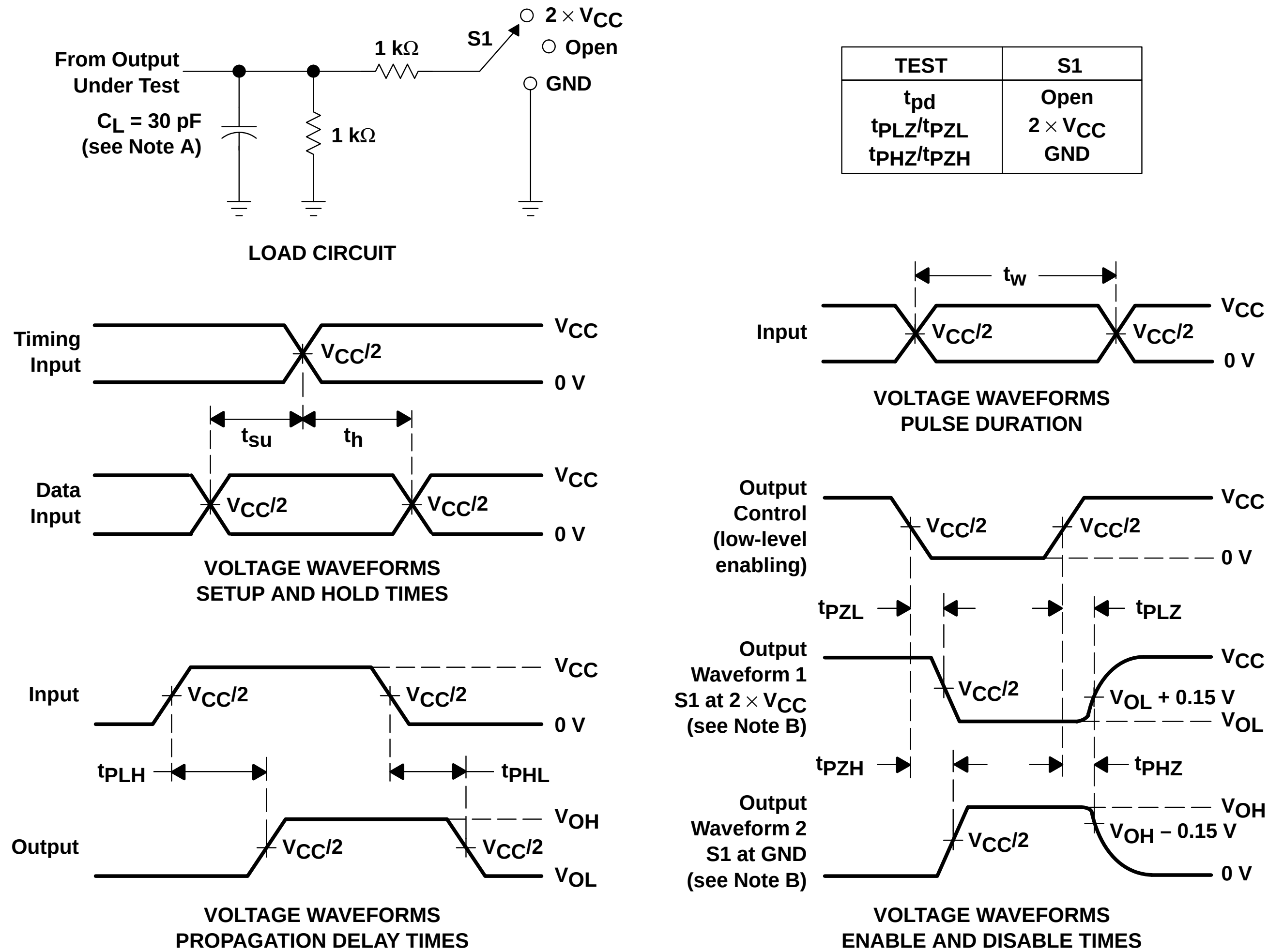
| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 2. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 1.8 V ± 0.15 V

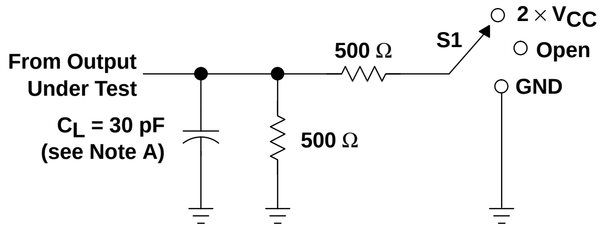



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

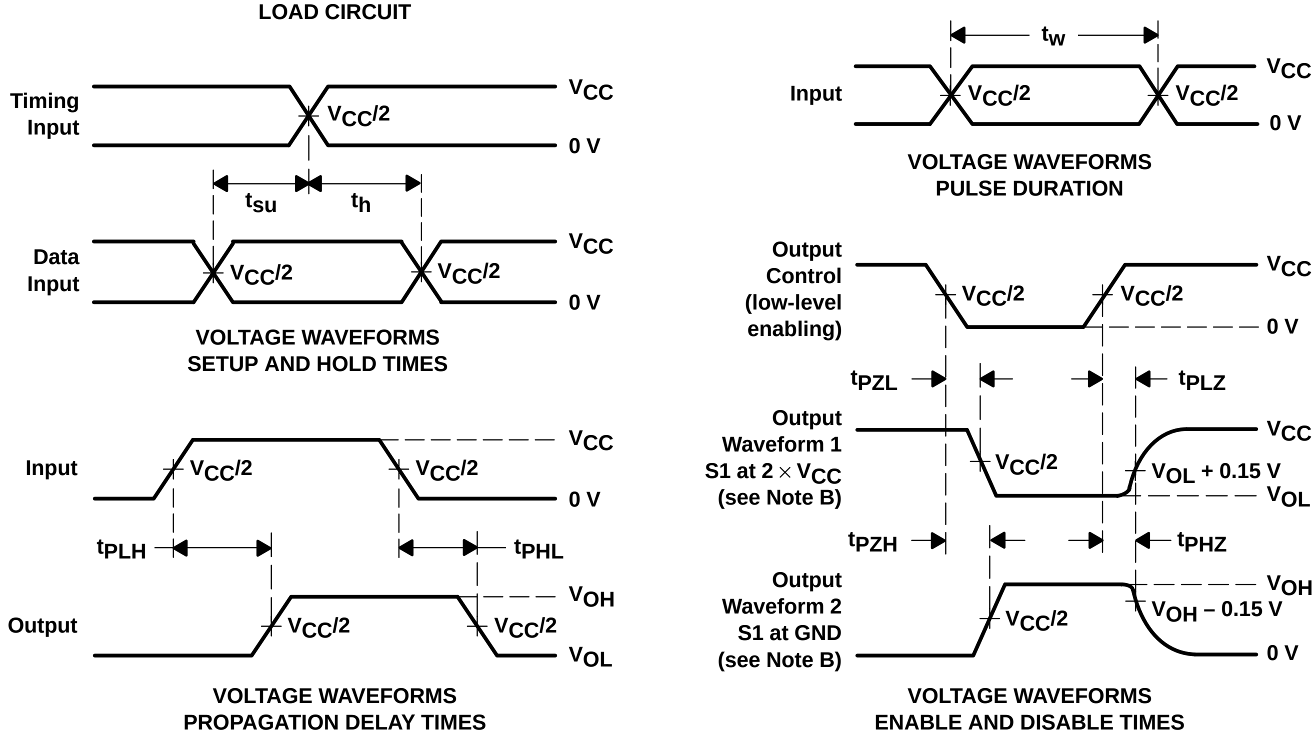
**Figure 3. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V




LOAD CIRCUIT

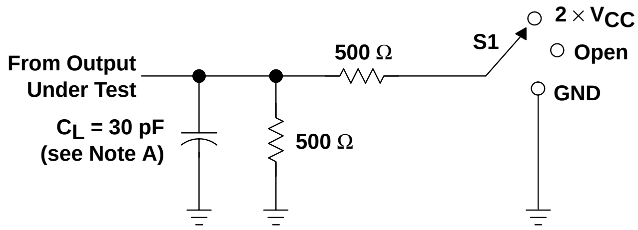
| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

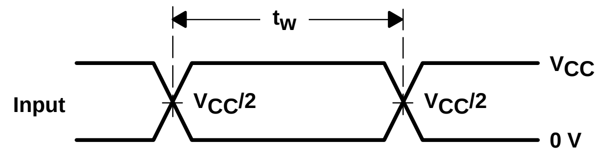
**Figure 4. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 3.3 V ± 0.3 V

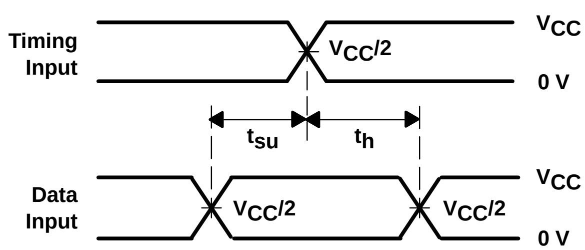



**LOAD CIRCUIT**

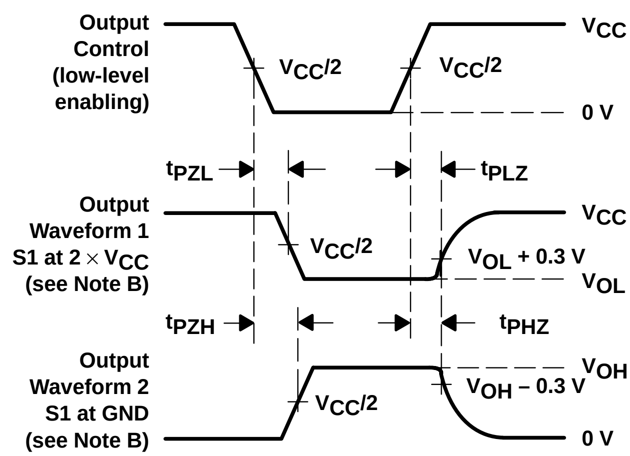
| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

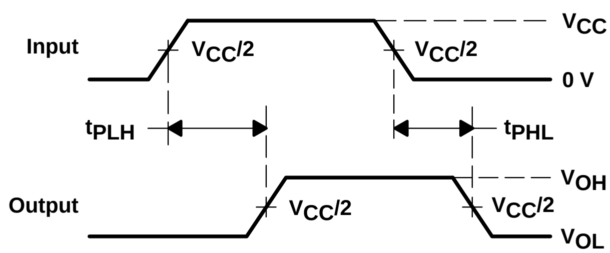



**VOLTAGE WAVEFORMS**
**PULSE DURATION**




**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**




**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**

**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 5. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AVC16835DGVR | ACTIVE | TVSOP | DGV | 56 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CVA835 | Samples |

[(1)] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

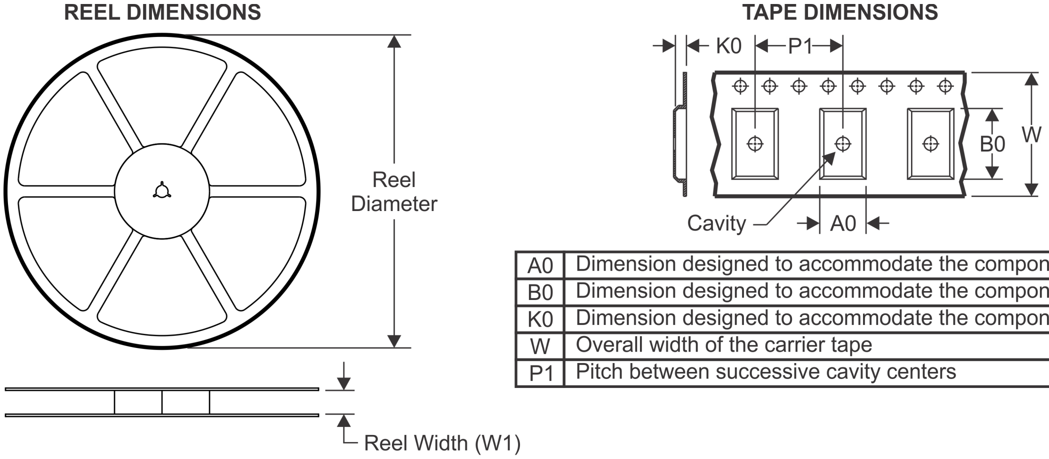
[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

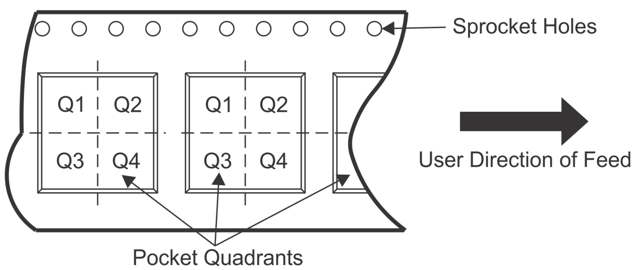
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

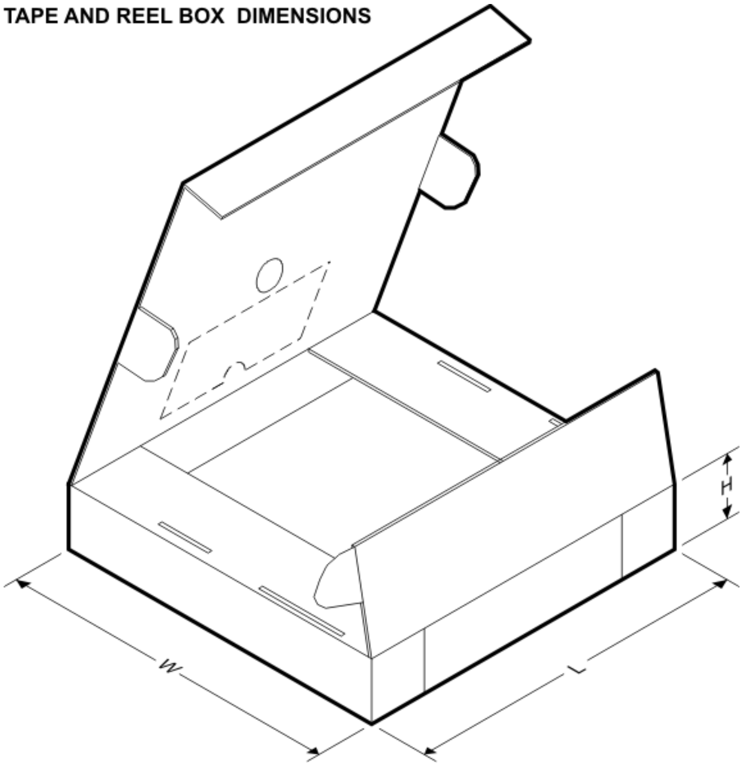
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AVC16835DGVR | TVSOP | DGV | 56 | 2000 | 330.0 | 24.4 | 6.8 | 11.7 | 1.6 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

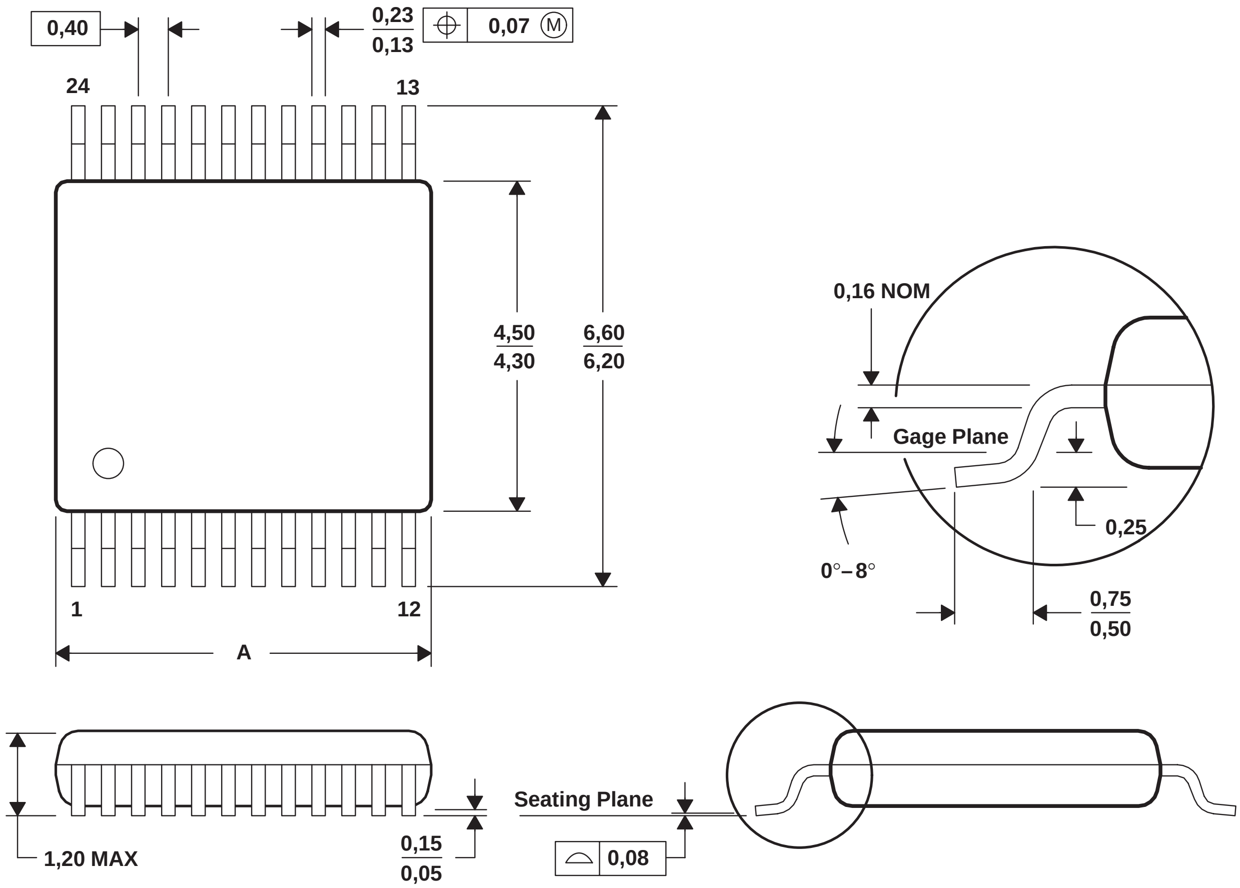



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AVC16835DGVR | TVSOP | DGV | 56 | 2000 | 367.0 | 367.0 | 45.0 |

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

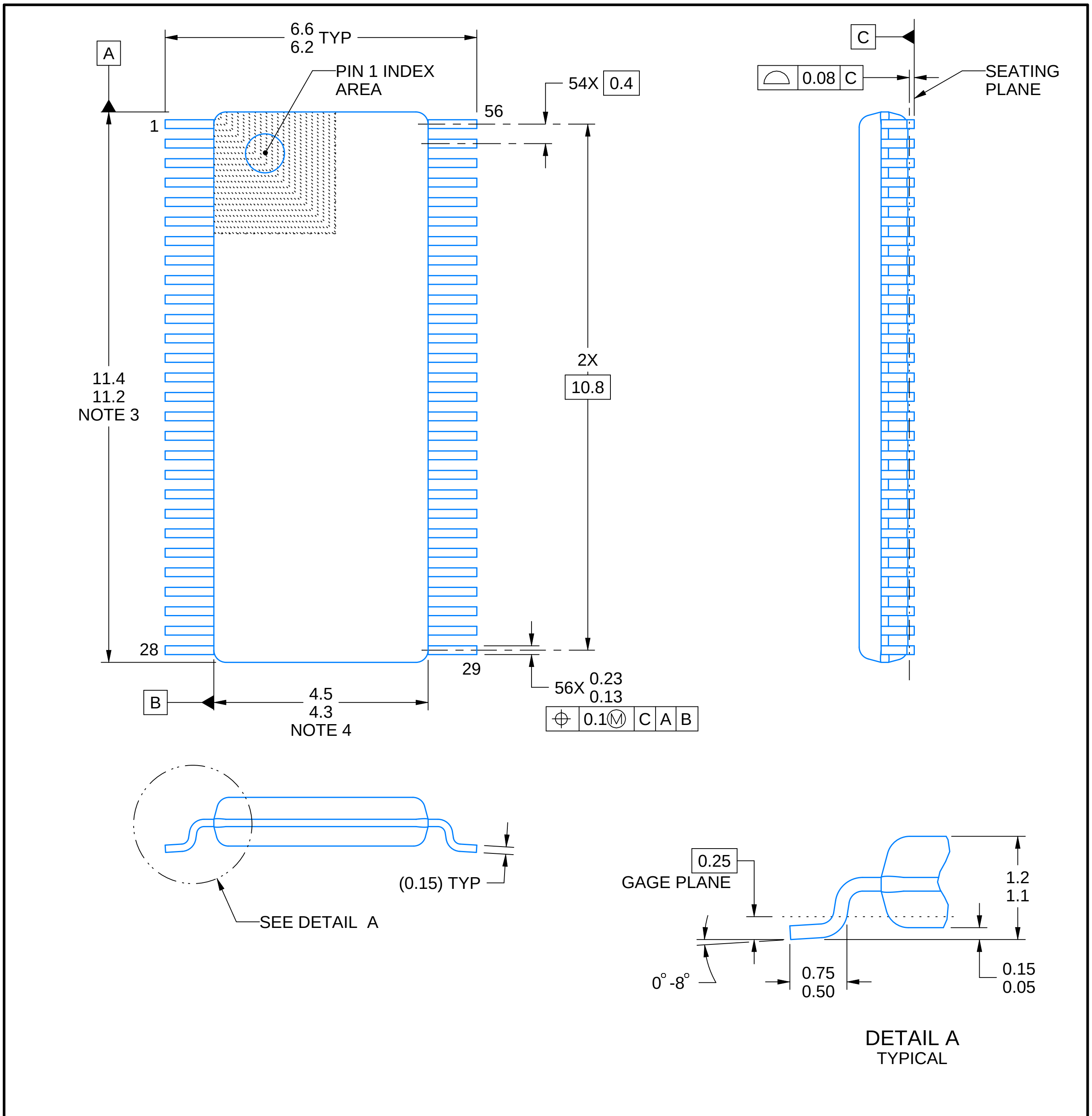
**24 PINS SHOWN**




| PINS ** / DIM | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

4073251/E 08/00

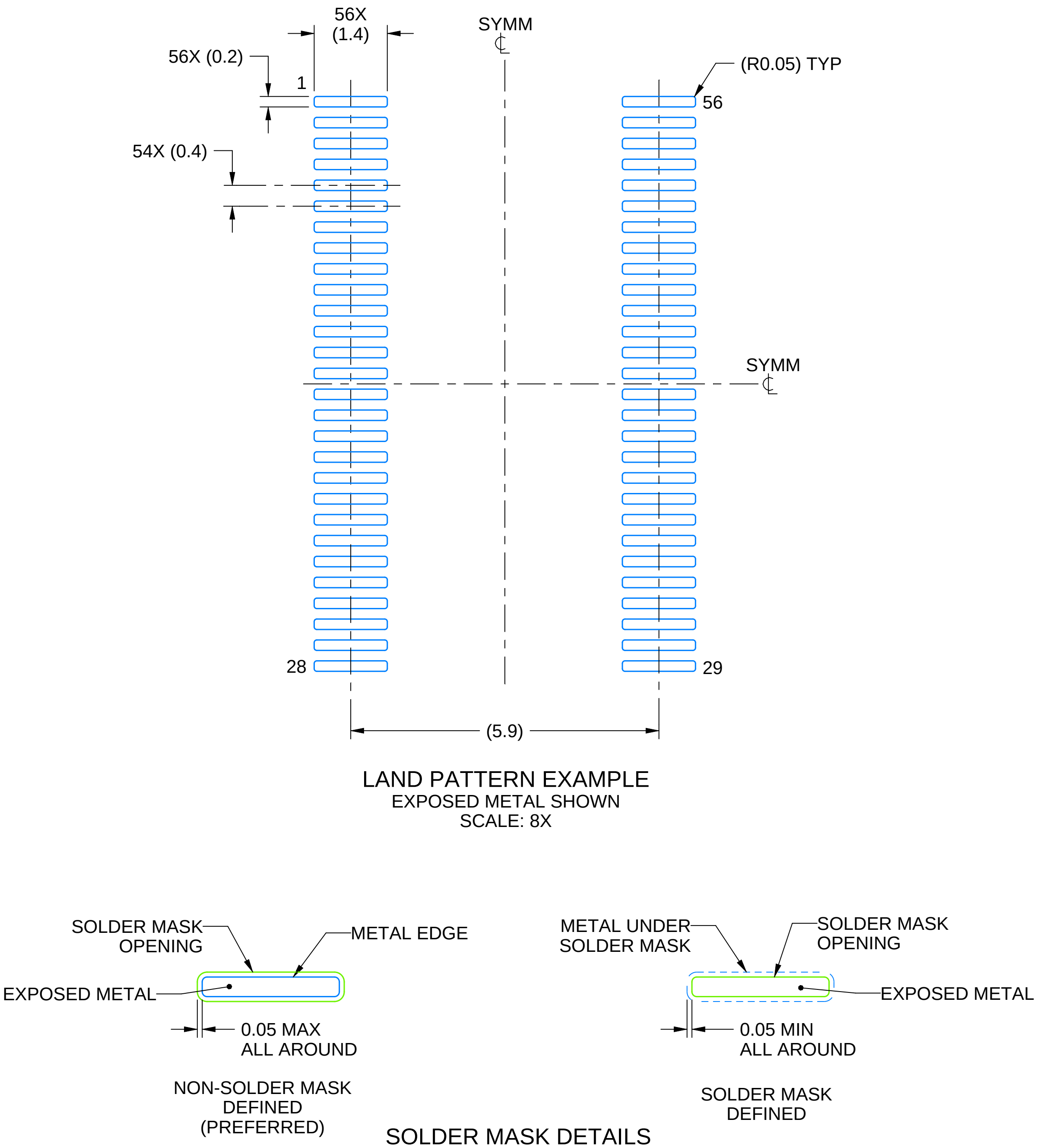
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194




4220240/B 12/2020

NOTES:

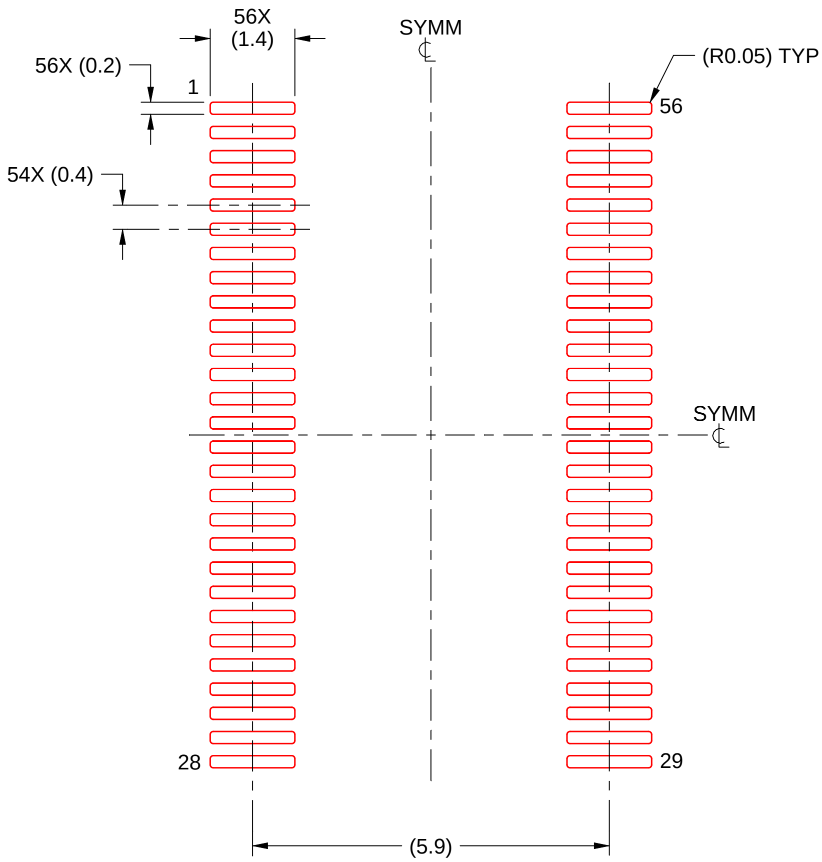
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-194.




4220240/B 12/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4220240/B 12/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.