STP52P3LLH6

P-channel -30 V, 0.01 Ω typ., -52 A, STripFET™ H6 Power MOSFET in TO-220 package

Datasheet - production data

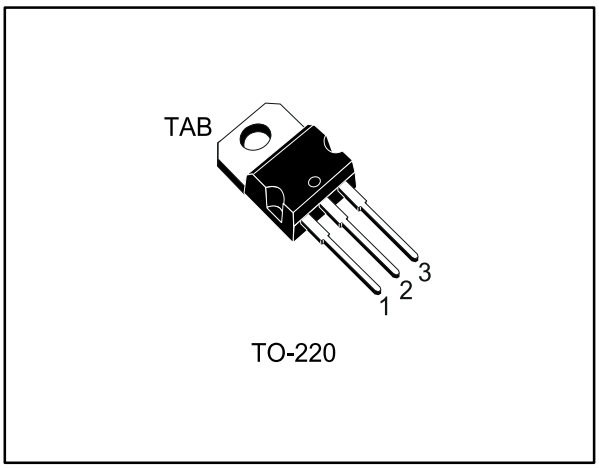
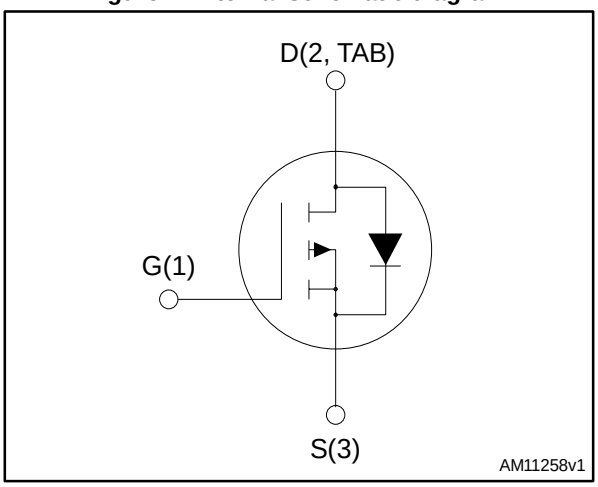


Figure 1: Internal schematic diagram



Order codes	V_{DSS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STP52P3LLH6	-30 V	0.012 Ω	-52 A	70 W

- Very low on-resistance
- Very low gate charge
- High avalanche
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Features

Table 1: Device summary

Order codes	Marking	Package	Packaging
STP52P3LLH6	52P3LLH6	TO-220	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-30	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	-52	A
I_D	Drain current (continuous) at T_C = 100 °C	-37.5	A
I_{DM} (1)	Drain current (pulsed)	-208	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	W
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature	175	°C

Notes:

(1)Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2.14	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	I_D = -250 µA, V_{GS} = 0	-30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = -30 V			-1	µA
		V_{GS} = 0, V_{DS} = -30 V, Tc = 125 °C			-10	µA
I_{GSS}	Gate body leakage current	V_{GS} = ± 20 V, V_{DS} = 0			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1		-2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = -10 V, I_D = -26 A		0.01	0.012	Ω
		V_{GS} = -4.5 V, I_D = -26 A		0.014	0.017	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = -25 V, f = 1 MHz, V_{GS} = 0	-	3350	-	pF
C_{oss}	Output capacitance		-	414	-	pF
C_{rss}	Reverse transfer capacitance		-	287	-	pF
Q_g	Total gate charge	V_{DD} = -15 V, I_D = -52 A V_{GS} = -4.5 V (see *Figure 14: "Gate charge test circuit"*)	-	33	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain charge		-	11	-	nC
R_g	Gate input resistance	I_D = 0 Gate bias = 0 Test signal level = 20 mV; f = 1MHz	-	1.5	-	Ω

Table 6: Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = -24 V, I_D = -15 A, R_G = 4.7 Ω, V_{GS} = -10 V (see *Figure 13: "Switching times test circuit for resistive load"*)	-	12.8	-	ns
t_r	Rise time		-	112	-	ns
$t_{d(off)}$	Turn-off delay time		-	61	-	ns
t_f	Fall time		-	45	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}(1)	Forward on voltage	I_{SD} = -52 A, V_{GS} = 0	-		-1.1	V
t_{rr}	Reverse recovery time	I_{SD} = -52 A, di/dt = 100 A/µs, V_{DD} = -24 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	25.2		ns
Q_{rr}	Reverse recovery charge		-	17.4		nC
I_{RRM}	Reverse recovery current		-	-1.4		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

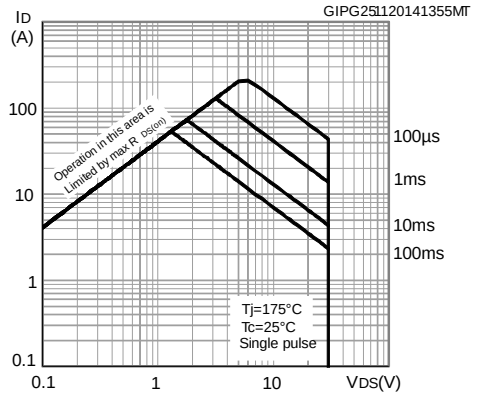


Figure 3: Thermal impedance

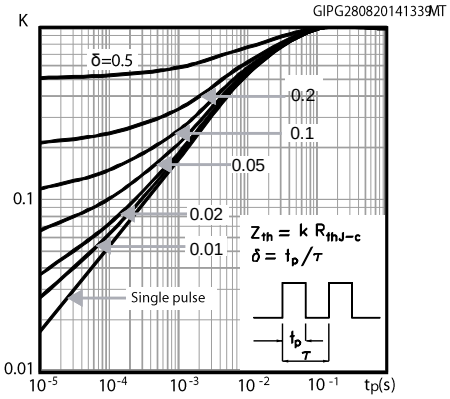


Figure 4: Output characteristics

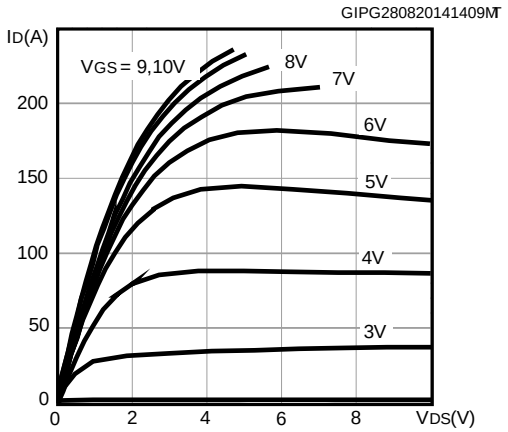


Figure 5: Transfer characteristics

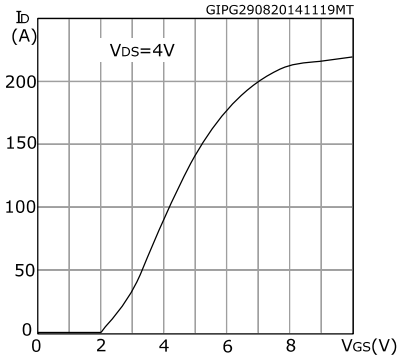


Figure 6: Gate charge vs gate-source voltage

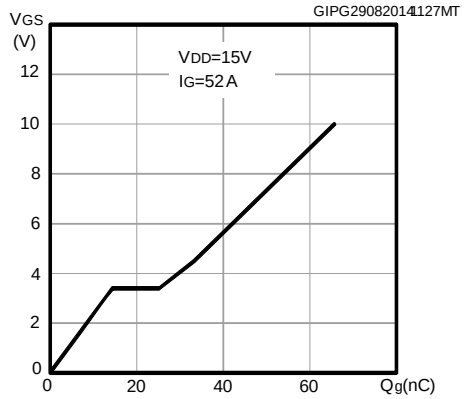


Figure 7: Static drain-source on-resistance

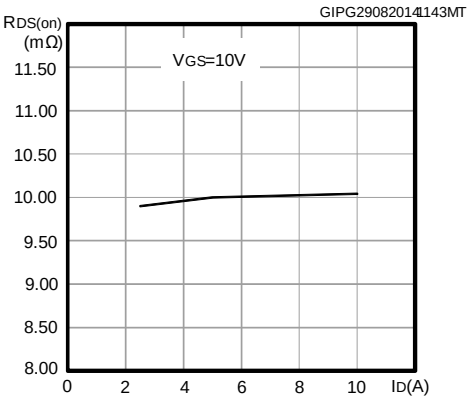


Figure 8: Capacitance variations

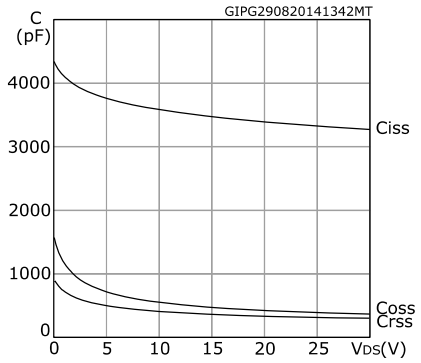


Figure 9: Normalized gate threshold voltage vs temperature

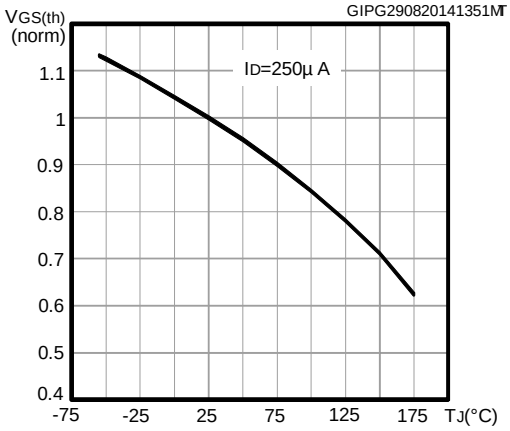


Figure 10: Normalized on-resistance vs temperature

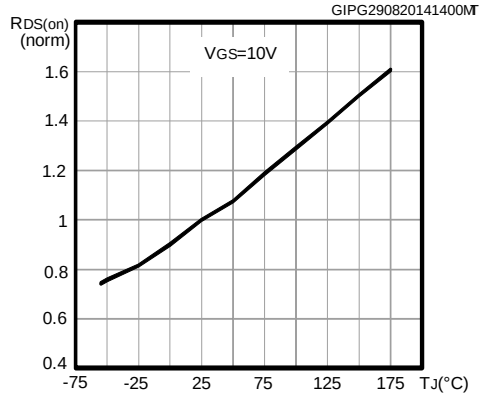


Figure 11: Normalized V(BR)DSS vs temperature

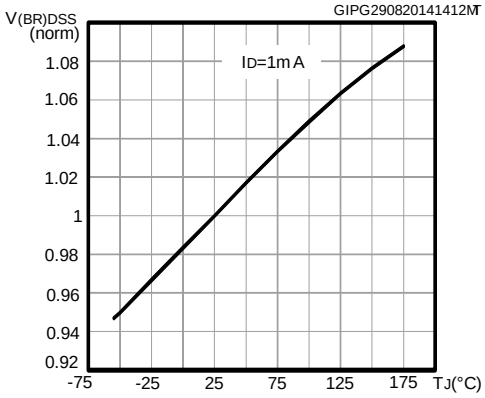
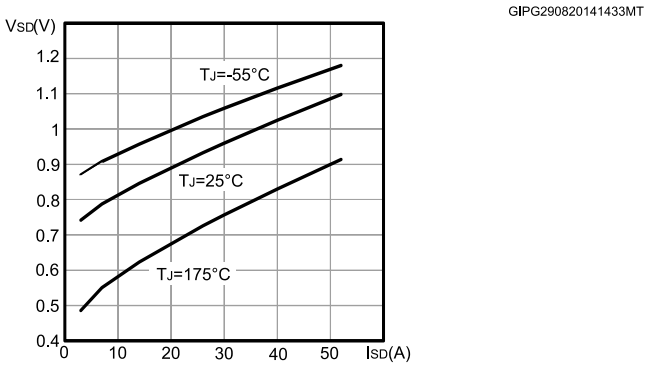


Figure 12: Source-drain diode forward characteristics



For the P-channel Power MOSFET, current and voltage polarities are reversed.

3 Test circuits

Figure 13: Switching times test circuit for resistive load

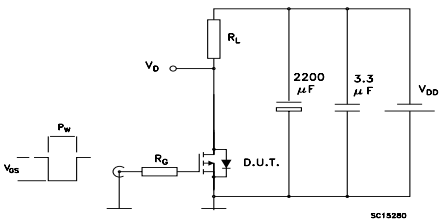


Figure 14: Gate charge test circuit

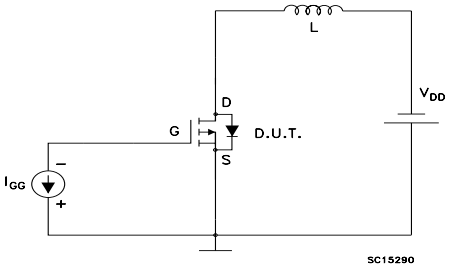
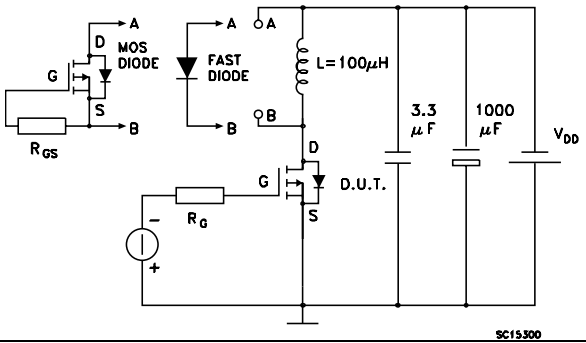


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220 package information

Figure 16: TO-220 type A package outline

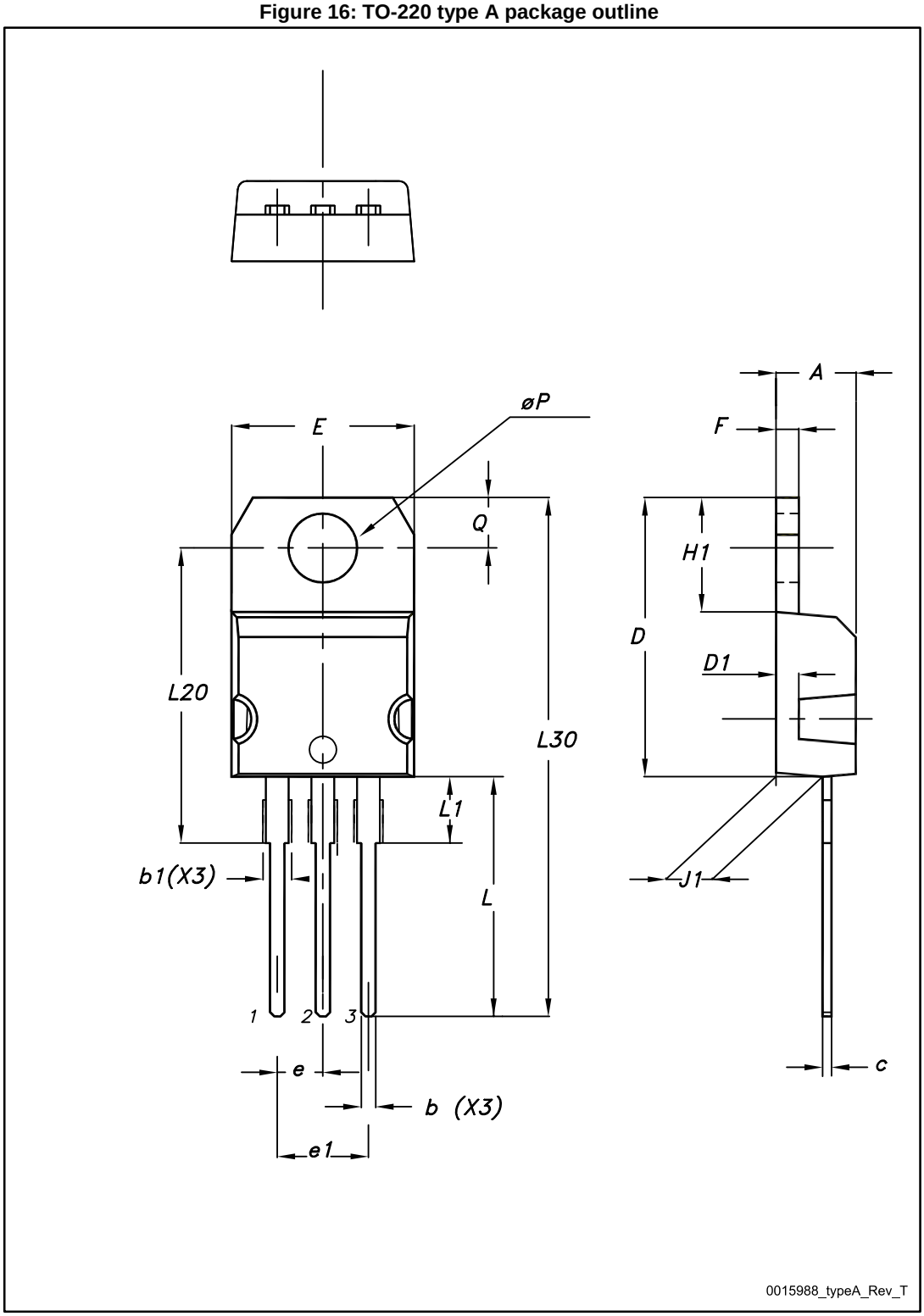


Table 8: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
24-Nov-2014	1	First release.
12-Oct-2015	2	Document status promoted from preliminary to production data. Minor text changes.

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