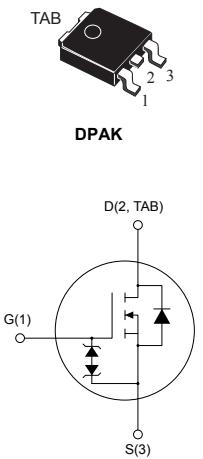


## N-channel 600 V, 550 mΩ typ., 8 A, MDmesh™ DM2 Power MOSFET in a DPAK package

### Features



AM0147SV1

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STD8N60DM2	600 V	600 mΩ	8 A	85 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast-recovery diode series. It offers very low recovery charge ( $Q_{rr}$ ) and time ( $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status link									
<a href="#">STD8N60DM2</a>									
Product summary									
<table border="1"> <tr> <td>Order code</td><td>STD8N60DM2</td></tr> <tr> <td>Marking</td><td>8N60DM2</td></tr> <tr> <td>Package</td><td>DPAK</td></tr> <tr> <td>Packing</td><td>Tape and reel</td></tr> </table>		Order code	STD8N60DM2	Marking	8N60DM2	Package	DPAK	Packing	Tape and reel
Order code	STD8N60DM2								
Marking	8N60DM2								
Package	DPAK								
Packing	Tape and reel								

## 1 Electrical ratings

**Table 1.** Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_{case} = 25^\circ\text{C}$	8	A
	Drain current (continuous) at $T_{case} = 100^\circ\text{C}$	5	
$I_{DM}^{(1)}$	Drain current (pulsed)	32	A
$P_{TOT}$	Total dissipation at $T_{case} = 25^\circ\text{C}$	85	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 8 \text{ A}$ ,  $di/dt = 900 \text{ A}/\mu\text{s}$ ,  $V_{DS}$  peak <  $V_{(BR)DSS}$ ,  $V_{DD} = 400 \text{ V}$
3.  $V_{DS} \leq 480 \text{ V}$

**Table 2.** Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.47	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

1. When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3.** Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	2.5	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	430	mJ

1. Pulse width limited by  $T_{jmax}$ .
2. Starting  $T_j = 25^\circ\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50 \text{ V}$ .

## 2 Electrical characteristics

( $T_{case} = 25^\circ C$  unless otherwise specified)

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 V, I_D = 1 mA$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0 V, V_{DS} = 600 V$			1	$\mu A$
		$V_{GS} = 0 V, V_{DS} = 600 V,$ $T_{case} = 125^\circ C^{(1)}$			100	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0 V, V_{GS} = \pm 25 V$			$\pm 5$	$\mu A$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 V, I_D = 4 A$		550	600	$m\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V$	-	449	-	$pF$
$C_{oss}$	Output capacitance		-	24	-	
$C_{rss}$	Reverse transfer capacitance		-	0.89	-	
$C_{oss eq.}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0$ to $480 V, V_{GS} = 0 V$	-	42	-	$pF$
$R_G$	Intrinsic gate resistance	$f = 1 MHz, I_D = 0 A$	-	6.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480 V, I_D = 8 A,$ $V_{GS} = 10 V$ (see Figure 14. Test circuit for gate charge behavior)	-	13.5	-	$nC$
$Q_{gs}$	Gate-source charge		-	3	-	
$Q_{gd}$	Gate-drain charge		-	7.7	-	

1.  $C_{oss eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300 V, I_D = 4 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	10	-	ns
$t_r$	Rise time		-	6	-	
$t_{d(off)}$	Turn-off delay time		-	25.4	-	
$t_f$	Fall time		-	9.5	-	

**Table 7. Source-drain diode**

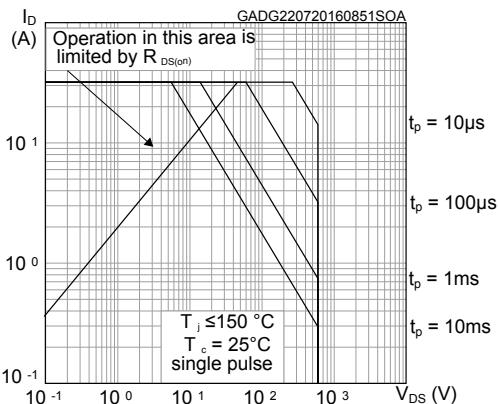
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 8 \text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ ,	-	80		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 15. Test circuit for inductive load switching and diode recovery times</a> )	-	188		nC
$I_{RRM}$	Reverse recovery current	$I_{SD} = 8 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ , (see <a href="#">Figure 15. Test circuit for inductive load switching and diode recovery times</a> )	-	4.7		A
$t_{rr}$	Reverse recovery time	$V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$	-	160		ns
$Q_{rr}$	Reverse recovery charge		-	640		nC
$I_{RRM}$	Reverse recovery current		-	8		A

1. Pulse width is limited by safe operating area.

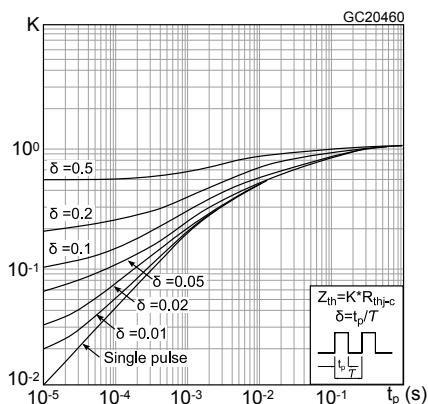
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

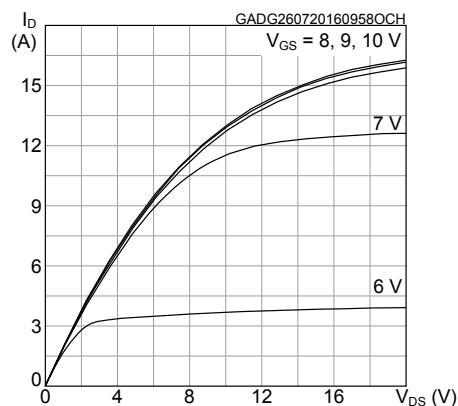
**Figure 1. Safe operating area**



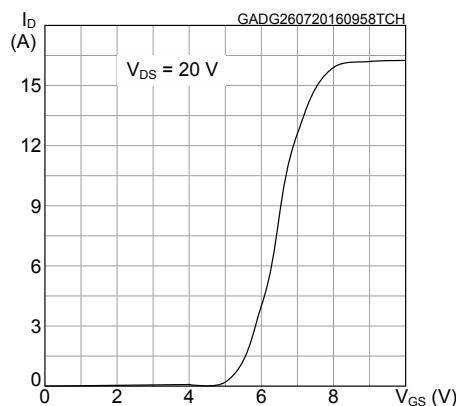
**Figure 2. Thermal impedance**



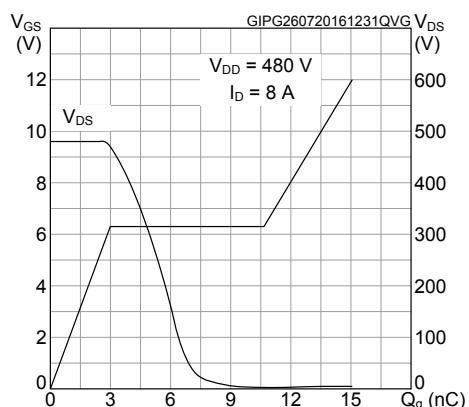
**Figure 3. Output characteristics**



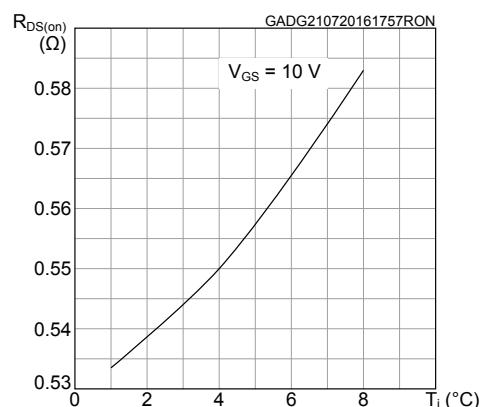
**Figure 4. Transfer characteristics**

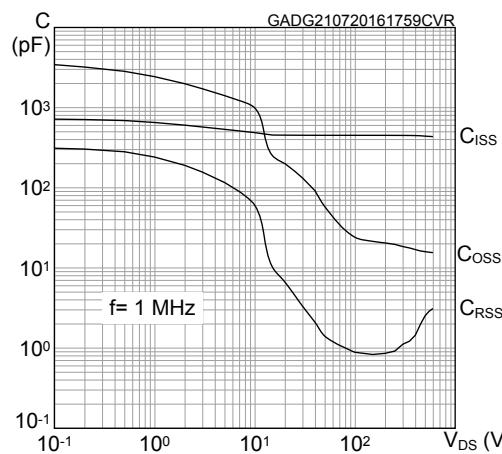
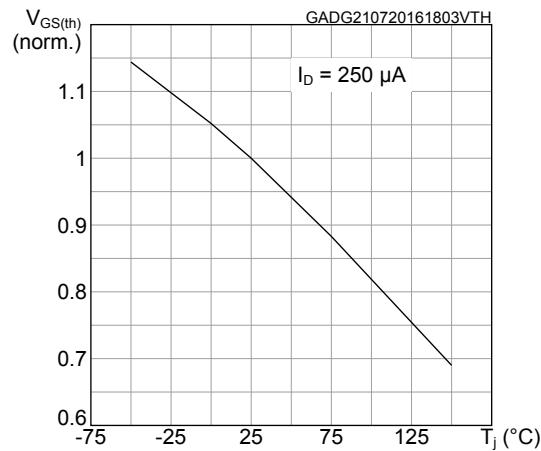
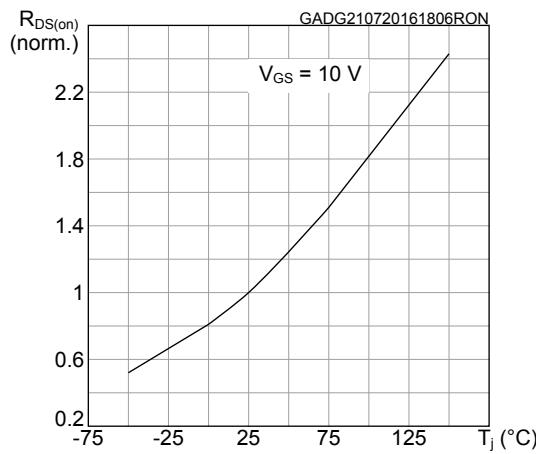
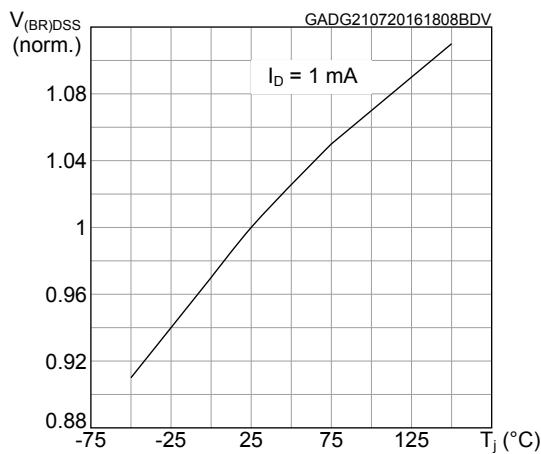
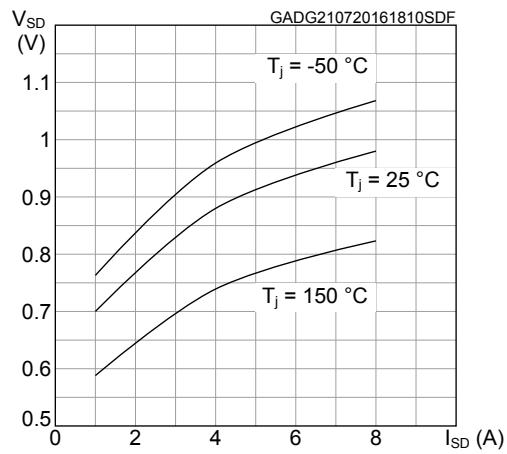
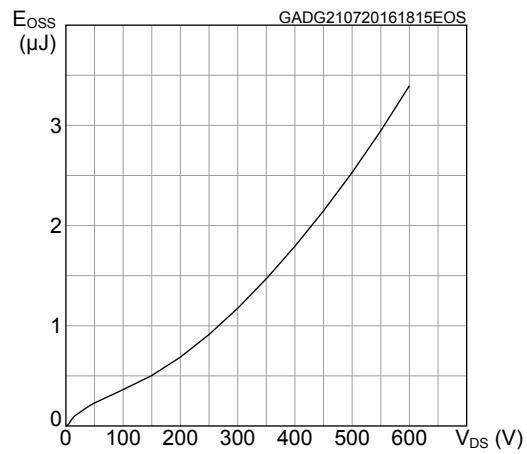


**Figure 5. Gate charge vs gate-source voltage**



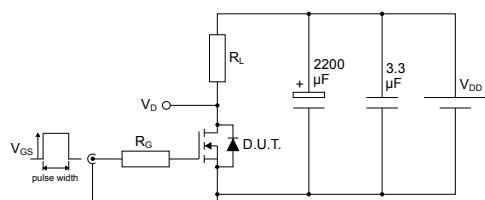
**Figure 6. Static drain-source on resistance**



**Figure 7. Capacitance variations**

**Figure 8. Normalized gate threshold voltage vs temperature**

**Figure 9. Normalized on-resistance vs temperature**

**Figure 10. Normalized V\_(BR)DSS vs temperature**

**Figure 11. Source-drain diode forward characteristics**

**Figure 12. Output capacitance stored energy**


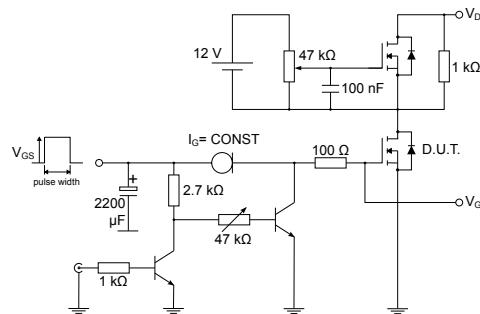
### 3 Test circuits

**Figure 13.** Test circuit for resistive load switching times



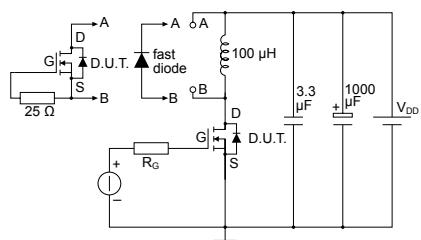
AM01468v1

**Figure 14.** Test circuit for gate charge behavior



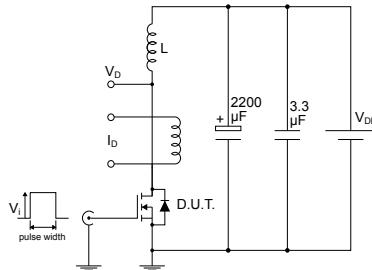
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**Figure 15.** Test circuit for inductive load switching and diode recovery times



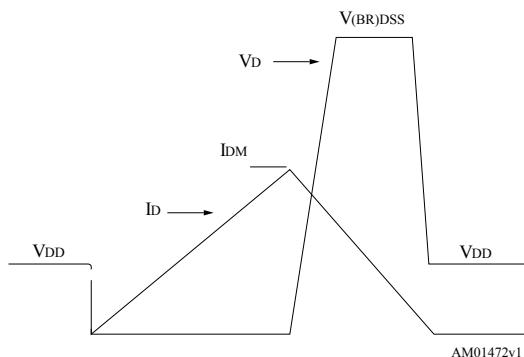
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**Figure 16.** Unclamped inductive load test circuit



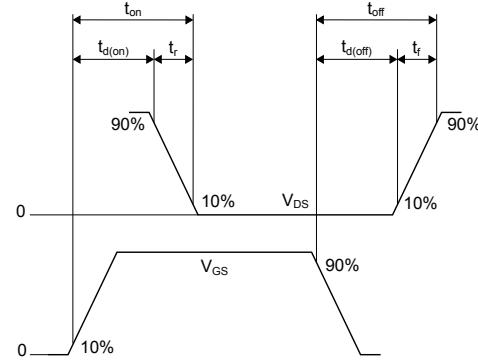
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**Figure 17.** Unclamped inductive waveform



AM01472v1

**Figure 18.** Switching time waveform



AM01473v1

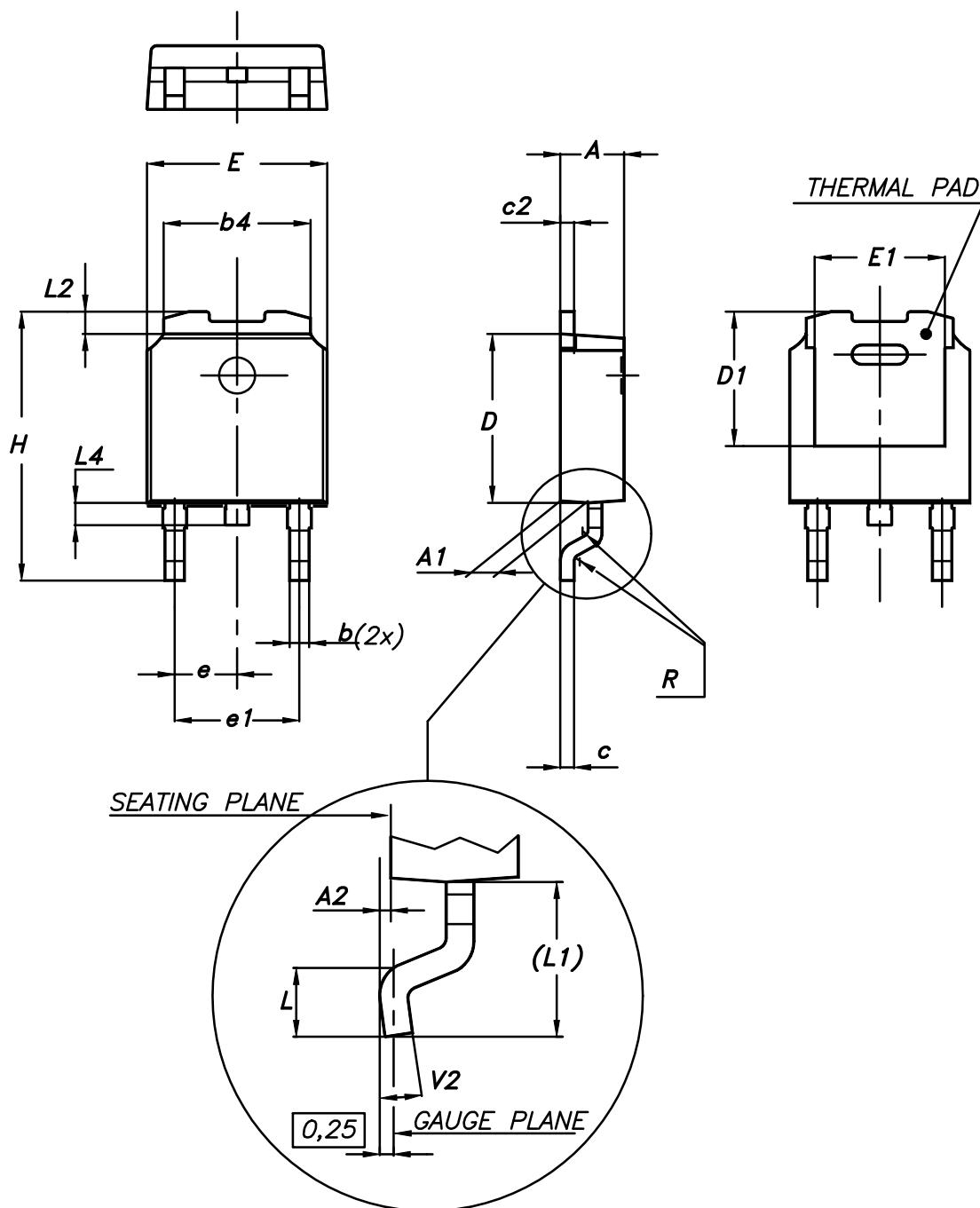
**4****Package information**

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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

#### 4.1 DPAK (TO-252) type A package information

Figure 19. DPAK (TO-252) type A package outline



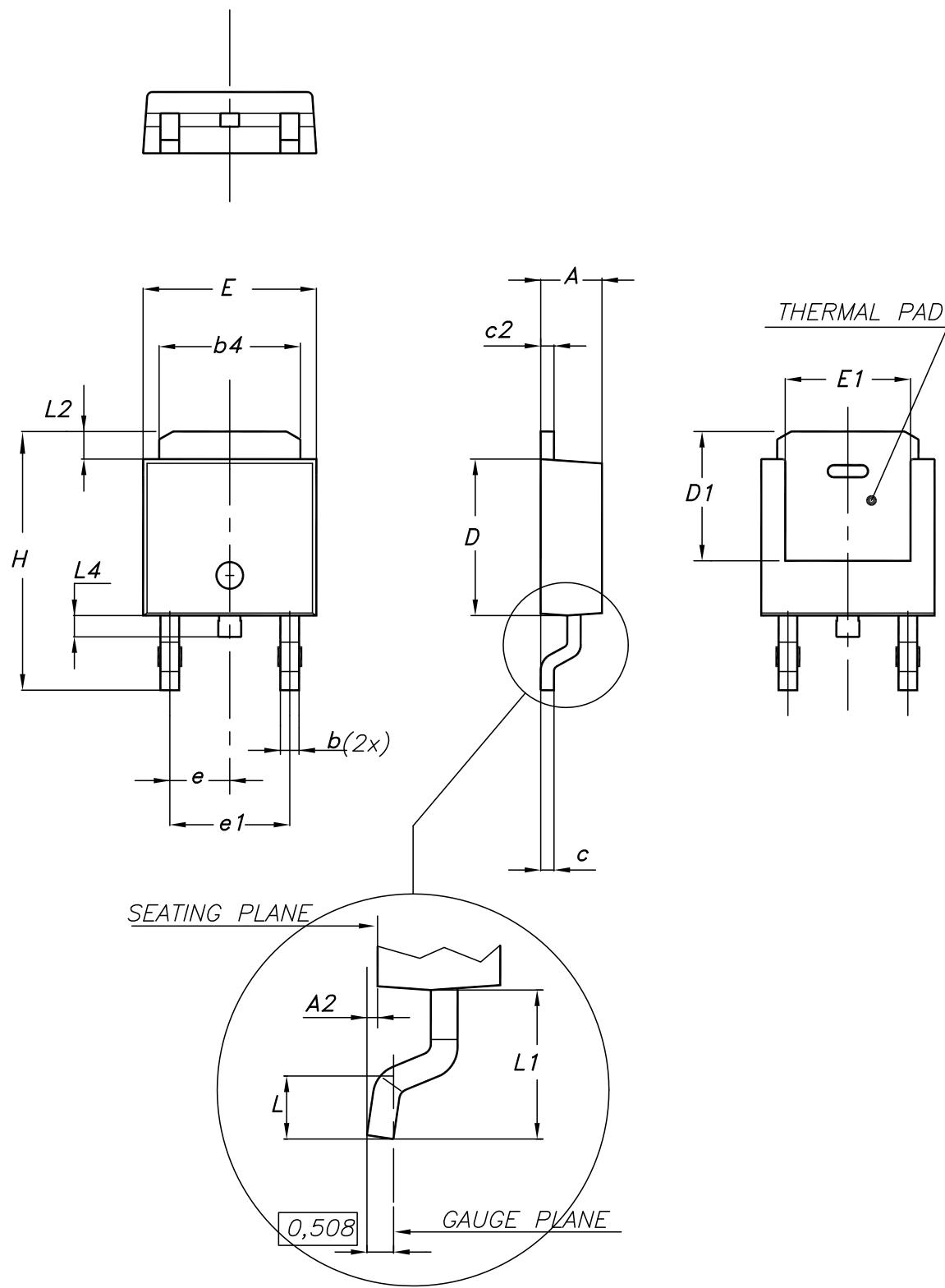
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**Table 8. DPAK (TO-252) type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

## 4.2 DPAK (TO-252) type E package information

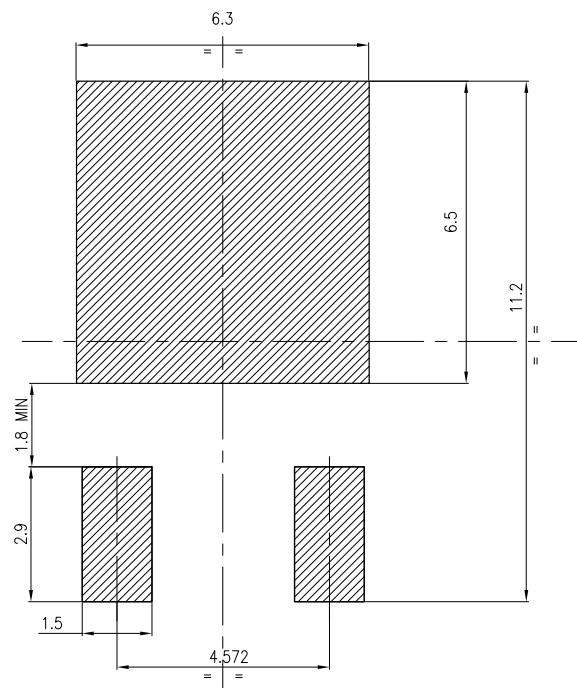
Figure 20. DPAK (TO-252) type E package outline



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**Table 9. DPAK (TO-252) type E mechanical data**

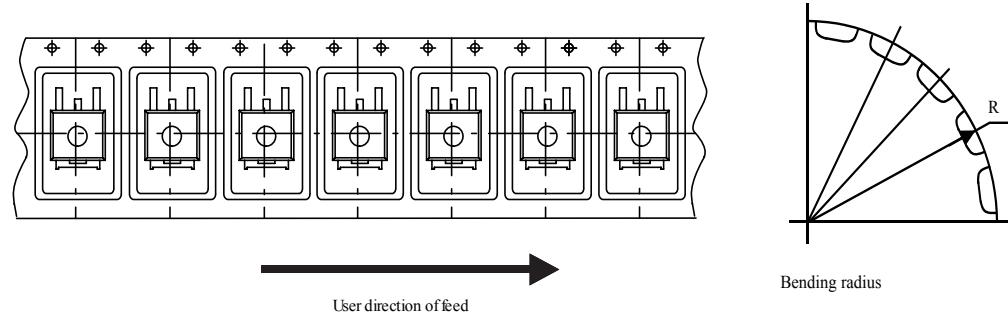
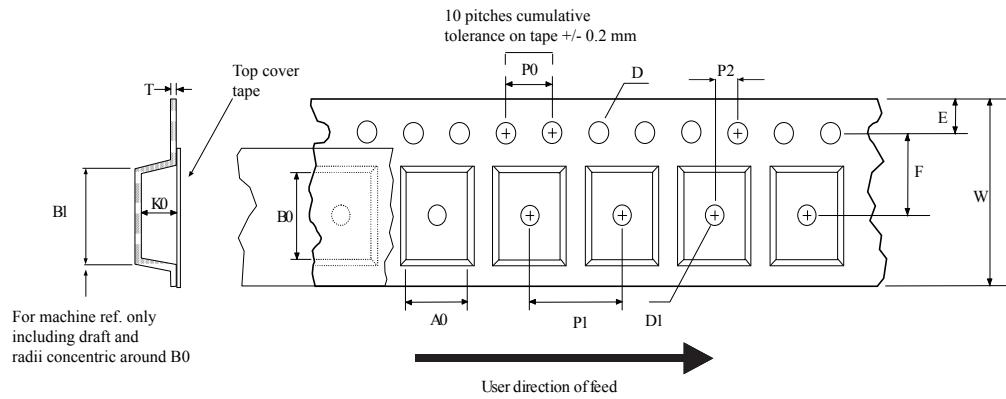
Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

**Figure 21. DPAK (TO-252) recommended footprint (dimensions are in mm)**

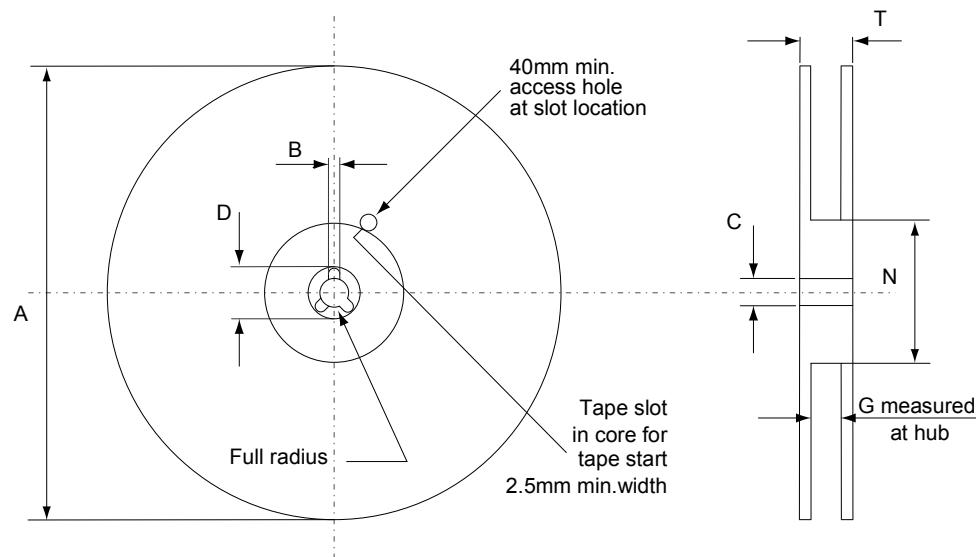
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## 4.3 DPAK (TO-252) packing information

**Figure 22. DPAK (TO-252) tape outline**



AM08852v1

**Figure 23. DPAK (TO-252) reel outline**

AM06038v1

**Table 10. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 11. Document revision history**

Date	Revision	Changes
12-May-2015	1	First release.
24-Nov-2016	2	Document status promoted from preliminary to production data. Updated title in cover page, <i>Section 1: "Electrical ratings"</i> and <i>Section 2: "Electrical characteristics"</i> . Added <i>Section 2.1: "Electrical characteristics (curves)"</i> .
07-Sep-2018	3	Removed maturity status indication from cover page. Added <a href="#">Section 4.2 DPAK (TO-252) type E package information</a> . Minor text changes

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