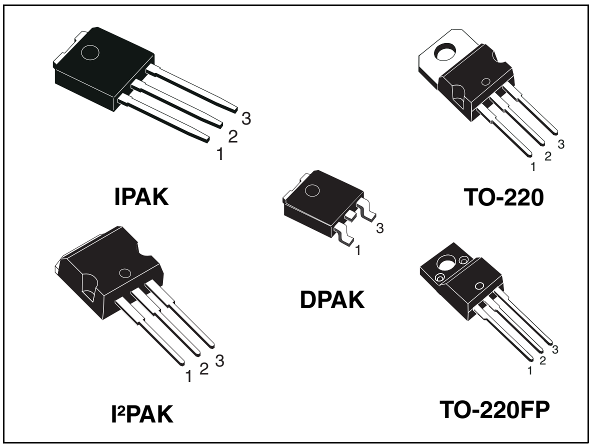
STD12N65M5, STF12N65M5, STI12N65M5 STP12N65M5, STU12N65M5

N-channel 650 V, 0.39 Ω, 8.5 A MDmesh™ V Power MOSFET DPAK, I^2PAK, TO-220FP, TO-220, IPAK

Features

Type	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D	P_{TOT}
STD12N65M5			8.5 A	70 W
STF12N65M5			8.5 A[(1)]	25 W
STI12N65M5	710 V	< 0.43 Ω	8.5 A	70 W
STP12N65M5			8.5 A	70 W
STU12N65M5			8.5 A	70 W

1. Limited only by maximum temperature allowed.



- Worldwide best $R_{DS(on)}$ * area
- Higher V_{DSS} rating and high dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

Applications

Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

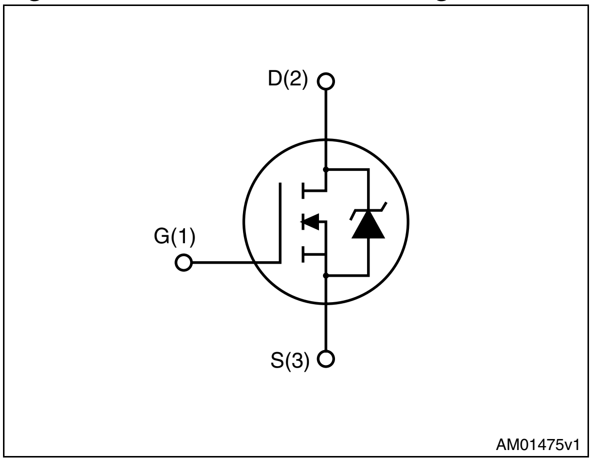


Table 1. Device summary

Order codes	Marking	Packages	Packaging
STD12N65M5		DPAK	Tape and reel
STF12N65M5		TO-220FP	Tube
STI12N65M5	12N65M5	I²PAK	Tube
STP12N65M5		TO-220	Tube
STU12N65M5		IPAK	Tube

Contents

1 Electrical ratings

Table 2. **Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220, IPAK, DPAK, I²PAK	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	650		V
V_{GS}	Gate-source voltage	25		V
I_D	Drain current (continuous) at T_C = 25 °C	8.5	8.5 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	5.4	5.4 (1)	A
I_{DM} (2)	Drain current (pulsed)	34	34 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	25	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2.5		A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	150		mJ
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; Tc = 25 °C)		2500	V
T_{stg}	Storage temperature	- 55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 8.5$ A, di/dt ≤ 400 A/µs; $V_{Peak} < V_{(BR)DSS}$, $V_{DD} = 400$ V

Table 3. **Thermal data**

Symbol	Parameter	Value					Unit
		DPAK	IPAK	I²PAK	TO-220	TO-220FP	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.79				5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max		100	62.5			°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	50					°C/W
T_l	Maximum lead temperature for soldering purpose		300				°C

1. When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 4.3 A		0.39	0.43	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	900 22 2	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0	-	64	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	21	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	2.5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 4.25 A, V_{GS} = 10 V (see *Figure 20*)	-	20 4.8 8.3	-	nC nC nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t_d (v) t_r (v) t_f (i) t_c(off)	Voltage delay time Voltage rise time Current fall time Crossing time	V_{DD} = 400 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 21* and *Figure 24*)	-	22.6 17.6 15.6 23.4	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				8.5 34	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 8.5 A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 8.5 A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 24*)		230 2.2 19		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 8.5 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 24*)		280 2.7 19		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 and I²PAK

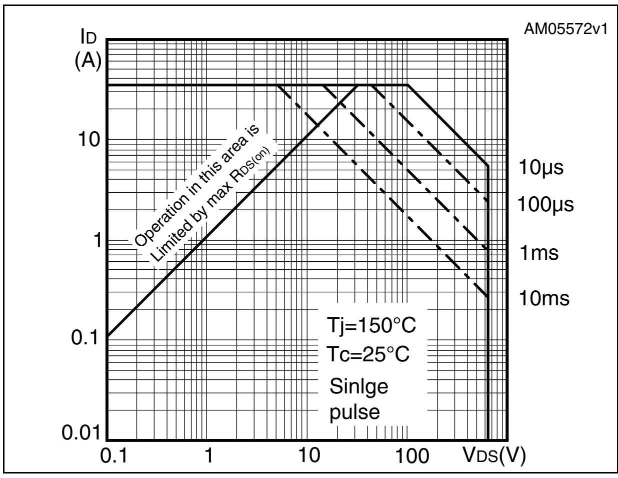


Figure 3. Thermal impedance for TO-220 and I²PAK

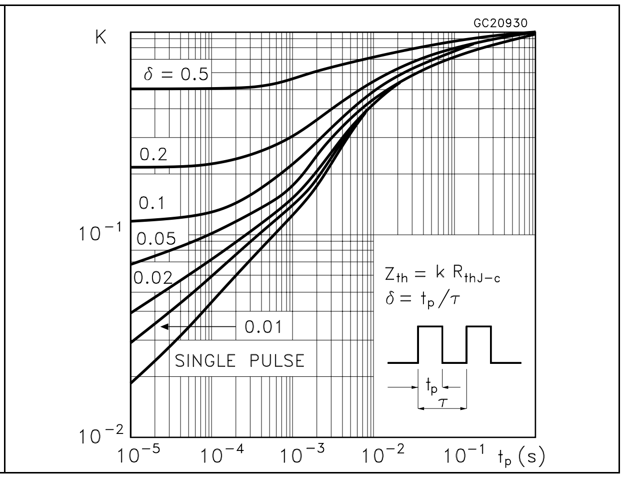


Figure 4. Safe operating area for TO-220FP

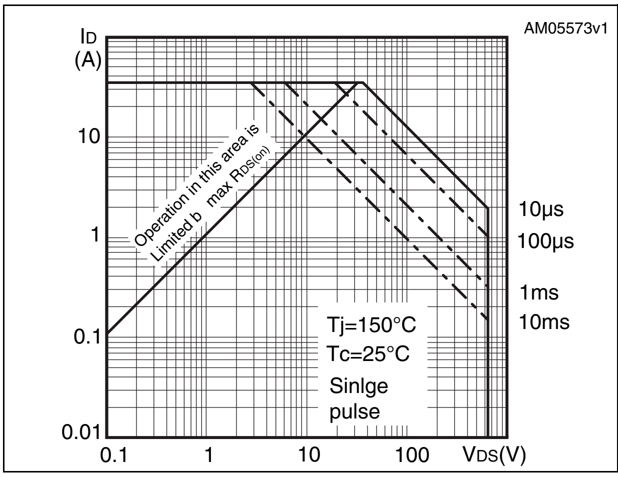


Figure 5. Thermal impedance for TO-220FP

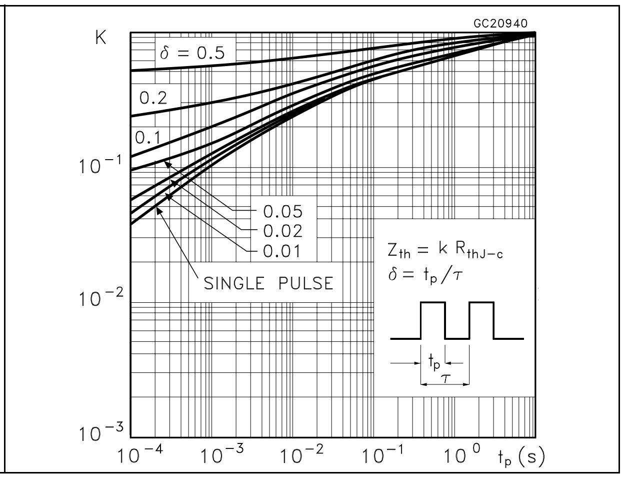


Figure 6. Safe operating area for DPAK, IPAK

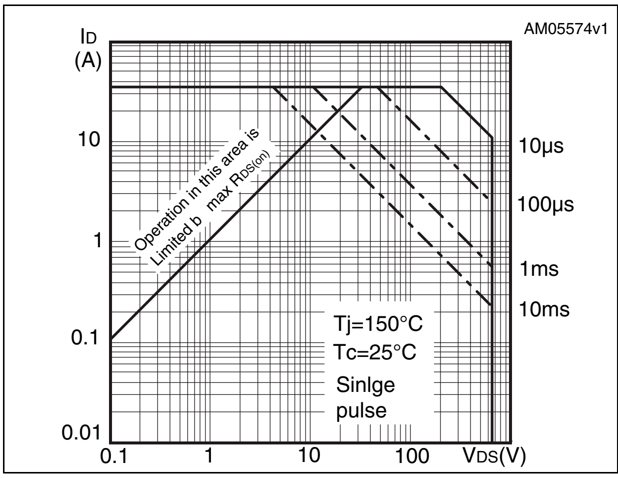


Figure 7. Thermal impedance for DPAK, IPAK

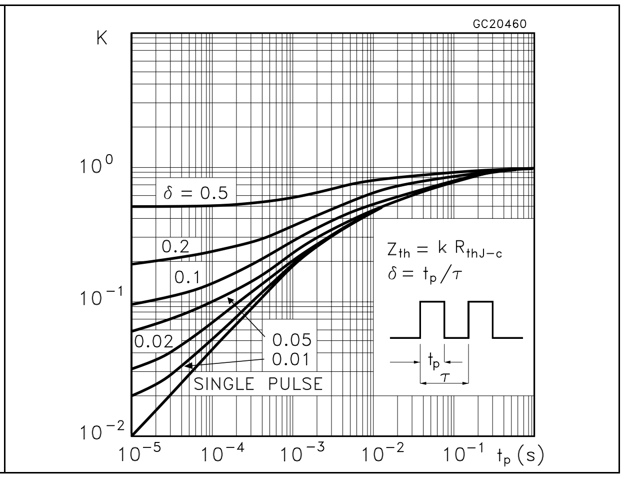


Figure 8. Output characteristics

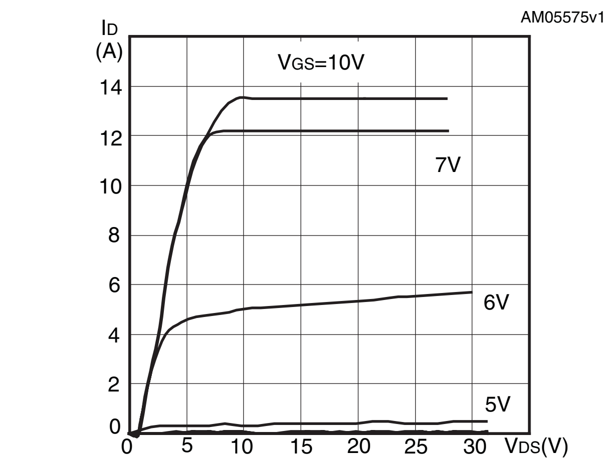


Figure 9. Transfer characteristics

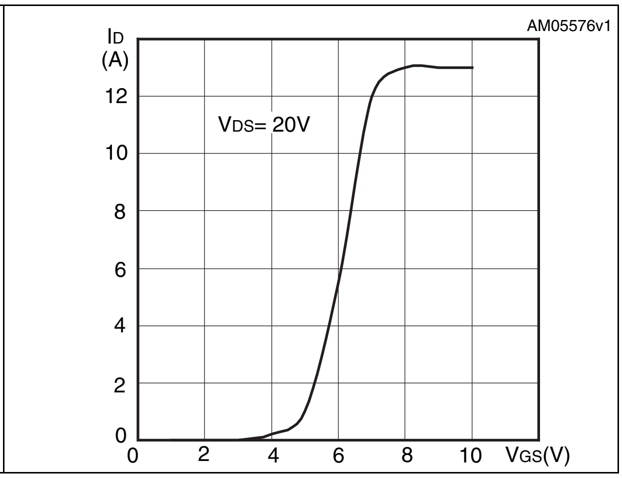


Figure 10. Gate charge vs gate-source voltage

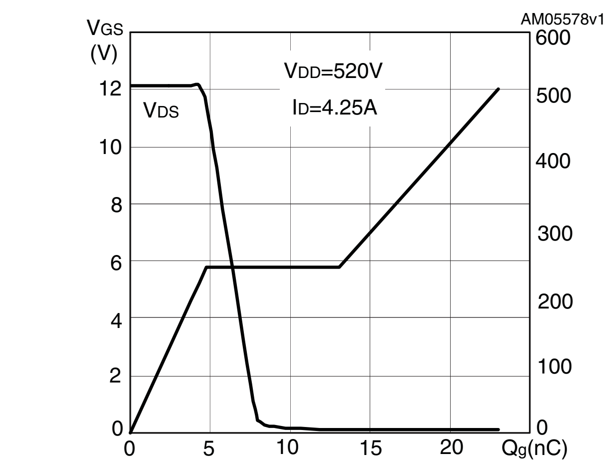


Figure 11. Static drain-source on resistance

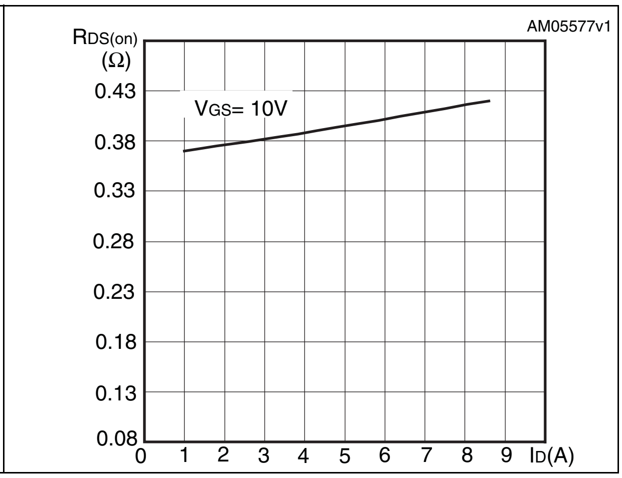


Figure 12. Capacitance variations

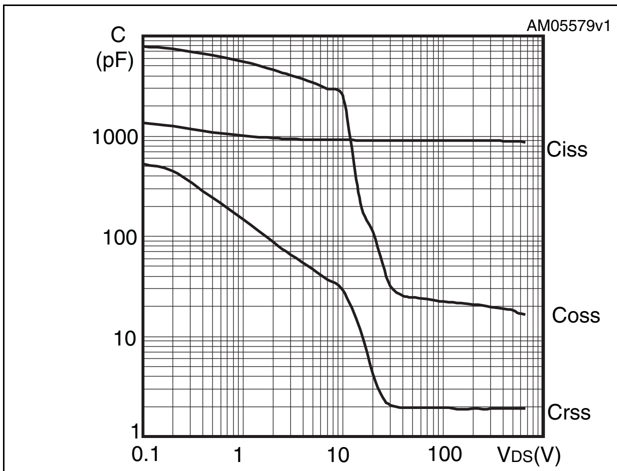


Figure 13. Output capacitance stored energy

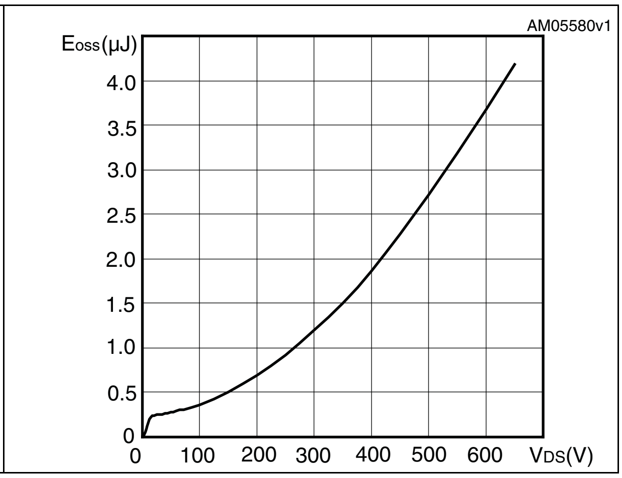


Figure 14. Normalized gate threshold voltage vs temperature

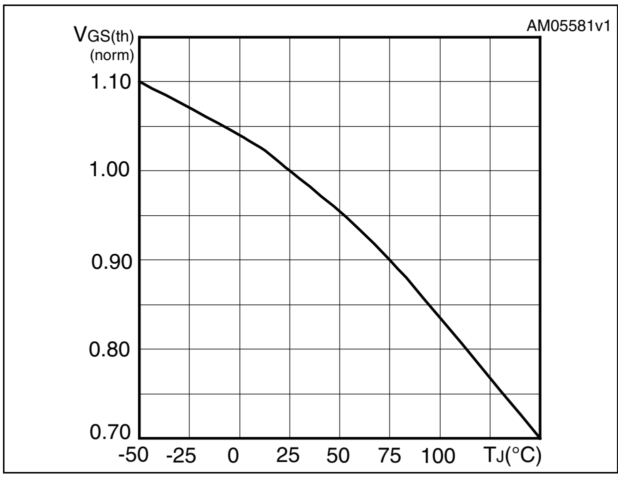


Figure 15. Normalized on resistance vs temperature

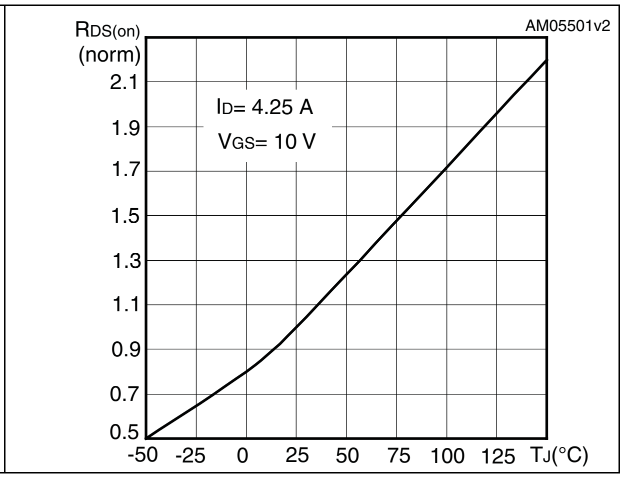


Figure 16. Source-drain diode forward characteristics

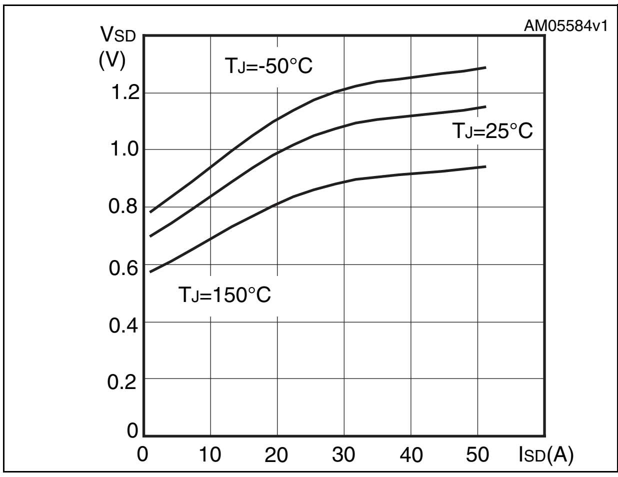


Figure 17. Normalized B_{VDSS} @ 1 mA vs temperature

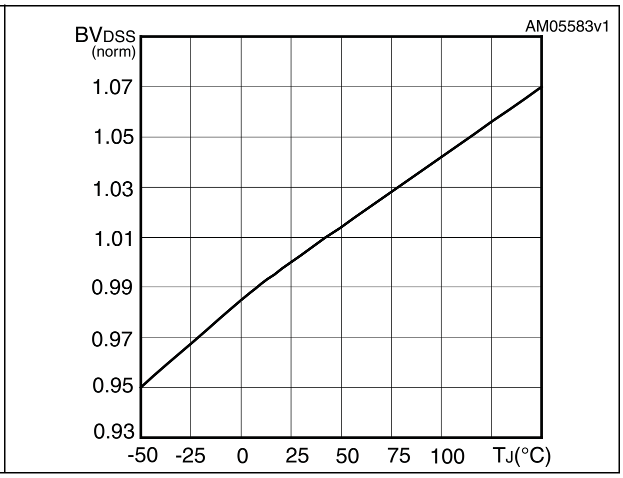
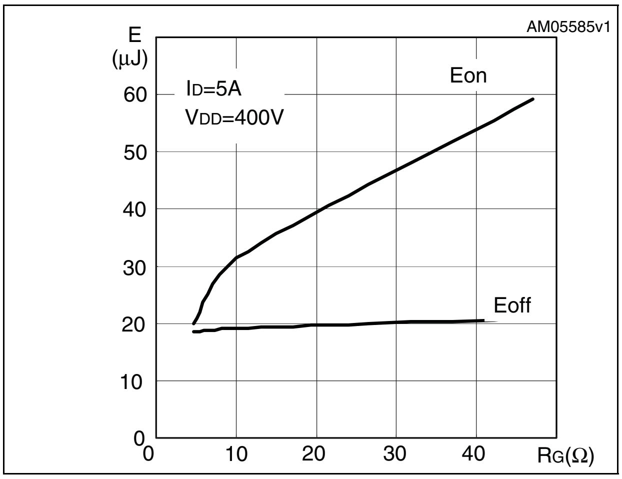


Figure 18. Switching losses vs gate resistance (1)



1. Eon including reverse recovery of a SiC diode

3 Test circuits

Figure 19. Switching times test circuit for resistive load

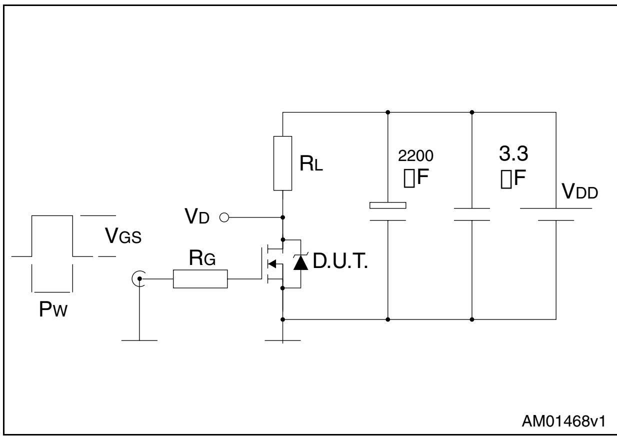


Figure 20. Gate charge test circuit

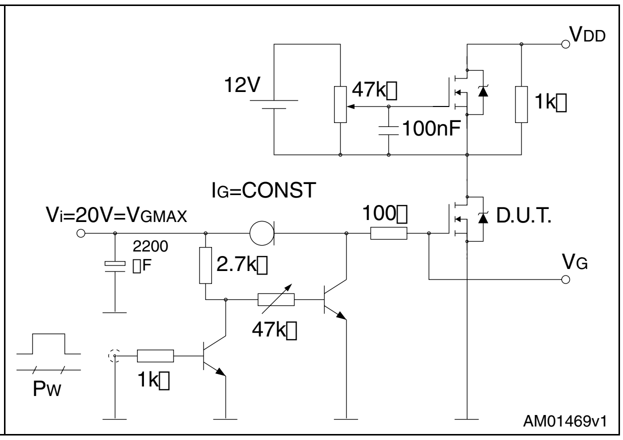


Figure 21. Test circuit for inductive load switching and diode recovery times

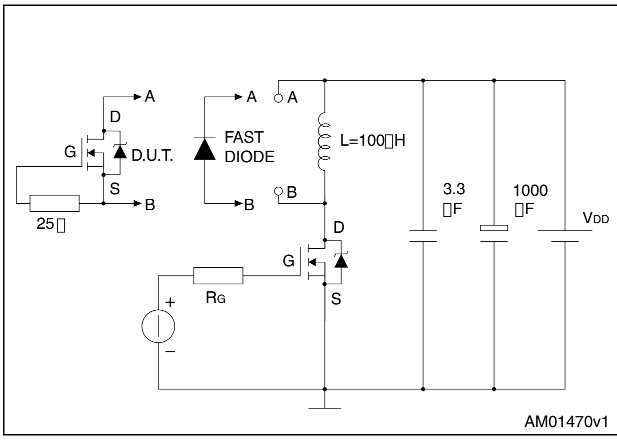


Figure 22. Unclamped inductive load test circuit

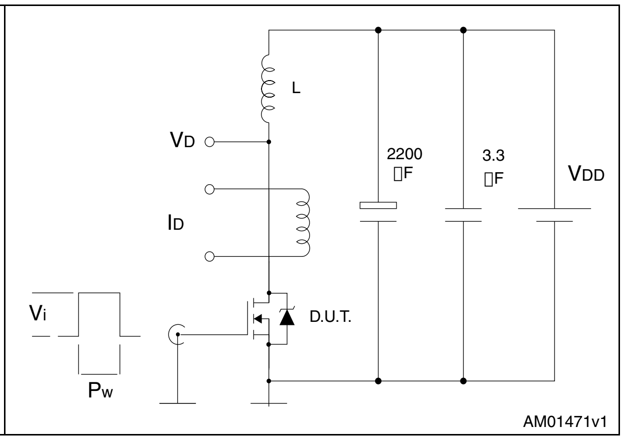


Figure 23. Unclamped inductive waveform

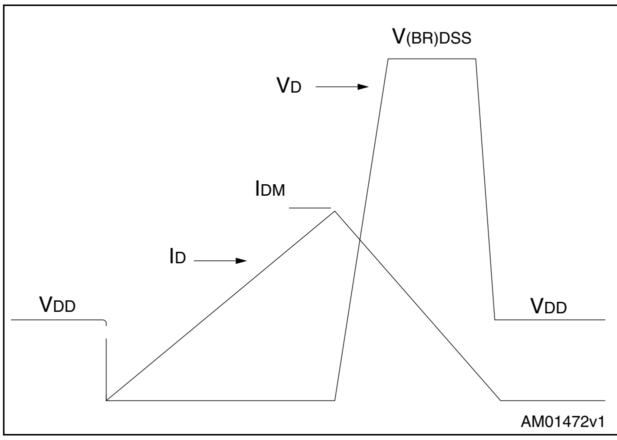
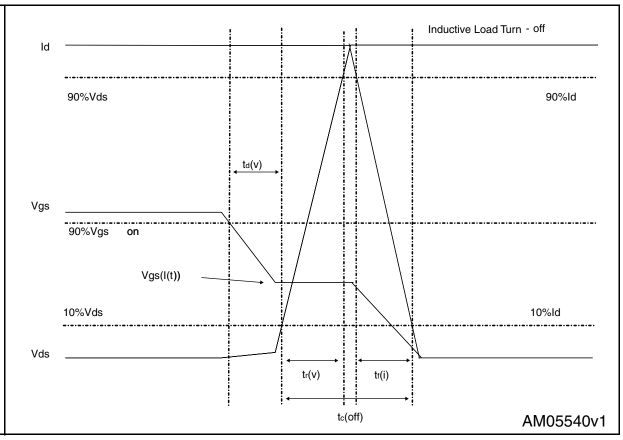


Figure 24. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) drawing

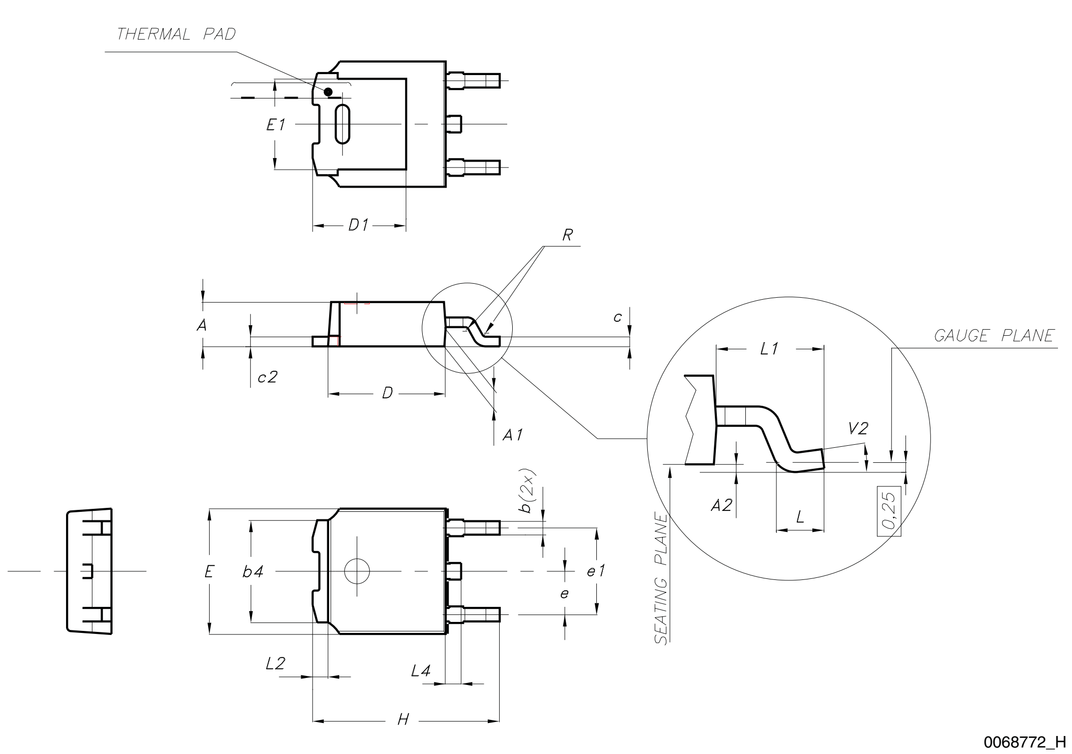
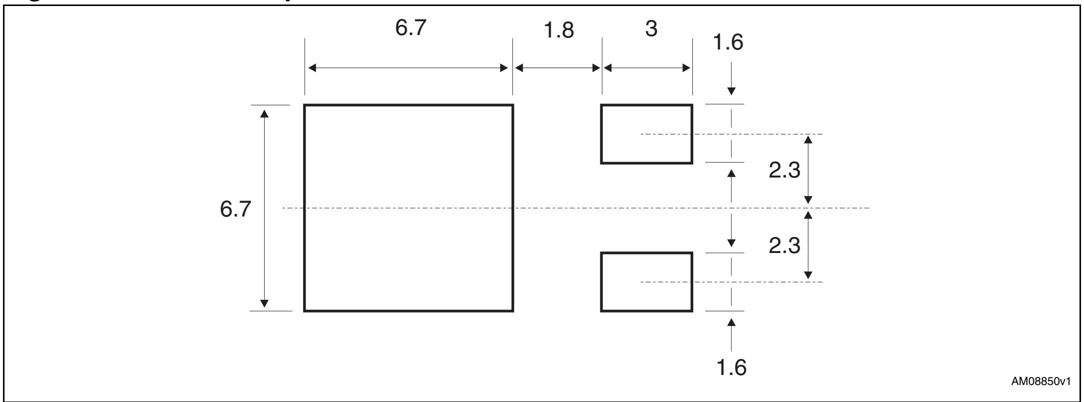


Figure 26. DPAK footprint[a]



a. All dimension are in millimeters

Table 9. IPAK (TO-251) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.3	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10 °	

Figure 27. IPAK (TO-251) drawing

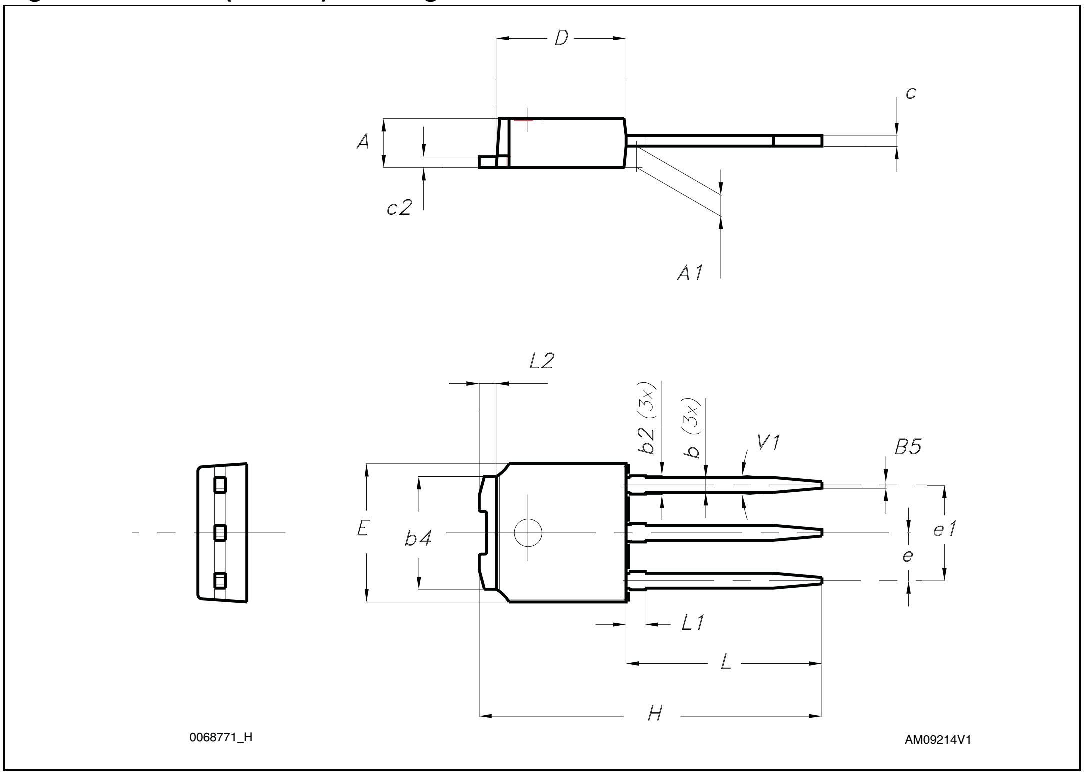


Table 10. I^2PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 28. I²PAK (TO-262) drawing

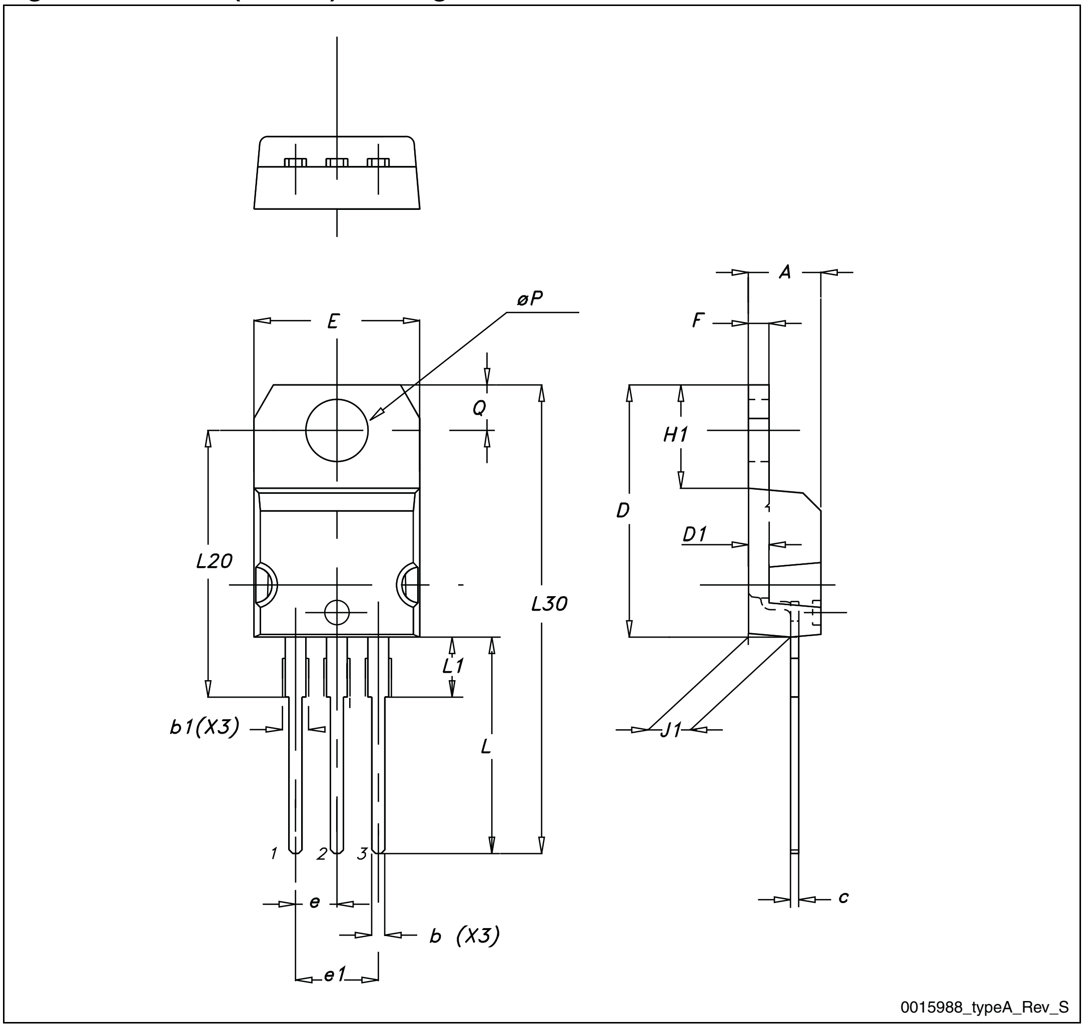


Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 29. TO-220 type A drawing

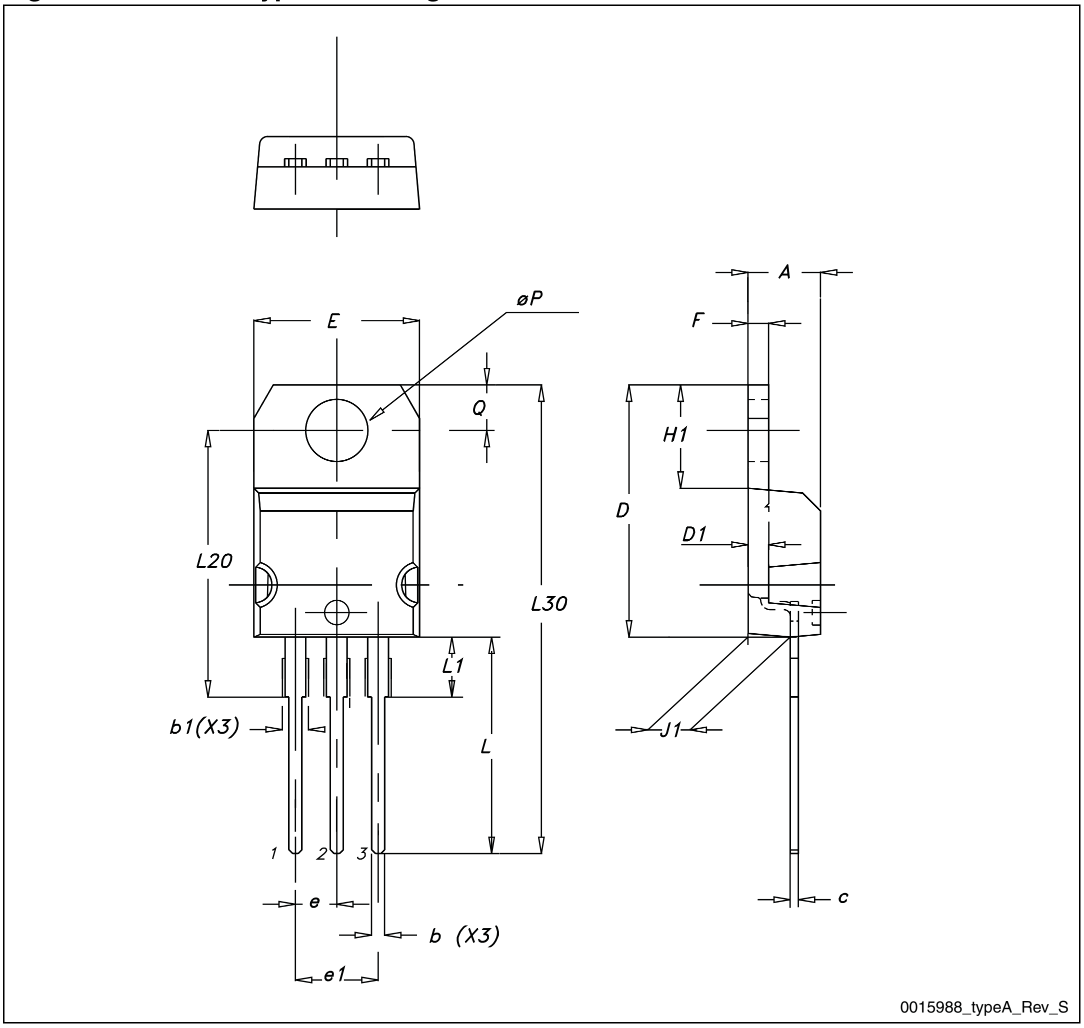
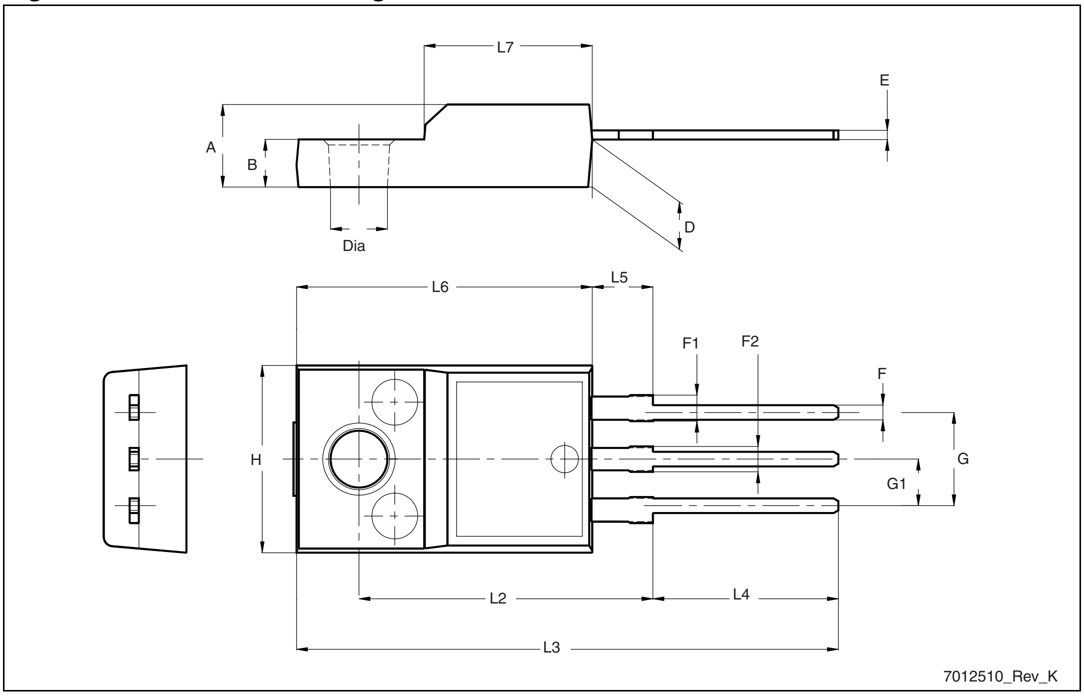


Table 12. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 30. TO-220FP drawing



5 Packaging mechanical data

Table 13. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 31. Tape

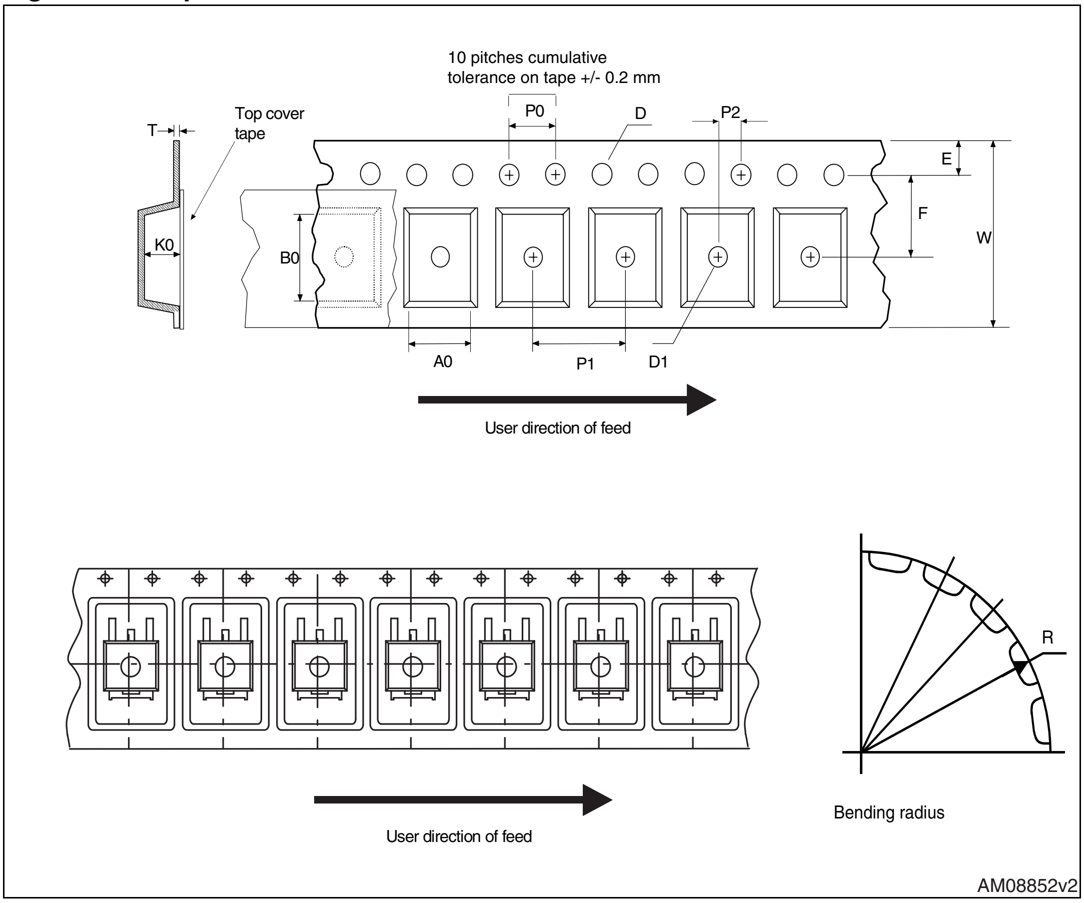
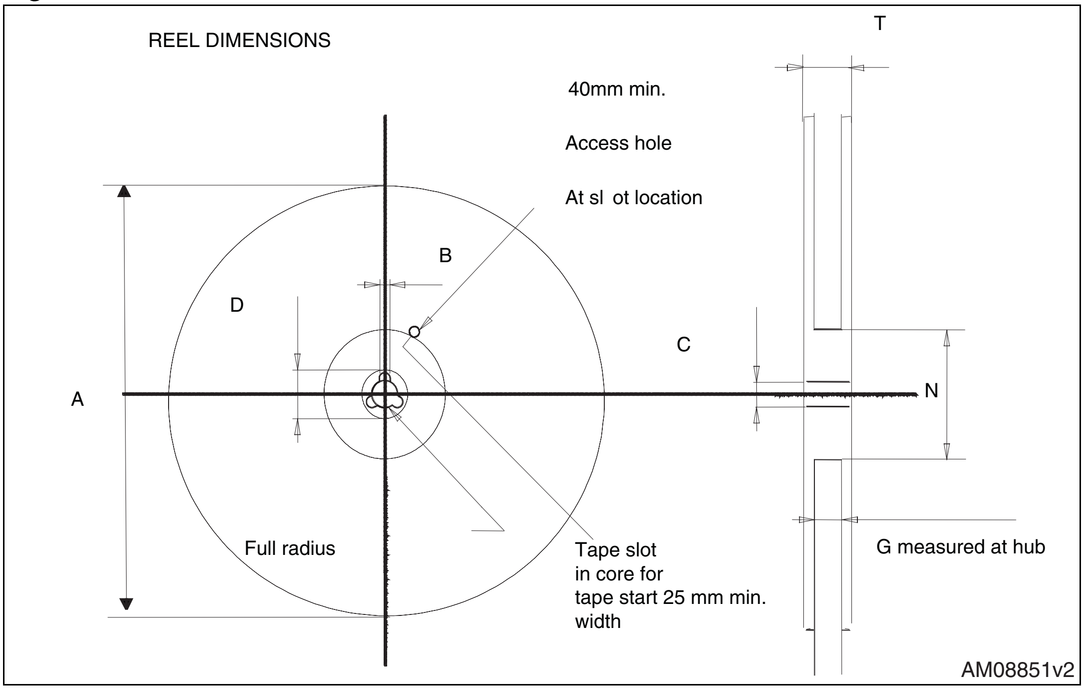


Figure 32. Reel



6 Revision history

Table 14. Document revision history

Date	Revision	Changes
24-Feb-2009	1	First release
27-Feb-2009	2	Corrected package information on first page
21-Jan-2010	3	Document status promoted from preliminary data to datasheet
29-Jun-2010	4	– *Figure 15: Normalized on resistance vs temperature* has been updated – V_{GS} vale in *Table 4* has been corrected
22-Jun-2011	5	Updated *Figure 18* and *Figure 20*. Updated gate charge in *Table 5* and switching time in *Table 6*.