SN74LVC2G157 单路 2 线至 1 线数据选择器多路复用器

1 特性

- 采用德州仪器 (TI) 的 NanoFree™封装
- 支持 5V V_{CC} 运行
- 输入电压高达 5.5V
- 电压为 3.3V 时，t_{pd} 最大值为 6ns
- 低功耗，I_{CC} 最大值为 10μA
- 电压为 3.3V 时，输出驱动为 ±24mA
- 典型 V_{OLP}（输出接地反弹）小于 0.8V（V_{CC} = 3.3V、T_A = 25°C 的条件下）
- 典型 V_{OHV}（输出 V_{OH} 下冲）大于 2V（V_{CC} = 3.3V、T_A = 25°C 的条件下）
- I_{off} 支持带电插入、局部关断模式和后驱动保护
- 可用作下行转换器，将最高 5.5V 的输入电压下行转换至 V_{CC} 电平
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范
- ESD 保护性能超出 JESD 22 标准
  - 2000V 人体放电模型 (A114-A)
  - 1000V 充电器件模型 (C101)

2 应用

- 条形码扫描仪
- 线缆解决方案
- 电子书
- 嵌入式 PC
- 现场变送器：温度或湿度传感器
- 指纹识别
- HVAC：暖通空调
- 网络附加存储 (NAS)
- 服务器主板和 PSU
- 软件定义无线电 (SDR)
- 电视：高清 (HDTV)、LCD 和数字电视
- 视频通信系统
- 无线数据存取卡、耳机、键盘、鼠标和局域网 (LAN) 卡

3 说明

这款单通道 2 线至 1 线数据选择器多路复用器采用 1.65V 至 5.5V V_{CC} 电压供电。

SN74LVC2G157 器件 具有 常见频闪 ($\overline{G}$) 输入。当选通脉冲处于高电平时，Y 处于低电平，而 $\overline{Y}$ 处于高电平。当选通脉冲为低电平时，从两个源之一选择一位并将其发送到输出。该器件提供真实和互补的数据。

NanoFree™ 封装技术是 IC 封装概念的一项重大突破，它将硅晶片用作封装。

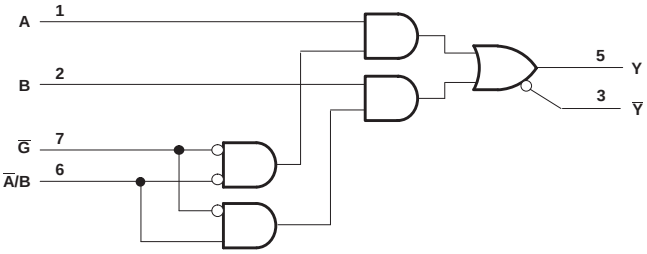
该器件完全 适用于 I_{off} 为了部分断电的应用。I_{off} 电路会禁用输出，从而在器件掉电时防止电流回流损坏器件。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN74LVC2G157DCT	SSOP (8)	2.95mm × 2.80mm
SN74LVC2G157DCU	超薄小外形尺寸封装 (VSSOP)(8)	2.30mm x 2.00mm
SN74LVC2G157YZP	DSBGA (8)	1.91mm × 0.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

逻辑图（正逻辑）



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision M (June 2015) to Revision N **Page**

- Changed YZP package pinout drawing to match mechanical data drawing; and, pin functions description for clarity ... 3
- Added additional thermal metrics for all packages. ... 5
- Added detailed feature description sections for Standard CMOS Inputs, Balanced High-Drive CMOS Push-Pull Outputs, and Negative Clamping Diodes. ... 8
- Added improved Design Requirements and Detailed Design Procedure ... 10
- Changed verbiage to better reflect recommendations for this specific device rather than logic devices in general. ... 12
- Added layout example for the YZP package. ... 12

Changes from Revision L (January 2014) to Revision M **Page**

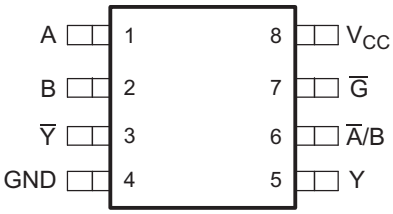
- Added *ESD Ratings* table. ... 4
- Added *Thermal Information table.* ... 5
- Added *Typical Characteristics* ... 6
- 已添加 *机械、封装和可订购信息* 部分。 ... 14

Changes from Revision K (January 2007) to Revision L **Page**

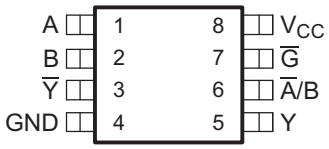
- 将文档更新为新的 TI 数据表格式。 ... 1
- 删除了*订购信息* 表 ... 1
- 已更新*特性* ... 1
- 已添加 *器件信息* 表 ... 1

5 Pin Configuration and Functions

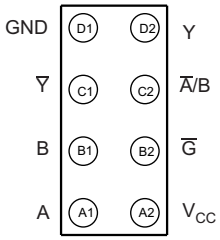
DCT Package
8-Pin SSOP
Top View



DCU Package
8-Pin VSSOP
Top View



YZP Package
8-Pin DSBGA
Bottom View



Drawing are not to scale. See mechanical drawings for dimensions

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SSOP, VSSOP	DSBGA		
A	1	A1	Input	Data Input A
$\overline{A}$/B	6	C2	Input	Input Selector
B	2	B1	Input	Data Input B
$\overline{G}$	7	B2	Input	Common Strobe Input
GND	4	D1	—	Ground
V_{CC}	8	A2	—	Positive Supply
Y	5	D2	Output	Output
$\overline{Y}$	3	C1	Output	Inverted Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high or low state(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C
T_J	Junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1).

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Recommended Operating Conditions (continued)

See (1).

			MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC2G157			UNIT
		DCT (SSOP)	DCU (VSSOP)	YZP (DSBGA)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192.0	289.9	99.9	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	70.2	86.9	1.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	105.2	208.5	27.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.7	23.1	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	103.6	206.5	27.8	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		1.65 V to 5.5 V	V_{CC} – 0.1			V
		I_{OH} = –4 mA		1.65 V	1.2			
		I_{OH} = –8 mA		2.3 V	1.9			
		I_{OH} = –16 mA		3 V	2.4			
		I_{OH} = –24 mA			2.3			
		I_{OH} = –32 mA		4.5 V	3.8			
V_{OL}		I_{OL} = 100 µA		1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA		1.65 V			0.45	
		I_{OL} = 8 mA		2.3 V			0.3	
		I_{OL} = 16 mA		3 V			0.4	
		I_{OL} = 24 mA					0.55	
		I_{OL} = 32 mA		4.5 V			0.55	
I_I	A, B, or control inputs	V_I = 5.5 V or GND		0 to 5.5 V			±5	µA
I_{off}		V_I or V_O = 5.5 V		0			±10	µA
I_{CC}		V_I = 5.5 V or GND,	I_O = 0	1.65 V to 5.5 V			10	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 5.5 V			500	µA
C_i		V_I = V_{CC} or GND		3.3 V		5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y or $\overline{Y}$	4.4	14	2.1	8	2	6	1.4	4	ns
	$\overline{A}$/B		4.9	16	2.5	9	2.1	6	1.6	4	
	$\overline{G}$		4.2	14	2	8	1.6	6	1.3	4	

6.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	35	35	37	40	pF

6.8 Typical Characteristics

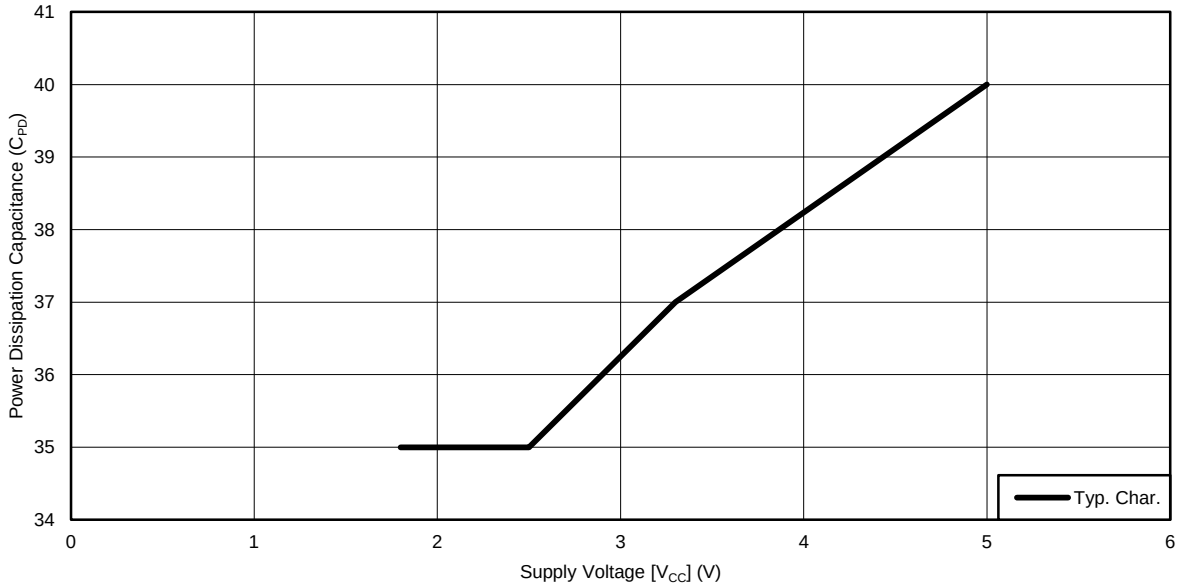
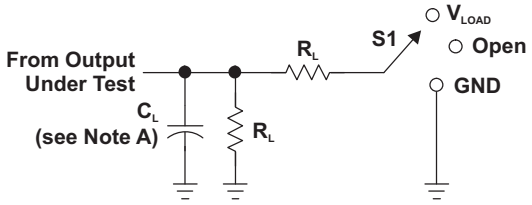


Figure 1. Voltage vs Capacitance

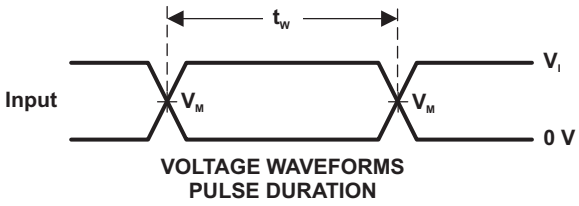
7 Parameter Measurement Information



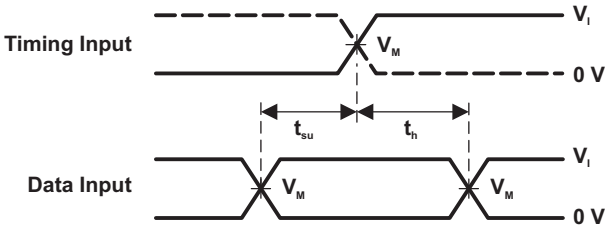
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

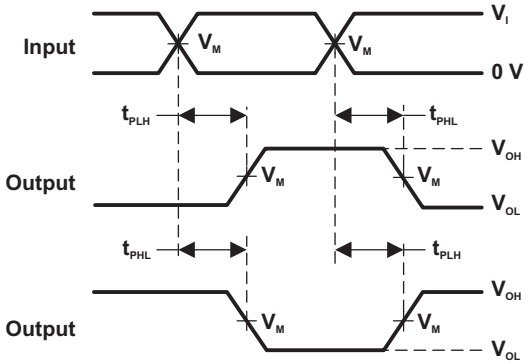
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



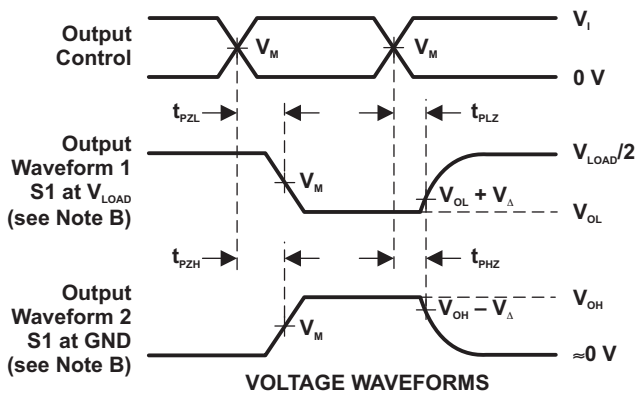
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

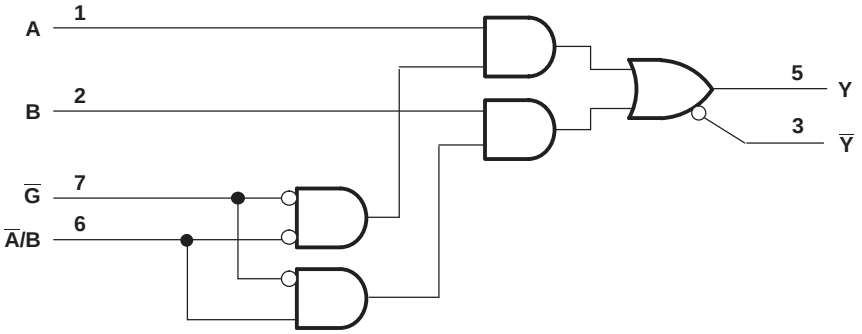
8.1 Overview

This single 2-line to 1-line data selector multiplexer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G157 device features a common strobe ($\overline{G}$) input. When the strobe is high, Y is low and $\overline{Y}$ is high. When the strobe is low, a single bit is selected from one of two sources and is routed to the outputs. The device provides true and complementary data.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



8.3 Feature Description

The SN74LVC2G157 device has a wide operating V_{CC} range of 1.65 V to 5.5 V, which allows it to be used in a broad range of systems. The 5.5 V I/Os allow down translation and also allow voltages at the inputs when V_{CC} = 0.

8.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* . The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics* , using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

8.3.3 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in Figure 3.

Feature Description (continued)

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

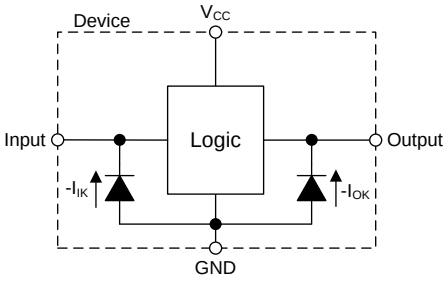


Figure 3. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 1 lists the functional modes for SN74LVC2G157.

Table 1. Function Table

INPUTS				OUTPUTS	
$\overline{G}$	$\overline{A}$/B	A	B	Y	$\overline{Y}$
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC2G157 allows a single controller input to receive data from two different digital signal sources. In this application, a digital temperature sensor's output and a digital photo sensor's output are multiplexed. Both of these sensors have a relatively slow read rate, typically less than one read per second.

9.2 Typical Application

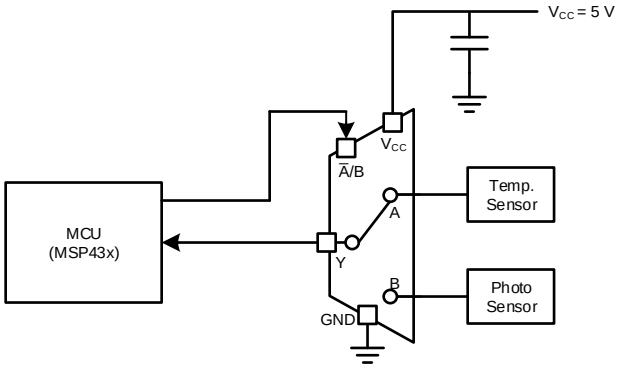


Figure 4. Multiplexer Controlled by Processor

9.2.1 Design Requirements

- 5-V Operation
- Selectable input from two digital signal sources
  - Select LOW: Temperature Sensor, 1 kbps 5-V signal
  - Select HIGH: Photo Sensor, 1 kbps 5-V signal
- 15 pF, low leakage CMOS load

9.2.1.1 Power

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions* . The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* .

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC2G157 plus the maximum supply current, I_{CC}, listed in *Electrical Characteristics* . The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in *Absolute Maximum Ratings*.

The SN74LVC2G157 can drive a load with a total capacitance less than or equal to 50 pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70 pF.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and C_{pd} Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

Typical Application (continued)

CAUTION

The maximum junction temperature, T_J(max) listed in

Absolute Maximum Ratings, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*

. These limits are provided to prevent damage to the device.

9.2.1.2 Inputs

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74LVC2G157, as specified in *Electrical Characteristics* , and the desired input transition rate. A 10 kΩ resistor value is often used due to these factors.

The SN74LVC2G157 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the *Recommended Operating Conditions* .

Refer to *Feature Description*for additional information regarding the inputs for this device.

9.2.1.3 Outputs

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics* . Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics* .

Unused outputs can be left floating.

Refer to *Feature Description* for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor, typically 0.1 µF, from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in Figure 7.
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC2G157 to the receiving device.
3. Ensure the resistive load at the output is larger than (V_{CC} / 25 mA) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*

Typical Application (continued)

9.2.3 Application Curve

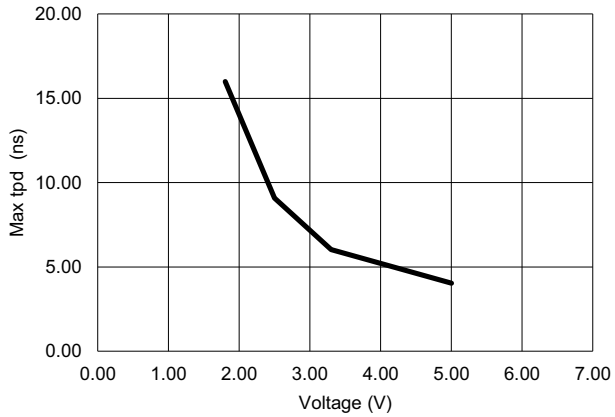


Figure 5. Max propagation delay vs voltage for the LVC logic family

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* . Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in Figure 7.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

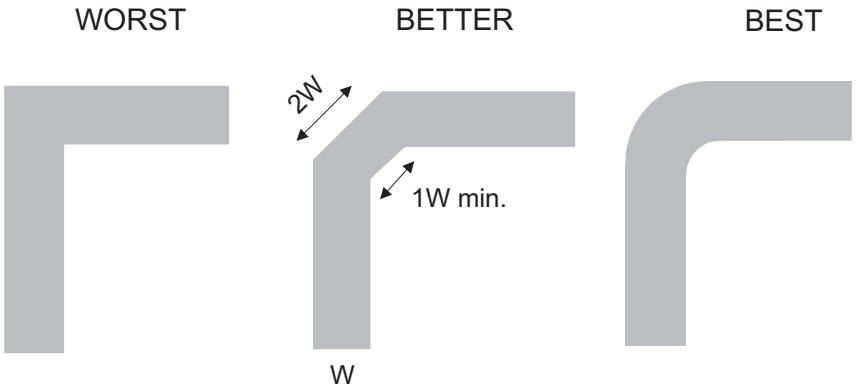


Figure 6. Trace Example

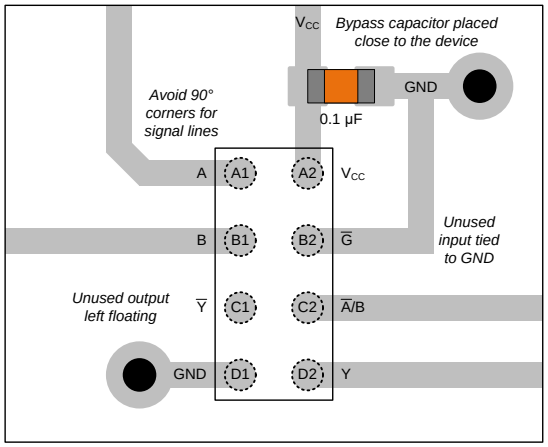


Figure 7. Example layout for SN74LVC2G157

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《CMOS 输入缓慢变化或悬空的影响》*，SCBA004
- *选择合适的德州仪器 (TI) 信号开关*，SZZA030

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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12.4 静电放电警告

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12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC2G157DCTRE4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C57 (R, Z)	Samples
74LVC2G157DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C57R	Samples
74LVC2G157DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C57R	Samples
SN74LVC2G157DCT3	ACTIVE	SM8	DCT	8	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 85	C57 Z	Samples
SN74LVC2G157DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C57 (R, Z)	Samples
SN74LVC2G157DCTRG4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C57 (R, Z)	Samples
SN74LVC2G157DCU3	ACTIVE	VSSOP	DCU	8	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 85	57 CZ	Samples
SN74LVC2G157DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(C57J, C57Q, C57R)	Samples
SN74LVC2G157DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(C57J, C57Q, C57R)	Samples
SN74LVC2G157YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(C37, C3N)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

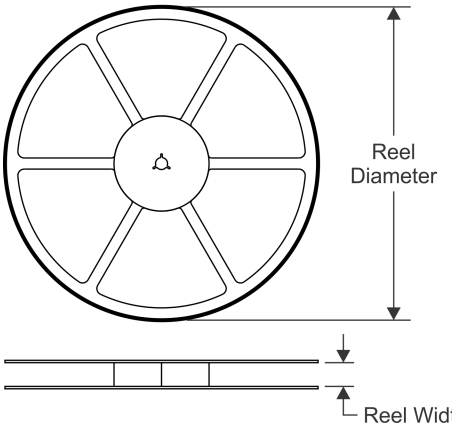
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

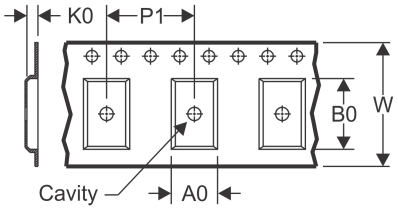
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

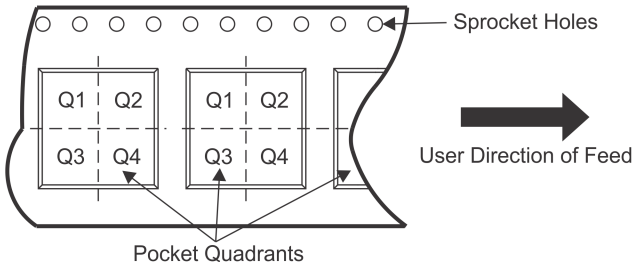


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

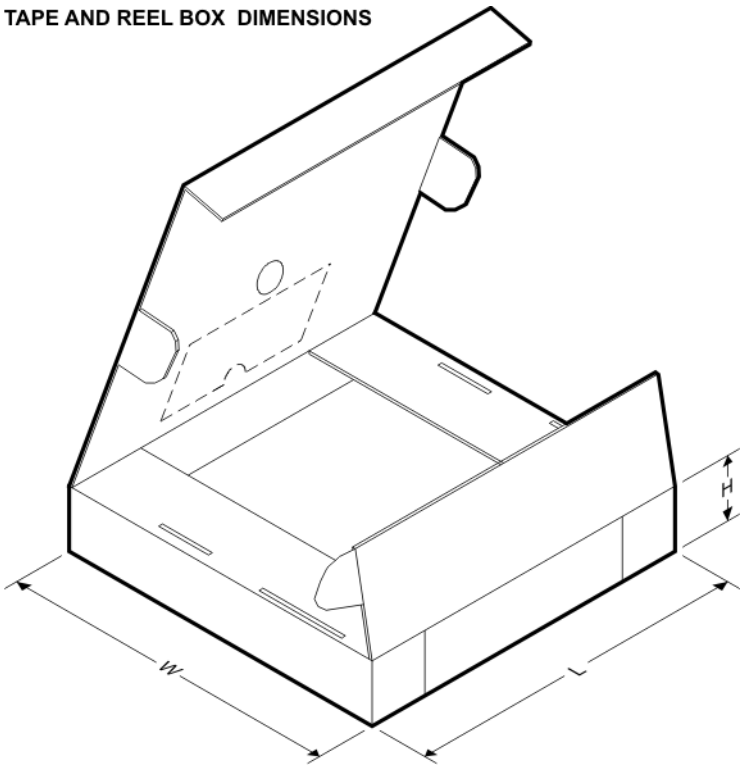
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC2G157DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
74LVC2G157DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G157DCT3	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G157DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G157DCTR	SM8	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
SN74LVC2G157DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G157DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G157DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G157DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G157DCUT	VSSOP	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G157YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

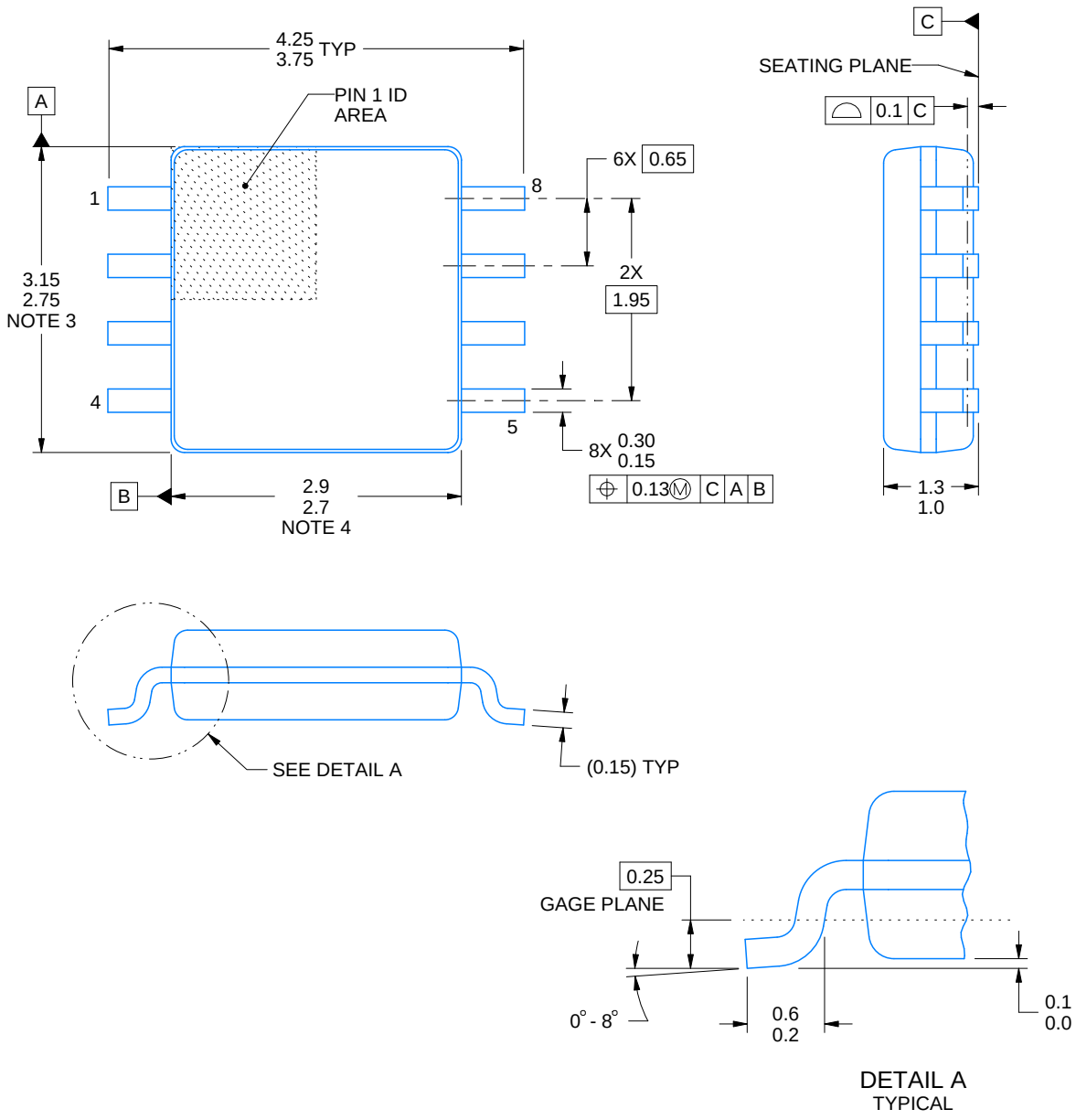
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC2G157DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
74LVC2G157DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G157DCT3	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G157DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G157DCTR	SM8	DCT	8	3000	183.0	183.0	20.0
SN74LVC2G157DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC2G157DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G157DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G157DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC2G157DCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G157YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

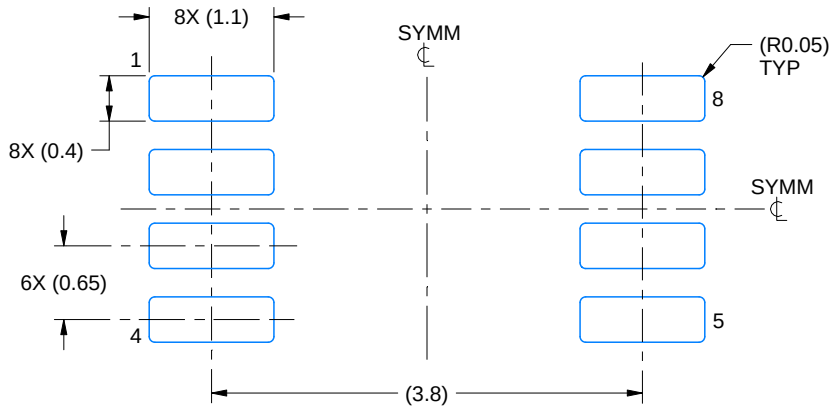
SMALL OUTLINE PACKAGE



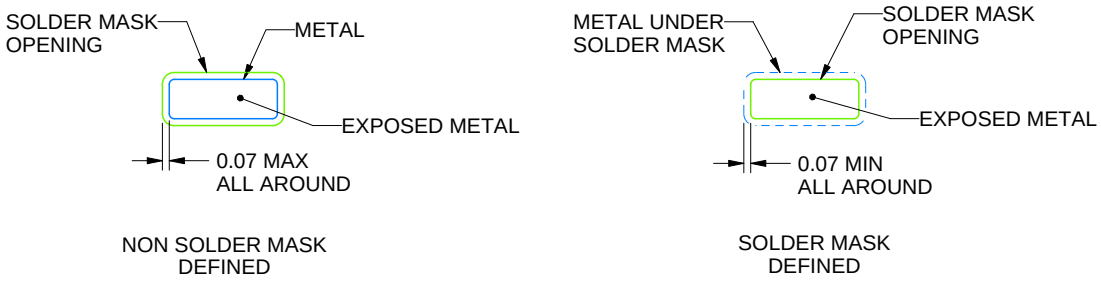
4220784/B 07/2020

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

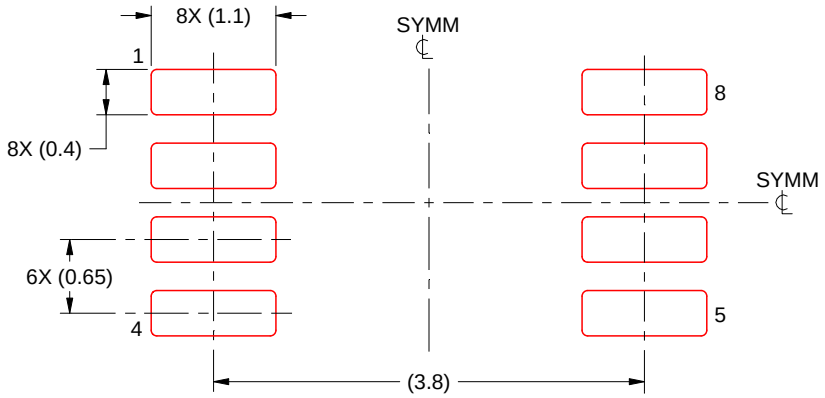


SOLDER MASK DETAILS

4220784/B 07/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/B 07/2020

NOTES: (continued)

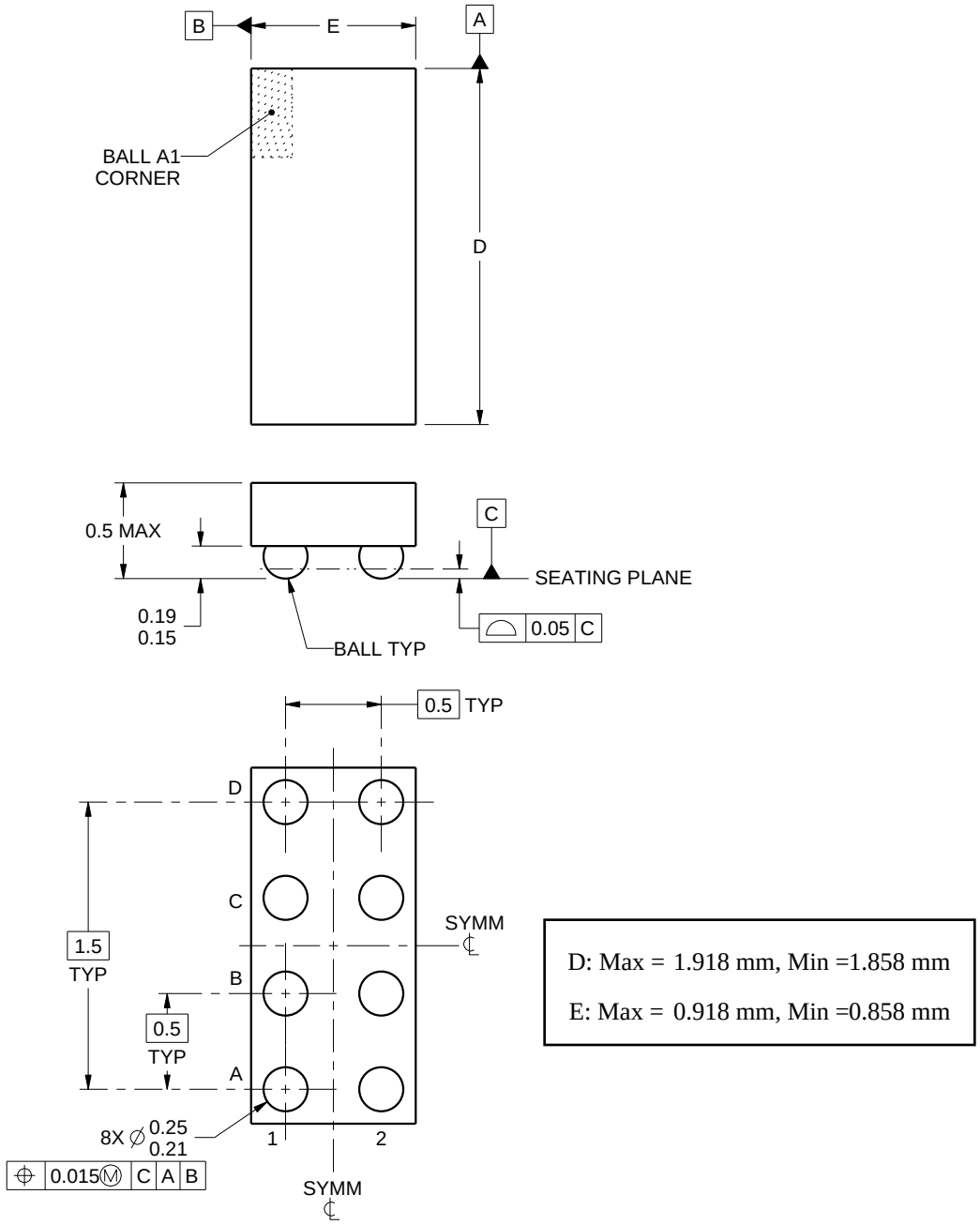
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0008

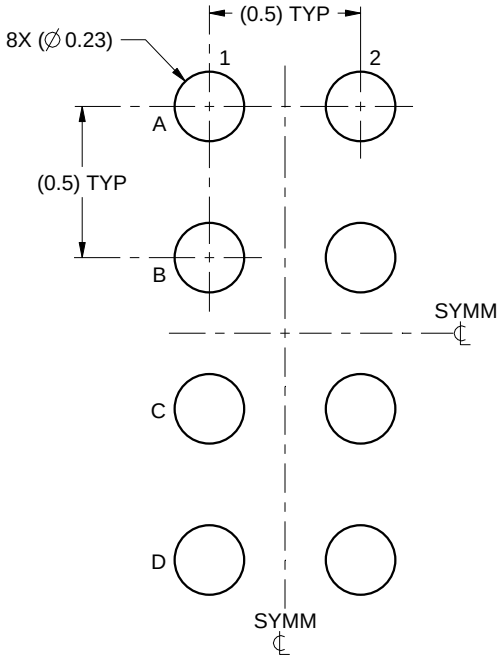
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

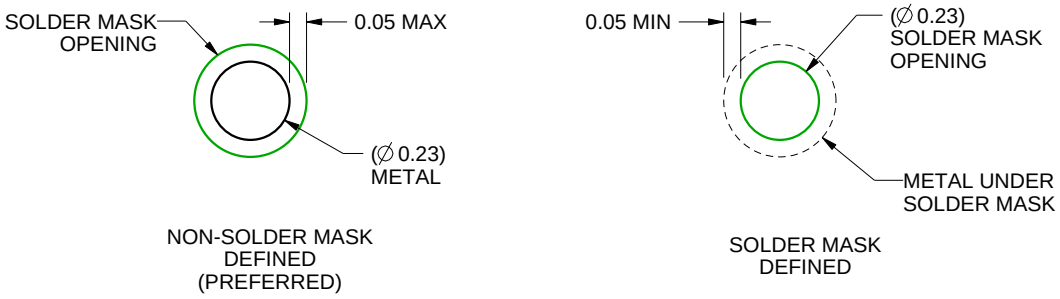


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

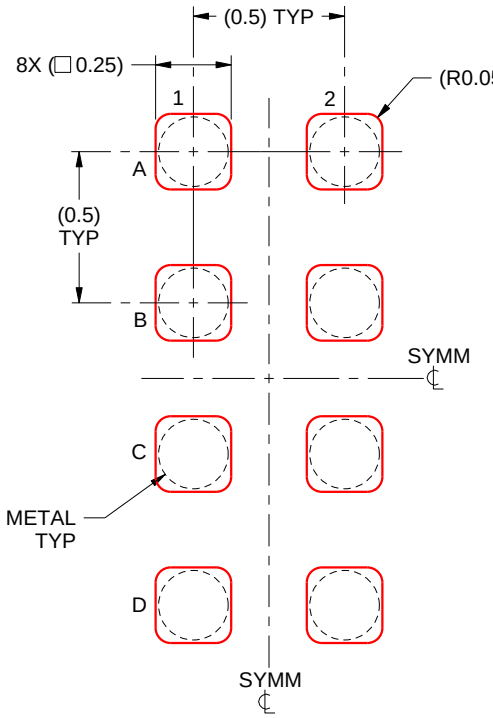


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



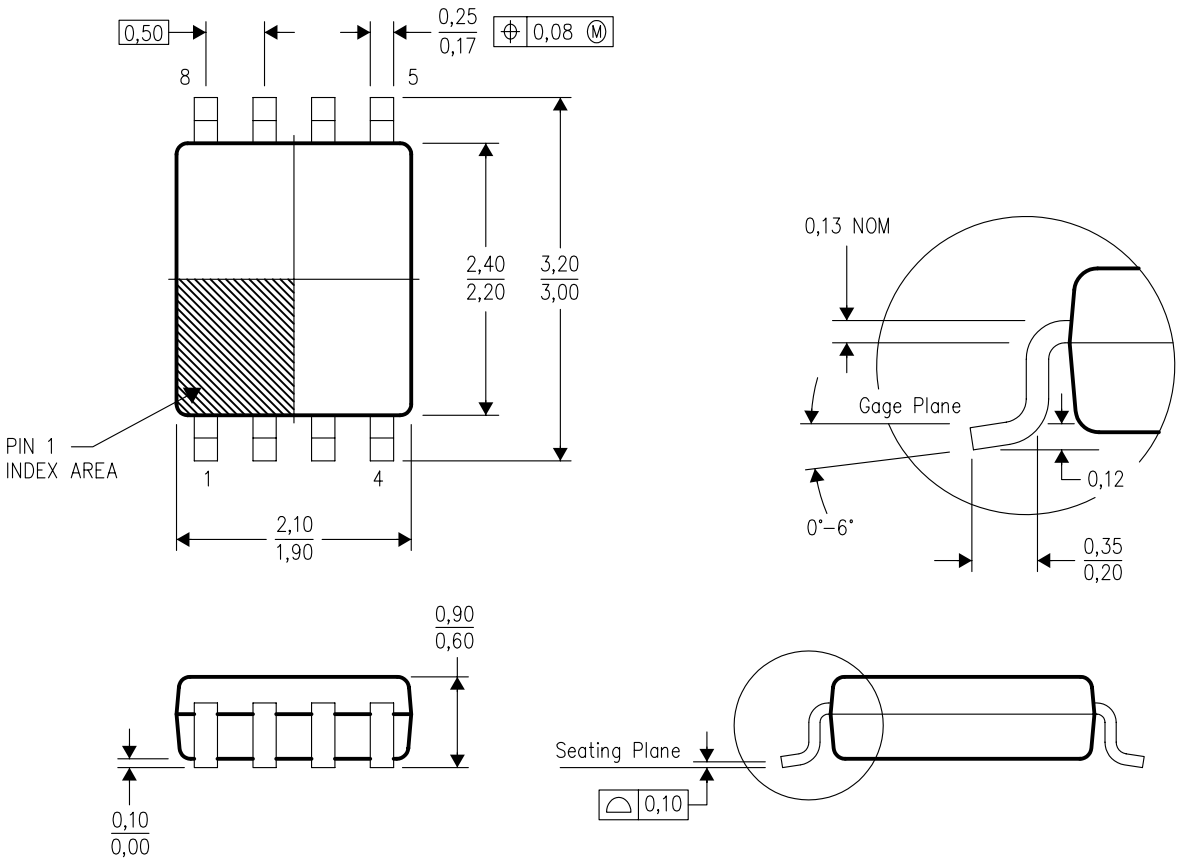
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

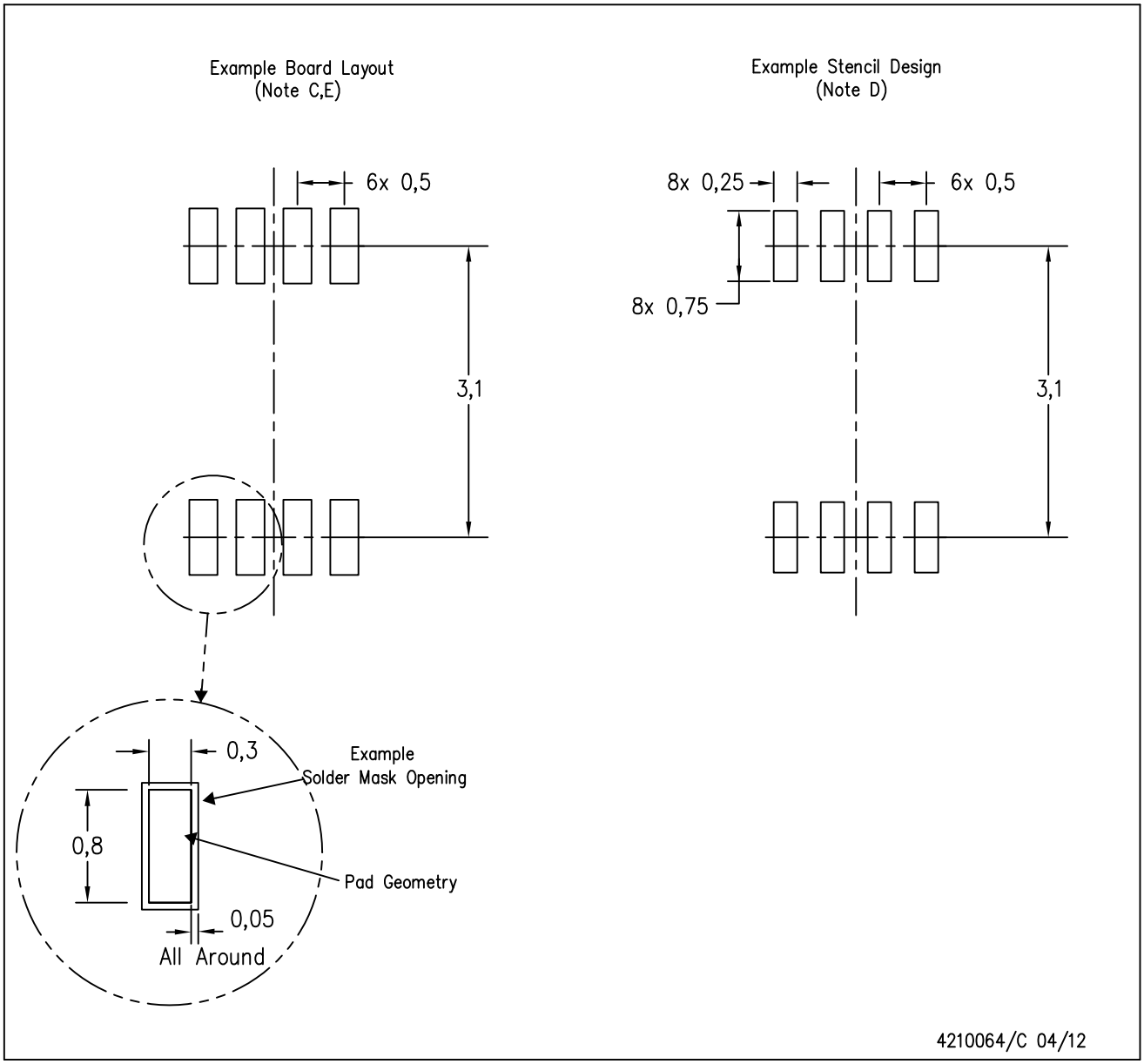
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4200503/F 07/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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