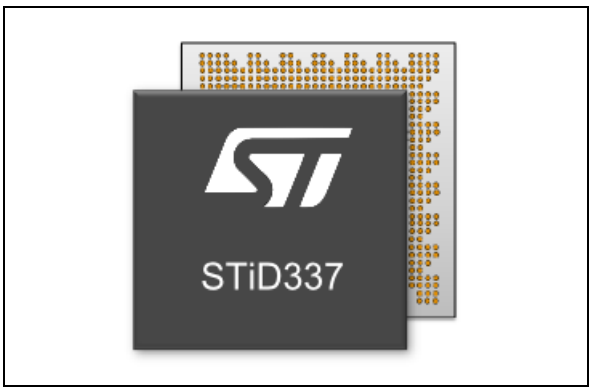
STiD337

Satellite transceiver ARM® Cortex®-based SoC with integrated DVB-S2/S2X forward link and IQ-streamer for return link

Data brief



Features

- Integrated DVB-S/S2/S2X demodulator
- Dual core ARM® Cortex®-A9 application CPU:
  - Up to 1.2 GHz and 6000 DMIPS
  - NEON™ accelerator
  - 512-Kbyte L2 cache
- DDR3/3L 16-bit interface running at up to 1066 MHz (DDR3-2133)
- Integrated ARM® Cortex®-M4 standby controller with low-power micro and power islands
- Quad ST231 offload CPUs
- IQ data pipe and streaming engine to high-speed DACs
- Sample-rate conversion filter including root-raised-cosine
- High-speed IQ signal DACs
- High-precision low-speed DACs
- Connectivity:
  - 2 x USB 2.0 ports
  - 1 x PCIe port
  - 1 x SD card
  - 1 x eMMC
  - 1 x RGMII muxed with internal Ethernet PHY
  - 4 x input transport streams
  - 6 x UART
  - 9 x I2C
- Package: FCBGA 16 mm x 16 mm, 0.65 mm pitch, 552 balls

Description

The STiD337 is a system-on-chip (SoC) for interactive satellite applications that includes an integrated DVB-S2/S2X demodulator for the satellite forward link with flexible GSE and MPEG-TS PID filtering.

The compute platform is based on a dual-core ARM® Cortex®-A9 architecture with Neon™ coprocessors and multiple ST231 DSP offload processors.

The return link implements an IQ streamer which streams a linked list of pre-calculated data to the integrated 10-bit DACs for IQ output to external up-converters.

Accurate Network clock recovery (NCR) with precision real-time control is implemented for the most demanding applications.

Multiple interfaces such as integrated Ethernet physical layer (PHY), USB, PCIe, VCXO, GPIO, SPI, I2C, and I2S are included to provide a complete low-cost satellite modem.

Revision history

Table 1. Document revision history

Date	Revision	Changes
20-Feb-2017	1	Initial release.