3-Channel RGBHV Video Buffer with I^2C Control, Selectable Filters, Monitor Pass-Thru, 2:1 Input MUX, and Selectable Input Bias Modes

Check for Samples: THS7327

FEATURES

- 3-Video Amplifiers for CVBS, S-Video, SD/ED/HD $Y'P'_BP'_R$, G'B'R', and R'G'B' Video
- HV Sync Paths With Adj. Schmitt Trigger
- 2:1 Input MUX
- I^2C™ Control of All Functions
- Integrated Low-Pass Filters on ADC Buffers
  - 5^{th} Order Butterworth Characteristics
  - Selectable Corner Frequencies of 9-MHz, 16-MHz, 35-MHz, and 75-MHz with Bypass (500-MHz)
- Selectable Input Bias Modes:
  - AC-Coupled with Sync-Tip Clamp
  - AC-Coupled with Bias
  - DC-Coupled with Offset Shift
  - DC-Coupled
- Monitor Pass-Thru Function:
  - Passes the Input Signal With no Filtering
  - 500-MHz BW and 1300 V/µs Slew Rate
  - 6-dB Gain With SAG Correction Capable
  - High Output Impedance in Disable State
- 2.7-V to 5-V Single Supply Operation
- Low 330 mW at 3.3-V Power Consumption
- Disable Function Reduces Current to < 1 µA
- Rail-to-Rail Output:
  - Output Swings Within 0.1 V From the Rails Which Allows AC or DC Output Coupling
- RoHS TQFP Package

APPLICATIONS

- Projectors
- Professional Video Systems
- LCD/DLP/LOCS Input Buffering

DESCRIPTION

Fabricated using the new complementary silicon-germanium (SiGe) BiCom-III process, the THS7327 is a low-power, single-supply 2.7-V to 5-V, 3-channel integrated video buffer with H and V Sync signal paths. It incorporates a selectable 5th order Butterworth anti-aliasing filter on each channel. The 9-MHz is a perfect choice for SDTV video including composite, S-Video™, and 480i/576i. The 16-MHz filter is ideal for EDTV 480p/576p and VGA signals. The 35-MHz filter is useful for HDTV 720p/1080i and SVGA signals. The 75-MHz filter is ideal for HDTV 1080p and XGA/SXGA signals. For UXGA/QXGA R'G'B' signals, the filter can be bypassed allowing a 500-MHz bandwidth, 1150-V/µs amplifier to buffer the signal.

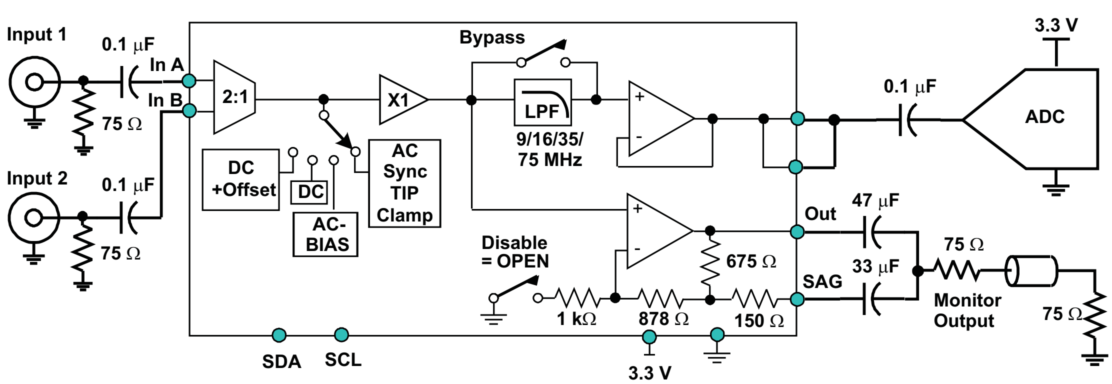


Figure 1. 3.3 V Single-Supply AC-Input/AC-Video Output System w/SAG Correction (1 of 3 Channels Shown)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

Each channel of the THS7327 is individually I^2C configurable for all functions including controlling the 2:1 input MUX. Its rail-to-rail output stage allows for both ac and dc coupling applications. The monitor pass-thru path allows for passing the input signal, with no filtering, on to other systems. This path has a 6-dB Gain, 500-MHz bandwidth, 1300V/μs slew rate, SAG correction capability, and a high output impedance while disabled to add to the flexibility of the THS7327.

As part of the THS7327 flexibility, the input can be selected for ac or dc coupled inputs. The ac-coupled modes include a sync-tip clamp option for CVBS/Y'/G'B'R' with sync or a fixed bias for the C'/P'_B/P'_R/R'G'B' channels without sync. The dc input options include a dc input or a dc+Offset shift to allow for a full sync dynamic range at the output with 0-V input.

The THS7327 is available in a RoHS-compliant TQFP package.

PACKAGING/ORDERING INFORMATION(1)

PACKAGED DEVICES	PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY
THS7327PHP	HTQFP-48 PowerPAD™	Tray, 250
THS7327PHPR		Tape and reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

			THS7327	UNIT
V_{SS}	Supply voltage, GND to V_A or GND to V_{DD}		5.5	V
V_I	Input voltage		–0.4 to V_A or V_{DD}	V
I_O	Output current		±100	mA
	Continuous power dissipation		See Dissipation Rating Table	
T_J	Maximum junction temperature, any condition(2)		+150	°C
T_J	Maximum junction temperature, continuous operation, long term reliability(3)		+125	°C
T_{stg}	Storage temperature range		–65 to +150	°C
	ESD ratings	HBM	1500	V
		CDM	1500	V
		MM	100	V

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING(1) (2) (T_J = +125°C)	
			T_A = +25°C	T_A = +85°C
HTQFP-48 with PowerPAD (PHP)	1.1	35	2.85 W	1.14 W

(1) This data was taken with a PowerPAD standard 3 inch by 3 inch, 4-layer PCB with internal ground plane connections to the PowerPAD.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase and long-term reliability starts to be reduced. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Digital supply voltage	2.7		5	V
V_A	Analog supply voltage. Must be equal to or greater than V_{DD}.	V_{DD}		5	V
T_A	Ambient temperature	–40		+85	°C

ELECTRICAL CHARACTERISTICS, $V_A = V_{DD} = 3.3$ V

R_L = 150 Ω || 5 pF to GND for monitor output, 19 kΩ || 8 pF load to GND for ADC buffer, ADC buffer filter = 9 MHz, and SAG pin shorted to monitor output pin (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/MAX/ TYP
AC PERFORMANCE								
Small-signal bandwidth (–3 dB)	Buffer output V_O = 0.2 V_{PP}	Filter select = 9 MHz(1)	9	7/10.4	6.9/10.5	6.8/10.5	MHz	Min/Max
		Filter select = 16 MHz(1)	16	13.1/9.6	12.9/19.7	12.8/19.7	MHz	Min/Max
		Filter select = 35 MHz(1)	35	28/40.5	27.8/41.3	27.7/41.3	MHz	Min/Max
		Filter select = 75 MHz(1)	75	61/86.8	60.5/90.3	60.4/90.3	MHz	Min/Max
		Filter select = bypass	500				MHz	Typ
	Monitor output		450				MHz	Typ
Large-signal bandwidth (–3 dB)	Buffer output V_O = 1 V_{PP}	Filter select = 9 MHz	9				MHz	Typ
		Filter select = 16 MHz	16				MHz	Typ
		Filter select = 35 MHz	35				MHz	Typ
		Filter select = 75 MHz	75				MHz	Typ
		Filter select = bypass	500				MHz	Typ
	Monitor output	V_O = 2 V_{PP}	300				MHz	Typ
Slew rate	Buffer output	Filter select = bypass: V_O = 1 V_{PP}	1050				V/μs	Typ
	Monitor output	V_O = 2 V_{PP}	1050				V/μs	Typ
Group delay at 100 kHz	Buffer output	Filter select = 9 MHz	56				ns	Typ
		Filter select = 16 MHz	31				ns	Typ
		Filter select = 35 MHz	16				ns	Typ
		Filter select = 75 MHz	8				ns	Typ
		Filter select = bypass	1.3				ns	Typ
	Monitor output		1.3				ns	Typ
Group delay variation with respect to 100 kHz	Buffer output	Filter select = 9 MHz: at 5.1 MHz	10.5				ns	Typ
		Filter select = 16 MHz: at 11 MHz	7.2				ns	Typ
		Filter select = 35 MHz: at 27 MHz	4				ns	Typ
		Filter select = 75 MHz: at 54 MHz	2				ns	Typ
Attenuation with respect to 100 kHz	Buffer output	Filter select = 9 MHz: at 5.75 MHz	0.4	–0.3/1.5	–0.35/1.55	–0.4/1.6	dB	Min/Max
		Filter select = 9 MHz: at 27 MHz	39	31	30.5	30	dB	Min
		Filter select = 16 MHz: at 11 MHz	0.5	–0.3/1.5	–0.35/1.55	–0.4/1.6	dB	Min/Max
		Filter select = 16 MHz: at 54 MHz	40	32	31.5	31	dB	Min
		Filter select = 35 MHz: at 27 MHz	1	–0.3/2.7	-0.35/2.75	–0.4/2.8	dB	Min/Max
		Filter select = 35 MHz: at 74 MHz	27	19	18.5	18	dB	Min
		Filter select = 75 MHz: at 54 MHz	0.6	–0.3/1.8	–0.4/1.9	–0.45/2	dB	Min/Max
		Filter select = 75 MHz: at 148 MHz	25	17	16.5	16	dB	Min
Differential gain	Buffer output	Filter select = 9 MHz: NTSC/PAL	0.3/0.45				%	Typ
	Monitor output	NTSC/PAL	0.07/0.08				%	Typ
Differential phase	Buffer output	Filter select = 9 MHz: NTSC/PAL	0.45/0.5				°	Typ
	Monitor output	NTSC/PAL	0.07/0.08				°	Typ
Total harmonic distortion f = 1 MHz	Buffer output V_O = 1 V_{PP}	Filter select = 9 MHz	–61				dB	Typ
		Filter select = 16 MHz	–60				dB	Typ
		Filter select = 35 MHz	–57				dB	Typ
		Filter select = 75 MHz	–55				dB	Typ
		Filter select = bypass	–60				dB	Typ
	Monitor output	V_O = 2 V_{PP}	–60				dB	Typ
Signal to noise ratio (unified weighting)	Buffer output	Filter select = 9 MHz	80				dB	Typ
		Filter select = 16 MHz	77				dB	Typ
		Filter select = 35 MHz	75				dB	Typ
		Filter select = 75 MHz	73				dB	Typ
		Filter select = bypass(2)	66				dB	Typ
	Monitor output	See (2)	71				dB	Typ

(1) Min/Max values listed are specified by design only.
(2) Bandwidth up to 100-MHz, no weighting, tilt null.

ELECTRICAL CHARACTERISTICS, V_A = V_{DD} = 3.3 V (continued)

R_L = 150 Ω || 5 pF to GND for monitor output, 19 kΩ || 8 pF load to GND for ADC buffer, ADC buffer filter = 9 MHz, and SAG pin shorted to monitor output pin (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/MAX/ TYP
AC PERFORMANCE (continued)								
Channel-to-channel crosstalk	Buffer output	Filter select = 9 MHz: at 5 MHz	–58				dB	Typ
		Filter select = 16 MHz: at 10 MHz	–65				dB	Typ
		Filter select = 35 MHz: at 27 MHz	–58				dB	Typ
		Filter select = 75 MHz: at 60 MHz	–58				dB	Typ
		Filter select = bypass: at 100 MHz	–47				dB	Typ
	Monitor output	F = 100 MHz	–35				dB	Typ
MUX isolation	Buffer output	Filter select = 9 MHz: at 5.5 MHz	65				dB	Typ
		Filter select = 16 MHz: at 11 MHz	65				dB	Typ
		Filter select = 35 MHz: at 27 MHz	65				dB	Typ
		Filter select = bypass: at 60 MHz	65				dB	Typ
	Monitor output	f = 100 MHz	66				dB	Typ
Gain	Buffer output	f = 100 kHz; V_O = 1 V_{PP}	0				dB	Typ
	Monitor output	f = 100 kHz; V_O = 2 V_{PP}	6	5.8/6.25	5.75/6.3	5.75/6.35	dB	Min/Max
Settling time	Buffer output	V_{IN} = 1 V_{PP}; 0.5% Settling	6				ns	Typ
	Monitor output		6				ns	Typ
Output impedance	Buffer output	f = 10 MHz	2				Ω	Typ
	Monitor output	f = 10 MHz	0.4				Ω	Typ
DC PERFORMANCE								
Output offset voltage	Buffer output	Bias = dc, filter = 16 MHz	65	130	135	135	mV	Max
	Monitor output	Bias = dc	20	90	95	95	mV	Max
Average offset voltage drift	Buffer output	Bias = dc				20	μV/°C	Typ
	Monitor output	Bias = dc				20	μV/°C	Typ
Bias output voltage	Buffer output	Bias = dc + shift, V_{IN} = 0 V	340	260/430	250/440	240/450	mV	Min/Max
		Bias = ac-bias	1.1	0.95/1.25	0.9/1.3	0.9/1.3	V	Min/Max
	Monitor output	Bias = dc + Shift, V_{IN} = 0 V	230	160/350	155/370	150/375	mV	Min/Max
		Bias = ac-bias	1.7	1.55/1.85	1.5/1.9	1.5/1.9	V	Min/Max
Sync tip clamp voltage	Buffer output	Bias = ac STC, clamp voltage	345	260/500	255/505	250/510	mV	Min/Max
	Monitor output		305	210/400	205/405	200/410	mV	Min/Max
Input bias current		Bias = dc – implies Ib out of the pin	–1.4	–3	–3.5	–3.5	μA	Max
Average bias current drift		Bias = dc				10	nA/°C	Typ
Sync tip clamp bias current		Bias = ac STC, low bias	2.3	0.9/3.5	0.8/3.7	0.7/3.8	μA	Min/Max
		Bias = ac STC, mid bias	5.9	4.2/8	4/8.2	3.9/8.3	μA	Min/Max
		Bias = ac STC, high bias	8.2	6.1/10.8	6/1	5.9/11.1	μA	Min/Max
INPUT CHARACTERISTICS								
Input voltage range		Bias = dc	0/1.8				V	Typ
Input resistance		Bias = ac-bias mode	25				kΩ	Typ
		Bias = dc, dc + shift, ac STC	3				MΩ	Typ
Input capacitance			1.5				pF	Typ
OUTPUT CHARACTERISTICS – MONITOR OUTPUT								
High output voltage swing		R_L = 150 Ω to 1.65 V	3.15	2.9	2.8	2.8	V	Min
		R_L = 150 Ω to GND	3.05	2.85	2.75	2.75	V	Min
		R_L = 75 Ω to 1.65 V	3.05				V	Min
		R_L = 75 Ω to GND	2.9				V	Min
Low output voltage swing		R_L = 150 Ω to 1.65 V	0.15	0.25	0.28	0.29	V	Min
		R_L = 150 Ω to GND	0.1	0.18	0.21	0.22	V	Min
		R_L = 75 Ω to 1.65 V	0.25				V	Min
		R_L = 75 Ω to GND	0.08				V	Min
Output current	Sourcing	R_L = 10 Ω to 1.65 V	80	50	47	45	mA	Min
	Sinking	R_L = 10 Ω to 1.65 V	75	50	47	45	mA	Min

ELECTRICAL CHARACTERISTICS, $V_A = V_{DD} = 3.3$ V (continued)

R_L = 150 Ω || 5 pF to GND for monitor output, 19 kΩ || 8 pF load to GND for ADC buffer, ADC buffer filter = 9 MHz, and SAG pin shorted to monitor output pin (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/MAX/ TYP
OUTPUT CHARACTERISTICS – BUFFER OUTPUT								
High output voltage swing (limited by input range and G = 0 dB)		Load = 19 kΩ || 8 pF to 1.65 V	2	1.8	1.75	1.75	V	Min
Low output voltage swing (limited by input range and G = 0 dB)			0.14	0.24	0.27	0.28	V	Max
Output current	Sourcing	R_L = 10 Ω to GND	80	50	47	45	mA	Min
	Sinking	R_L = 10 Ω to 1.65 V	75	50	47	45	mA	Min
POWER SUPPLY – ANALOG								
Maximum operating voltage		V_A	3.3	5.5	5.5	5.5	V	Max
Minimum operating voltage		V_A	3.3	2.7	2.7	2.7	V	Min
Maximum quiescent current		V_A, dc + shift mode, V_{IN} = 100 mV	100	120	123	125	mA	Max
Minimum quiescent current		V_A, dc + shift mode, V_{IN} = 100 mV	100	80	77	75	mA	Min
Power-supply rejection (+PSRR)		Buffer output	50				dB	Typ
POWER SUPPLY – DIGITAL								
Maximum operating voltage		V_{DD}	3.3	5.5	5.5	5.5	V	Max
Minimum operating voltage		V_{DD}	3.3	2.7	2.7	2.7	V	Min
Maximum quiescent current		V_{DD}, V_{IN} = 0 V	0.65	1.2	1.3	1.4	mA	Max
Minimum quiescent current		V_{DD}, V_{IN} = 0 V	0.65	0.35	0.3	0.25	mA	Min
DISABLE CHARACTERISTICS – ALL CHANNELS DISABLED								
Quiescent current		All 3 channels disabled (3)	0.1				μA	Typ
Turn-on time delay (t_{ON})		Time for Is to reach 50% of final value after I²C control is initiated	5				μs	Typ
Turn-on time delay (t_{OFF})			2				μs	Typ
DIGITAL CHARACTERISTICS(4)								
High level input voltage		V_{IH}	2.3				V	Typ
Low level input voltage		V_{IL}	1.0				V	Typ
HV SYNC CHARACTERISTICS – R_{LOAD} = 1 kΩ To GND								
Schmitt trigger adj. pin voltage		Reference for Schmitt trigger	1.48	1.35/1.6	1.3/1.65	1.27/1.68	V	Min/Max
Schmitt trigger threshold range		Allowable range for Schmitt trigger adj.	0.9 to 2				V	Typ
Schmitt trigger VT+		Positive going input voltage threshold relative to Schmitt trigger threshold	0.25				V	Typ
Schmitt trigger VT–		Negative going input voltage threshold relative to Schmitt trigger threshold	–0.3				V	Typ
Schmitt trigger threshold pin input resistance		Input Resistance into Control Pin	10				kΩ	Typ
H V sync input impedance			10				MΩ	Typ
H V sync high output voltage		1 kΩ to GND	3.15	3.05	3	3	V	Min
H V sync low output voltage		1 kΩ to GND	0.01	0.05	0.1	0.1	V	Max
H V sync source current		10 Ω to GND	50	35	30	30	mA	Min
H V sync sink current		10 Ω to 3.3V	35	25	23	21	mA	Min
H V delay		Delay from input to output	6.5				ns	Typ
H V to buffer output skew		No filter on buffer channel	5				ns	Typ

(3) Note that the I²C circuitry is still active while in disable mode. The current shown is while there is no activity with the THS7327 circuitry.
(4) Standard CMOS logic.

ELECTRICAL CHARACTERISTICS, $V_A = V_{DD} = 5$ V

R_L = 150 Ω || 5 pF to GND for monitor output, 19 kΩ || 8 pF load to GND for ADC buffer, ADC buffer filter = 9 MHz, and SAG pin shorted to monitor output pin (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/MAX/ TYP
AC PERFORMANCE								
Small-signal bandwidth (–3 dB)	Buffer output V_O = 0.2 V_{PP}	Filter select = 9 MHz(1)	9	6.8/10.4	6.7/10.5	6.7/10.5	MHz	Min/Max
		Filter select = 16 MHz(1)	16	13.1/9.6	12.9/19.7	12.8/19.7	MHz	Min/Max
		Filter select = 35 MHz(1)	35	28/40.5	27.8/41.3	27.7/41.3	MHz	Min/Max
		Filter select = 75 MHz(1)	78	64/89	63.5/92.3	63.4/92.4	MHz	Min/Max
		Filter select = bypass	500				MHz	Typ
	Monitor output		500				MHz	Typ
Large-signal bandwidth (–3 dB)	Buffer output V_O = 1 V_{PP}	Filter select = 9 MHz	9				MHz	Typ
		Filter select = 16 MHz	16				MHz	Typ
		Filter select = 35 MHz	35				MHz	Typ
		Filter select = 75 MHz	78				MHz	Typ
		Filter select = bypass	500				MHz	Typ
	Monitor output	V_O = 2 V_{PP}	425				MHz	Typ
Slew rate	Buffer output	Filter select = bypass: V_O = 1 V_{PP}	1150				V/µs	Typ
	Monitor output	V_O = 2 V_{PP}	1300				V/µs	Typ
Group delay at 100 kHz	Buffer output	Filter select = 9 MHz	56				ns	Typ
		Filter select = 16 MHz	31				ns	Typ
		Filter select = 35 MHz	16				ns	Typ
		Filter select = 75 MHz	8				ns	Typ
		Filter select = bypass	1.3				ns	Typ
	Monitor output		1.25				ns	Typ
Group delay variation with respect to 100 kHz	Buffer output	Filter select = 9 MHz: at 5.1 MHz	10.5				ns	Typ
		Filter select = 16 MHz: at 11 MHz	7.2				ns	Typ
		Filter select = 35 MHz: at 27 MHz	4				ns	Typ
		Filter select = 75 MHz: at 54 MHz	2				ns	Typ
Attenuation with respect to 100 kHz	Buffer output (2)	Filter select = 9 MHz: at 5.75 MHz	0.4	–0.3/1.5	–0.35/1.55	–0.4/1.6	dB	Min/Max
		Filter select = 9 MHz: at 27 MHz	39	31	30.5	30	dB	Min
		Filter select = 16 MHz: at 11 MHz	0.5	–0.3/1.5	–0.35/1.55	–0.4/1.6	dB	Min/Max
		Filter select = 16 MHz: at 54 MHz	40	32	31.5	31	dB	Min
		Filter select = 35 MHz: at 27 MHz	1	–0.3/2.7	–0.35/2.75	–0.4/2.8	dB	Min/Max
		Filter select = 35 MHz: at 74 MHz	27	19	18.5	18	dB	Min
		Filter select = 75 MHz: at 54 MHz	0.6	–0.3/1.8	–0.4/1.9	–0.45/2	dB	Min/Max
		Filter select = 75 MHz: at 148 MHz	25	17	16.5	16	dB	Min
Differential gain	Buffer output	Filter select = 9 MHz: NTSC/PAL	0.3/0.45				%	Typ
	Monitor output	NTSC/PAL	0.07/0.08				%	Typ
Differential phase	Buffer output	Filter select = 9 MHz: NTSC/PAL	0.45/0.5				°	Typ
	Monitor output	NTSC/PAL	0.07/0.08				°	Typ
Total harmonic distortion f = 1 MHz	Buffer output V_O = 1 V_{PP}	Filter select = 9 MHz	–61				dB	Typ
		Filter select = 16 MHz	–60				dB	Typ
		Filter select = 35 MHz	–57				dB	Typ
		Filter select = 75 MHz	–55				dB	Typ
		Filter select = bypass	–60				dB	Typ
	Monitor output	V_O = 2 V_{PP}	–60				dB	Typ
Signal to noise ratio (unified weighting)	Buffer output	Filter select = 9 MHz	80				dB	Typ
		Filter select = 16 MHz	77				dB	Typ
		Filter select = 35 MHz	75				dB	Typ
		Filter select = 75 MHz	73				dB	Typ
		Filter select = bypass(3)	66				dB	Typ
	Monitor output	See (3)	71				dB	Typ

(1) Min/Max values listed are specified by design only.
(2) Performance specified by design, characterization, and 3.3-V testing only.
(3) Bandwidth up to 100-MHz, no weighting, tilt null.

ELECTRICAL CHARACTERISTICS, $V_A = V_{DD}$ = 5 V (continued)

R_L = 150 Ω || 5 pF to GND for monitor output, 19 kΩ || 8 pF load to GND for ADC buffer, ADC buffer filter = 9 MHz, and SAG pin shorted to monitor output pin (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/MAX/ TYP
AC PERFORMANCE (continued)								
Channel-to-channel crosstalk	Buffer output	Filter select = 9 MHz: at 5 MHz	–58				dB	Typ
		Filter select = 16 MHz: at 10 MHz	–65				dB	Typ
		Filter select = 35 MHz: at 27 MHz	–58				dB	Typ
		Filter select = 75 MHz: at 60 MHz	–58				dB	Typ
		Filter select = bypass: at 100 MHz	–47				dB	Typ
	Monitor output	F = 100 MHz	–35				dB	Typ
MUX isolation	Buffer output	Filter select = 9 MHz: at 5.5 MHz	65				dB	Typ
		Filter select = 16 MHz: at 11 MHz	65				dB	Typ
		Filter select = 35 MHz: at 27 MHz	65				dB	Typ
		Filter select = bypass: at 60 MHz	65				dB	Typ
	Monitor output	f = 100 MHz	66				dB	Typ
Gain	Buffer output	f = 100 kHz; V_O = 1 V_{PP}	0				dB	Typ
	Monitor output	f = 100 kHz; V_O = 2 V_{PP}	6	5.8/6.25	5.75/6.3	5.75/6.35	dB	Min/Max
Settling time	Buffer output	V_{IN} = 1 V_{PP}; 0.5% settling	6				ns	Typ
	Monitor output		6				ns	Typ
Output impedance	Buffer output	f = 10 MHz	2				Ω	Typ
	Monitor output	f = 10 MHz	0.4				Ω	Typ
DC PERFORMANCE								
Output offset voltage	Buffer output	Bias = dc, filter = 16 MHz	50	120	125	125	mV	Max
	Monitor output	Bias = dc	5	80	85	85	mV	Max
Average offset voltage drift	Buffer output	Bias = dc				20	μV/°C	Typ
	Monitor output	Bias = dc				20	μV/°C	Typ
Bias output voltage	Buffer output	Bias = dc + shift, V_{IN} = 0 V	345	265/450	255/455	250/460	mV	Min/Max
		Bias = ac-bias	1.55	1.4/1.7	1.35/1.75	1.35/1.75	V	Min/Max
	Monitor output	Bias = dc + shift, V_{IN} = 0 V	230	150/340	145/345	140/350	mV	Min/Max
		Bias = ac-bias	2.65	2.5/2.8	2.45/2.85	2.45/2.85	V	Min/Max
Sync tip clamp output voltage	Buffer output	Bias = ac STC, clamp voltage	350	265/500	260/505	255/510	mV	Min/Max
	Monitor output		305	210/400	205/405	200/410	mV	Min/Max
Input bias current		Bias = dc – implies Ib out of the pin	–1.4	–3	–3.5	–3.5	μA	Max
Average bias current drift		Bias = dc				10	nA/°C	Typ
Sync tip clamp bias current		Bias = ac STC, low bias	2.45	1/3.9	0.9/4	0.8/4.1	μA	Min/Max
		Bias = ac STC, mid bias	6.35	4.3/8.4	4.1/8.6	4/8.7	μA	Min/Max
		Bias = ac STC, high bias	8.75	6.4/11.2	6.2/11.4	6.1/11.5	μA	Min/Max
INPUT CHARACTERISTICS								
Input voltage range		Bias = dc	0/2.5	0/2.45	0/2.4	0/2.4	V	Typ
Input resistance		Bias = ac-bias mode	20				kΩ	Typ
		Bias = dc, dc + shift, ac STC	3				MΩ	Typ
Input capacitance			2				pF	Typ
OUTPUT CHARACTERISTICS – MONITOR OUTPUT								
High output voltage swing		R_L = 150 Ω to 2.5 V	4.8	4.65	4.6	4.6	V	Min
		R_L = 150 Ω to GND	4.7	4.55	4.5	4.5	V	Min
		R_L = 75 Ω to 2.5 V	4.7				V	Min
		R_L = 75 Ω to GND	4.6				V	Min
Low output voltage swing		R_L = 150 Ω to 2.5 V	0.19	0.25	0.28	0.3	V	Min
		R_L = 150 Ω to GND	0.11	0.19	0.23	0.24	V	Min
		R_L = 75 Ω to 2.5 V	0.24				V	Min
		R_L = 75 Ω to GND	0.085				V	Min
Output current	Sourcing	R_L = 10 Ω to 2.5 V	110	85	80	75	mA	Min
	Sinking	R_L = 10 Ω to 2.5 V	115	85	80	75	mA	Min

ELECTRICAL CHARACTERISTICS, $V_A = V_{DD}$ = 5 V (continued)

R_L = 150 Ω || 5 pF to GND for monitor output, 19 kΩ || 8 pF load to GND for ADC buffer, ADC buffer filter = 9 MHz, and SAG pin shorted to monitor output pin (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/MAX/ TYP
OUTPUT CHARACTERISTICS – BUFFER OUTPUT								
High output voltage swing (limited by input range and G = 0 dB)		Load = 19 kΩ || 8 pF to 2.5 V	3.4	3.1	3	3	V	Min
Low output voltage swing (limited by input range and G = 0 dB)			0.14	0.24	0.27	0.28	V	Max
Output current	Sourcing	R_L = 10 Ω to GND	110	85	80	75	mA	Min
	Sinking	R_L = 10 Ω to 2.5V	80	85	80	75	mA	Min
POWER SUPPLY – ANALOG								
Maximum operating voltage		V_A	5	5.5	5.5	5.5	V	Max
Minimum operating voltage		V_A	5	2.7	2.7	2.7	V	Min
Maximum quiescent current		V_A, dc + shift mode, V_{IN} = 100 mV	118	145	148	150	mA	Max
Minimum quiescent current		V_A, dc + shift mode, V_{IN} = 100 mV	118	95	92	90	mA	Min
Power-supply rejection (+PSRR)		Buffer output	46				dB	Typ
POWER SUPPLY – DIGITAL								
Maximum operating voltage		V_{DD}	5	5.5	5.5	5.5	V	Max
Minimum operating voltage		V_{DD}	5	2.7	2.7	2.7	V	Min
Maximum quiescent current		V_{DD}, V_{IN} = 0 V	1	2	3	3	mA	Max
Minimum quiescent current		V_{DD}, V_{IN} = 0 V	1	0.5	0.4	0.4	mA	Min
DISABLE CHARACTERISTICS – ALL CHANNELS DISABLED								
Quiescent current		All channels disabled [4]	1				μA	Typ
Turn-on time delay (t_{ON})		Time for Is to reach 50% of final value after I^2C control is initiated	5				μs	Typ
Turn-on time delay (t_{OFF})			2				μs	Typ
DIGITAL CHARACTERISTICS[5]								
High level input voltage		V_{IH}	3.5				V	Typ
Low level input voltage		V_{IL}	1.5				V	Typ
HV SYNC CHARACTERISTICS[6]								
Schmitt trigger adj. pin voltage		Reference for Schmitt trigger	1.55	1.45/1.65	1.4/1.7	1.37/1.73	V	Min/Max
Schmitt trigger threshold range		Allowable range for Schmitt trigger adj.	0.9 to 2				V	Typ
Schmitt trigger VT+		Positive going input voltage threshold relative to Schmitt trigger threshold	0.25				V	Typ
Schmitt trigger VT–		Negative going input voltage threshold relative to Schmitt trigger threshold	–0.3				V	Typ
Schmitt trigger threshold pin input resistance		Input resistance into control pin	10				kΩ	Typ
H V sync input impedance			10				MΩ	Typ
H V sync high output voltage		1 kΩ to GND	4.8	4.7	4.6	4.6	V	Min
H V sync low output voltage		1 kΩ to GND	0.01	0.05	0.1	0.1	V	Max
H V sync source current		10 Ω to GND	90	60	55	55	mA	Min
H V sync sink current		10 Ω to 5 V	50	30	27	25	mA	Min
H V delay		Delay from input to output	6.5				ns	Typ
H V to buffer output skew		No filter on buffer channel	5				ns	Typ

(4) Note that the I^2C circuitry is still active while in disable mode. The current shown is while there is no activity with the THS7327 I^2C circuitry.
(5) Standard CMOS logic.
(6) Schmitt trigger threshold is defined by (VT+ – VT–)/2.

TIMING REQUIREMENTS FOR I²C INTERFACE(1)(2)

At V_{DD} = 2.7 V to 5 V.

PARAMETER		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	Clock frequency, SCL	0	100	0	400	kHz
$t_{w(H)}$	Pulse duration, SCL high	4		0.6		μs
$t_{w(L)}$	Pulse duration, SCL low	4.7		1.3		μs
t_r	Rise time, SCL and SDA		1000		300	ns
t_f	Fall time, SCL and SDA		300		300	ns
$t_{su(1)}$	Setup time, SDA to SCL	250		100		ns
$t_{h(1)}$	Hold time, SCL to SDA	0		0		ns
$t_{(buf)}$	Bus free time between stop and start conditions	4.7		1.3		μs
$t_{su(2)}$	Setup time, SCL to start condition	4.7		0.6		μs
$t_{h(2)}$	Hold time, start condition to SCL	4		0.6		μs
$t_{su(3)}$	Setup time, SCL to stop condition	4		0.6		μs
C_b	Capacitive load for each bus line		400		400	pF

(1) The THS7327 I²C address = 01011(A1)(A0)(R/$\overline{W}$). See the *Application Information* section for more information.
(2) The THS7327 was designed to comply with Version 2.1 of the I²C specification.

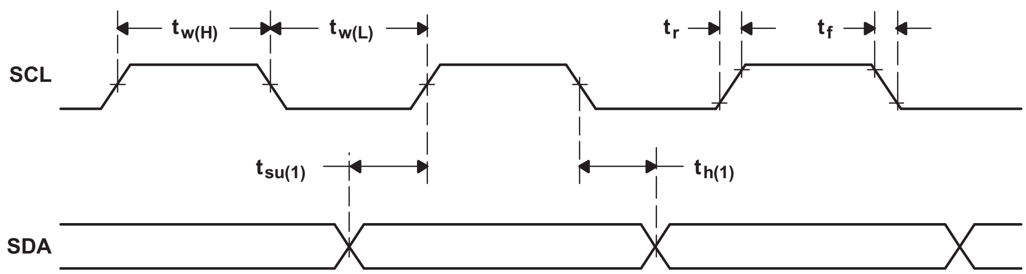


Figure 2. SCL and SDA Timing

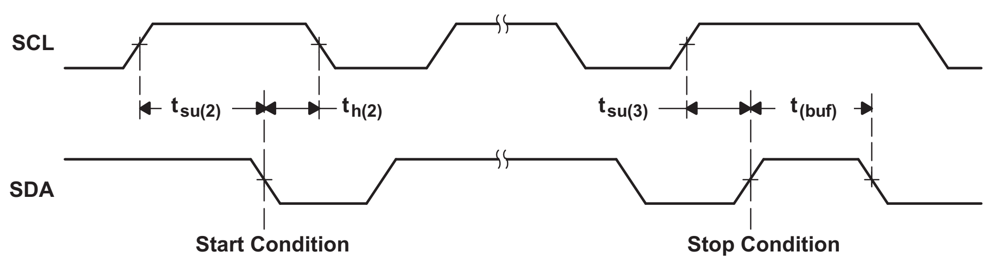
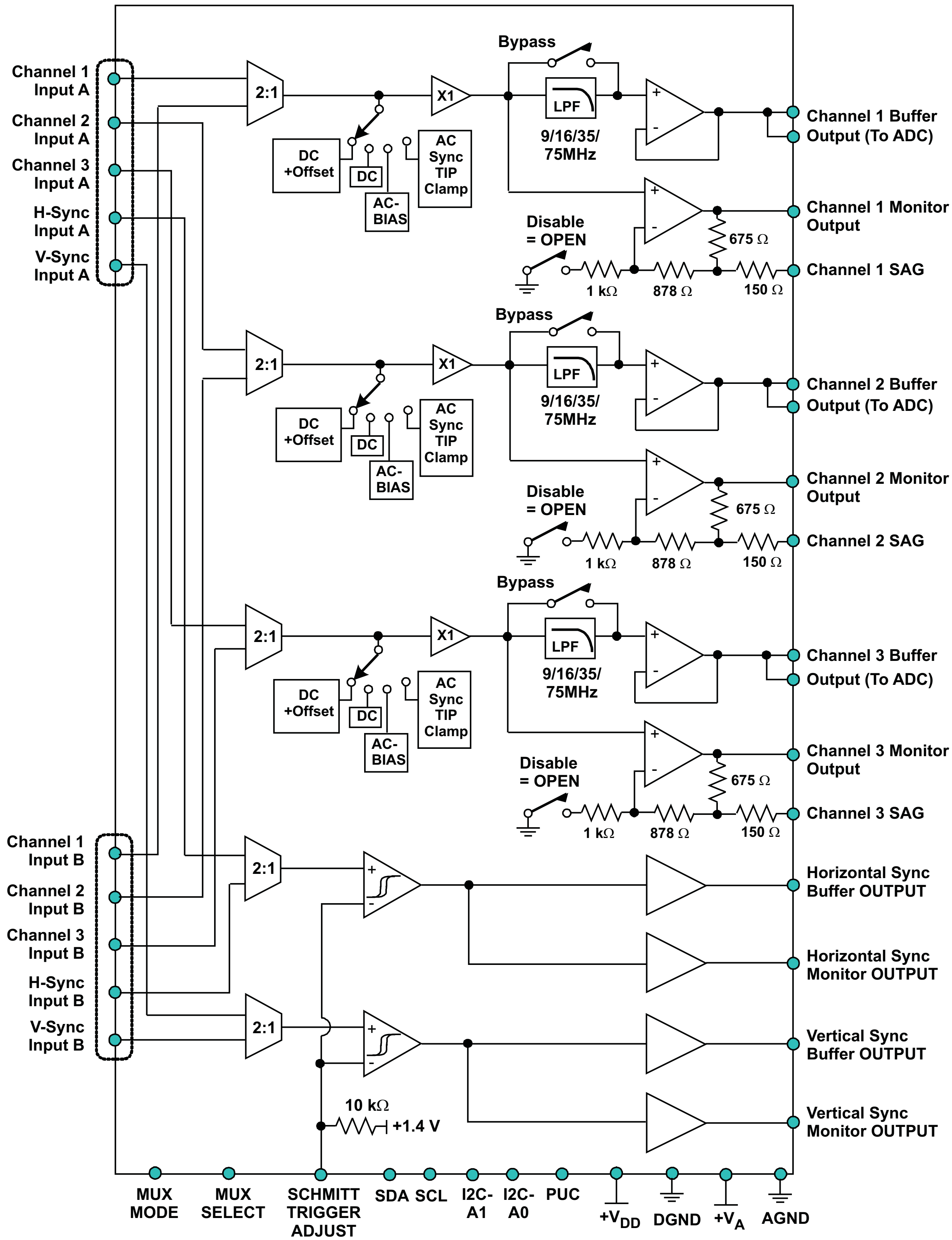


Figure 3. Start and Stop Conditions

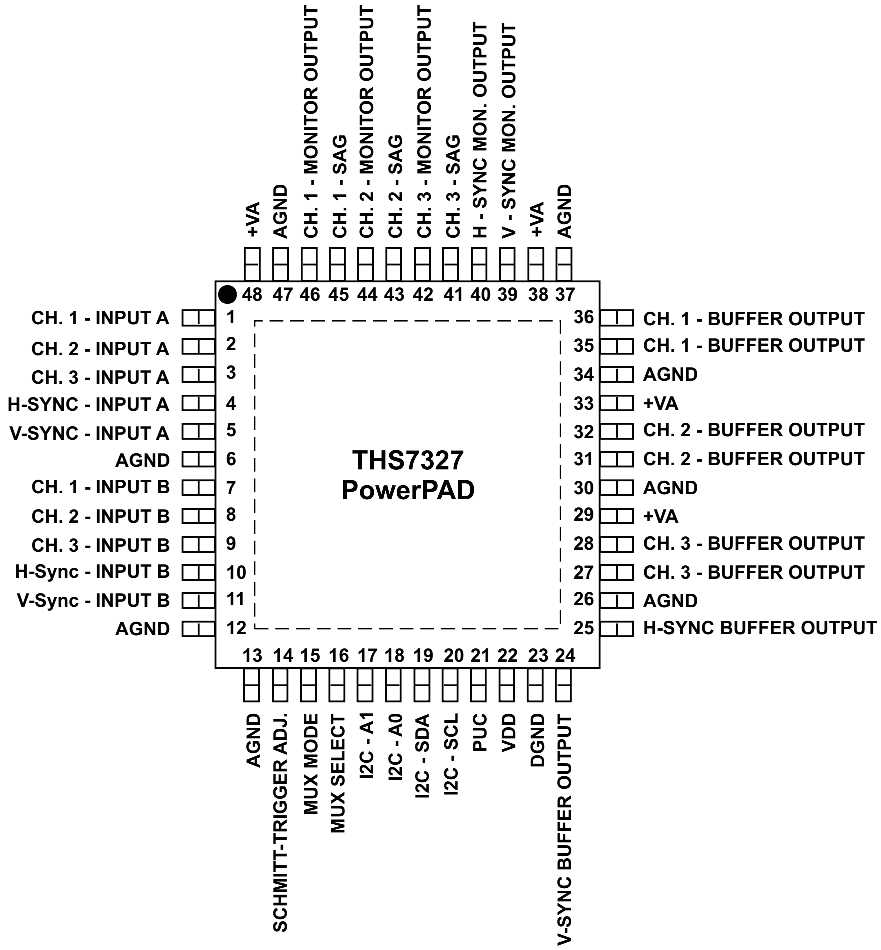
FUNCTIONAL DIAGRAM



NOTE: The I[2]C address of the THS7327 is 01011(A1)(A0)(R/$\overline{W}$).

PIN CONFIGURATION

THS7327PHP
HTQFP-48 (PHP)
(Top View)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO. HTQFP-48		
CH. 1 – input A	1	I	Video input channel 1 – input A
CH. 2 – input A	2	I	Video input channel 2 – input A
CH. 3 – input A	3	I	Video input channel 3 – input A
H-sync – input A	4	I	Horizontal sync – input A
V-sync – input A	5	I	Vertical sync – input A
CH. 1 – input B	7	I	Video input channel 1 – input B
CH. 2 – input B	8	I	Video input channel 2 – input B
CH. 3 – input B	9	I	Video input channel 3 – input B
H-sync – input B	10	I	Horizontal sync – input B
V-sync – input B	11	I	Vertical sync – input B
I^2C-A1	17	I	I^2C slave address control bit A1 – connect to V_{S+} for a Logic 1 preset value or GND for a logic 0 preset value.
I^2C-A0	18	I	I^2C slave address control bit A0 – connect to V_{S+} for a Logic 1 preset value or GND for a logic 0 preset value.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO. HTQFP-48		
I^2C-SDA	19	I/O	Serial data line of the I^2C bus. Pull-up resistor should have a minimum value = 2-kΩ and a maximum value = 19-kΩ. Pull up to V_{S+}.
I^2C-SCL	20	I	I^2C bus clock line. Pull-up resistor should have a minimum value = 2-kΩ and a maximum value = 19-kΩ. Pull up to V_{S+}.
PUC	21	I	Power-up condition – connect to GND for all channels disabled upon power-up. Connect to V_{DD} (logic high) to set buffer outputs to OFF and monitor outputs ON with ac-bias configuration on channels 1 to 3 and HV syncs are enabled.
MUX MODE	15	I	Sets the MUX configuration control – connect to logic low for MUX select (pin 16) control of the MUX. Connect to logic high for I^2C control of the MUX.
MUX select	16	I	Controls the MUX selection when MUX MODE (pin 15) is set to logic low. Connect to logic low for MUX selector set to input A. Connect to logic high for MUX selector set to input B.
CH. 1 – buffer output	35, 36	O	Output channel 1 from either CH. 1 – input A or CH. 1 – input B – connect to ADC / Scalar / Decoder
CH. 2 – buffer output	31, 32	O	Output channel 1 from either CH. 2 – input A or CH. 2 – input B – connect to ADC / Scalar / Decoder
CH. 3 – buffer output	27, 28	O	Output channel 3 from either CH. 3 – input A or CH. 3 – input B – connect to ADC / Scalar / Decoder
Horizontal sync output	25	O	Horizontal sync output – Connect to ADC / Scalar H-sync input
Vertical sync output	24	O	Vertical sync output – Connect to ADC / Scalar V-sync input
CH. 1 - SAG	45	O	Video monitor pass-thru output channel 1 SAG correction pin. If SAG is not used, connect directly to CH. 1 – output pin 46.
CH. 1 – output	46	O	Video monitor pass-thru output channel 1 from either CH. 1 – input A or CH. 1 – input B
CH. 2 - SAG	43	O	Video monitor pass-thru output channel 2 SAG correction pin. If SAG is not used, connect directly to CH. 2 – output pin 44.
CH. 2 – output	44	O	Video monitor pass-thru output channel 2 from either CH. 2 – input A or CH. 2 – input B
CH. 3 - SAG	41	O	Video monitor pass-thru output channel 3 SAG correction pin. If SAG is not used, connect directly to CH. 3 – output pin 42.
CH. 3 – output	42	O	Video monitor pass-thru output channel 3 from either CH. 3 – input A or CH. 3 – input B
Horizontal sync monitor output	40	O	Horizontal sync monitor pass-thru output
Vertical sync monitor output	39	O	Vertical sync monitor pass-thru output
AGND	6, 12, 13, 26, 30, 34, 37, 47	I	Ground reference pin for analog signals. Internally these pins connect to DGND. Although it is recommended to have the AGND and DGND connected to the proper signals for best results.
$+V_A$	29, 33, 38, 48	I	Analog positive power-supply input pins – connect to 2.7 V to 5 V. Must be equal to or greater than V_{DD}.
V_{DD}	22	I	Digital positive supply pin for I^2C circuitry and HV sync outputs – connect to 2.7 V to 5 V.
DGND	23	I	Digital GND pin for HV circuitry and I^2C circuitry.
Schmitt trigger adjust	14	I	Defaults to 1.45V (TTL compatible). Connect to external voltage reference to adjust HV sync input thresholds from 0.9-V to 2-V range.

TYPICAL CHARACTERISTICS: 3.3 V

SLEW RATE vs OUTPUT VOLTAGE

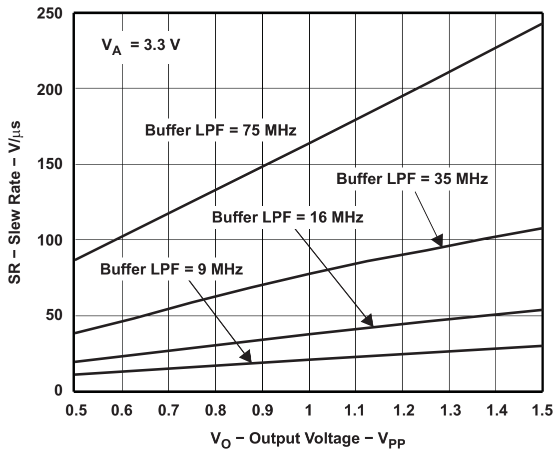


Figure 4.

SLEW RATE vs OUTPUT VOLTAGE

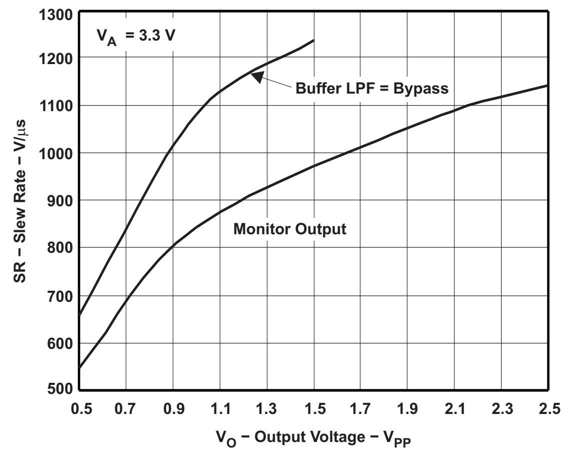


Figure 5.

TYPICAL CHARACTERISTICS: 5 V

SLEW RATE vs OUTPUT VOLTAGE

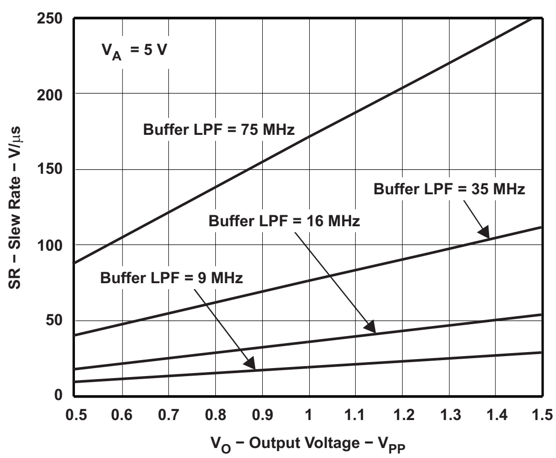


Figure 6.

SLEW RATE vs OUTPUT VOLTAGE

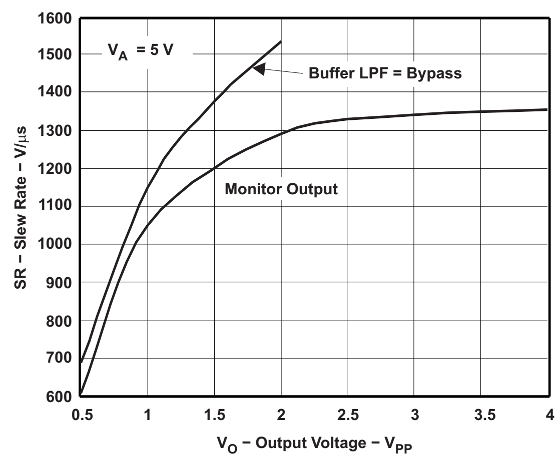


Figure 7.

APPLICATION INFORMATION

The THS7327 is targeted for RGB + HV sync video buffer applications. Although it can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters of the THS7327. Built on the complementary Silicon Germanium (SiGe) BiCom-3 process, the THS7327 incorporates many features not typically found in integrated video parts while consuming low power. Each channel configuration is completely independent of the other channels. This allows for ANY configuration for each channel to be dictated by the end user rather than the device—resulting in a highly flexible system. The THS7327 has the following features:

- I^2C Interface for easy interfacing to the system
- Single-supply 2.7-V to 5-V operation with low quiescent current of 100-mA at 3.3-V
- 2:1 input MUX
- Input configuration accepting dc, dc + shift, ac bias, or ac sync-tip clamp selection.
- Unity Gain Buffer path to drive analog-to-digital converter (ADC)/Scalar/Decoder.
- Selectable 5th-order low-pass filter on buffer path for digital-to-analog converter (DAC) reconstruction or ADC image rejection:
  - 9-MHz for SDTV NTSC and 480i, PAL/SECAM and 576i, and S-Video signals.
  - 16-MHz for EDTV 480p and 576p $Y'P'_BP'_R$ signals and R'G'B' (G'B'R') VGA signals.
  - 35-MHz for HDTV 720p and 1080i $Y'P'_BP'_R$ signals and R'G'B' SVGA and XGA signals.
  - 75-MHz for HDTV 1080p and R'G'B' SXGA signals.
  - Bypass mode for passing R'G'B' UXGA, QXGA or higher signals.
- Monitor Pass-thru path has an internal fixed gain of 2V/V (6 dB) amplifier that can drive two video lines with dc coupling, traditional ac coupling, or SAG corrected ac coupling.
- While disabled, the Monitor Pass-Thru path has a high output impedance (> 500 kΩ || 8 pF)
- Power Up Control (PUC) allows the THS7327 to be fully disabled or have the Monitor Pass-Thru function (with AC-Bias mode on all channels) enabled upon initial power-up.
- MUX is controlled by either I^2C or GPIO pin based on the MUX Mode pin logic.
- H and V Sync paths have an externally adjustable Schmitt Trigger threshold
- Disable mode which reduces quiescent current to as low as 0.1-µA.

OPERATING VOLTAGE

The THS7327 is designed to operate from 2.7 V to 5 V over a –40°C to +85°C temperature range. The impact on performance over the entire temperature range is negligible due to the implementation of thin film resistors and low-temperature coefficient capacitors.

The power supply pins should have a 0.1-µF to 0.01-µF capacitor placed as close as possible to these pins. Failure to do so may result in the THS7327 outputs ringing or oscillating. Additionally, a large capacitor, such as 22 µF to 100 µF, should be placed on the power-supply line to minimize issues with 50-Hz/60-Hz line frequencies.

INPUT VOLTAGE

The THS7327 input range allows for an input signal range from ground to about (V_{S+} – 1.6 V). But, due to the internal fixed gain of 2V/V (6 dB), the output is generally the limiting factor for the allowable linear input range. For example, with a 5-V supply, the linear input range is from GND to 3.4 V. But due to the gain, the linear output range limits the allowable linear input range to be from GND to at most 2.5 V.

INPUT OVERVOLTAGE PROTECTION

The THS7327 is built using a high-speed complementary bipolar and CMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All input and output device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 8.

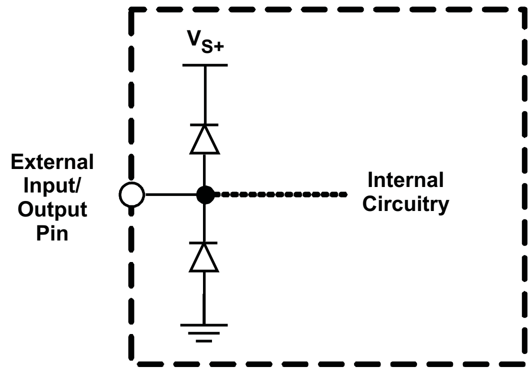


Figure 8. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above and below the supplies. The protection diodes can typically support 30-mA of continuous current when overdriven.

TYPICAL CONFIGURATION

The THS7327 is typically used as a video buffer driving a video ADC (such as the TVP7001) with 0-dB gain and the monitor output path drives an output line with 6-dB gain along with horizontal (H) and vertical (V) sync signals. The versatility of the THS7327 allows virtually any video signal to be utilized. This includes standard-definition (SD), enhanced-definition (ED), and high-definition (HD) Y'P'$_B$P'$_R$ (sometimes labeled Y'U'V' or incorrectly labeled Y'C'$_B$C'$_R$) signals, S-Video Y'/C' signals, and the composite video baseband signal (CVBS) of a SD video system. These signals can also be R'G'B' (or G'B'R') or other variations on the placement of the sync signals commonly called R'G'sB' (sync on Green) or R'sG'sB's (sync on all signals). Additionally, the THS7327 handles the digital H and V sync signals with the noise immunity enhancement of a schmitt trigger. This schmitt trigger defaults to 1.45 V, but can be set externally to be anywhere form 0.9 V to 2.0 V for added flexibility.

Simple control of the I^{2}C configures the THS7327 for any configuration conceivable. For example, the THS7327 can be configured to have Channel 1 Input connected to input A while Channels 2 and 3 could be connected to input B. See the multiple application notes sections explaining the I^{2}C interface later in this document on how to configure these options.

Note that the Y' term is used for the luma channels throughout this document rather than the more common luminance (Y) term. This is to account for the true definition of luminance as stipulated by the CIE - International Commission on Illumination. Video departs from true luminance since a nonlinear term, gamma, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then used to mathematically create luma (Y'). Thus, true luminance (Y) is not maintained and hence, the difference in terminology.

This rationale is also used for the chroma (C') term. Chroma is derived from the non-linear R'G'B' terms and thus it is non-linear. True chrominance (C) is derived from linear RGB and hence the difference between chroma (C') and chrominance (C). The color difference signals (P'$_B$ / P'$_R$ / U' / V') are also referenced this way to denote the non-linear (gamma corrected) signals.

R'G'B' (commonly mislabeled RGB) is also called G'B'R' (again commonly mislabeled as GBR) in professional video systems. The SMPTE component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This is consistent with the Y'P'$_B$P'$_R$ nomenclature. Because the luma channel (Y') carries the sync information and the green channel (G') also carries the sync information, it makes logical sense that G' be placed first in the system. Since the blue color difference channel (P'_B) is next and the red color difference channel (P'_R) is last, then it also makes logical sense to place the B' signal on the second channel and the R' signal on the third channel respectfully. Thus, hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems, sync is embedded on all three channels, but may not always be the case in all systems.

I^2C INTERFACE NOTES

The I^2C interface is used to access the internal registers of the THS7327. I^2C is a two-wire serial interface developed by Philips Semiconductor (see the I^2C-Bus Specification, Version 2.1, January 2000). The THS7327 was designed to comply with version 2.1 specifications. The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C-compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device. The THS7327 works as a slave and supports the standard mode transfer (100 kbps) and fast mode transfer (400 kbps) as defined in the I^2C-Bus specification. The THS7327 has been tested to be fully functional with the high-speed mode (3.4 Mbps) but it is **not** specified at this time.

The basic I^2C start and stop access cycles are shown in Figure 9.

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

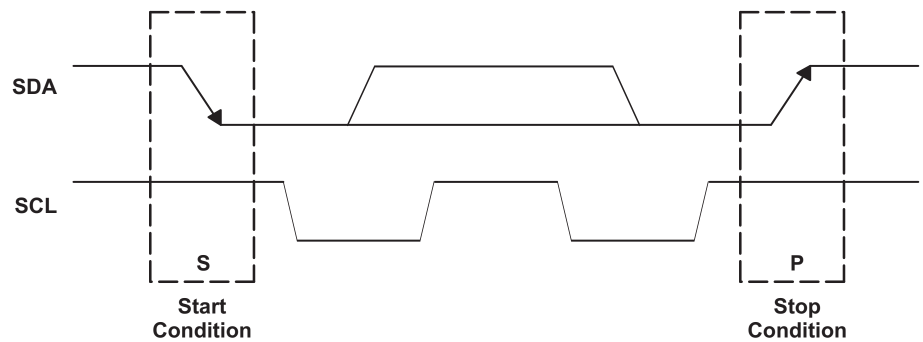


Figure 9. I^2C Start and Stop Conditions

GENERAL I^2C PROTOCOL

- The *master* initiates data transfer by generating a *start condition*. The *start condition* exist when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 9. All I^2C-compatible devices should recognize a *start condition*.
- The master then generates the SCL pulses and transmits the 7-bit address and the *read/write direction bit* R/W on the SDA line. During all transmissions, the master ensures that data are *valid*. A *valid data* condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 10). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see Figure 11) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.
- The master generates further SCL cycles to either *transmit* data to the slave (R/W bit 1) or *receive* data from the slave (R/W bit 0). In either case, the *receiver* needs to acknowledge the data sent by the *transmitter*. So, an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (see Figure 12).

- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see Figure 9). This releases the bus and stops the communication link with the addressed slave. All I²C-compatible devices must recognize the *stop condition*. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a *start condition* followed by a matching address.

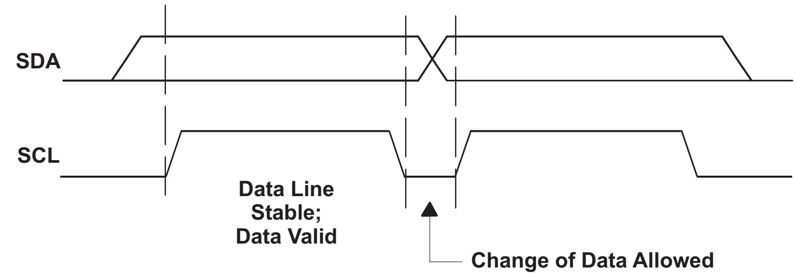


Figure 10. I²C Bit Transfer

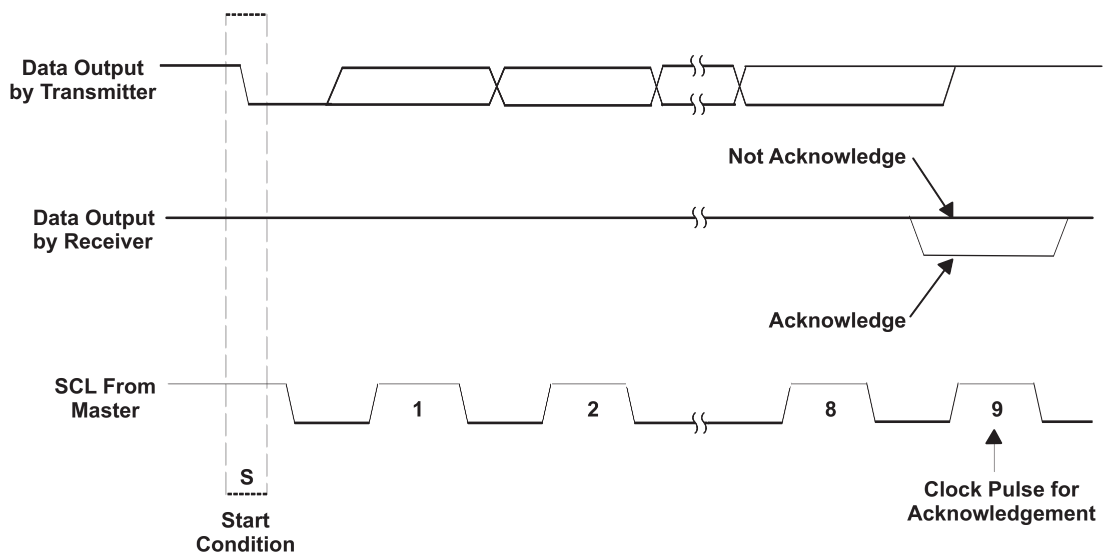


Figure 11. I²C Acknowledge

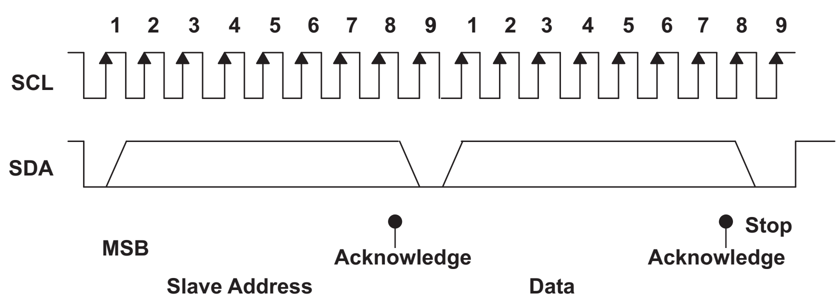


Figure 12. I²C Address and Data Cycles

During a write cycle, the transmitting device must not drive the SDA signal line during the acknowledge cycle, so that the receiving device may drive the SDA signal low. After each byte transfer following the address byte, the receiving device pulls the SDA line low for one SCL clock cycle. A stop condition is initiated by the transmitting device after the last byte is transferred. An example of a write cycle can be found in Figure 13 and Figure 14. Note that the THS7327 does not allow multiple write transfers to occur. See the *Example— Writing to the THS7327* section for more information.

During a read cycle, the slave receiver acknowledges the initial address byte if it decodes the address as its address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not acknowledge (A) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop (P) condition. This sequence terminates a read cycle as shown in Figure 15 and Figure 16. Note that the THS7327 does not allow multiple read transfers to occur. See the *Example— Reading from the THS7327* section for more information.

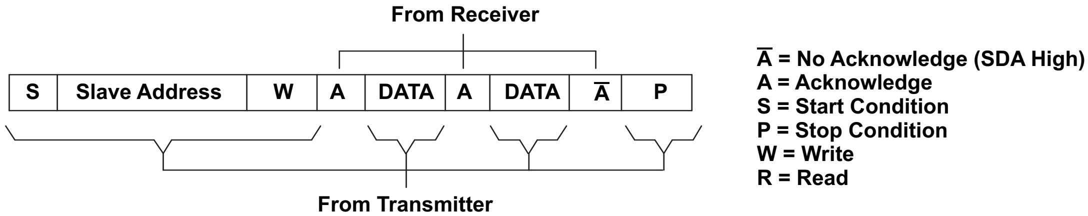


Figure 13. I²C Write Cycle

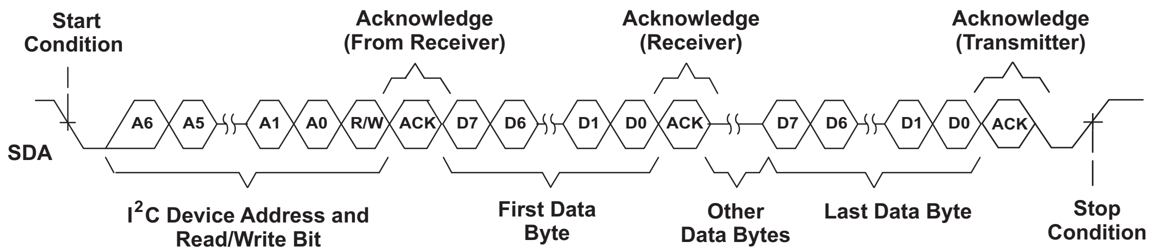


Figure 14. Multiple Byte Write Transfer

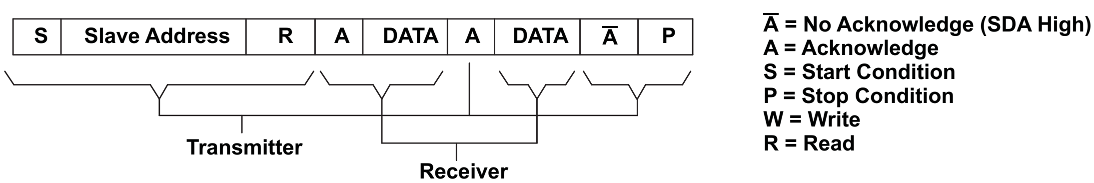


Figure 15. I²C Read Cycle

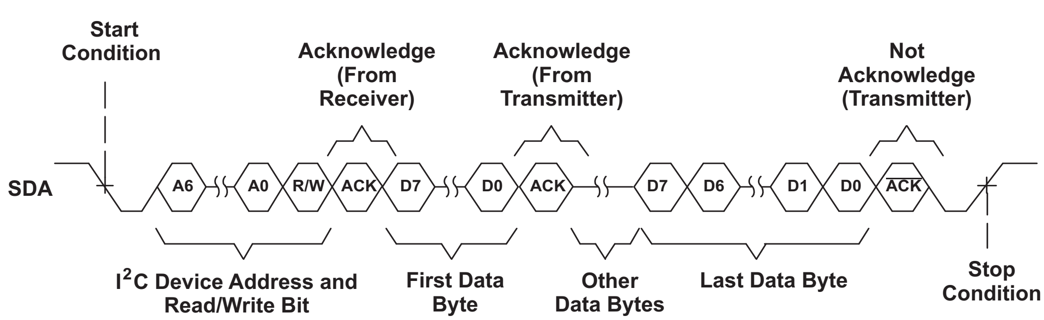


Figure 16. Multiple Byte Read Transfer

Slave Address

Both the SDA and the SCL must be connected to a positive supply voltage via a pull-up resistor. These resistors should comply with the I^2C specification that ranges from 2 kΩ to 19 kΩ. When the bus is free, both lines are high. The address byte is the first byte received following the START condition from the master device. The first five bits (MSBs) of the address are factory preset to 01011. The next two bits of the THS7327 address are controlled by the logic levels appearing on the I^2C-A1 and I^2C-A0 pins. The I^2C-A1 and I^2C-A0 address inputs can be connected to V_{S+} for logic 1, GND for logic 0, or it can be actively driven by TTL/CMOS logic levels. The device address is set by the state of these pins and is not latched. Thus, a dynamic address control system could be used to incorporate several devices on the same system. Up to four THS7327 devices can be connected to the same I^2C Bus without requiring additional *glue* logic. Table 1 lists the possible addresses for the THS7327.

Table 1. THS7327 Slave Addresses

FIXED ADDRESS					SELECTABLE WITH ADDRESS PINS		READ/WRITE BIT
Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2 (A1)	Bit 1 (A0)	Bit 0
0	1	0	1	1	0	0	0
0	1	0	1	1	0	0	1
0	1	0	1	1	0	1	0
0	1	0	1	1	0	1	1
0	1	0	1	1	1	0	0
0	1	0	1	1	1	0	1
0	1	0	1	1	1	1	0
0	1	0	1	1	1	1	1

Channel Selection Register Description (Subaddress) and Power-Up Condition (PUC) Pin

The THS7327 operates using only a single byte transfer protocol similar to Figure 13 and Figure 15. The internal subaddress registers and the functionality of each are found in Table 2. When writing to the device, it is required to send one byte of data to the corresponding internal subaddress. If control of all three channels is desired, then the master has to cycle through all the subaddresses (channels) one at a time, see the *Example— Writing to the THS7327* section for the proper procedure of writing to the THS7327.

During a read cycle, the THS7327 sends the data in its selected subaddress (or channel) in a single transfer to the master device requesting the information. See the *Example— Reading from the THS7327* section for the proper procedure on reading from the THS7327.

On power up, the THS7327 registers are dictated by the power-up control (PUC) pin. If the PUC pin is tied to GND, the THS7327 will power-up in a fully disabled state. If the PUC pin is tied to V_{DD}, upon power-up the THS7327 will be configured with HV sync on, buffer path disabled, monitor path Enabled, and input bias mode set to AC-Bias on all input channels. It remains in this state until a valid write sequence is made to the THS7327. A total of 12 bytes of data completely configures all channels of the THS7327. As such, configuring the THS7327 is accomplished quickly and easily.

Table 2. THS7327 Channel Selection Register Bit Assignments

REGISTER NAME	BIT ADDRESS ($b_7b_6b_5....b_0$)
Channel 1	0000 0001
Channel 2	0000 0010
Channel 3	0000 0011
Channel H and V Sync and Disable Controls	0000 0100

Channel Register Bit Descriptions

Each bit of the subaddress (channel selection) control register as described above allows the user to individually control the functionality of the THS7327. The benefit of this process allows the user to control the functionality of each channel independent of the other channels. The bit description is decoded in Table 3 and Table 4.

Table 3. THS7327 Channel Register (Ch. 1 thru 3) Bit Decoder Table – Use with Register Bit Codes (0000 0001), (0000 0010), and (0000 0011)

BIT	FUNCTION	BIT VALUE(S)	RESULT
(MSB) 7	Sync-Tip Clamp Filter	0	500-kHz Filter on the STC circuit
		1	5-MHz Filter on the STC circuit
6, 5, 4, 3	MUX Selection + Low Pass Filter	0 0 0 0	MUX Input A; LPF = 9-MHz
		0 0 0 1	MUX Input A; LPF = 16-MHz
		0 0 1 0	MUX Input A; LPF = 35-MHz
		0 0 1 1	MUX Input A; LPF = 75-MHz
		0 1 0 0	MUX Input A; LPF = Bypass
		0 1 0 1	MUX Input B; LPF = 9-MHz
		0 1 1 0	MUX Input B; LPF = 16-MHz
		0 1 1 1	MUX Input B; LPF = 35-MHz
		1 0 0 0	MUX Input B; LPF = 75-MHz
		1 0 0 1	MUX Input B; LPF = Bypass
		1 0 1 0	Reserved—Do Not Care
		1 0 1 1	Reserved—Do Not Care
		1 1 0 0	Reserved—Do Not Care
		1 1 0 1	Reserved—Do Not Care
		1 1 1 0	Reserved—Do Not Care
		1 1 1 1	Reserved—Do Not Care
2, 1, 0 (LSB)	Input Mode + Operation	0 0 0	Disables both Monitor and Buffer Paths of the Respective Channel/Register
		0 0 1	Channel Mute
		0 1 0	Input Mode = DC
		0 1 1	Input Mode = DC + Shift
		1 0 0	Input Mode = AC-Bias
		1 0 1	Input Mode = AC-STC with Low Bias
		1 1 0	Input Mode = AC-STC with Mid Bias
		1 1 1	Input Mode = AC-STC with High Bias

Bits 7 (MSB) – Controls the sync-tip clamp filter. Useful only when AC-STC input mode is selected.

Bit 6, 5, 4, 3 – Selects the Input MUX channel and the Buffer low pass filter

Bits 2, 1, and 0 (LSB) – Configures the channel mode and operation. See Table 4, bits 6 and 5 for more information with respect to enable/disable state

Table 4. THS7327 Channel Register (HV Sync Channel + ADC State) Bit Decoder Table – Use in Conjunction With Register Bit Code (0000 0100)

BIT	FUNCTION	BIT VALUE(S)	RESULT
(MSB) 7	Reserved – Do Not Care	X	Reserved—Do Not Care
6	Monitor Pass-Thru Path Disable Mode (Use in Conjunction with Table 3)	0	Disables All Monitor Channels regardless of Bits 2:0 of Registers 1-3
		1	Enable Monitor Channels Functions Dictated by each Programmed Register Code
5	Buffer Path Disable Mode (Use in Conjunction with Table 3)	0	Disable All Buffer Channels regardless of Bits 2:0 of Registers 1-3
		1	Enable Buffer Channel Functions Dictated by each Programmed Register Code
4, 3	Vertical Sync Channel MUX Selection	0 0	MUX Input A
		0 1	MUX Input B
		1 0	Reserved—Do Not Care
		1 1	Reserved—Do Not Care
2, 1	Horizontal Sync Channel MUX Selection	0 0	MUX Input A
		0 1	MUX Input B
		1 0	Reserved—Do Not Care
		1 1	Reserved—Do Not Care
0 (LSB)	HV Sync Paths Disable Mode	0	Disable H and V Sync Channels
		1	Enable H and V Sync Channels

Bit (MSB) 7 – Reserved – Do Not Care

Bit 6 – Master Monitor Path Disable. Disables All Monitor Channels regardless of what is programmed into each Register Channel (1 to 3).

Bit 5 – Master Buffer Path Disable. Disables All Buffer Channels regardless of what is programmed into each Register Channel (1 to 3).

Bits 4, 3 – Selects the Input MUX channel for the Vertical Sync

Bits 2, 1 – Selects the Input MUX channel for the Horizontal Sync

Bit 0 (LSB) – Enables or Disables the H and V Sync Channels.

EXAMPLE – WRITING TO THE THS7327

The proper way to write to the THS7327 is illustrated as follows:

An I^2C master initiates a write operation to the THS7327 by generating a start condition (S) followed by the THS7327 I^2C address (as shown below), in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the THS7327, the master presents the subaddress (channel) it wants to write consisting of one byte of data, MSB first. The THS7327 acknowledges the byte after completion of the transfer. Finally the master presents the data it wants to write to the register (channel) and the THS7327 acknowledges the byte. The I^2C master then terminates the write operation by generating a stop condition (P). Note that the THS7327 does not support multi-byte transfers. To write to all three channels – or registers – this procedure must be repeated for each register one series at a time (that is, repeat steps 1 through 8 for each channel).

Step 1	0
I^2C Start (Master)	S

Step 2	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	0

Where each X Logic state is defined by I^2C-A1 and I^2C-A0 pins being tied to either V_{S+} or GND.

Step 3	9
I^2C Acknowledge (Slave)	A

Step 4	7	6	5	4	3	2	1	0
I^2C Write Channel Address (Master)	0	0	0	0	0	Addr	Addr	Addr

Where Addr is determined by the values shown in Table 2.

Step 5	9
I^2C Acknowledge (Slave)	A

Step 6	7	6	5	4	3	2	1	0
I^2C Write Data (Master)	Data	Data	Data	Data	Data	Data	Data	Data

Where Data is determined by the values shown in Table 3 or Table 4.

Step 7	9
I^2C Acknowledge (Slave)	A

Step 8	0
I^2C Stop (Master)	P

EXAMPLE – READING FROM THE THS7327

The read operation consists of two phases. The first phase is the address phase. In this phase, an I^2C master initiates a write operation to the THS7327 by generating a start condition (S) followed by the THS7327 I^2C address, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledges from the THS7327, the master presents the subaddress (channel) of the register it wants to read. After the cycle is acknowledged (A), the master terminates the cycle immediately by generating a stop condition (P).

The second phase is the data phase. In this phase, an I^2C master initiates a read operation to the THS7327 by generating a start condition followed by the THS7327 I^2C address (as shown below for a read operation), in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the THS7327, the I^2C master receives one byte of data from the THS7327. After the data byte has been transferred from the THS7327 to the master, the master generates a not acknowledge followed by a stop. Similar to the Write function, to read all channels Steps 1 through 11 must be repeated for each and every channel desired.

THS7327 Read Phase 1:

Step 1	0
I^2C Start (Master)	S

Step 2	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	0

Where each X Logic state is defined by I^2C-A1 and I^2C-A0 pins being tied to either V_{S+} or GND.

Step 3	9
I^2C Acknowledge (Slave)	A

Step 4	7	6	5	4	3	2	1	0
I^2C Read Channel Address (Master)	0	0	0	0	0	Addr	Addr	Addr

Where Addr is determined by the values shown in Table 2.

Step 5	9
I^2C Acknowledge (Slave)	A

Step 6	0
I^2C Start (Master)	P

THS7327 Read Phase 2:

Step 7	0
I^2C Start (Master)	S

Step 8	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	1

Where each X Logic state is defined by I^2C-A1 and I^2C-A0 pins being tied to either V_{S+} or GND.

Step 9	9
I^2C Acknowledge (Slave)	A

Step 10	7	6	5	4	3	2	1	0
I^2C Read Data (Slave)	Data	Data	Data	Data	Data	Data	Data	Data

Where Data is determined by the Logic values contained in the Channel Register.

Step 11	9
I^2C Not-Acknowledge (Master)	$\overline{A}$

Step 12	0
I^2C Stop (Master)	P

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2008) to Revision C **Page**

- Changed first DC Performance, *Bias output voltage, Buffer output* parameter row +25°C, 0°C to +70°C, and –40°C to +85°C specifications in 3.3-V Electrical Characteristics table 5
- Changed first DC Performance, *Bias output voltage, Monitor output* parameter row +25°C, 0°C to +70°C, and –40°C to +85°C specifications in 3.3-V Electrical Characteristics table 5
- Changed DC Performance, *Sync tip clamp voltage, Buffer output* parameter +25°C, 0°C to +70°C, and –40°C to +85°C specifications in 3.3-V Electrical Characteristics table 5
- Changed first DC Performance, *Bias output voltage, Buffer output* parameter row +25°C, 0°C to +70°C, and –40°C to +85°C specifications in 5-V Electrical Characteristics table 8
- Changed first DC Performance, *Bias output voltage, Monitor output* parameter row +25°C, 0°C to +70°C, and –40°C to +85°C specifications in 5-V Electrical Characteristics table 8
- Changed DC Performance, *Sync tip clamp output voltage, Buffer output* parameter +25°C, 0°C to +70°C, and –40°C to +85°C specifications in 5-V Electrical Characteristics table 8

Changes from Revision A (February 2007) to Revision B **Page**

- Changed the V_{SS} and V_I rows of the *Absolute Maximum Ratings* table 2
- Changed the *Recommended Operating Conditions* table 3
- Added *Digital Characteristics* section to *3.3V Electrical Characteristics* table 4
- Added *Digital Characteristics* section to *5 V Electrical Characteristics* table 7
- Changed footnote 1 of the *Timing Requirements for I^2C Interface* table 10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS7327PHP	ACTIVE	HTQFP	PHP	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	THS7327	Samples
THS7327PHPR	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	THS7327	Samples
THS7327PHPRG4	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	THS7327	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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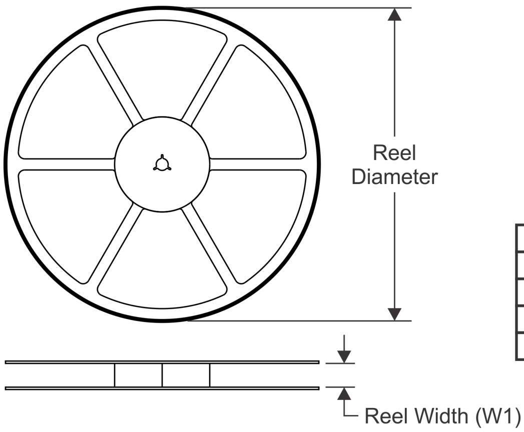
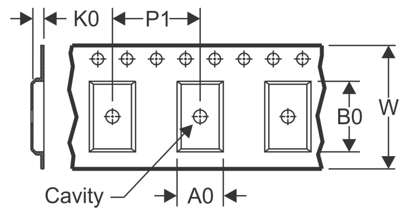
TAPE AND REEL INFORMATION

REEL DIMENSIONS

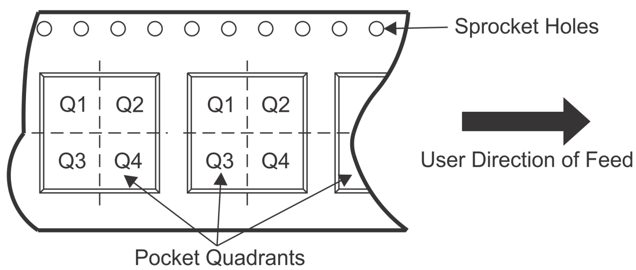


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

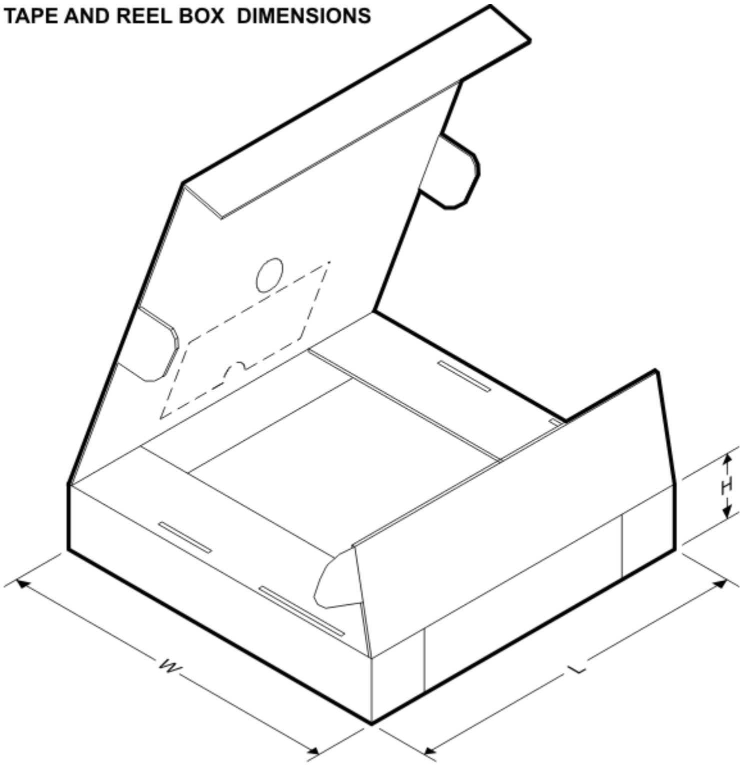
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7327PHPR	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7327PHPR	HTQFP	PHP	48	1000	350.0	350.0	43.0

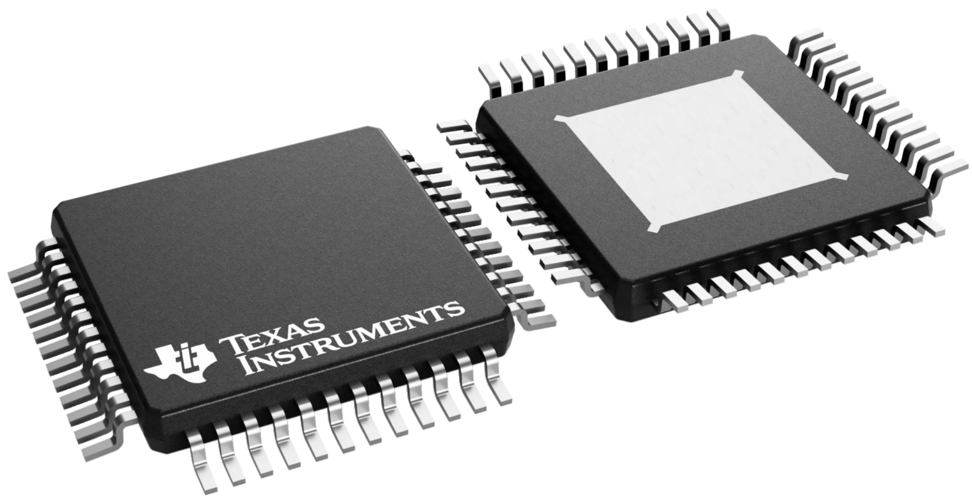
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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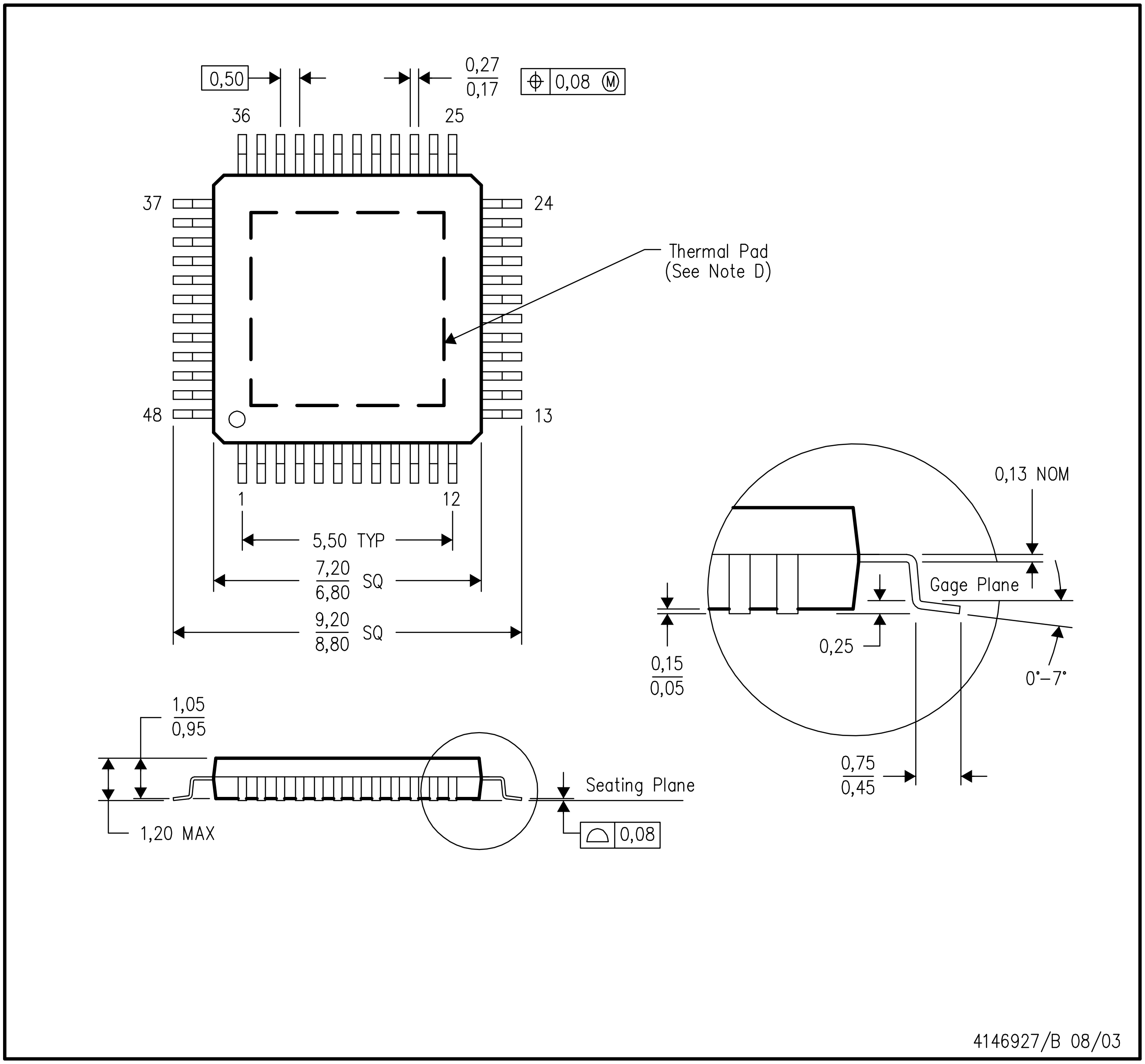
PHP (S-PQFP-G48)　　PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MS-026

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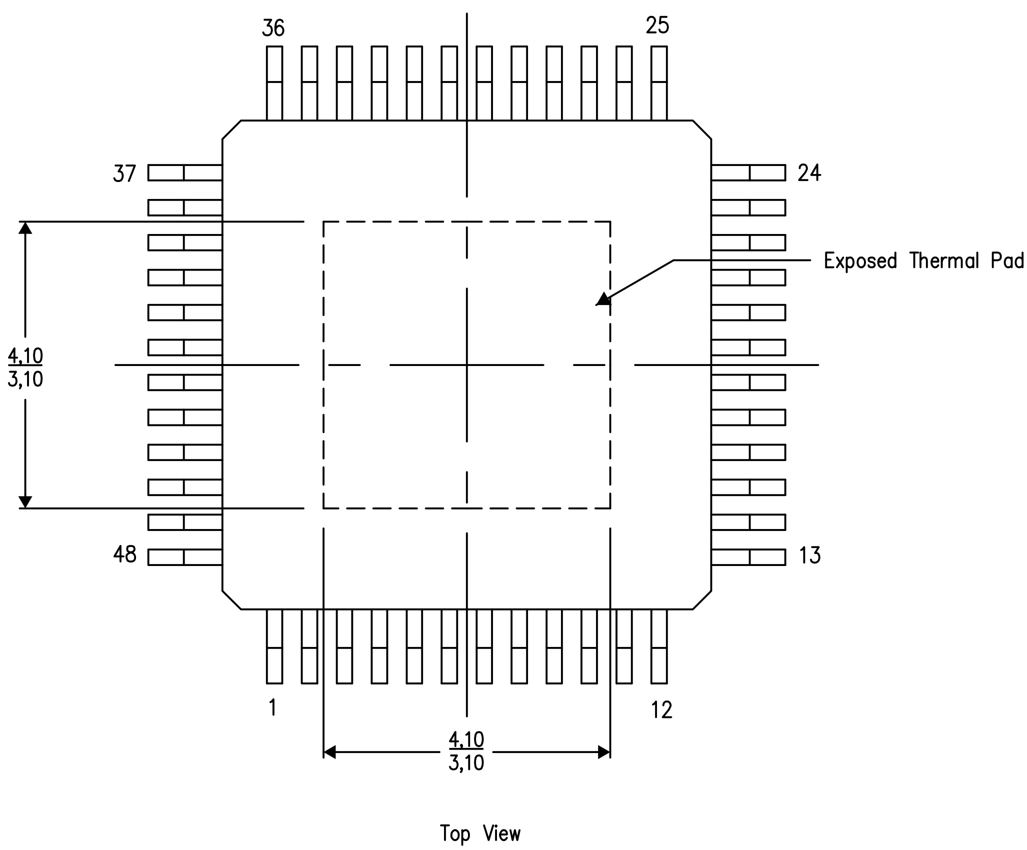
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206329–3/P 03/15

NOTE: A. All linear dimensions are in millimeters

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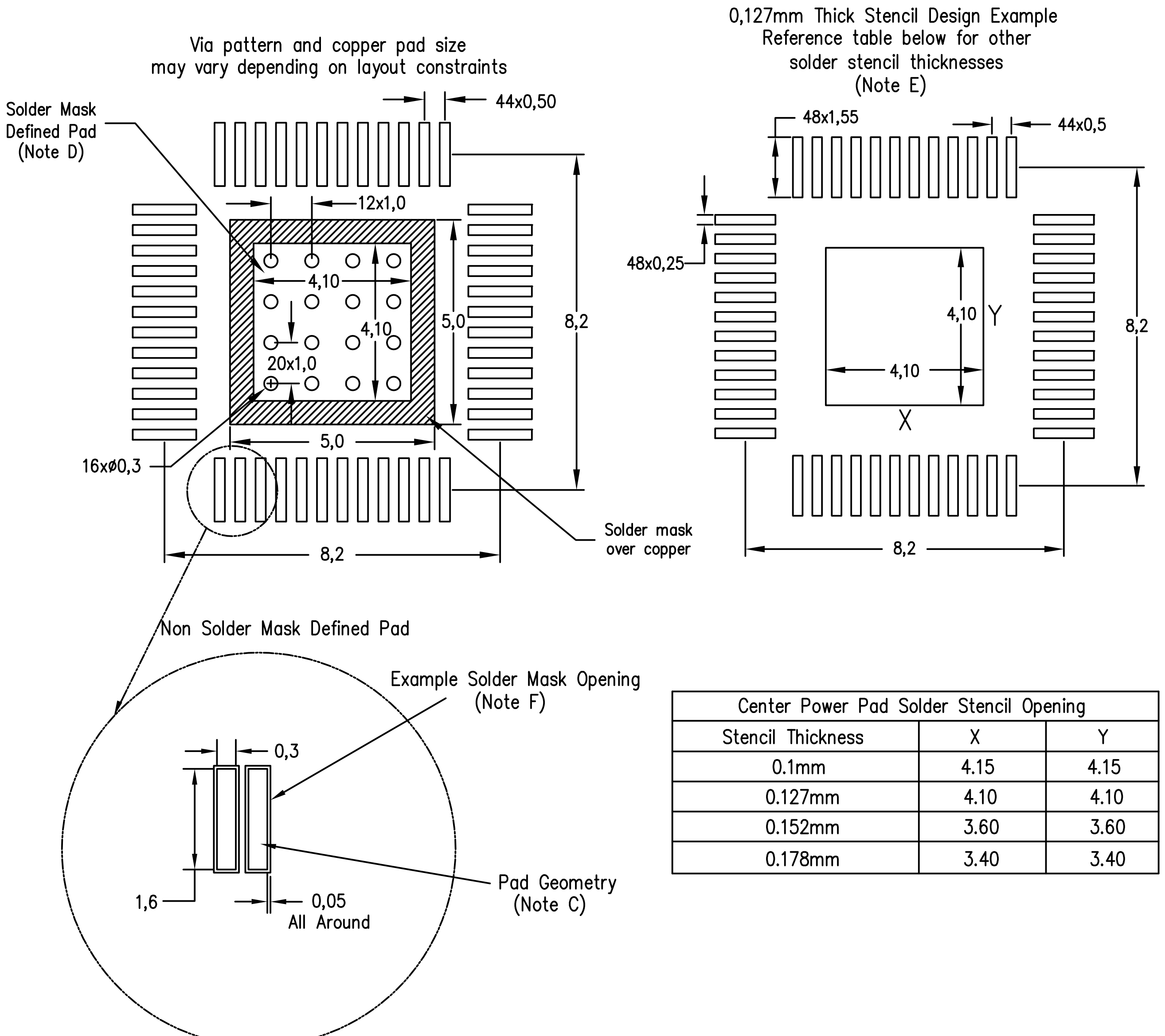
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.15	4.15
0.127mm	4.10	4.10
0.152mm	3.60	3.60
0.178mm	3.40	3.40

4207626–3/I 10/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.