

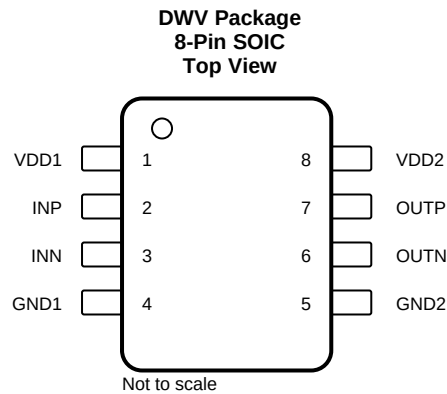
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4 Revision History

DATE	REVISION	NOTES
October 2018	*	Initial release.

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VDD1	—	High-side power supply, 3.0 V to 5.5 V. See the Power Supply Recommendations section for power-supply decoupling recommendations.
2	INP	I	Noninverting analog input
3	INN	I	Inverting analog input
4	GND1	—	High-side analog ground
5	GND2	—	Low-side analog ground
6	OUTN	O	Inverting analog output
7	OUTP	O	Noninverting analog output
8	VDD2	—	Low-side power supply, 3.0 V to 5.5 V. See the Power Supply Recommendations section for power-supply decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

see ⁽¹⁾

		MIN	MAX	UNIT
Power-supply voltage	VDD1 to GND1	−0.3	6.5	V
	VDD2 to GND2	−0.3	6.5	
Input voltage	INP, INN	GND1 − 6	VDD1 + 0.5	V
Output voltage	OUTP, OUTN	GND2 − 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	−10	10	mA
Temperature	Junction, T _J		150	°C
	Storage, T _{stg}	−65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ , HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD Classification Level C6	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-side power supply	VDD1 to GND1	3.0	5	5.5	V
	Low-side power supply	VDD2 to GND2	3.0	3.3	5.5	V
ANALOG INPUTS						
V _{Clipping}	Differential input voltage before clipping output	V _{IN} = V _{INP} − V _{INN}		±64		mV
V _{FSR}	Specified linear differential input full-scale	V _{IN} = V _{INP} − V _{INN}	−50		50	mV
	Absolute common-mode input voltage ⁽¹⁾	(V _{INP} + V _{INN}) / 2 to GND1	−2		VDD1	V
V _{CM}	Operating common-mode input voltage	(V _{INP} + V _{INN}) / 2 to GND1	−0.032		VDD1 − 2.2	V
TEMPERATURE RANGE						
T _A	Specified ambient temperature		−40		125	°C

- (1) Steady-state voltage supported by the device in case of a system failure. See the specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the [Absolute Maximum Ratings](#) table.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		AMC1302-Q1	UNIT
		DWV (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	98.45	mW
		VDD1 = VDD2 = 3.6 V	56.52	
P_{D1}	Maximum power dissipation (high-side supply)	VDD1 = 5.5 V	53.90	mW
		VDD1 = 3.6 V	30.60	
P_{D2}	Maximum power dissipation (low-side supply)	VDD2 = 5.5 V	44.55	mW
		VDD2 = 3.6 V	25.92	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance ⁽¹⁾	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage ⁽¹⁾	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2 × 0.0105 mm)	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	
DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01 ⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2121	V _{PK}
V _{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave); see Figure 4	1500	V _{RMS}
		At DC voltage	2121	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification test)	7071	V _{PK}
		V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production test)	8485	
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 60065, 1.2/50-μs waveform, V _{TEST} = 1.6 × V _{IOSM} = 12800 V _{PK} (qualification)	8000	V _{PK}
q _{pd}	Apparent charge ⁽⁴⁾	Method a, after input/output safety test subgroup 2 / 3, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.2 × V _{IORM} = 2545 V _{PK} , t _m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.6 × V _{IORM} = 3394 V _{PK} , t _m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s, V _{pd(m)} = 1.875 × V _{IORM} = 3977 V _{PK} , t _m = 1 s	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.5 V _{PP} at 1 MHz	~1	pF
R _{IO}	Insulation resistance, input to output ⁽⁵⁾	V _{IO} = 500 V at T _A = 25°C	> 10 ¹²	Ω
		V _{IO} = 500 V at 100°C ≤ T _A ≤ 125°C	> 10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	> 10 ⁹	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V _{ISO}	Withstand isolation voltage	V _{TEST} = V _{ISO} = 5000 V _{RMS} or 7071 V _{DC} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} = 6000 V _{RMS} , t = 1 s (100% production test)	5000	V _{RMS}

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current			266	mA
				406	
P_S	Safety input, output, or total power ⁽¹⁾			1463	mW
T_S	Maximum safety temperature			150	°C

- (1) The maximum safety temperature, T_S , has the same value as the maximum junction temperature, T_J , specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S . These limits vary with the ambient temperature, T_A .

The junction-to-air thermal resistance, $R_{\theta JA}$, in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.

$P_S = I_S \times VDD1_{max} + I_S \times VDD2_{max}$, where $VDD1_{max}$ is the maximum high-side voltage and $VDD2_{max}$ is the maximum low-side supply voltage.

6.9 Electrical Characteristics

minimum and maximum specifications apply from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $VDD1 = 3.0\text{ V}$ to 5.5 V , $VDD2 = 3.0\text{ V}$ to 5.5 V , $INP = -50\text{ mV}$ to $+50\text{ mV}$, and $INN = GND1 = 0\text{ V}$; typical specifications are at $T_A = 25^\circ\text{C}$, $VDD1 = 5\text{ V}$, and $VDD2 = 3.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V _{CMov}	Common-mode overvoltage detection level	(V _{INP} + V _{INN}) / 2 to GND1	VDD1 – 2.1			V
	Hysteresis of common-mode overvoltage detection level		60			mV
V _{OS}	Input offset voltage ⁽¹⁾	initial, at T _A = 25°C, V _{INP} = V _{INN} = GND1	–100	±10	100	μV
TCV _{OS}	Input offset drift ⁽¹⁾		–0.8	±0.15	0.8	μV/°C
CMRR	Common-mode rejection ratio	f _{IN} = 0 Hz, V _{CM min} ≤ V _{CM} ≤ V _{CM max}	–100			dB
		f _{IN} = 10 kHz, V _{CM min} ≤ V _{CM} ≤ V _{CM max}	–98			
C _{IN}	Single-ended input capacitance ⁽²⁾	INN = GND1, f _{IN} = 300 kHz	4			pF
C _{IND}	Differential input capacitance ⁽²⁾	f _{IN} = 300 kHz	2			pF
R _{IN}	Single-ended input resistance ⁽²⁾	INN = GND1	4.75			kΩ
R _{IND}	Differential input resistance ⁽²⁾		4.9			kΩ
I _{IB}	Input bias current	INP = INN = GND1; I _{IB} = (I _{IBP} + I _{IBN}) / 2	–48.5	–36	–28.5	μA
TCI _{IB}	Input bias current drift		±1.5			nA/°C
I _{IO}	Input offset current	I _{IO} = I _{IBP} – I _{IBN}	±10			nA

- (1) The typical value includes one sigma statistical variation.

- (2) See [Figure 47](#).

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Electrical Characteristics (continued)

minimum and maximum specifications apply from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD1} = 3.0\text{ V}$ to 5.5 V , $V_{DD2} = 3.0\text{ V}$ to 5.5 V , $\text{INP} = -50\text{ mV}$ to $+50\text{ mV}$, and $\text{INN} = \text{GND1} = 0\text{ V}$; typical specifications are at $T_A = 25^{\circ}\text{C}$, $V_{DD1} = 5\text{ V}$, and $V_{DD2} = 3.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
ANALOG OUTPUT							
	Nominal gain		41				
E _G	Gain error ⁽¹⁾	initial, at T _A = 25°C	-0.3%	±0.05%	0.3%		
TCE _G	Gain error drift ⁽¹⁾		-50	±15	50	ppm/°C	
	Nonlinearity ⁽¹⁾		-0.03%	±0.01%	0.03%		
	Nonlinearity drift		±1			ppm/°C	
THD	Total harmonic distortion	V _{IN} = 100 mV _{PP} , f _{IN} = 10 kHz, BW = 100 kHz	-85			dB	
	Output noise	V _{INP} = V _{INN} = GND1, BW = 100 kHz	260			μV _{RMS}	
SNR	Signal-to-noise ratio	V _{IN} = 100 mV _{PP} , f _{IN} = 1 kHz, BW = 10 kHz	80	84		dB	
		V _{IN} = 100 mV _{PP} , f _{IN} = 10 kHz, BW = 100 kHz	70				
PSRR	Power-supply rejection ratio	PSRR vs VDD1, at DC	-104			dB	
		PSRR vs VDD1, 100-mV and 10-kHz ripple	-108				
		PSRR vs VDD2, at DC	-104				
		PSRR vs VDD2, 100-mV and 10-kHz ripple	-87				
V _{CMout}	Common-mode output voltage		1.39	1.44	1.49	V	
V _{FAILSAFE}	Failsafe differential output voltage	V _{CM} > V _{CMov} or VDD1 ≤ VDD1 _{UV}	-2.6			-2.5	V
BW	Output bandwidth		220	280		kHz	
R _{OUT}	Output resistance	On OUTP or OUTN	< 0.2			Ω	
	Output short-circuit current		±14			mA	
CMTI	Common-mode transient immunity	GND1 – GND2 = 1 kV	55	80		kV/μs	
POWER SUPPLY							
VDD1 _{POR}	VDD1 power on reset threshold voltage	VDD1 falling	1.75	2.15	2.7	V	
IDD1	High-side supply current	3.0 V ≤ VDD1 ≤ 3.6 V	6.2			mA	
		4.5 V ≤ VDD1 ≤ 5.5 V	7.2				
IDD2	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V	5.3			mA	
		4.5 V ≤ VDD2 ≤ 5.5 V	5.9				

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time of OUTP, OUTN		1.3		μs
t_f	Fall time of OUTP, OUTN		1.3		μs
	INP, INN to OUTP, OUTN signal delay (50% – 10%)		1.0	1.5	μs
	INP, INN to OUTP, OUTN signal delay (50% – 50%)		1.6	2.1	μs
	INP, INN to OUTP, OUTN signal delay (50% – 90%)		2.5	3.0	μs
t_{AS}	Analog startup time		500		μs

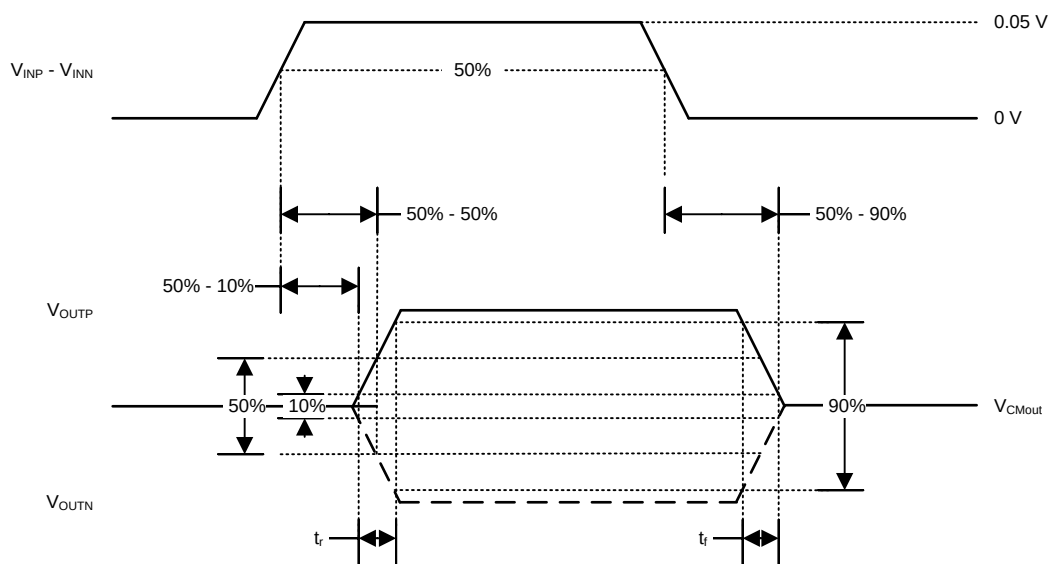


Figure 1. Rise, Fall, and Delay Time Waveforms

6.11 Insulation Characteristics Curves

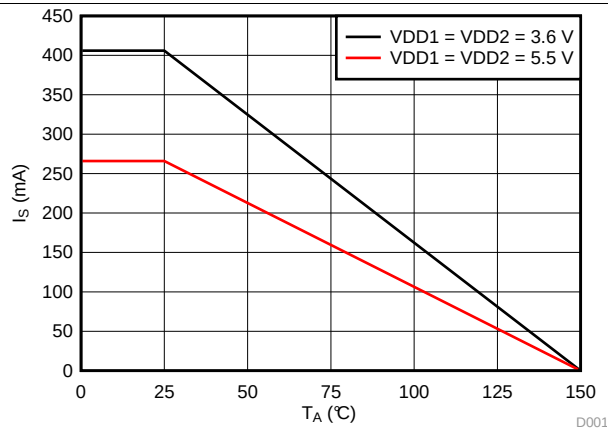


Figure 2. Thermal Derating Curve for Safety-Limiting Current per VDE

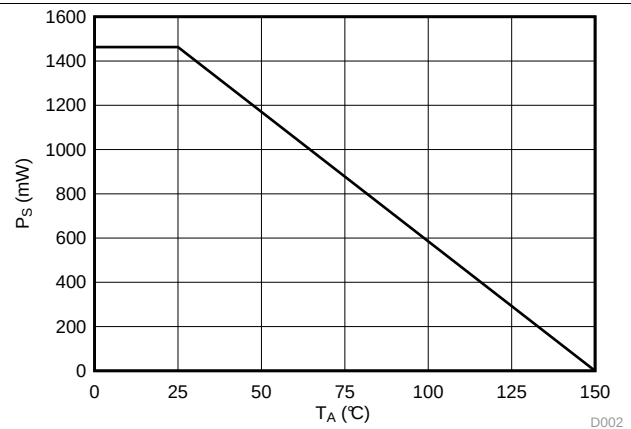
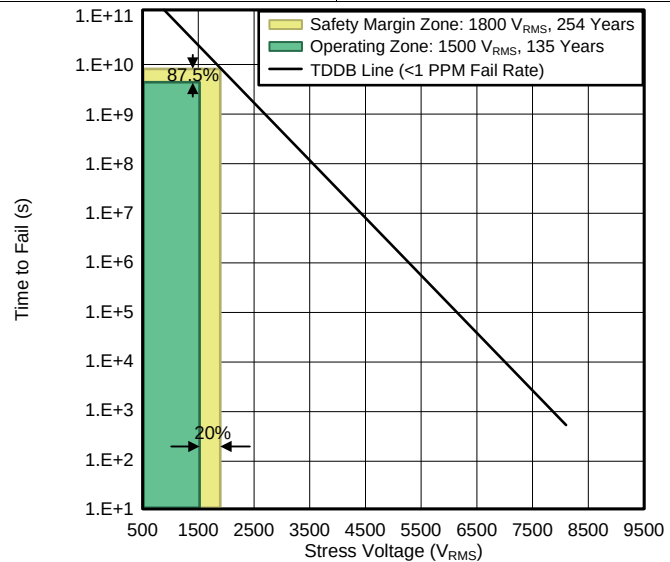


Figure 3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz,
isolation working voltage = 1500 V_{RMS} , operating lifetime = 135 years

Figure 4. Reinforced Isolation Capacitor Lifetime Projection

6.12 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.3\text{ V}$, $V_{INP} = -50\text{ mV}$ to 50 mV , $V_{INN} = \text{GND1}$, and $f_{IN} = 10\text{ kHz}$ (unless otherwise noted)

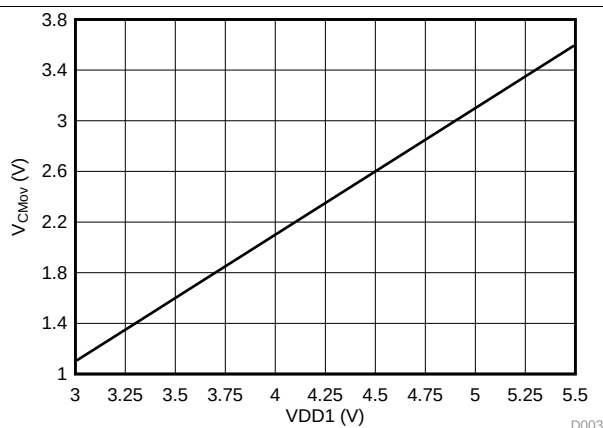


Figure 5. Common-Mode Overvoltage Detection Level vs High-Side Supply Voltage

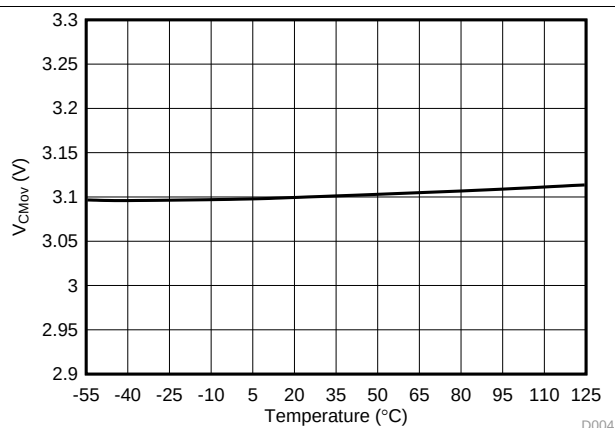


Figure 6. Common-Mode Overvoltage Detection Level vs Temperature

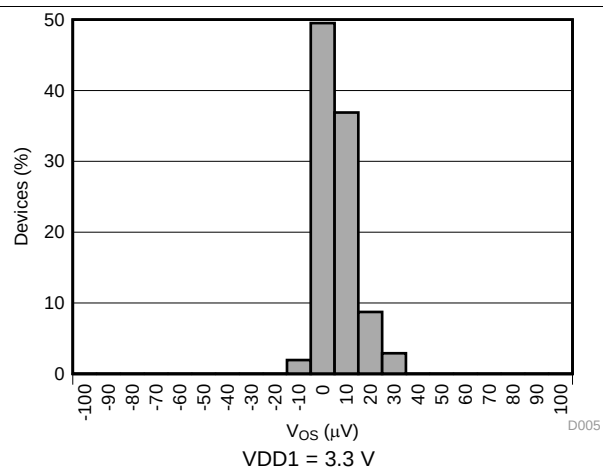


Figure 7. Input Offset Voltage Histogram

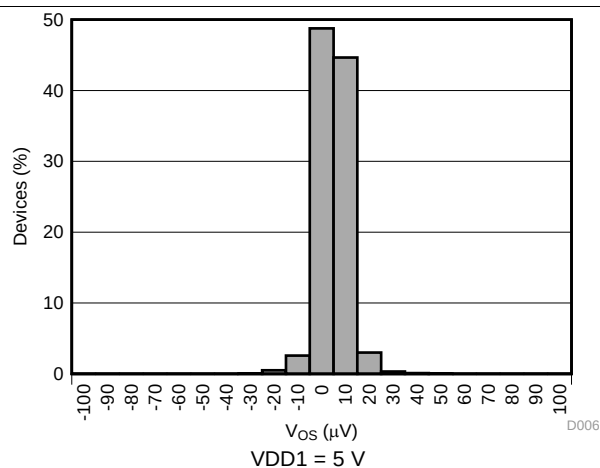


Figure 8. Input Offset Voltage Histogram

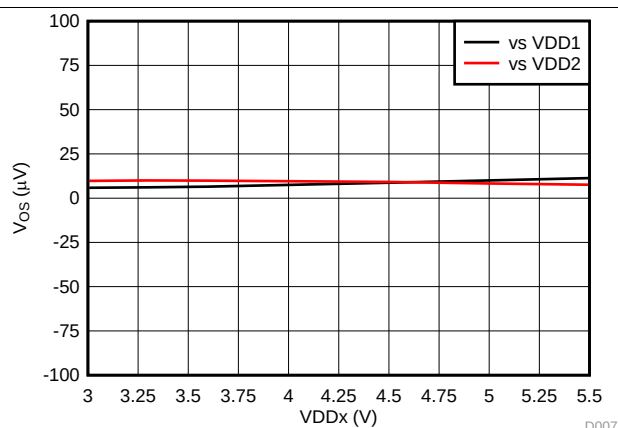


Figure 9. Input Offset Voltage vs Supply Voltage

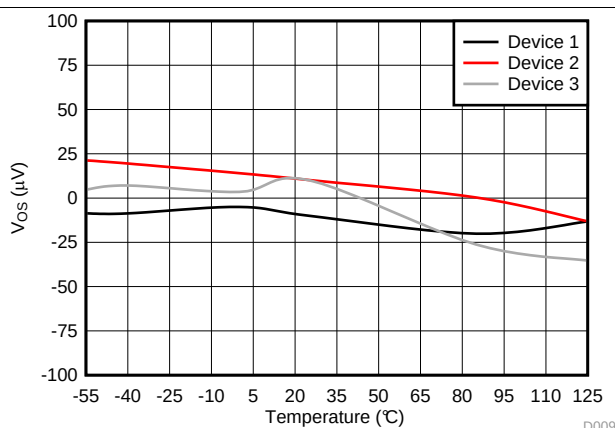


Figure 10. Input Offset Voltage vs Temperature

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.3\text{ V}$, $V_{INP} = -50\text{ mV to } 50\text{ mV}$, $V_{INN} = \text{GND1}$, and $f_{IN} = 10\text{ kHz}$ (unless otherwise noted)

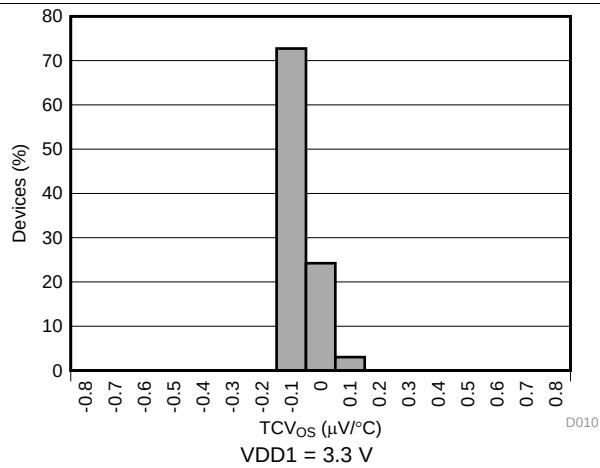


Figure 11. Input Offset Drift Histogram

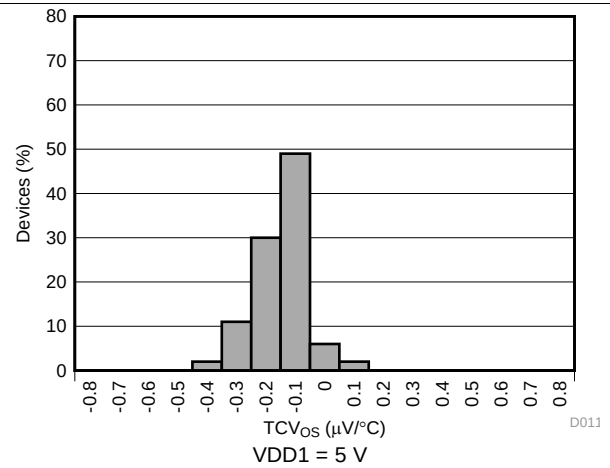


Figure 12. Input Offset Drift Histogram

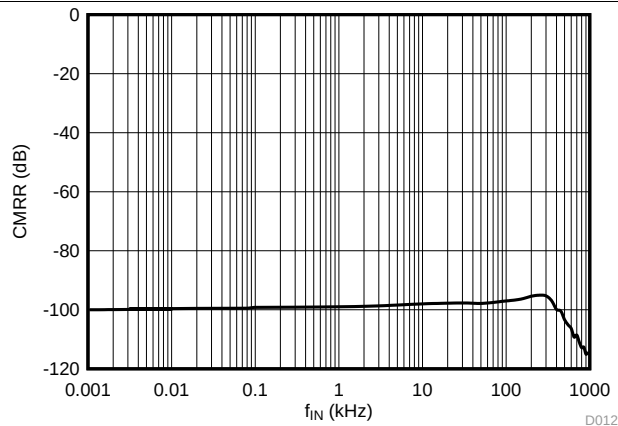


Figure 13. Common-Mode Rejection Ratio vs Input Frequency

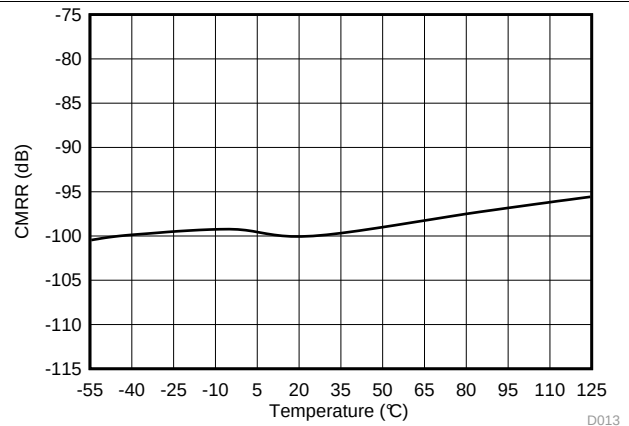


Figure 14. Common-Mode Rejection Ratio vs Temperature

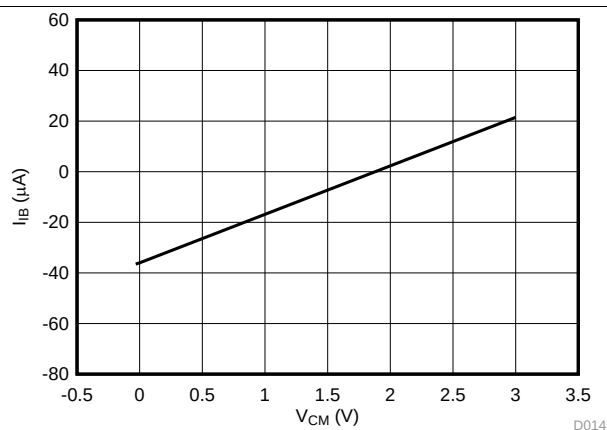


Figure 15. Input Bias Current vs Common-Mode Input Voltage

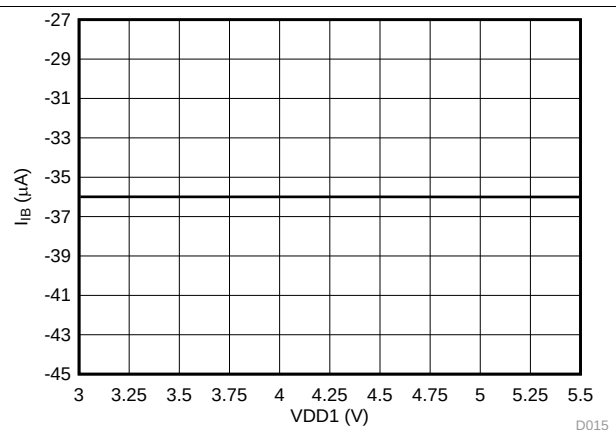


Figure 16. Input Bias Current vs High-Side Supply Voltage

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.3\text{ V}$, $V_{INP} = -50\text{ mV}$ to 50 mV , $V_{INN} = \text{GND1}$, and $f_{IN} = 10\text{ kHz}$ (unless otherwise noted)

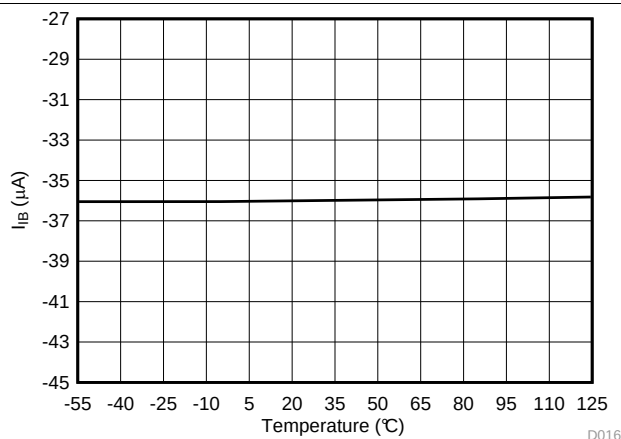


Figure 17. Input Bias Current vs Temperature

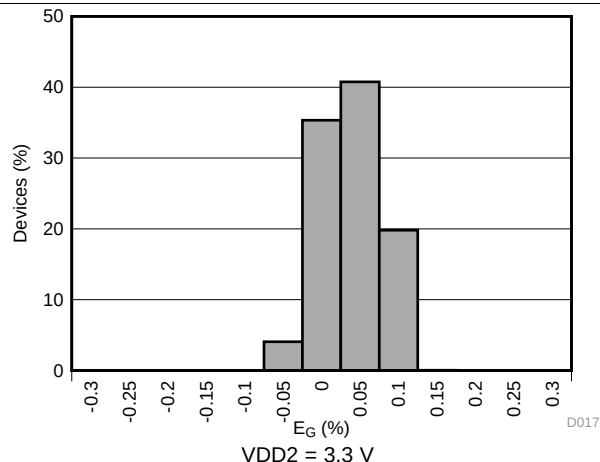


Figure 18. Gain Error Histogram

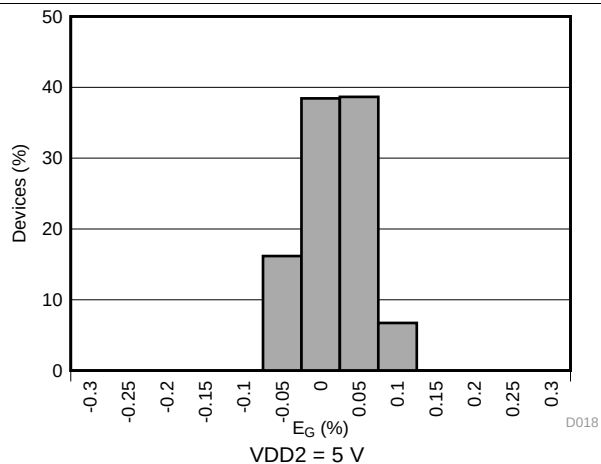


Figure 19. Gain Error Histogram

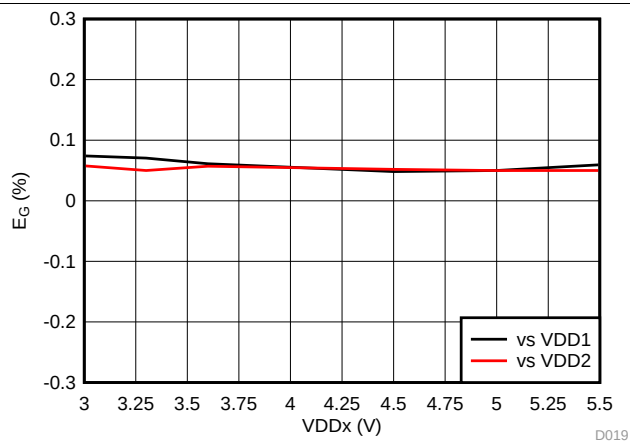


Figure 20. Gain Error vs Supply Voltage

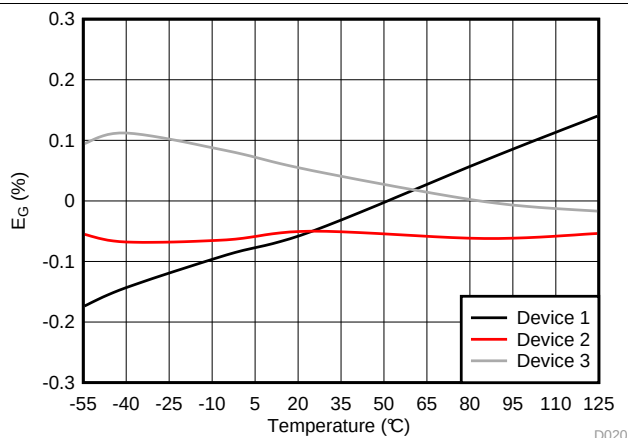


Figure 21. Gain Error vs Temperature

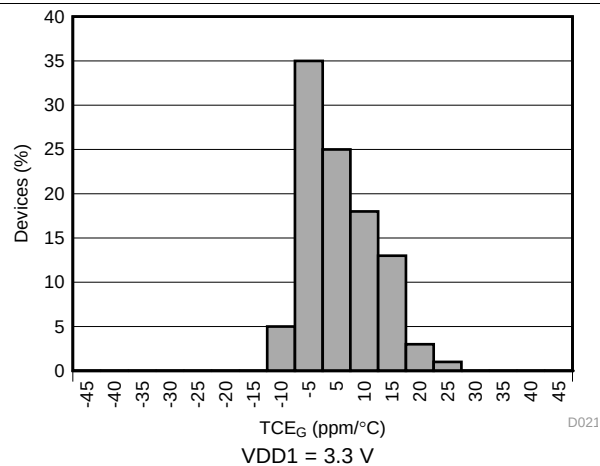


Figure 22. Gain Error Drift Histogram

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.3\text{ V}$, $V_{INP} = -50\text{ mV}$ to 50 mV , $V_{INN} = \text{GND1}$, and $f_{IN} = 10\text{ kHz}$ (unless otherwise noted)

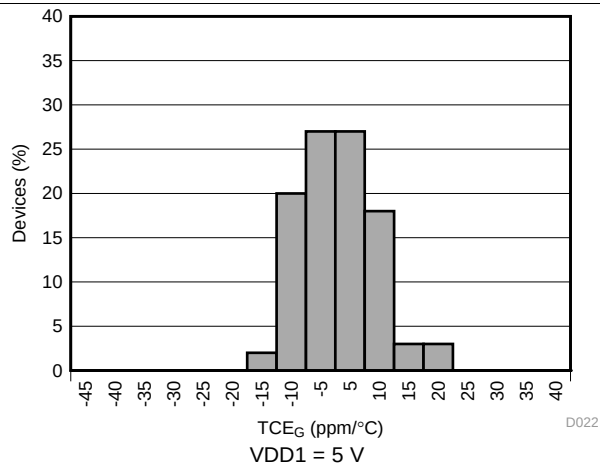


Figure 23. Gain Error Drift Histogram

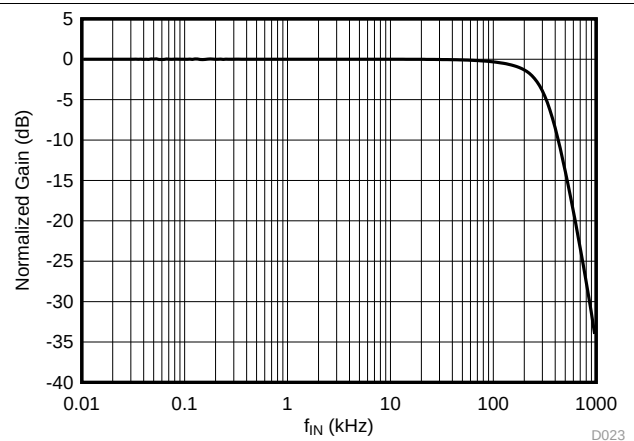


Figure 24. Normalized Gain vs Input Frequency

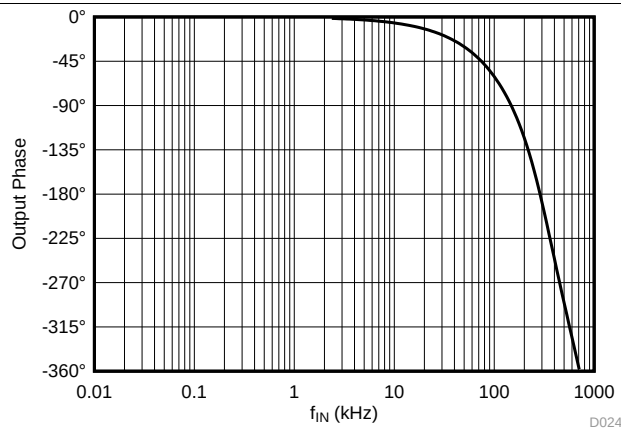


Figure 25. Output Phase vs Input Frequency

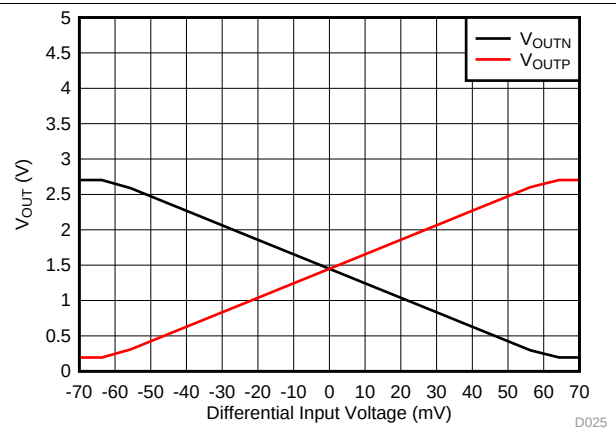


Figure 26. Output Voltage vs Input Voltage

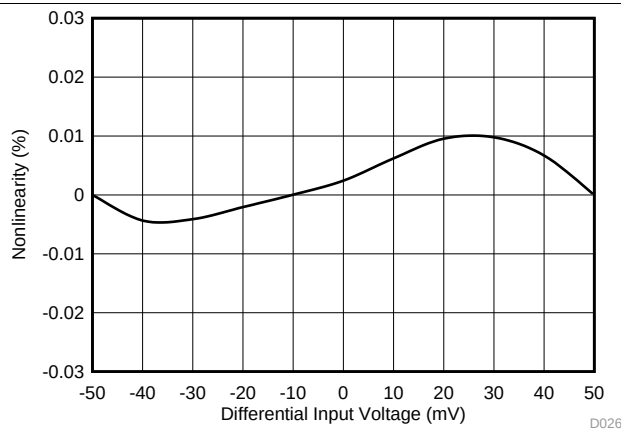


Figure 27. Nonlinearity vs Input Voltage

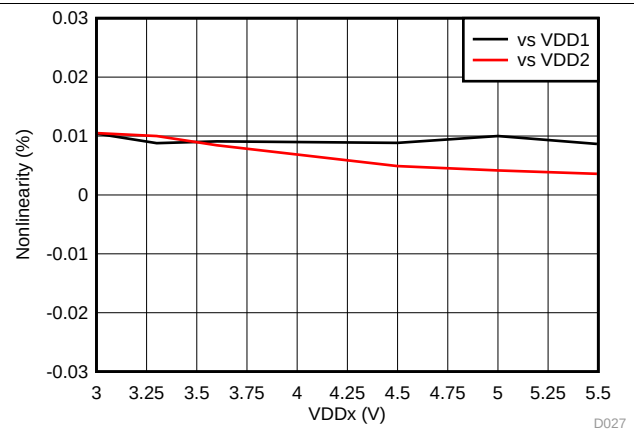


Figure 28. Nonlinearity vs Supply Voltage

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.3\text{ V}$, $V_{INP} = -50\text{ mV}$ to 50 mV , $V_{INN} = \text{GND1}$, and $f_{IN} = 10\text{ kHz}$ (unless otherwise noted)

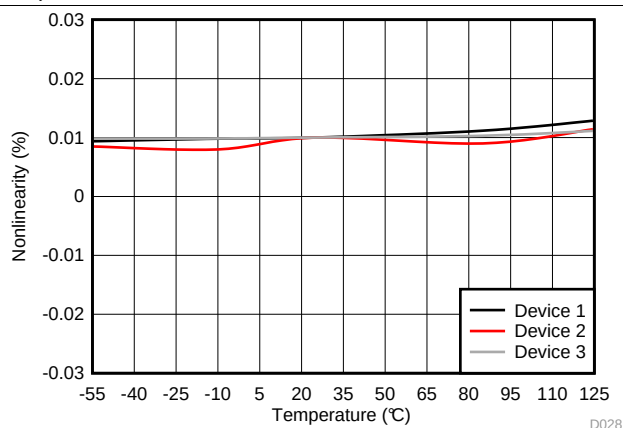


Figure 29. Nonlinearity vs Temperature

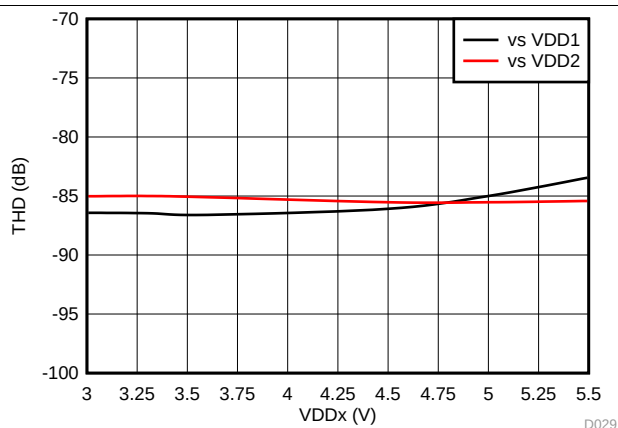


Figure 30. Total Harmonic Distortion vs Supply Voltage

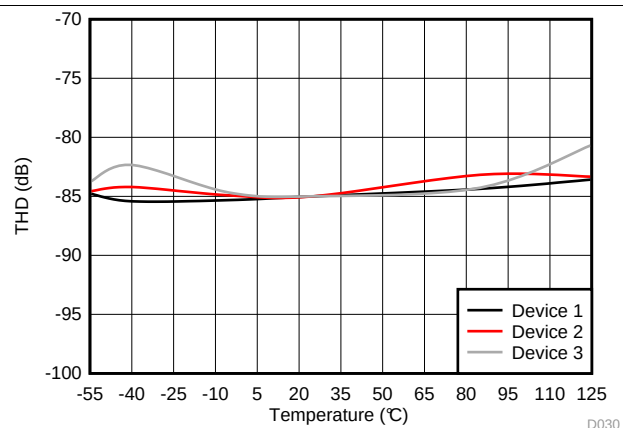


Figure 31. Total Harmonic Distortion vs Temperature

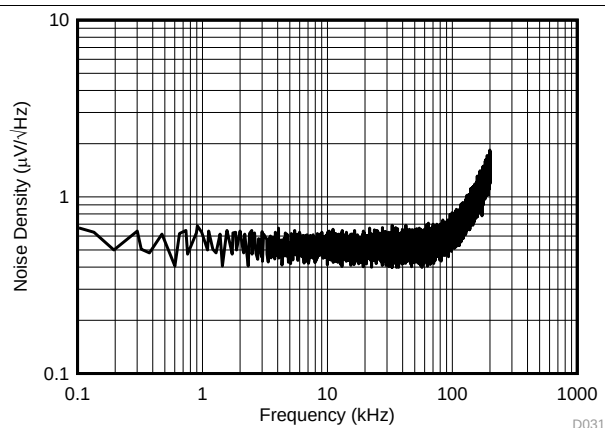


Figure 32. Output Noise Density vs Frequency

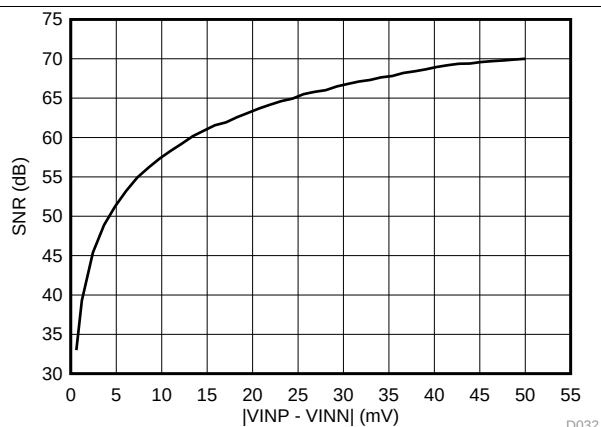


Figure 33. Signal-to-Noise Ratio vs Input Voltage

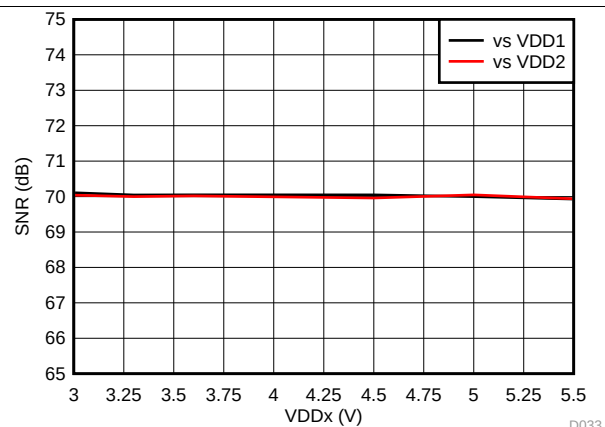


Figure 34. Signal-to-Noise Ratio vs Supply Voltage

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.3\text{ V}$, $V_{INP} = -50\text{ mV to } 50\text{ mV}$, $V_{INN} = \text{GND1}$, and $f_{IN} = 10\text{ kHz}$ (unless otherwise noted)

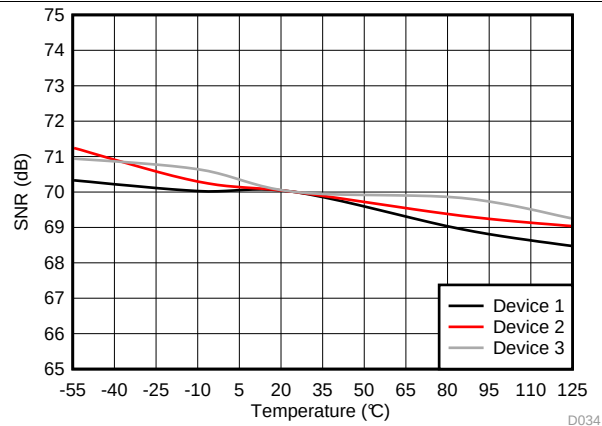


Figure 35. Signal-to-Noise Ratio vs Temperature

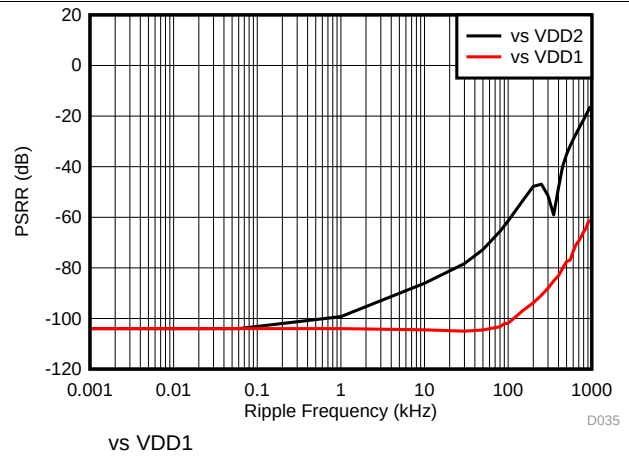


Figure 36. Power-Supply Rejection Ratio vs Ripple Frequency

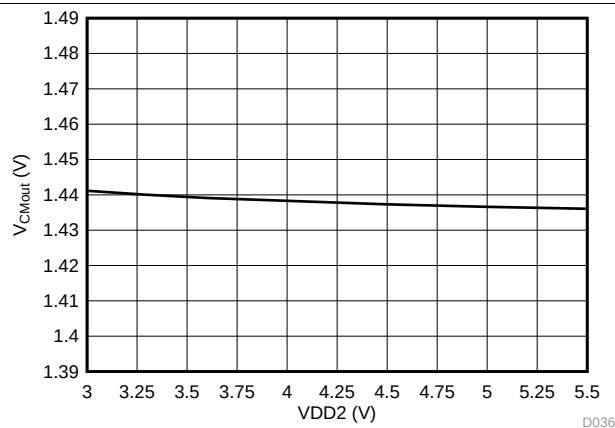


Figure 37. Output Common-Mode Voltage vs Low-Side Supply Voltage

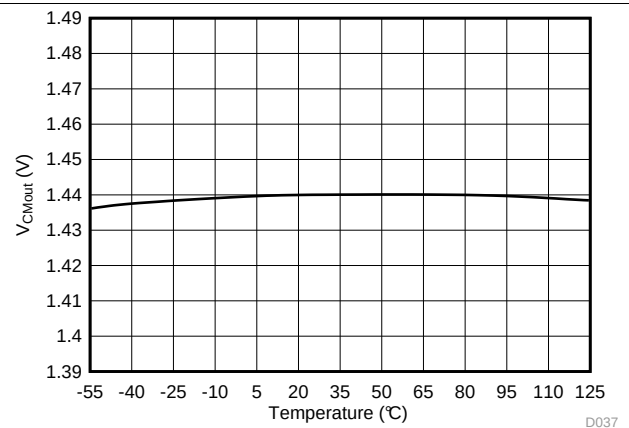


Figure 38. Output Common-Mode Voltage vs Temperature

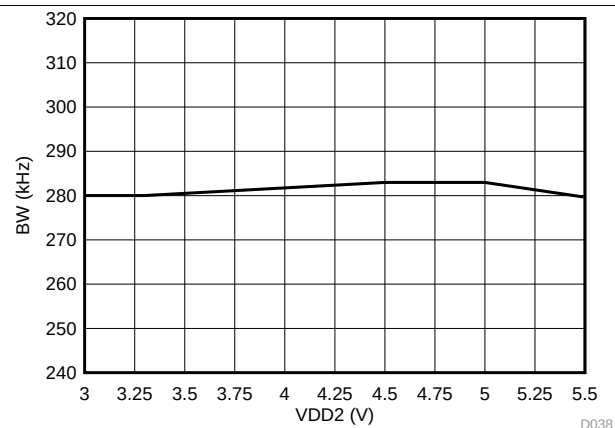


Figure 39. Output Bandwidth vs Low-Side Supply Voltage

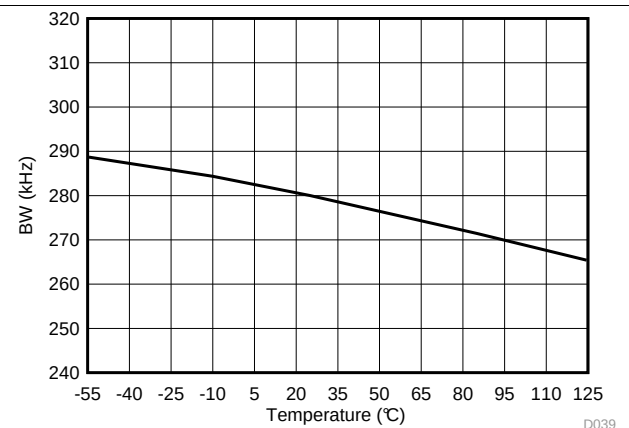


Figure 40. Output Bandwidth vs Temperature

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.3\text{ V}$, $V_{INP} = -50\text{ mV to } 50\text{ mV}$, $V_{INN} = \text{GND1}$, and $f_{IN} = 10\text{ kHz}$ (unless otherwise noted)

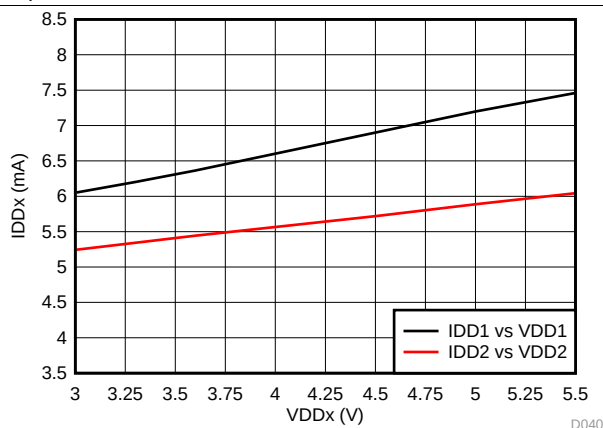


Figure 41. Supply Current vs Supply Voltage

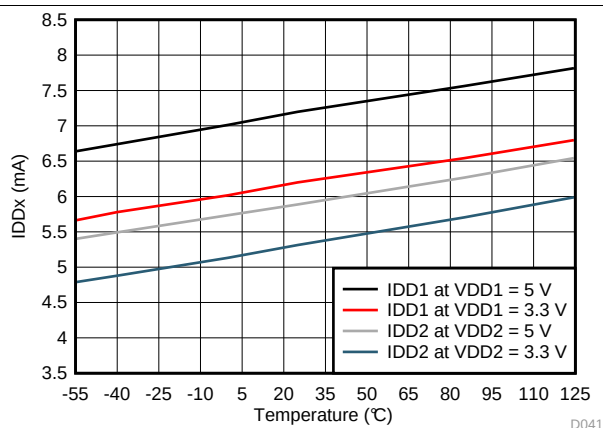


Figure 42. Supply Current vs Temperature

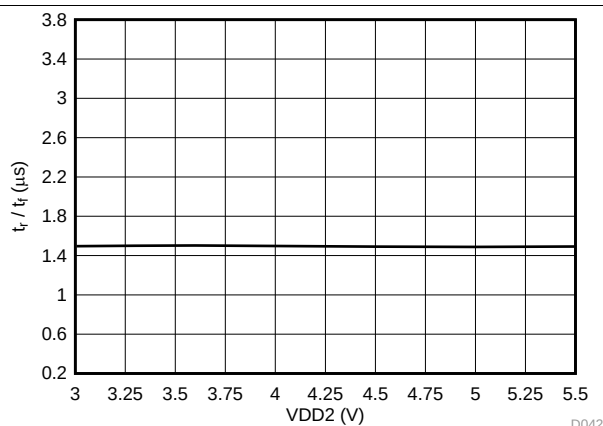


Figure 43. Output Rise and Fall Time vs Low-Side Supply Voltage

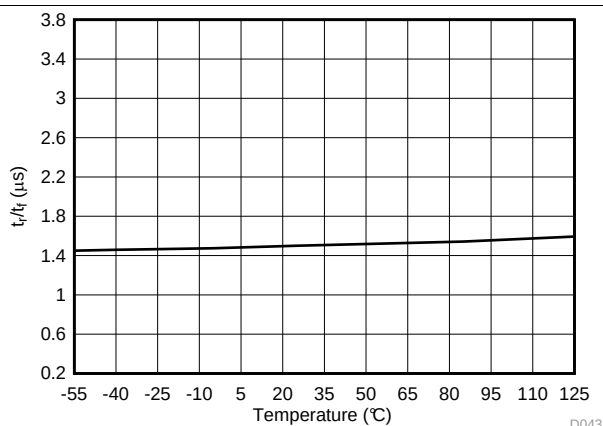


Figure 44. Output Rise and Fall Time vs Temperature

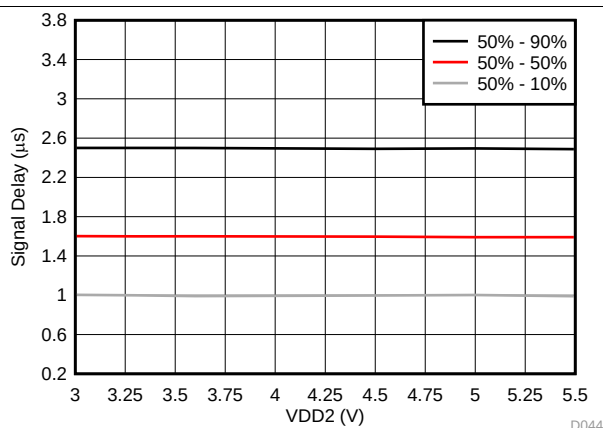


Figure 45. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

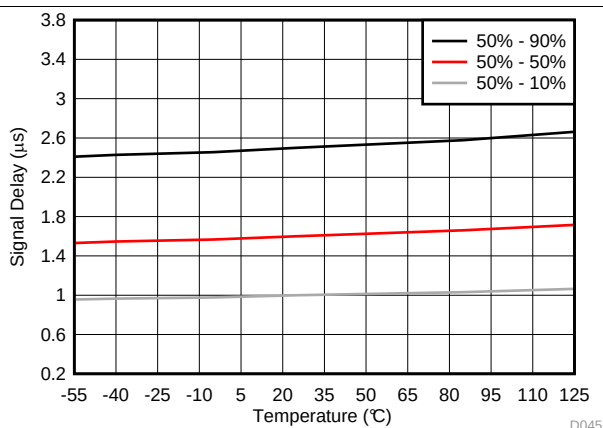


Figure 46. V_{IN} to V_{OUT} Signal Delay vs Temperature

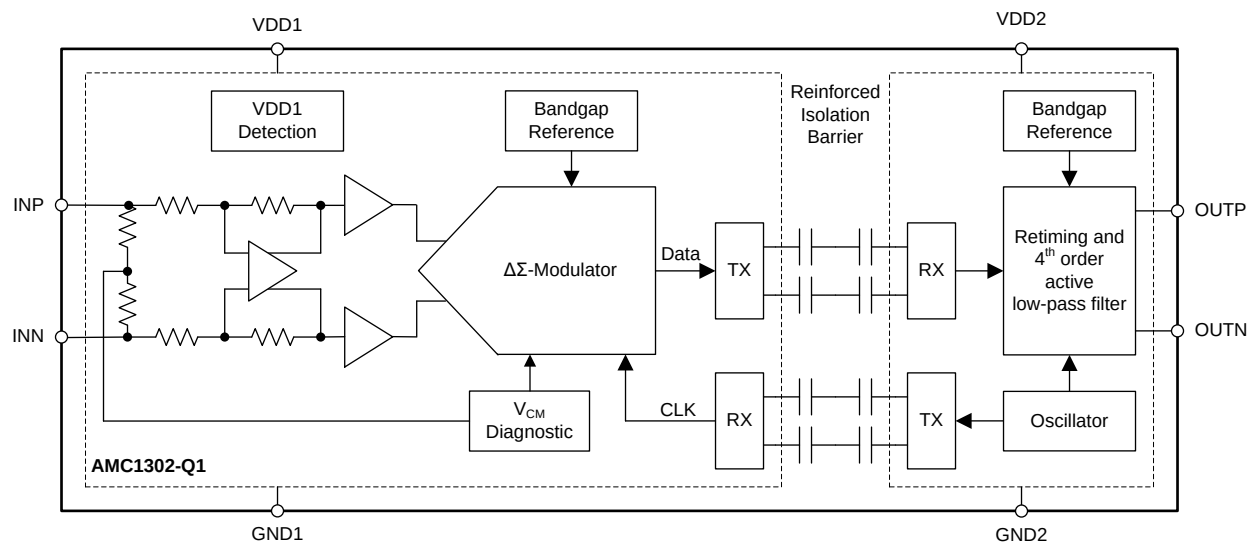
7 Detailed Description

7.1 Overview

The AMC1302-Q1 is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully-differential amplifier that drives a second-order, delta-sigma ($\Delta\Sigma$) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (called TX in the [Functional Block Diagram](#)) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed by a fourth-order analog filter on the low-side and presented as a differential output of the device.

The SiO₂-based, double-capacitive isolation barrier supports a high level of magnetic field immunity, as described in [ISO72x Digital Isolator Magnetic-Field Immunity](#). The digital modulation used in the AMC1302-Q1 (see also the [Isolation Channel Signal Transmission](#) section for more details) and the isolation barrier characteristics result in high reliability and common-mode transient immunity.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The differential amplifier input stage of the AMC1302-Q1 feeds a second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator. The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the [Isolation Channel Signal Transmission](#) section.

Figure 47 depicts the equivalent input structure of the AMC1302-Q1 with the relevant components. The total gain of the device results from a combination of the gain of the fully-differential input amplifier and the gain of the active output filter.

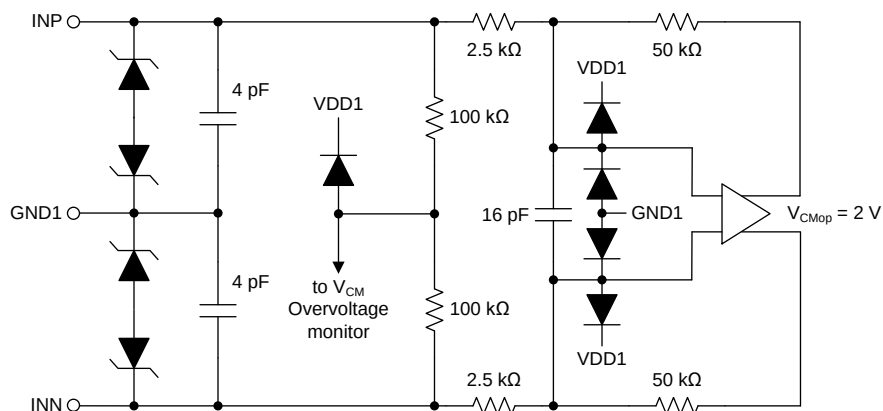


Figure 47. Equivalent Analog Input Circuit

There are two restrictions on the analog input signals (INP and INN). First, if the input voltage exceeds the range $GND1 - 6\text{ V}$ to $VDD1 + 0.5\text{ V}$, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (V_{FSR}) and within the specified common-mode input voltage range (V_{CM}); see the [Recommended Operating Conditions](#) table for detailed specifications.

Feature Description (continued)

7.3.2 Isolation Channel Signal Transmission

The AMC1302-Q1 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO₂-based isolation barrier. As shown in Figure 48, the transmitter modulates the bitstream at TX IN with an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent the digital *zero*. The nominal frequency of the carrier used inside the AMC1302-Q1 is 480 MHz.

The receiver demodulates the signal after advanced signal conditioning and produces the output. The AMC1302-Q1 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions caused by the high-frequency carrier and IO buffer switching.

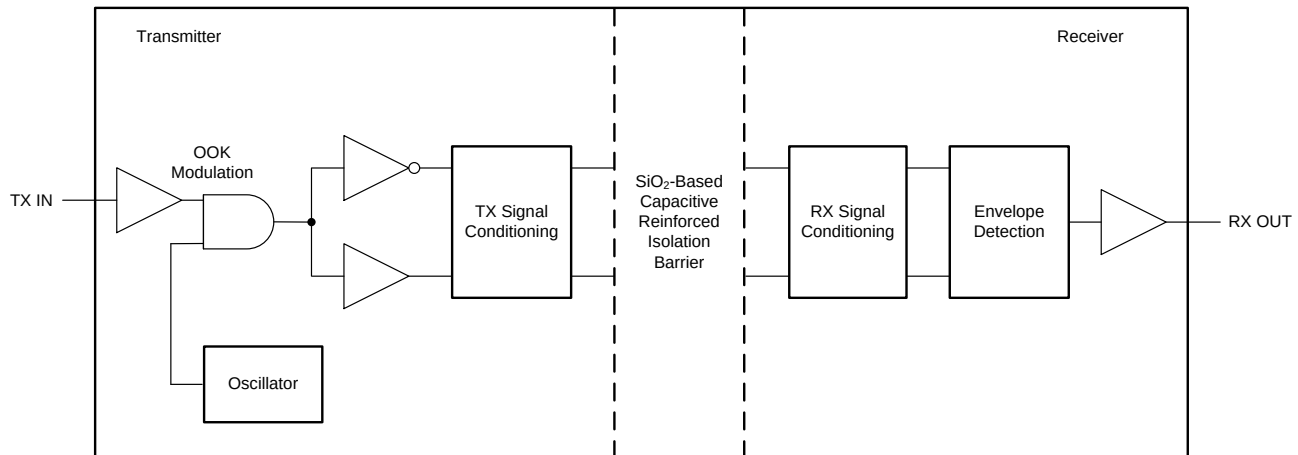


Figure 48. Block Diagram of an Isolation Channel

Figure 49 shows the concept of the OOK scheme.

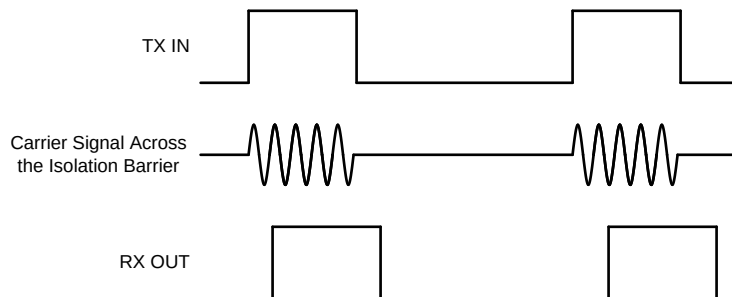


Figure 49. OOK-Based Modulation Scheme

Feature Description (continued)

7.3.3 Fail-Safe Output

The AMC1302-Q1 offers a fail-safe output that simplifies diagnostics on a system level. The fail-safe output is active in two cases:

- When the high-side supply VDD1 of the AMC1302-Q1 is missing, or
- When the common-mode input voltage, that is $V_{CM} = (V_{INP} + V_{INN}) / 2$, exceeds the minimum common-mode overvoltage detection level V_{CMOV} of $V_{DD1} - 2\text{ V}$

Figure 50 and Figure 51 show the fail-safe output of the AMC1302-Q1 as a negative differential output voltage value that does not occur under normal device operation. Use the $V_{FAILSAFE}$ voltage specified in the [Electrical Characteristics](#) table as a reference value for the fail-safe detection on a system level.



Figure 50. Typical Negative Clipping Output of the AMC1302-Q1



Figure 51. Typical Failsafe Output of the AMC1302-Q1

7.4 Device Functional Modes

The AMC1302-Q1 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the [Recommended Operating Conditions](#) table. The device does not require any specific power-supply sequence. Consider the analog startup time t_{AS} as defined in the [Switching Characteristics](#) table when the high-side power supply VDD1 powers up with the low-side power supply VDD2 already operating in the specified range.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The low input voltage range, very low nonlinearity, and temperature drift make the AMC1302-Q1 a high-performance solution for automotive applications where low-power dissipation, shunt-based current sensing with high common-mode voltage levels is required.

8.2 Typical Application

Isolated amplifiers are widely used in traction inverters, on-board chargers, and dc/dc converters. The input structure of the AMC1302-Q1 is optimized for use with very low-value shunt resistors in current-sensing applications.

Figure 52 shows a typical operation of the AMC1302-Q1 for current sensing in a traction inverter application. Phase current measurement is accomplished through the shunt resistors, R_{SHUNT} (in this case, a two-pin shunt). The differential input and the high common-mode transient immunity of the AMC1302-Q1 ensure reliable and accurate operation even in high-noise environments (such as the power stage of the motor drive). The high-impedance input and wide input voltage range make the [AMC1311-Q1](#) suitable for DC bus voltage sensing.

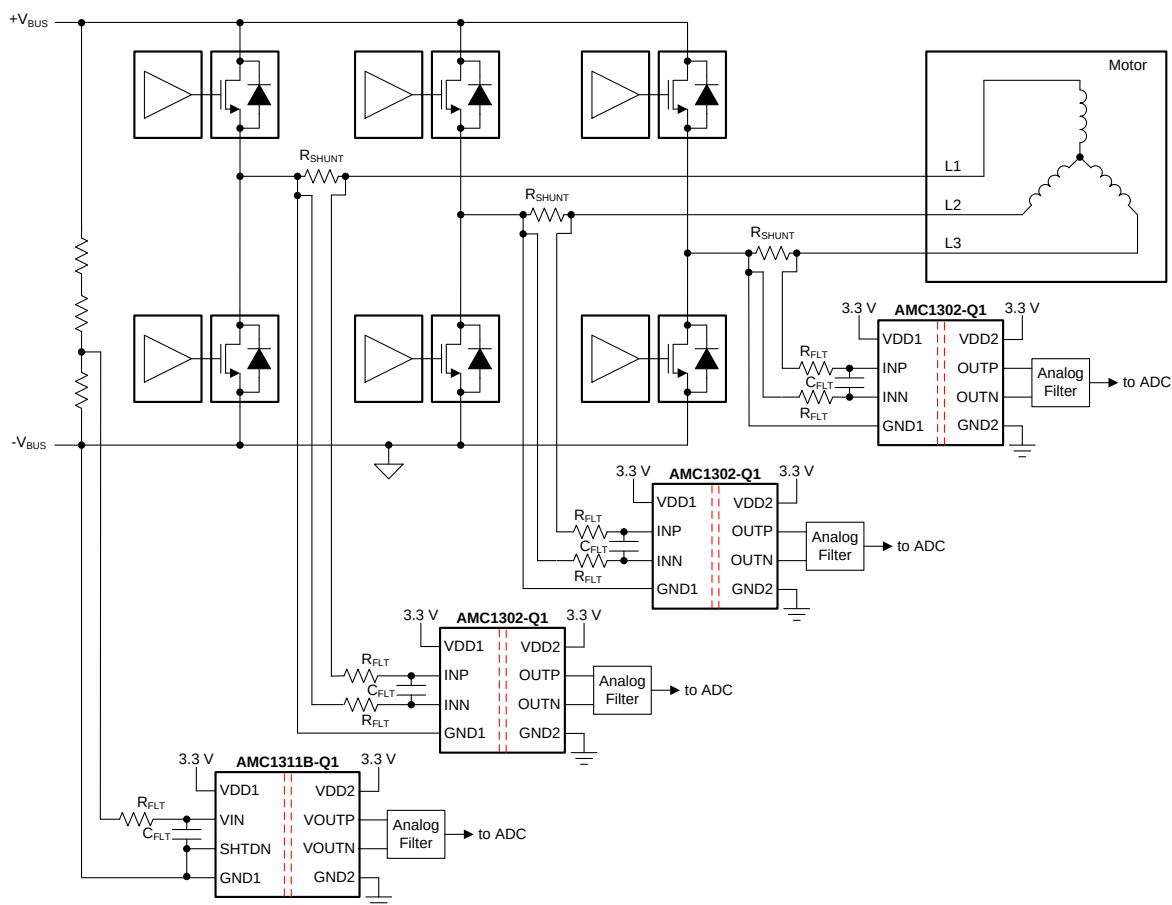


Figure 52. Using the AMC1302-Q1 for Current Sensing in Traction Inverters

Typical Application (continued)

8.2.1 Design Requirements

Table 1 lists the parameters for this typical application.

Table 1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across the shunt for a linear response	±50 mV (maximum)
Signal delay (90% settling)	3 μs (maximum)
High common-mode transient immunity (CMTI)	140 kV/μs (typical)

8.2.2 Detailed Design Procedure

The high-side power supply (VDD1) for the AMC1302-Q1 is derived from the power supply of the upper gate driver. Further details are provided in the [Power Supply Recommendations](#) section.

The floating ground reference (GND1) is derived from one of the ends of the shunt resistor that is connected to the negative input of the AMC1302-Q1 (INN). If a four-pin shunt is used, the inputs of the AMC1302-Q1 device are connected to the inner leads and GND1 is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT} :

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $V_{SHUNT} \leq \pm 50 \text{ mV}$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$

For systems using single-ended input ADCs, Figure 53 shows an example of a TLV313-Q1-based signal conversion and filter circuit as used on the AMC1302EVM, where V_{CM_ADC} is the common-mode input voltage of the ADC. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance.

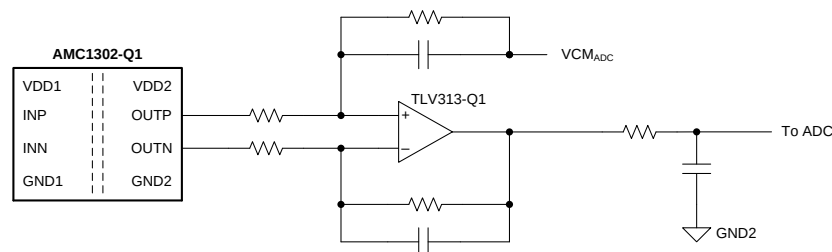


Figure 53. Connecting the AMC1302-Q1 Output to Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see [18-Bit, 1MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise](#) and [18-Bit Data Acquisition Block \(DAQ\) Optimized for Lowest Power](#), available for download at www.ti.com.

8.2.3 Application Curves

In traction inverter applications, the power switches must be protected in case of an overcurrent condition. To allow for fast powering off of the system, a low delay caused by the isolated amplifier is required. [Figure 54](#) shows the typical full-scale step response of the AMC1302-Q1. Consider the delay of the required window comparator and the MCU to calculate the overall response time of the system.

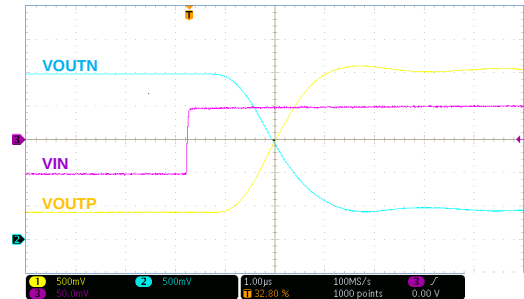


Figure 54. Step Response of the AMC1302-Q1

The high linearity and low temperature drift of the offset and gain errors of the AMC1302-Q1 (see the [Typical Characteristics](#) section) allows design of motor drives with low torque ripple.

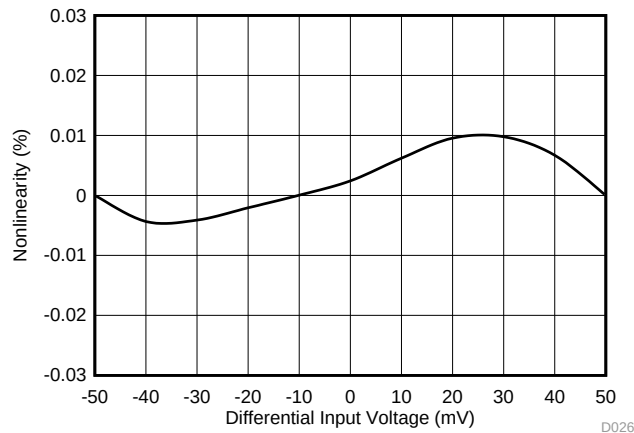


Figure 55. Typical Nonlinearity of the AMC1302-Q1

8.3 What to Do and What Not to Do

Do not leave the inputs of the AMC1302-Q1 unconnected (floating) when the device is powered up. If both device inputs are left floating, the input bias current drives these inputs to the output common-mode of the analog front-end of approximately 2 V. If the high-side supply voltage VDD1 is below 4 V, the internal common-mode overvoltage detector turns on and the output functions as described in the [Fail-Safe Output](#) section, which may lead to an undesired reaction on the system level.

9 Power Supply Recommendations

In a typical traction inverter application, the high-side power supply (VDD1) for the device is derived from the floating power supply of the upper gate driver. For lowest system-level cost, a Zener diode can be used to limit the voltage to 5 V or 3.3 V $\pm$ 10%. Alternatively, a low-cost low-dropout (LDO) regulator (for example, the [LP2951-XX-Q1](#)) may be used to minimize noise on the power supply. TI recommends a low-ESR decoupling capacitor of 0.1 μ F to filter this power-supply path. Place this capacitor (C1 in [Figure 56](#)) as close as possible to the VDD1 pin of the AMC1302-Q1 for best performance. Use an additional 2.2- μ F decoupling capacitor (C2) for filtering lower-frequency noise. The floating ground reference (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (INN) of the device. If a four-pin shunt is used, the device inputs are connected to the inner leads, and GND1 is connected to one of the outer leads of the shunt.

To decouple the digital power supply on the controller side, use a 0.1- μ F capacitor (C3) placed as close to the VDD2 pin of the AMC1302-Q1 as possible, followed by an additional capacitor from 1 μ F to 10 μ F (C4).

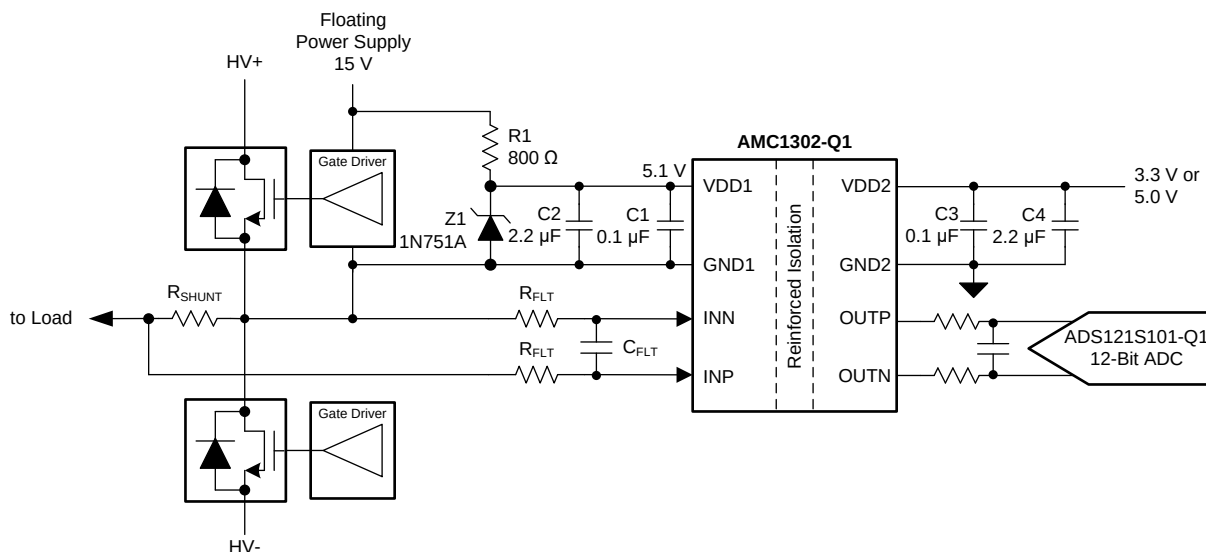


Figure 56. Zener-Diode-Based, High-Side Power Supply

10 Layout

10.1 Layout Guidelines

Figure 57 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1302-Q1 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1302-Q1 and keep the layout of both connections symmetrical.

10.2 Layout Example

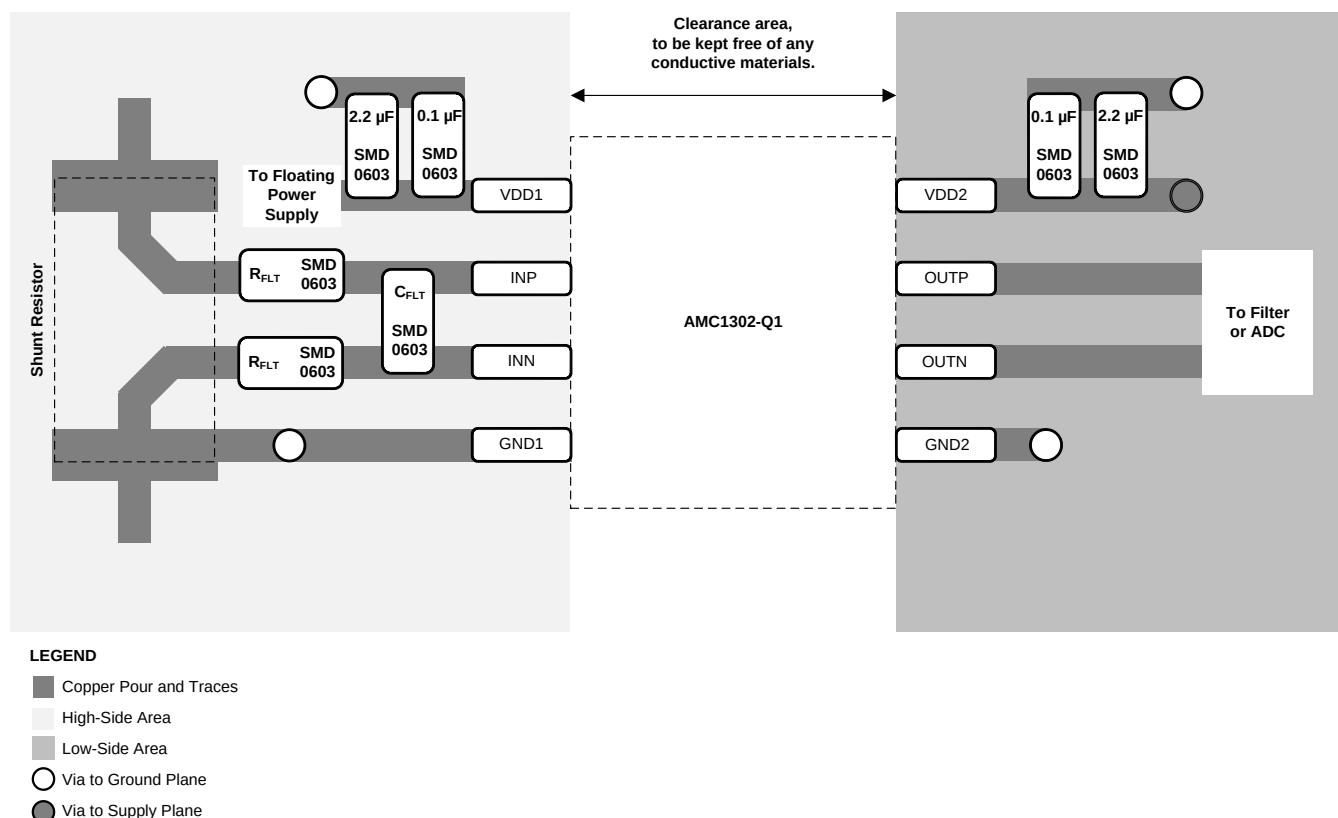


Figure 57. Recommended Layout of the AMC1302-Q1

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Texas Instruments, [Isolation Glossary](#) application report

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ADC121S101x-Q1 Single-Channel, 0.5 to 1-Msps, 12-Bit Analog-to-Digital Converter data sheet](#)
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics](#) application report
- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity](#) application report
- Texas Instruments, [AMC1311x-Q1 High-Impedance, 2-V Input, Reinforced Isolated Amplifiers](#) data sheet
- Texas Instruments, [TLV313-Q1 Low-Power, Rail-to-Rail In/Out, 750- \$\mu\$ V Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems](#) data sheet
- Texas Instruments, [LP2951-xx-Q1 Adjustable Micropower Voltage Regulators With Shutdown](#) data sheet
- Texas Instruments, [AMC130x Evaluation Module](#) user's guide
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise](#) user's guide
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Power](#) user's guide
- Texas Instruments, [SN6501-Q1 Transformer Driver for Isolated Power Supplies](#) data sheet

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1302QDWVQ1	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1302Q	Samples
AMC1302QDWVRQ1	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1302Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

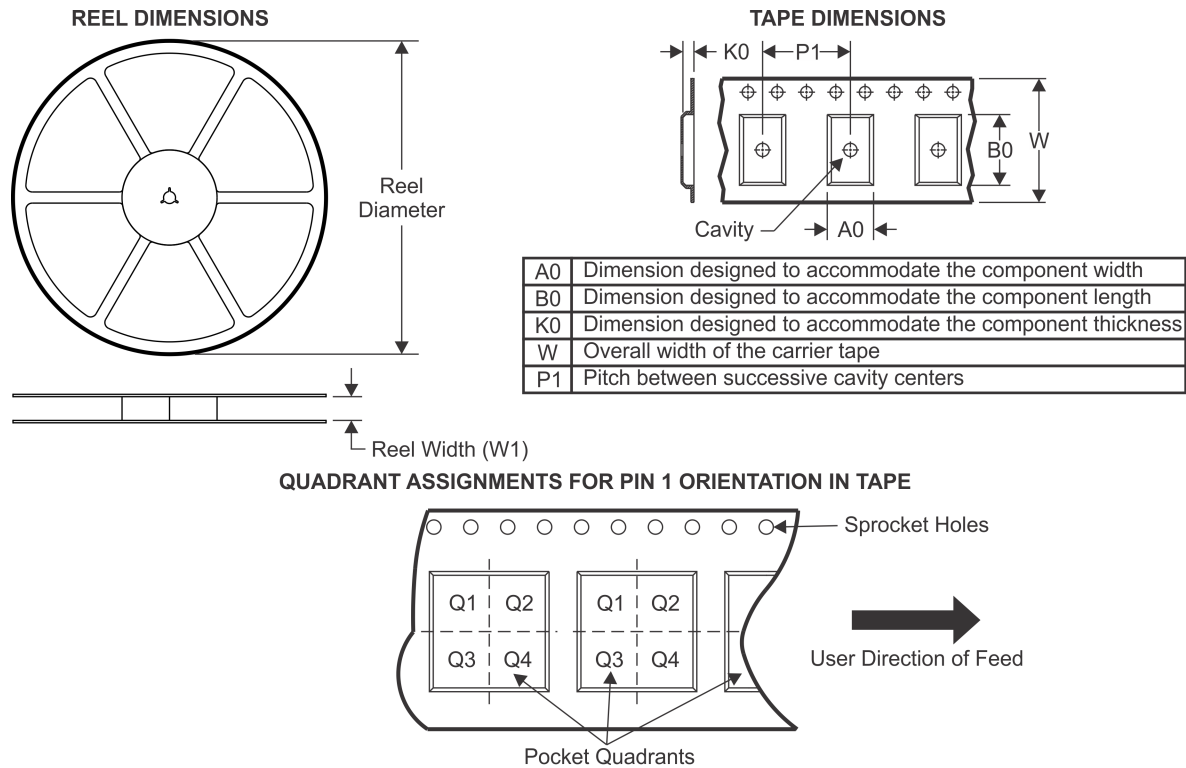
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AMC1302-Q1 :

- Catalog: [AMC1302](#)

NOTE: Qualified Version Definitions:

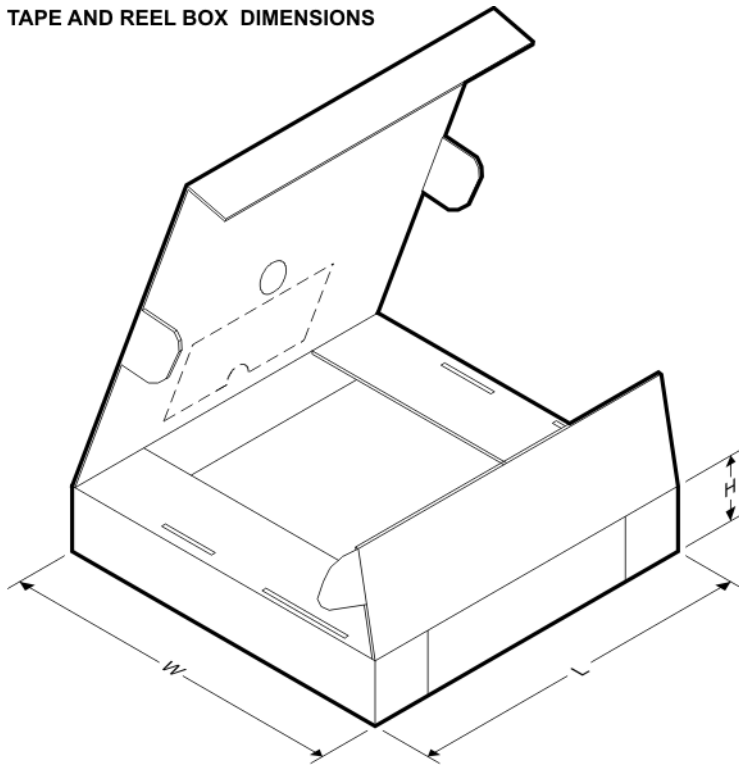
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1302QDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

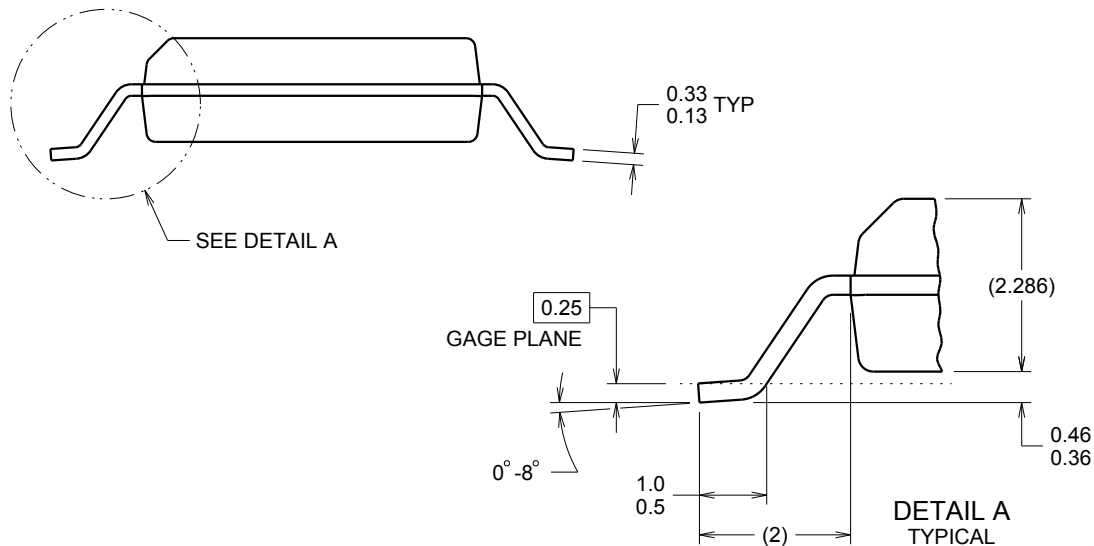


*All dimensions are nominal

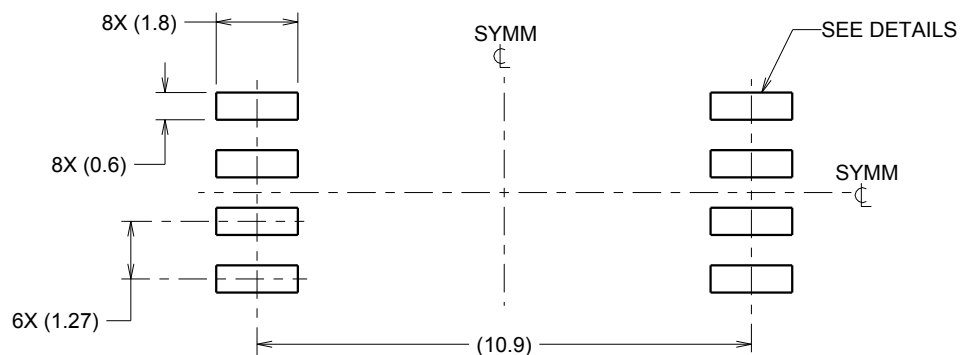
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1302QDWVRQ1	SOIC	DWV	8	1000	350.0	350.0	43.0

SOIC - 2.8 mm max height

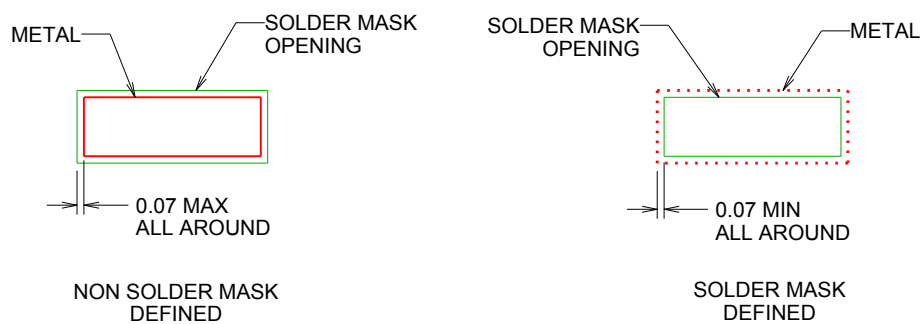
PIN 1 ID AREA
 11.5 ± 0.25 TYP
 5.95
 5.75
 NOTE 3
 1
 4
 8
 5
 6X 1.27
 2X 3.81
 8X 0.51
 0.31
 7.6
 7.4
 NOTE 4
 A
 B
 SEATING PLANE
 0.1 C
 2.8 MAX
 C
 A
 B
 S



1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

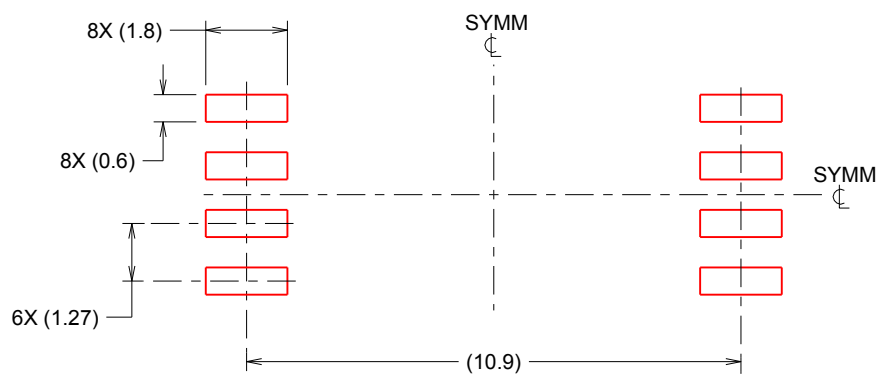


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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