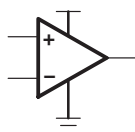


## FAMILY OF LOW-POWER WIDE BANDWIDTH SINGLE SUPPLY OPERATIONAL AMPLIFIERS WITH AND WITHOUT SHUTDOWN

### FEATURES

- Rail-To-Rail Output
- $V_{ICR}$  Includes Ground
- Gain-Bandwidth Product . . . 9 MHz
- Supply Current . . . 730  $\mu$ A/Channel
- Single, Duals, and Quad Versions
- Ultralow Power Down Mode  
 $I_{DD}(SHDN) = 4 \mu$ A/Channel
- Specified Temperature Range  
–40°C to 125°C . . . Industrial Grade
- Supply Voltage Range . . . 2.7 V to 5.5 V
- Ultrasmall Packaging  
5 or 6 Pin SOT-23 (TLV2630/1)  
8 or 10 Pin MSOP (TLV2632/3)
- Universal Op-Amp EVM (See SLOU060  
for More Information)

Operational Amplifier



### DESCRIPTION

The TLV263x single supply operational amplifiers provide rail-to-rail output with an input range that includes ground. The TLV263x takes the minimum operating supply voltage down to 2.7 V over the extended industrial temperature range (–40°C to 125°C) while adding the rail-to-rail output swing feature. The TLV263x also provides a 9 MHz gain-bandwidth product from only 730  $\mu$ A of supply current. The maximum recommended supply voltage is 5.5 V, which, when coupled with a 2.7-V minimum, allows the devices to be operated from lithium ion cells.

The combination of wide bandwidth, low noise, and low distortion makes it ideal for high speed and high resolution data converter applications. The ground input range allows it to directly interface to ground rail referred systems.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

The 2.7-V operation makes it compatible with Li-Ion powered systems and the operating supply voltage range of many micro-power microcontrollers available today including TI's MSP430.

AMPLIFIER SELECTION TABLE

| DEVICE         | $V_{DD}$<br>[V] | $I_{DD}/ch$<br>[ $\mu$ A] | $V_{ICR}$<br>[V]                      | GBW<br>[MHz] | SLEW RATE<br>[V/ $\mu$ s] | $V_n$ , 1 kHz<br>[nV/ $\sqrt{Hz}$ ] | $I_O$<br>[mA] |
|----------------|-----------------|---------------------------|---------------------------------------|--------------|---------------------------|-------------------------------------|---------------|
| OPAx343        | 2.5–5.5         | 850                       | –0.3 to $V_{DD} + 0.3$                | 5.5          | 6                         | 25                                  | 40            |
| OPAx743        | 3.5–12          | 1100                      | –0.1 to $V_{DD} + 0.1$                | 7            | 10                        | 30                                  | 20            |
| TLV278x        | 1.8–3.6         | 650                       | –0.2 to $V_{DD} + 0.2$                | 8            | 5                         | 9                                   | 10            |
| <b>TLV263x</b> | <b>2.7–5.5</b>  | <b>730</b>                | <b>GND to <math>V_{DD} - 1</math></b> | <b>9</b>     | <b>9.5</b>                | <b>50</b>                           | <b>28</b>     |
| TLV262x        | 2.7–5.5         | 750                       | 1 V to $V_{DD} + 0.2$                 | 11           | 10                        | 27                                  | 28            |
| OPAx353        | 2.7–5.5         | 8000                      | –0.1 to $V_{DD} + 0.1$                | 44           | 22                        | 7                                   | 40            |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TLV2630, TLV2631**  
**TLV2632, TLV2633**  
**TLV2634, TLV2635**

SLOS362A – JUNE 2001 – REVISED JANUARY 2005

**PACKAGE/ORDERING INFORMATION<sup>(1)</sup>**

| PRODUCT                 | PACKAGE  | PACKAGE CODE | SYMBOL | SPECIFIED TEMPERATURE RANGE | ORDER NUMBER                                           | TRANSPORT MEDIA       |
|-------------------------|----------|--------------|--------|-----------------------------|--------------------------------------------------------|-----------------------|
| Single with Shutdown    |          |              |        |                             |                                                        |                       |
| TLV2630ID               | SOIC–8   | D            | —      | –40°C to 125°C              | TLV2630ID<br>TLV2630IDR                                | Tube<br>Tape and Reel |
| TLV2630IDBV             | SOT–23–6 | DBV          | VAYI   |                             | TLV2630IDBVR <sup>†</sup><br>TLV2630IDBVT <sup>‡</sup> | Tape and Reel         |
| TLV2630IP               | DIP–8    | P            | —      |                             | TLV2630IP                                              | Tube                  |
| Single without Shutdown |          |              |        |                             |                                                        |                       |
| TLV2631ID               | SOIC–8   | D            | —      | –40°C to 125°C              | TLV2631ID<br>TLV2631IDR                                | Tube<br>Tape and Reel |
| TLV2631IDBV             | SOT–23–5 | DBV          | VAZI   |                             | TLV2631IDBVR <sup>†</sup><br>TLV2631IDBVT <sup>‡</sup> | Tape and Reel         |
| TLV2631IP               | DIP–8    | P            | —      |                             | TLV2631IP                                              | Tube                  |
| Dual without Shutdown   |          |              |        |                             |                                                        |                       |
| TLV2632ID               | SOIC–8   | D            | —      | –40°C to 125°C              | TLV2632ID<br>TLV2632IDR                                | Tube<br>Tape and Reel |
| TLV2632IDGK             | MSOP–8   | DGK          | AKG    |                             | TLV2632IDGK<br>TLV2632IDGKR                            | Tube<br>Tape and Reel |
| TLV2632IP               | DIP–8    | P            | —      |                             | TLV2632IP                                              | Tube                  |
| Dual with Shutdown      |          |              |        |                             |                                                        |                       |
| TLV2633ID               | SOIC–14  | D            | —      | –40°C to 125°C              | TLV2633ID<br>TLV2633IDR                                | Tube<br>Tape and Reel |
| TLV2633IDGS             | MSOP–10  | DGS          | AKK    |                             | TLV2633IDGS<br>TLV2633IDGSR                            | Tube<br>Tape and Reel |
| TLV2633IN               | DIP–14   | N            | —      |                             | TLV2633IN                                              | Tube                  |
| Quad without Shutdown   |          |              |        |                             |                                                        |                       |
| TLV2634ID               | SOIC–14  | D            | —      | –40°C to 125°C              | TLV2634ID<br>TLV2634IDR                                | Tube<br>Tape and Reel |
| TLV2634IN               | DIP–14   | N            | —      |                             | TLV2634IN                                              | Tube                  |
| TLV2634IPW              | TSSOP–14 | PW           | —      |                             | TLV2634IPW<br>TLV2634IPWR                              | Tube<br>Tape and Reel |
| Quad with Shutdown      |          |              |        |                             |                                                        |                       |
| TLV2635ID               | SOIC–16  | D            | —      | –40°C to 125°C              | TLV2635ID<br>TLV2635IDR                                | Tube<br>Tape and Reel |
| TLV2635IN               | DIP–16   | N            | —      |                             | TLV2635IN                                              | Tube                  |
| TLV2635IPW              | TSSOP–16 | PW           | —      |                             | TLV2635IPW<br>TLV2635IPWR                              | Tube<br>Tape and Reel |

<sup>†</sup> The SOT23 package devices are only available taped and reeled. The **R** Suffix denotes quantities (3,000 pieces per reel).

<sup>‡</sup> The **T** Suffix denotes smaller quantities (250 pieces per mini-reel).

1. For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

|                                                              |                                                |
|--------------------------------------------------------------|------------------------------------------------|
| Supply voltage, $V_{DD}$ (see Note 1)                        | 6 V                                            |
| Differential input voltage, $V_{ID}$                         | $\pm V_{DD}$                                   |
| Input voltage range, $V_I$ (see Note 1)                      | GND to $V_{DD} - 1$ V                          |
| Input current, $I_I$ (any input)                             | $\pm 10$ mA                                    |
| Output current, $I_O$                                        | $\pm 40$ mA                                    |
| Continuous total power dissipation                           | See Dissipation Rating Table                   |
| Operating free-air temperature range, $T_A$ : I-suffix       | $-40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ |
| Maximum junction temperature, $T_J$                          | $150^{\circ}\text{C}$                          |
| Storage temperature range, $T_{Stg}$                         | $-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$ |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | $260^{\circ}\text{C}$                          |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values, except differential voltages, are with respect to GND.

**recommended operating conditions**

|                                            |               | MIN        | MAX          | UNIT               |
|--------------------------------------------|---------------|------------|--------------|--------------------|
| Supply voltage, $V_{DD}$                   | Single supply | 2.7        | 5.5          | V                  |
|                                            | Split supply  | $\pm 1.35$ | $\pm 2.75$   |                    |
| Common-mode input voltage range, $V_{ICR}$ |               | GND        | $V_{DD} - 1$ | V                  |
| Operating free-air temperature, $T_A$      | I-suffix      | -40        | 125          | $^{\circ}\text{C}$ |
| Shutdown on/off voltage level <sup>‡</sup> | $V_{IL}$      |            | 0.4          | V                  |
|                                            | $V_{IH}$      | 2          |              |                    |

<sup>‡</sup> Relative to GND.

**electrical characteristics at specified free-air temperature,  $V_{DD} = 2.7$  V, 5 V (unless otherwise noted)**

**dc performance**

| PARAMETER                                                      | TEST CONDITIONS                                                | $T_A$                 | MIN | TYP | MAX  | UNIT                           |
|----------------------------------------------------------------|----------------------------------------------------------------|-----------------------|-----|-----|------|--------------------------------|
| $V_{IO}$ Input offset voltage                                  | $V_{IC} = V_{DD}/2$ ,<br>$V_O = V_{DD}/2$                      | 25 $^{\circ}\text{C}$ |     | 250 | 3500 | $\mu\text{V}$                  |
|                                                                |                                                                | Full range            |     |     | 4500 |                                |
|                                                                |                                                                | 25 $^{\circ}\text{C}$ |     | 250 | 4200 | $\mu\text{V}$                  |
|                                                                |                                                                | Full range            |     |     | 5200 |                                |
| $\alpha_{VIO}$ Temperature coefficient of input offset voltage |                                                                | 25 $^{\circ}\text{C}$ |     | 3   |      | $\mu\text{V}/^{\circ}\text{C}$ |
| CMRR Common-mode rejection ratio                               | $V_{IC} = \text{GND to } V_{DD} - 1 \text{ V}$                 | 25 $^{\circ}\text{C}$ | 76  | 100 |      | dB                             |
|                                                                |                                                                | Full range            | 67  |     |      |                                |
|                                                                |                                                                | 25 $^{\circ}\text{C}$ | 77  | 100 |      |                                |
|                                                                |                                                                | Full range            | 74  |     |      |                                |
| $A_{VD}$ Large-signal differential voltage amplification       | $R_L = 2 \text{ k}\Omega$ , $V_{O(PP)} = V_{DD} - 1 \text{ V}$ | 25 $^{\circ}\text{C}$ | 90  | 100 |      | dB                             |
|                                                                |                                                                | Full range            | 82  |     |      |                                |

**electrical characteristics at specified free-air temperature,  $V_{DD} = 2.7\text{ V}$ ,  $5\text{ V}$  (unless otherwise noted)**  
**(continued)**

**input characteristics**

| PARAMETER         |                               | TEST CONDITIONS                                                              | T <sub>A</sub> <sup>†</sup> | MIN | TYP  | MAX | UNIT |
|-------------------|-------------------------------|------------------------------------------------------------------------------|-----------------------------|-----|------|-----|------|
| I <sub>IO</sub>   | Input offset current          | V <sub>IC</sub> = V <sub>DD</sub> /2,<br>V <sub>O</sub> = V <sub>DD</sub> /2 | 25°C                        |     | 1    | 50  | pA   |
|                   |                               |                                                                              | Full range                  |     |      | 100 |      |
| I <sub>IB</sub>   | Input bias current            |                                                                              | 25°C                        |     | 1    | 50  |      |
|                   |                               |                                                                              | Full range                  |     |      | 200 |      |
| r <sub>i(d)</sub> | Differential input resistance |                                                                              | 25°C                        |     | 1000 |     | GΩ   |
| C <sub>i(c)</sub> | Common-mode input capacitance | f = 1 kHz                                                                    | 25°C                        |     | 12   |     | pF   |

$^\dagger$  Full range is –40°C to 125°C for the I-suffix.

**output characteristics**

| PARAMETER                             | TEST CONDITIONS                                             | $T_A^\dagger$           | MIN  | TYP   | MAX  | UNIT |
|---------------------------------------|-------------------------------------------------------------|-------------------------|------|-------|------|------|
| $V_{OH}$ High-level output voltage    | $V_{IC} = V_{DD}/2$ , $I_{OH} = -1\text{ mA}$               | $V_{DD} = 2.7\text{ V}$ | 25°C | 2.6   | 2.67 | V    |
|                                       |                                                             | Full range              |      | 2.55  |      |      |
|                                       |                                                             | $V_{DD} = 5\text{ V}$   | 25°C | 4.92  | 4.98 |      |
|                                       |                                                             | Full range              |      | 4.9   |      |      |
|                                       | $V_{IC} = V_{DD}/2$ , $I_{OH} = -10\text{ mA}$              | $V_{DD} = 2.7\text{ V}$ | 25°C | 2.25  | 2.43 |      |
|                                       |                                                             | Full range              |      | 2.15  |      |      |
|                                       |                                                             | $V_{DD} = 5\text{ V}$   | 25°C | 4.7   | 4.8  |      |
|                                       |                                                             | Full range              |      | 4.65  |      |      |
| $V_{OL}$ Low-level output voltage     | $V_{IC} = V_{DD}/2$ , $I_{OL} = 1\text{ mA}$                | $V_{DD} = 2.7\text{ V}$ | 25°C | 0.03  | 0.1  | mV   |
|                                       |                                                             | Full range              |      |       | 0.15 |      |
|                                       |                                                             | $V_{DD} = 5\text{ V}$   | 25°C | 0.025 | 0.08 |      |
|                                       |                                                             | Full range              |      |       | 0.1  |      |
|                                       | $V_{IC} = V_{DD}/2$ , $I_{OL} = 10\text{ mA}$               | $V_{DD} = 2.7\text{ V}$ | 25°C | 0.26  | 0.45 |      |
|                                       |                                                             | Full range              |      |       | 0.47 |      |
|                                       |                                                             | $V_{DD} = 5\text{ V}$   | 25°C | 0.2   | 0.3  |      |
|                                       |                                                             | Full range              |      |       | 0.35 |      |
| $I_O$ Output current                  | $V_{DD} = 2.7\text{ V}$ ,<br>$V_O = 0.5\text{ V}$ from rail | Sourcing                | 25°C |       | 14   | mA   |
|                                       |                                                             | Sinking                 |      |       | 19   |      |
|                                       | $V_{DD} = 5\text{ V}$ ,<br>$V_O = 0.5\text{ V}$ from rail   | Sourcing                |      |       | 28   |      |
|                                       |                                                             | Sinking                 |      |       | 28   |      |
| $I_{OS}$ Short-circuit output current | Sourcing                                                    | $V_{DD} = 2.7\text{ V}$ | 25°C |       | 50   | mA   |
|                                       |                                                             | $V_{DD} = 5\text{ V}$   |      |       | 95   |      |
|                                       | Sinking                                                     | $V_{DD} = 2.7\text{ V}$ |      |       | 50   |      |
|                                       |                                                             | $V_{DD} = 5\text{ V}$   |      |       | 95   |      |

$^\dagger$  Full range is –40°C to 125°C for the I-suffix.

**power supply**

| PARAMETER                                                                  | TEST CONDITIONS                                                    | $T_A^\dagger$ | MIN | TYP | MAX  | UNIT |
|----------------------------------------------------------------------------|--------------------------------------------------------------------|---------------|-----|-----|------|------|
| $I_{DD}$ Supply current (per channel)                                      | $V_O = V_{DD}/2$ , $\overline{\text{SHDN}} = V_{DD}$               | 25°C          |     | 730 | 1000 | μA   |
|                                                                            |                                                                    | Full range    |     |     | 1350 |      |
| PSRR Supply voltage rejection ratio<br>( $\Delta V_{DD} / \Delta V_{IO}$ ) | $V_{DD} = 2.7\text{ V}$ to $5.5\text{ V}$ ,<br>$V_{IC} = V_{DD}/2$ | 25°C          | 70  | 90  |      | dB   |
|                                                                            |                                                                    | Full range    | 65  |     |      |      |

$^\dagger$  Full range is –40°C to 125°C for the I-suffix.

electrical characteristics at specified free-air temperature,  $V_{DD} = 2.7\text{ V}$ ,  $5\text{ V}$  (unless otherwise noted)  
(continued)

dynamic performance

| PARAMETER |                                  | TEST CONDITIONS                                                       |                                                         | $T_A^\dagger$ | MIN | TYP | MAX | UNIT             |
|-----------|----------------------------------|-----------------------------------------------------------------------|---------------------------------------------------------|---------------|-----|-----|-----|------------------|
| GBWP      | Gain-bandwidth product           | $R_L = 2\text{ k}\Omega$ , $C_L = 10\text{ pF}$ , $f = 10\text{ kHz}$ |                                                         | 25°C          | 9   |     |     | MHz              |
| SR+       | Positive slew rate at unity gain | $R_L = 2\text{ k}\Omega$ , $C_L = 50\text{ pF}$                       | $V_{DD} = 2.7\text{ V}$ ,<br>$V_{O(PP)} = 1.7\text{ V}$ |               | 6   |     |     | V/ $\mu\text{s}$ |
|           |                                  |                                                                       | $V_{DD} = 5\text{ V}$ ,<br>$V_{O(PP)} = 3.5\text{ V}$   |               | 6   |     |     |                  |
| SR−       | Negative slew rate at unity gain | $R_L = 2\text{ k}\Omega$ , $C_L = 50\text{ pF}$                       | $V_{DD} = 2.7\text{ V}$ ,<br>$V_{O(PP)} = 1.7\text{ V}$ |               | 10  |     |     | V/ $\mu\text{s}$ |
|           |                                  |                                                                       | $V_{DD} = 5\text{ V}$ ,<br>$V_{O(PP)} = 3.5\text{ V}$   |               | 9.5 |     |     | V/ $\mu\text{s}$ |
| $\phi_m$  | Phase margin                     | $R_L = 2\text{ k}\Omega$ , $C_L = 10\text{ pF}$                       |                                                         |               | 50  |     |     | °                |
|           | Gain margin                      |                                                                       |                                                         |               | 20  |     |     | dB               |

$^\dagger$  Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for the I-suffix.

noise/distortion performance

| PARAMETER                                    | TEST CONDITIONS                                                            | $T_A$ | MIN | TYP    | MAX | UNIT                   |
|----------------------------------------------|----------------------------------------------------------------------------|-------|-----|--------|-----|------------------------|
| THD + N Total harmonic distortion plus noise | $V_{O(PP)} = V_{DD}/2$ ,<br>$R_L = 2\text{ k}\Omega$ , $f = 10\text{ kHz}$ | 25°C  |     | 0.003% |     |                        |
|                                              |                                                                            |       |     | 0.02%  |     |                        |
|                                              |                                                                            |       |     | 0.095% |     |                        |
| $V_n$ Equivalent input noise voltage         | $f = 1\text{ kHz}$                                                         |       |     | 50     |     | nV/ $\sqrt{\text{Hz}}$ |
|                                              | $f = 10\text{ kHz}$                                                        |       |     | 30     |     |                        |
| $I_n$ Equivalent input noise current         | $f = 1\text{ kHz}$                                                         |       |     | 0.9    |     | fA/ $\sqrt{\text{Hz}}$ |

shutdown characteristics

| PARAMETER                                                                               | TEST CONDITIONS                                    | $T_A^\dagger$ | MIN | TYP | MAX | UNIT          |
|-----------------------------------------------------------------------------------------|----------------------------------------------------|---------------|-----|-----|-----|---------------|
| $I_{DD(SHDN)}$ Supply current, per channel in shutdown mode (TLV2630, TLV2633, TLV2635) | $\overline{\text{SHDN}} = 0.4\text{ V}$            | 25°C          |     | 4   | 17  | $\mu\text{A}$ |
|                                                                                         |                                                    | Full range    |     |     | 19  |               |
| $t_{(on)}$ Amplifier turnon time $^\ddagger$                                            | $R_L = 2\text{ k}\Omega$ ,<br>$C_L = 10\text{ pF}$ | 25°C          |     | 4.5 |     | $\mu\text{s}$ |
|                                                                                         |                                                    |               |     | 1.5 |     |               |
| $t_{(off)}$ Amplifier turnoff time $^\ddagger$                                          |                                                    |               |     | 200 |     | ns            |

$^\dagger$  Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for the I-suffix.

$^\ddagger$  Disable time and enable time are defined as the interval between application of the logic signal to  $\overline{\text{SHDN}}$  and the point at which the supply current has reached half its final value.

**DISSIPATION RATING TABLE**

| PACKAGE    | $\Theta_{JC}$<br>(°C/W) | $\Theta_{JA}$<br>(°C/W) | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | $T_A = 125^\circ\text{C}$<br>POWER RATING |
|------------|-------------------------|-------------------------|---------------------------------------------|-------------------------------------------|
| D (8)      | 38.3                    | 176                     | 710 mW                                      | 142 mW                                    |
| D (14)     | 26.9                    | 122.3                   | 1022 mW                                     | 204.4 mW                                  |
| D (16)     | 25.7                    | 114.7                   | 1090 mW                                     | 218 mW                                    |
| DBV (5)    | 55                      | 324.1                   | 385 mW                                      | 77.1 mW                                   |
| DBV (6)    | 55                      | 294.3                   | 425 mW                                      | 85 mW                                     |
| DGK (8)    | 54.2                    | 259.9                   | 481 mW                                      | 96.1 mW                                   |
| DGS (10)   | 54.1                    | 259.7                   | 485 mW                                      | 97 mW                                     |
| N (14, 16) | 32                      | 78                      | 1600 mW                                     | 320.5 mW                                  |
| P (8)      | 41                      | 104                     | 1200 mW                                     | 240.4 mW                                  |
| PW (14)    | 29.3                    | 173.6                   | 720 mW                                      | 144 mW                                    |
| PW (16)    | 28.7                    | 161.4                   | 774 mW                                      | 154.9 mW                                  |

## TYPICAL CHARACTERISTICS

**Table of Graphs**

|                |                                              |                              | FIGURE |
|----------------|----------------------------------------------|------------------------------|--------|
| $V_{IO}$       | Input offset voltage                         | vs Common-mode input voltage | 1, 2   |
| CMRR           | Common-mode rejection ratio                  | vs Frequency                 | 3      |
| $V_{OH}$       | High-level output voltage                    | vs High-level output current | 4, 6   |
| $V_{OL}$       | Low-level output voltage                     | vs Low-level output current  | 5, 7   |
| $I_{DD}$       | Supply current                               | vs Supply voltage            | 8      |
| $I_{DD}$       | Supply current                               | vs Free-air temperature      | 9      |
| PSRR           | Power supply rejection ratio                 | vs Frequency                 | 10     |
| $A_{VD}$       | Differential voltage amplification & phase   | vs Frequency                 | 11     |
|                | Gain-bandwidth product                       | vs Supply voltage            | 12     |
|                |                                              | vs Free-air temperature      | 13     |
| SR             | Slew rate                                    | vs Supply voltage            | 14     |
|                |                                              | vs Free-air temperature      | 15, 16 |
| $\phi_m$       | Phase margin                                 | vs Load capacitance          | 17     |
| $V_n$          | Equivalent input noise voltage               | vs Frequency                 | 18     |
|                | Crosstalk                                    | vs Frequency                 | 19     |
|                | Voltage-follower large-signal pulse response |                              | 20     |
|                | Voltage-follower small-signal pulse response |                              | 21     |
| $I_{DD}(SHDN)$ | Shutdown supply current                      | vs Free-air temperature      | 22     |
| $I_{DD}(SHDN)$ | Shutdown supply current                      | vs Supply voltage            | 23     |
| $I_{DD}(SHDN)$ | Shutdown supply current/output voltage       | vs Time                      | 24     |

## TYPICAL CHARACTERISTICS

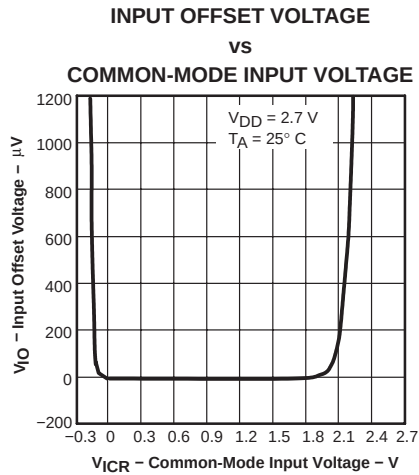


Figure 1

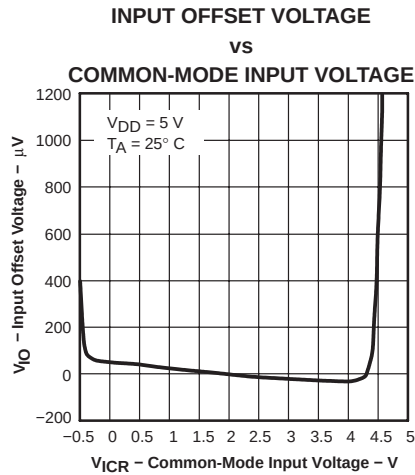


Figure 2

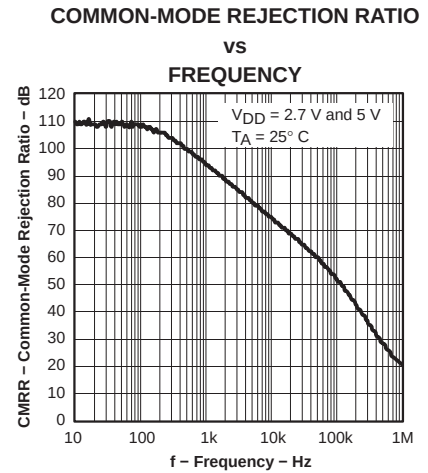


Figure 3

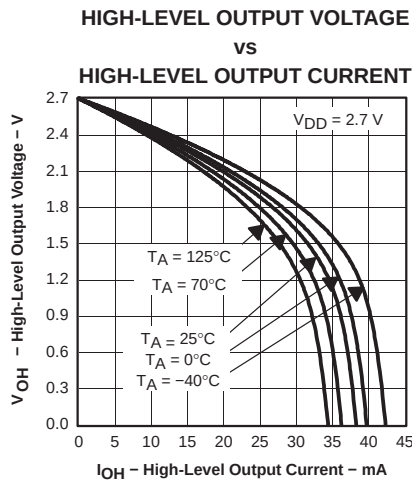


Figure 4

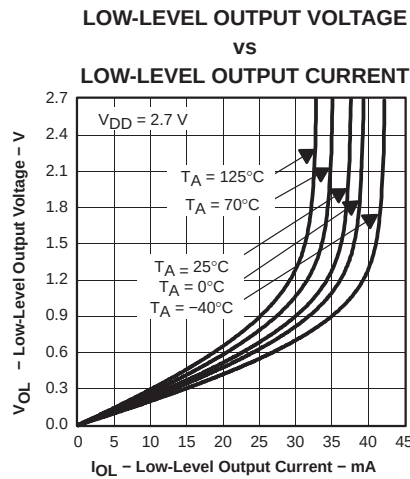


Figure 5

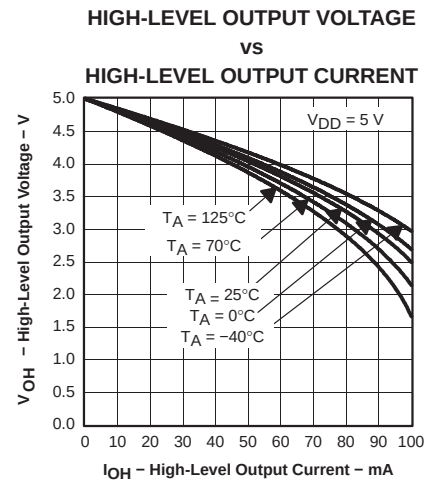


Figure 6

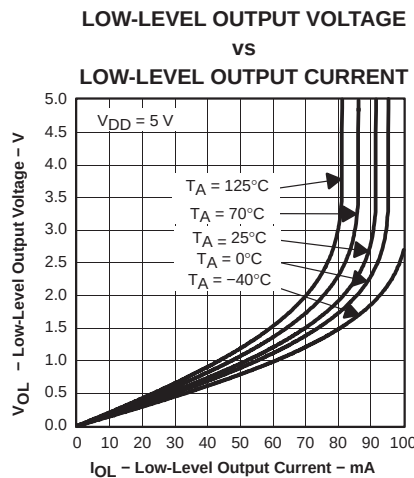


Figure 7

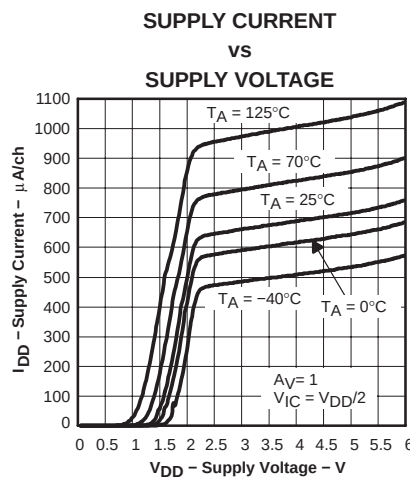


Figure 8

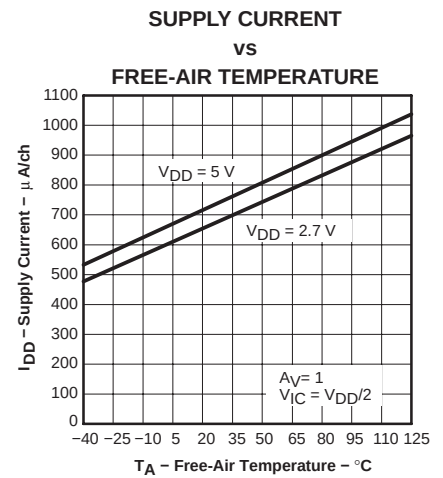


Figure 9

## TYPICAL CHARACTERISTICS

POWER SUPPLY REJECTION RATIO

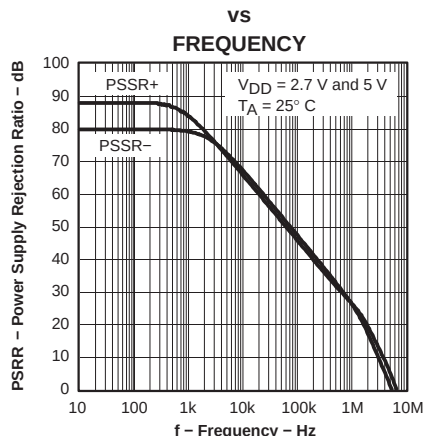


Figure 10

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE

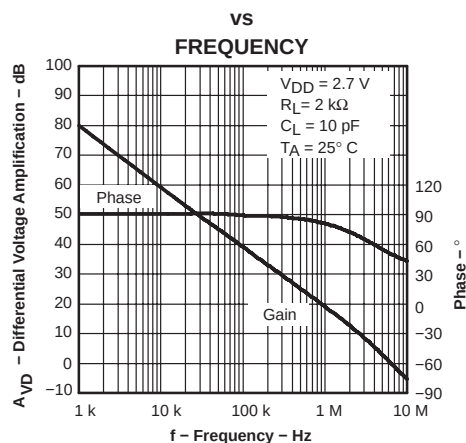


Figure 11

GAIN-BANDWIDTH PRODUCT

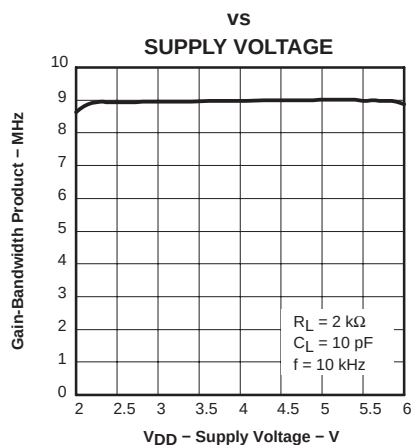


Figure 12

GAIN-BANDWIDTH PRODUCT

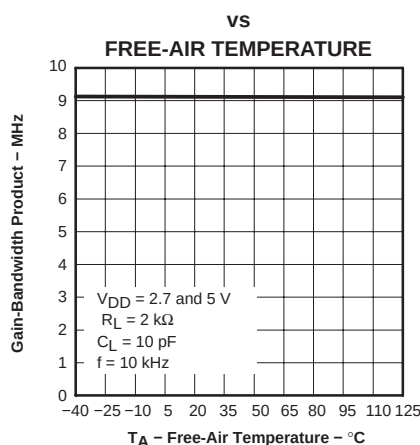


Figure 13

SLEW RATE

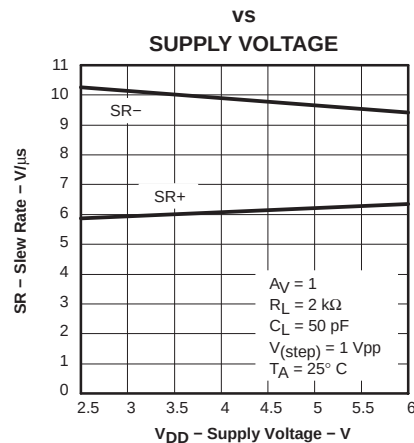


Figure 14

SLEW RATE

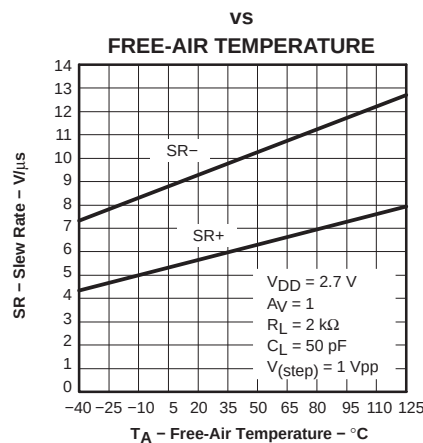


Figure 15

SLEW RATE

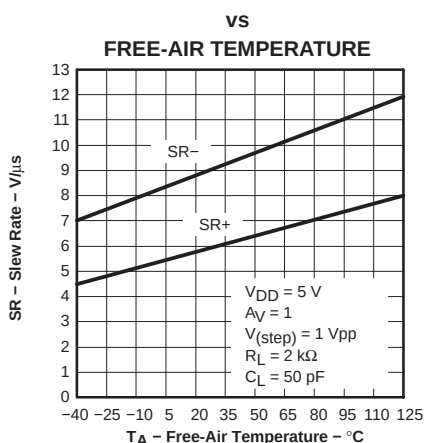


Figure 16

PHASE MARGIN

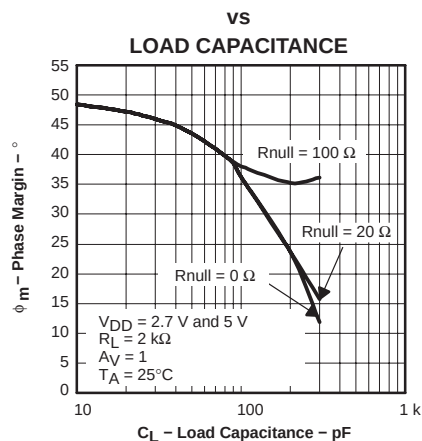


Figure 17



## TYPICAL CHARACTERISTICS

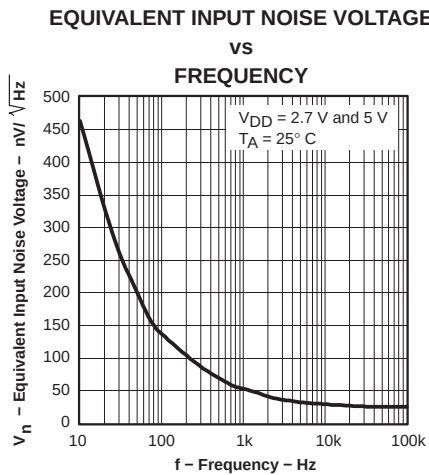


Figure 18

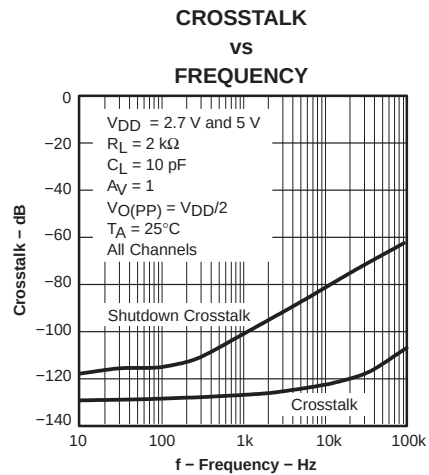


Figure 19

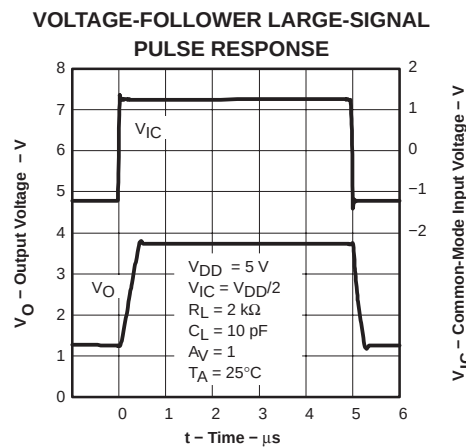


Figure 20

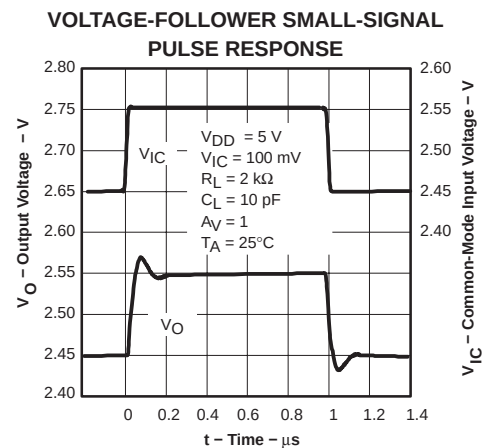


Figure 21

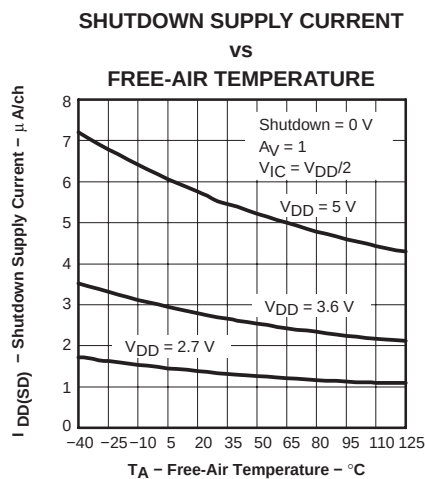


Figure 22

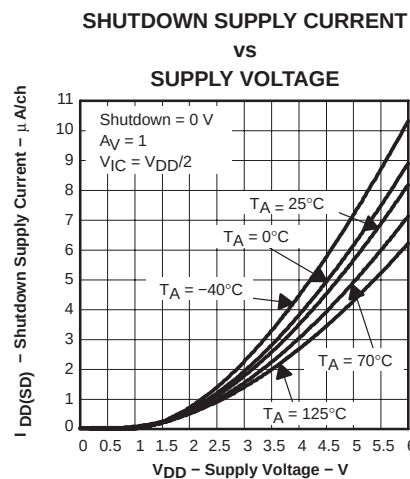


Figure 23

## TYPICAL CHARACTERISTICS

### SHUTDOWN SUPPLY CURRENT / OUTPUT VOLTAGE vs TIME

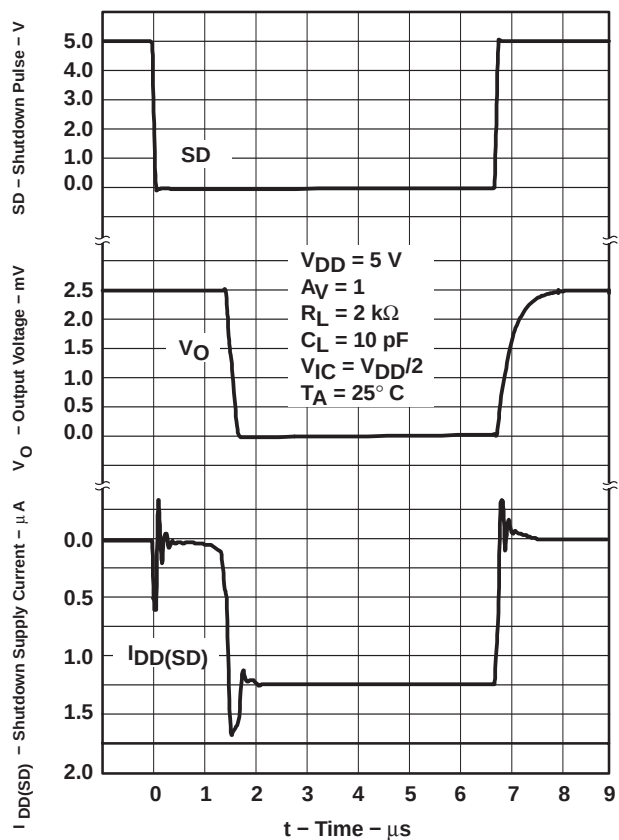
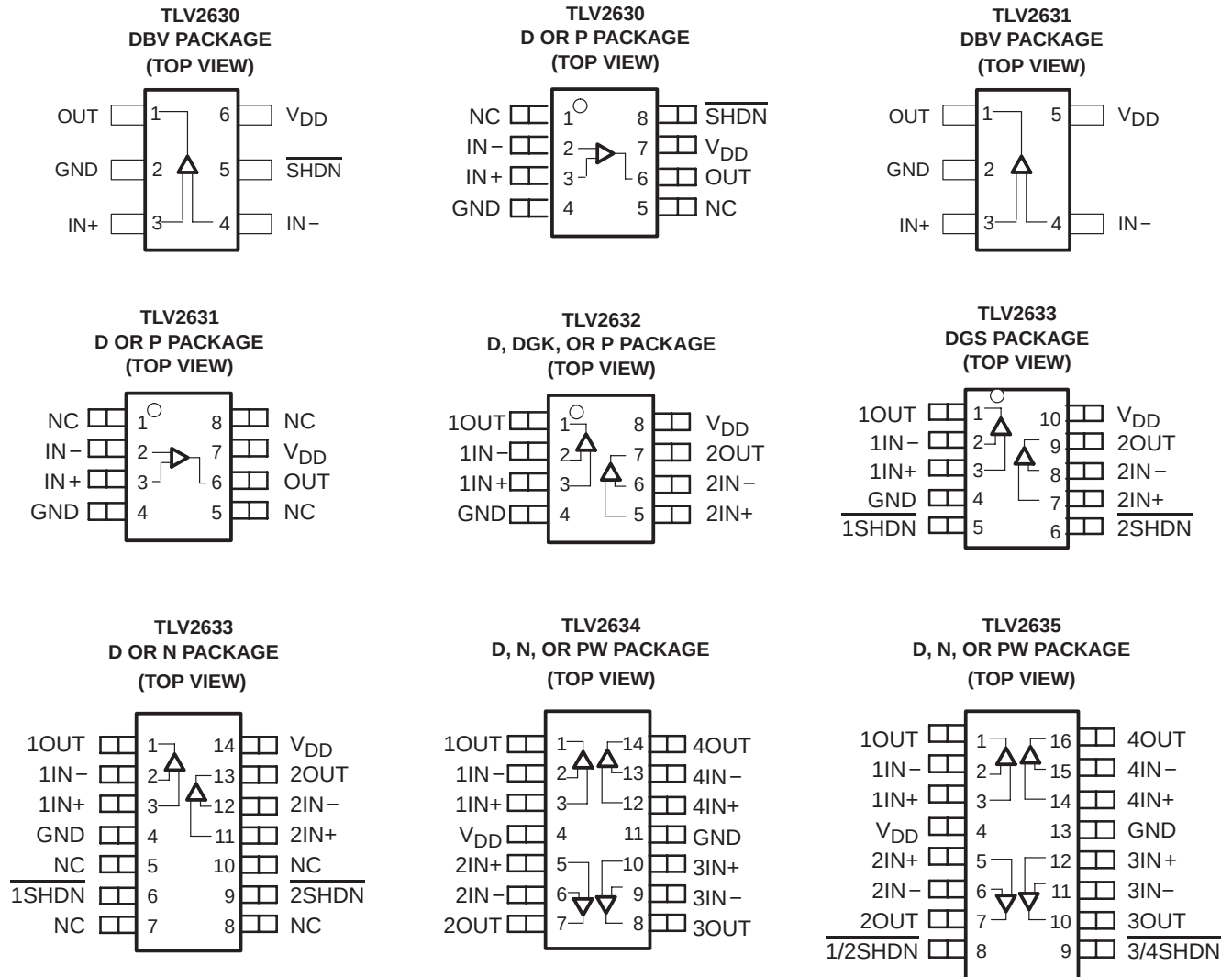


Figure 24

## TLV263x PACKAGE PINOUTS



NC – No internal connection

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV2630IDBVR     | ACTIVE        | SOT-23       | DBV                | 6    | 3000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | VAYI                    | <a href="#">Samples</a> |
| TLV2631IDBVR     | ACTIVE        | SOT-23       | DBV                | 5    | 3000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | VAZI                    | <a href="#">Samples</a> |
| TLV2631IDBVT     | ACTIVE        | SOT-23       | DBV                | 5    | 250            | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | VAZI                    | <a href="#">Samples</a> |
| TLV2632IDGKR     | ACTIVE        | VSSOP        | DGK                | 8    | 2500           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | AKG                     | <a href="#">Samples</a> |
| TLV2632IDR       | ACTIVE        | SOIC         | D                  | 8    | 2500           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2632I                   | <a href="#">Samples</a> |
| TLV2634ID        | ACTIVE        | SOIC         | D                  | 14   | 50             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2634I                   | <a href="#">Samples</a> |
| TLV2634IPWR      | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2634I                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

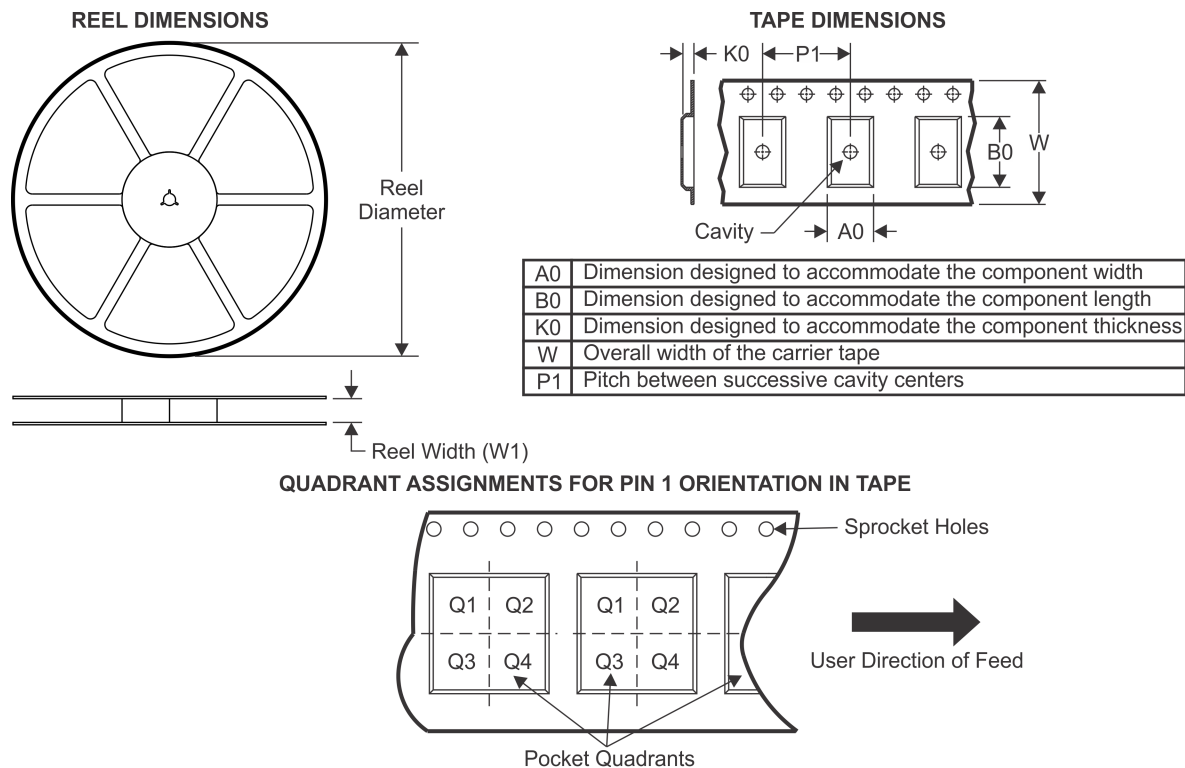
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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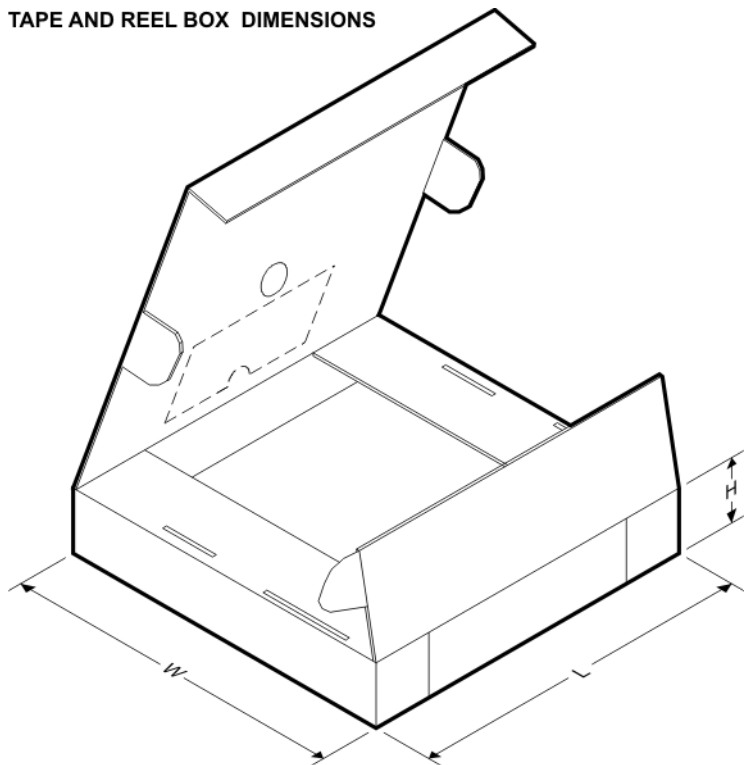
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV2630IDBVR | SOT-23       | DBV             | 6    | 3000 | 180.0              | 9.0                | 3.15    | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TLV2631IDBVR | SOT-23       | DBV             | 5    | 3000 | 180.0              | 9.0                | 3.15    | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TLV2631IDBVT | SOT-23       | DBV             | 5    | 250  | 180.0              | 9.0                | 3.15    | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TLV2632IDGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TLV2632IDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TLV2634IPWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV2630IDBVR | SOT-23       | DBV             | 6    | 3000 | 182.0       | 182.0      | 20.0        |
| TLV2631IDBVR | SOT-23       | DBV             | 5    | 3000 | 182.0       | 182.0      | 20.0        |
| TLV2631IDBVT | SOT-23       | DBV             | 5    | 250  | 182.0       | 182.0      | 20.0        |
| TLV2632IDGKR | VSSOP        | DGK             | 8    | 2500 | 358.0       | 335.0      | 35.0        |
| TLV2632IDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TLV2634IPWR  | TSSOP        | PW              | 14   | 2000 | 853.0       | 449.0      | 35.0        |



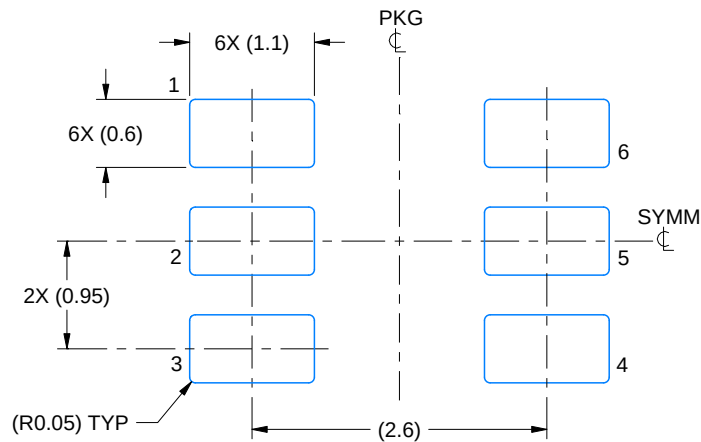


# EXAMPLE BOARD LAYOUT

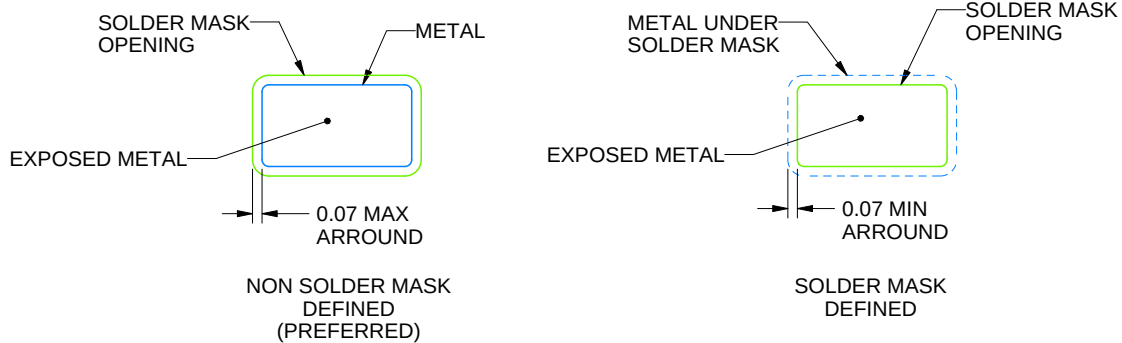
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

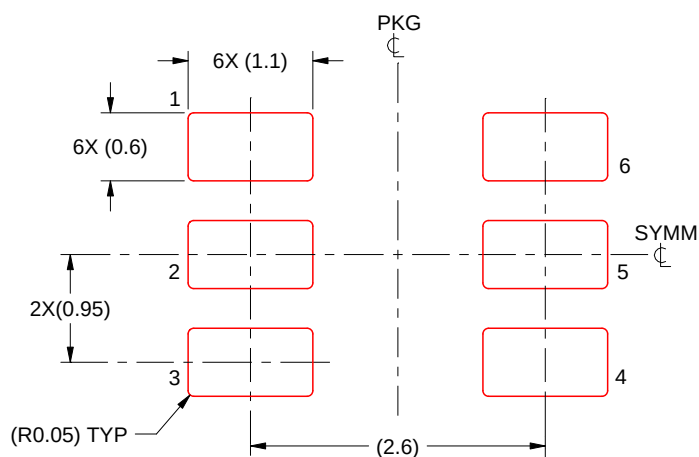
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

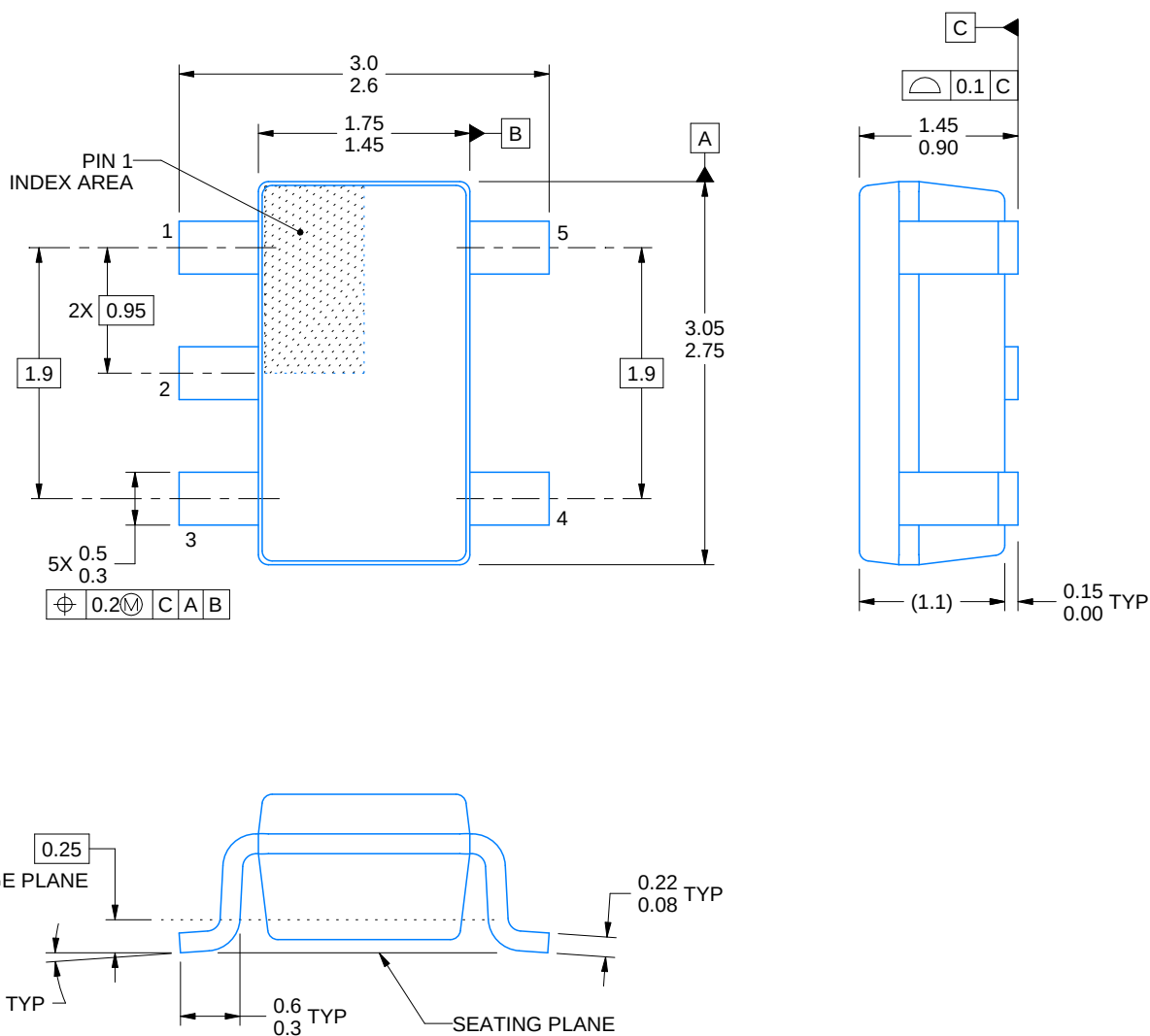


DBV0005A

# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/E 09/2019

## NOTES:

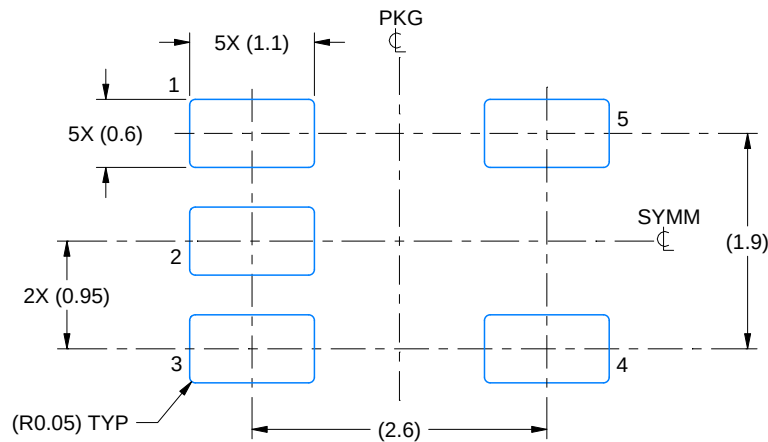
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

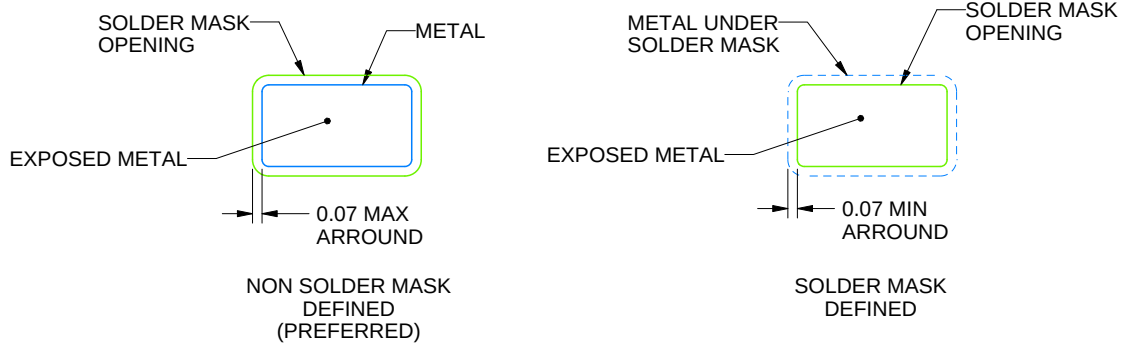
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

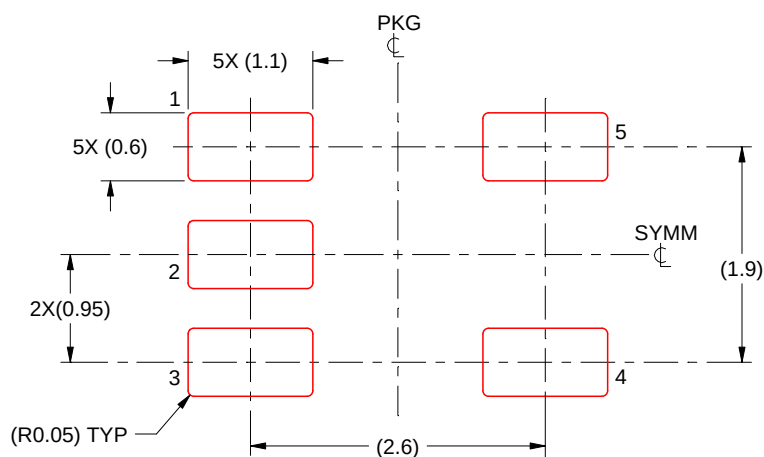
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

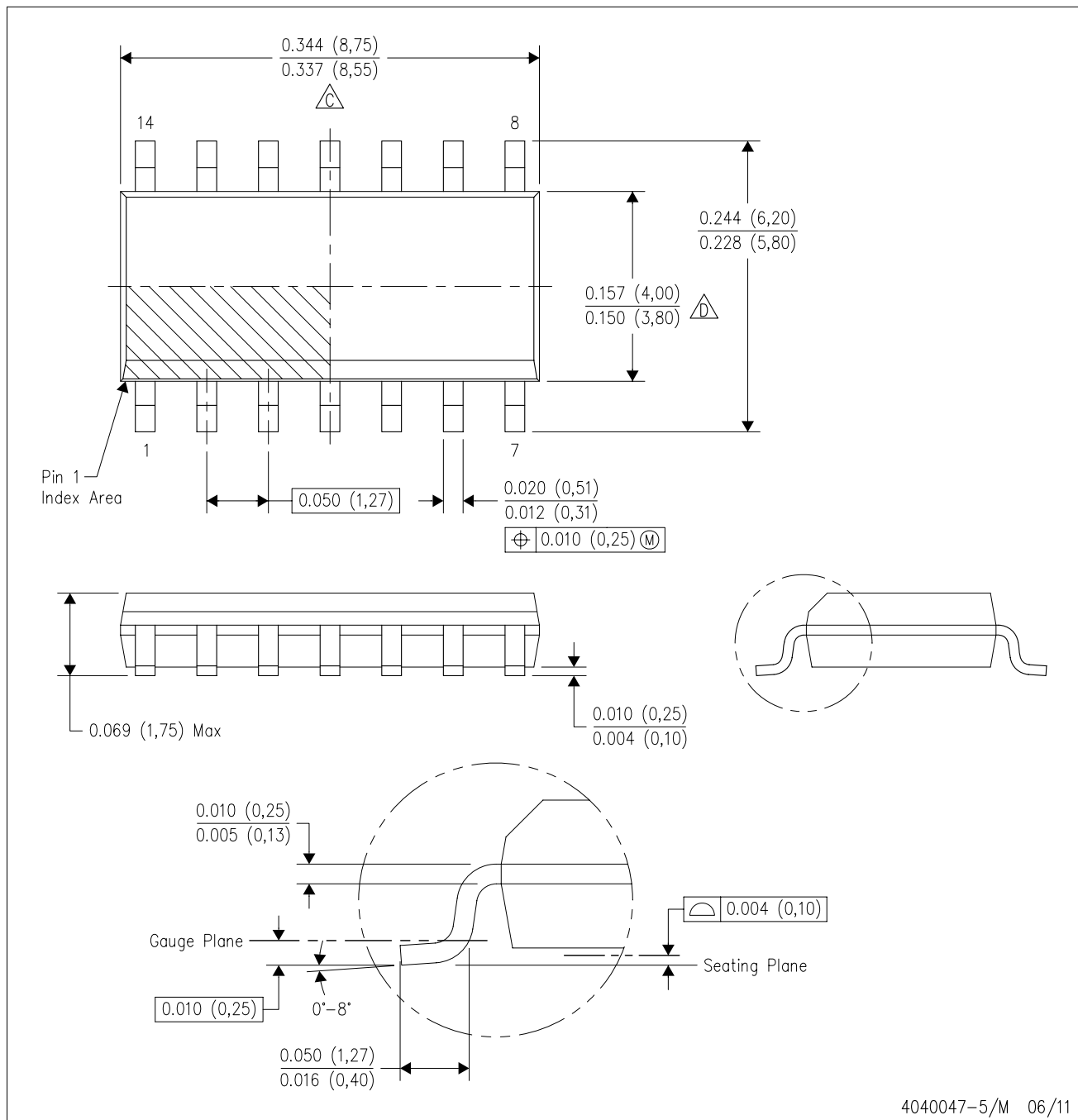
4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



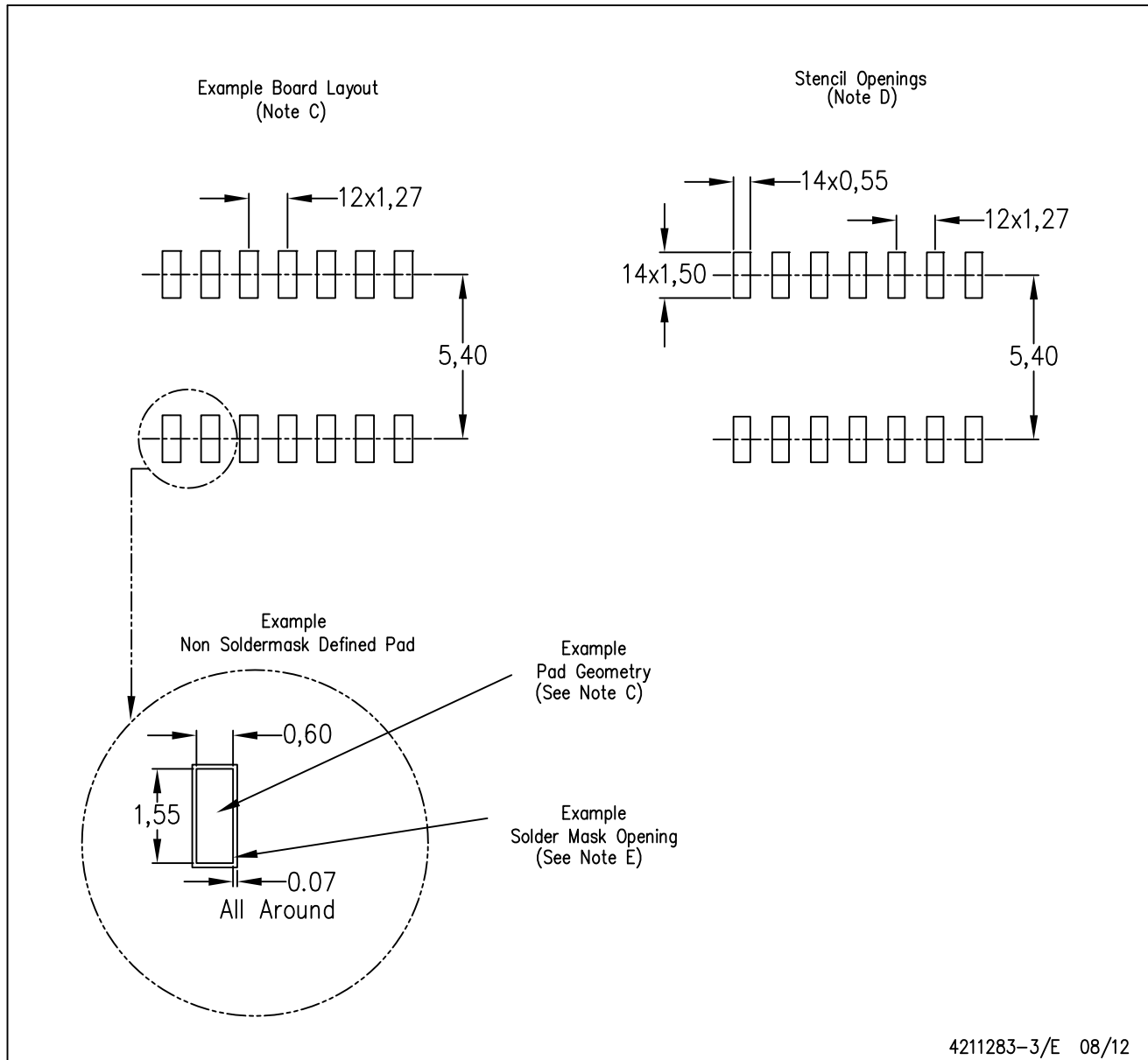
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

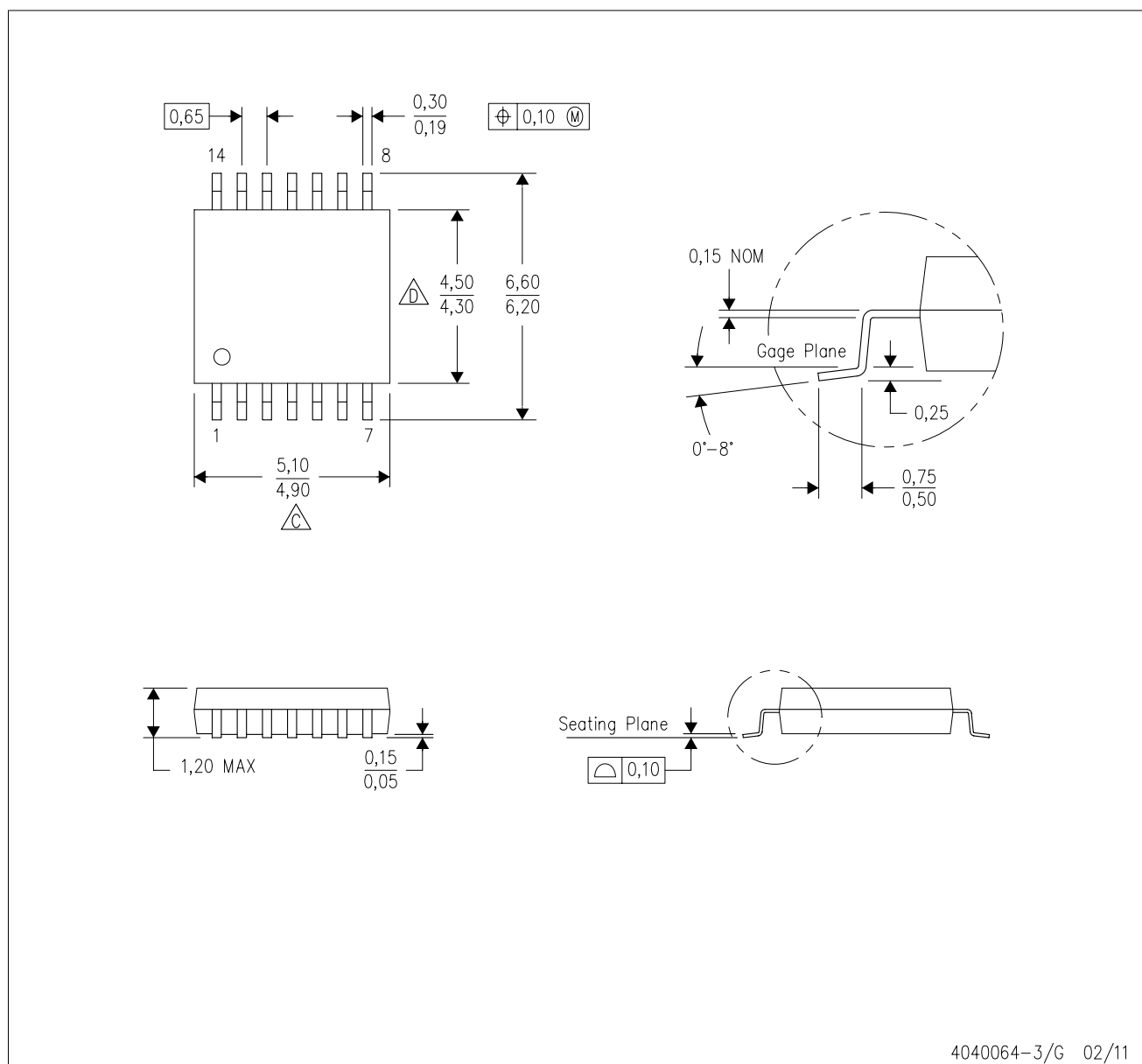
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

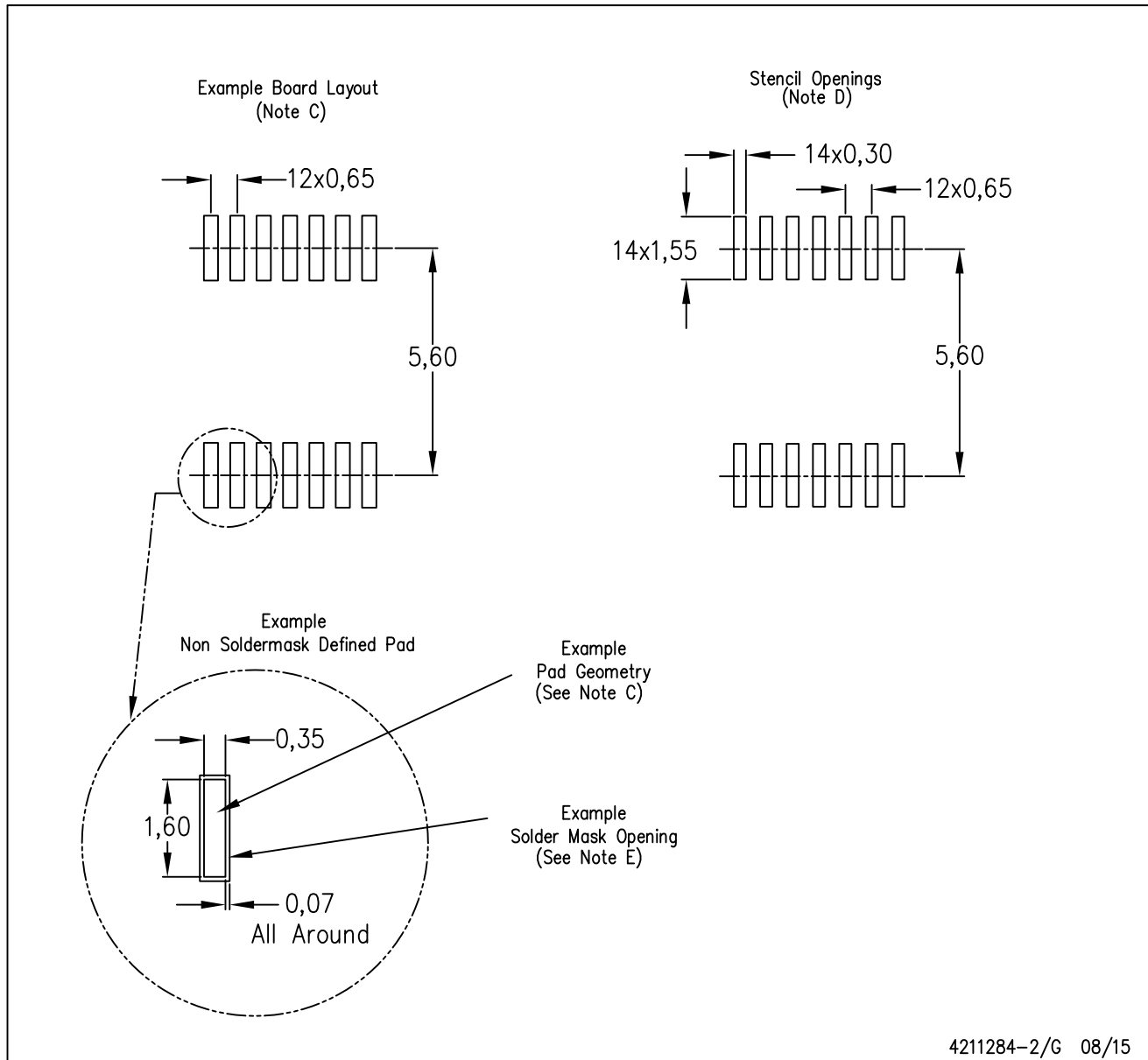


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

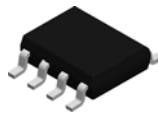


PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

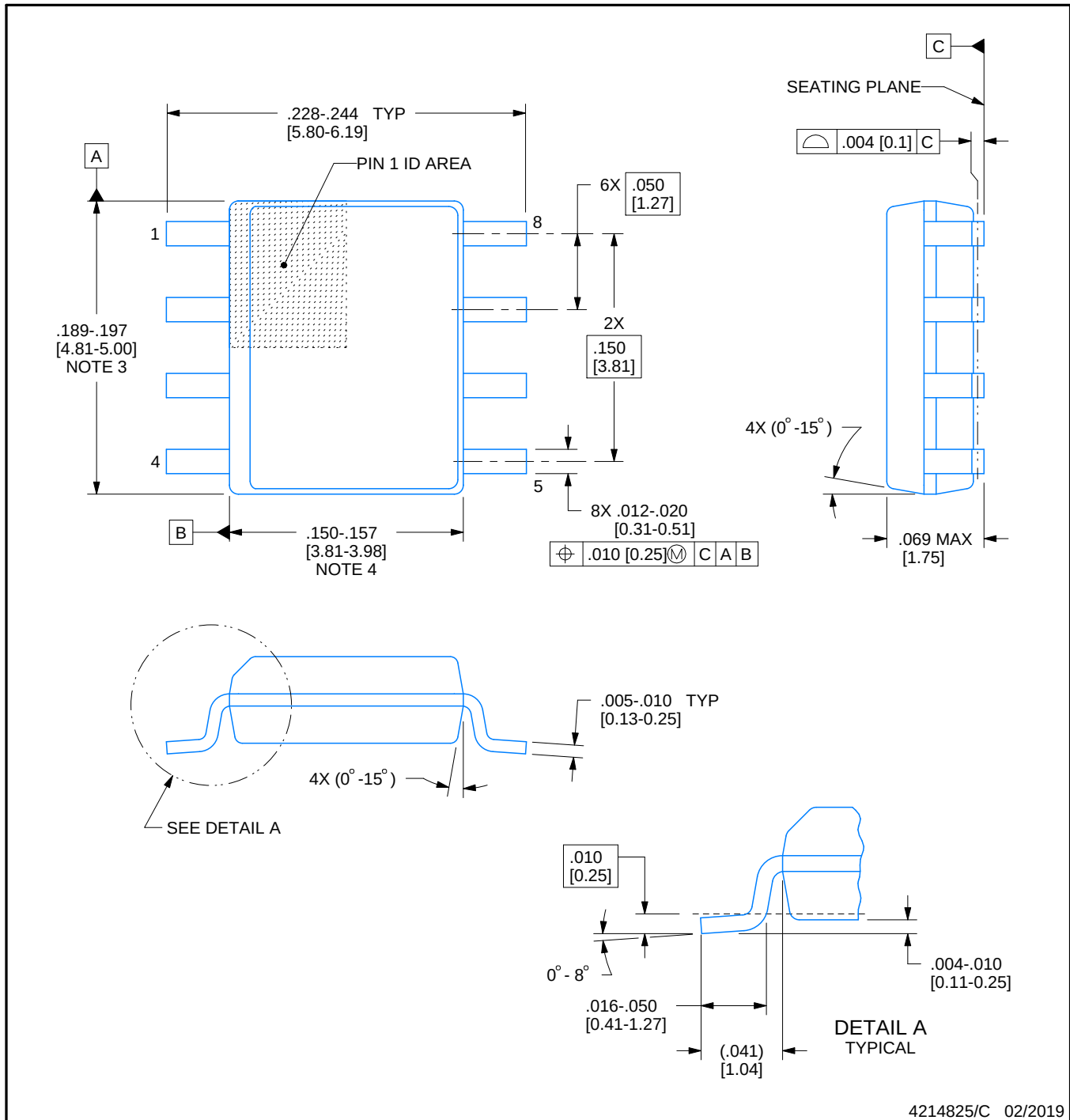


**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

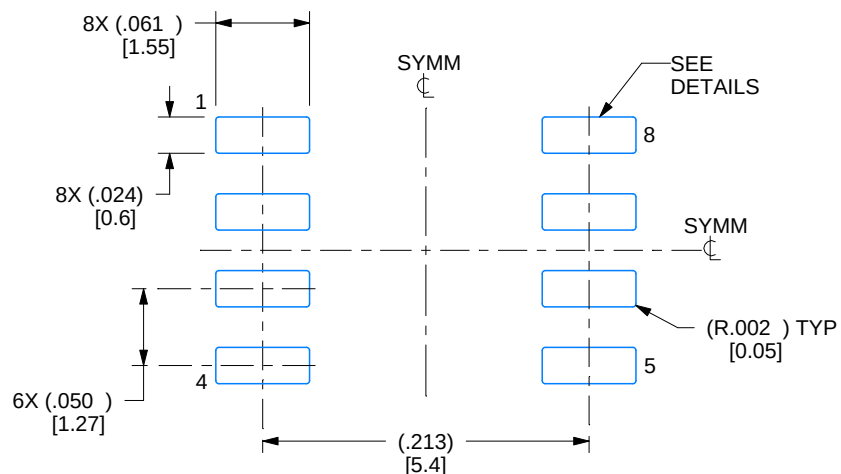
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

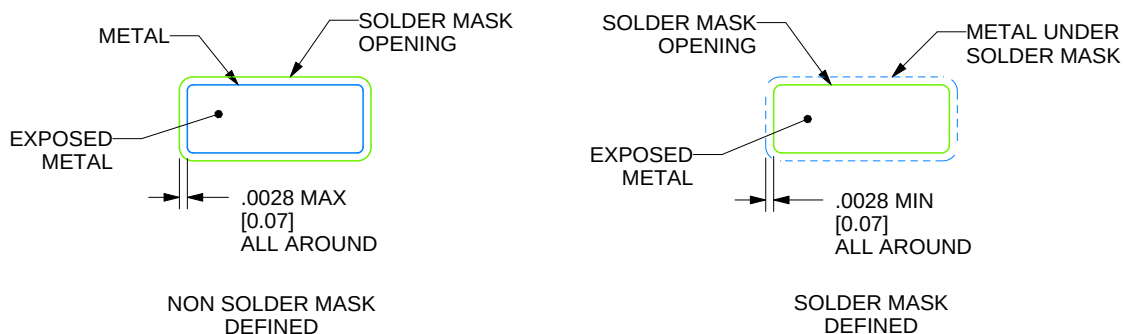
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

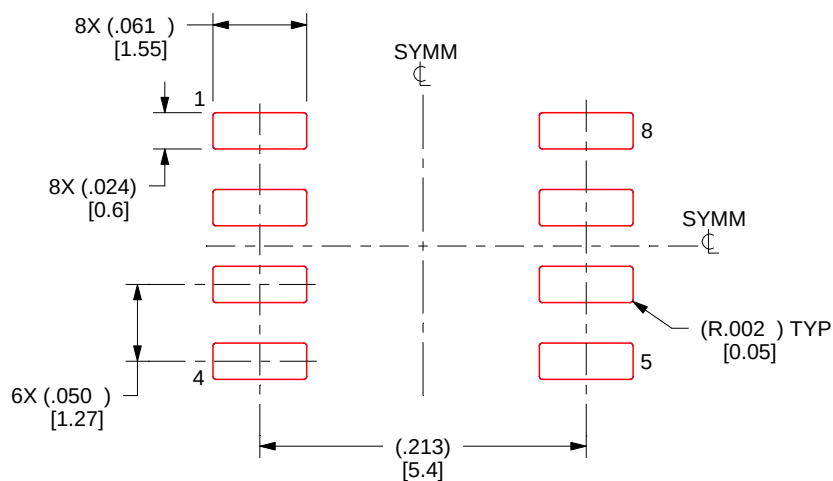
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

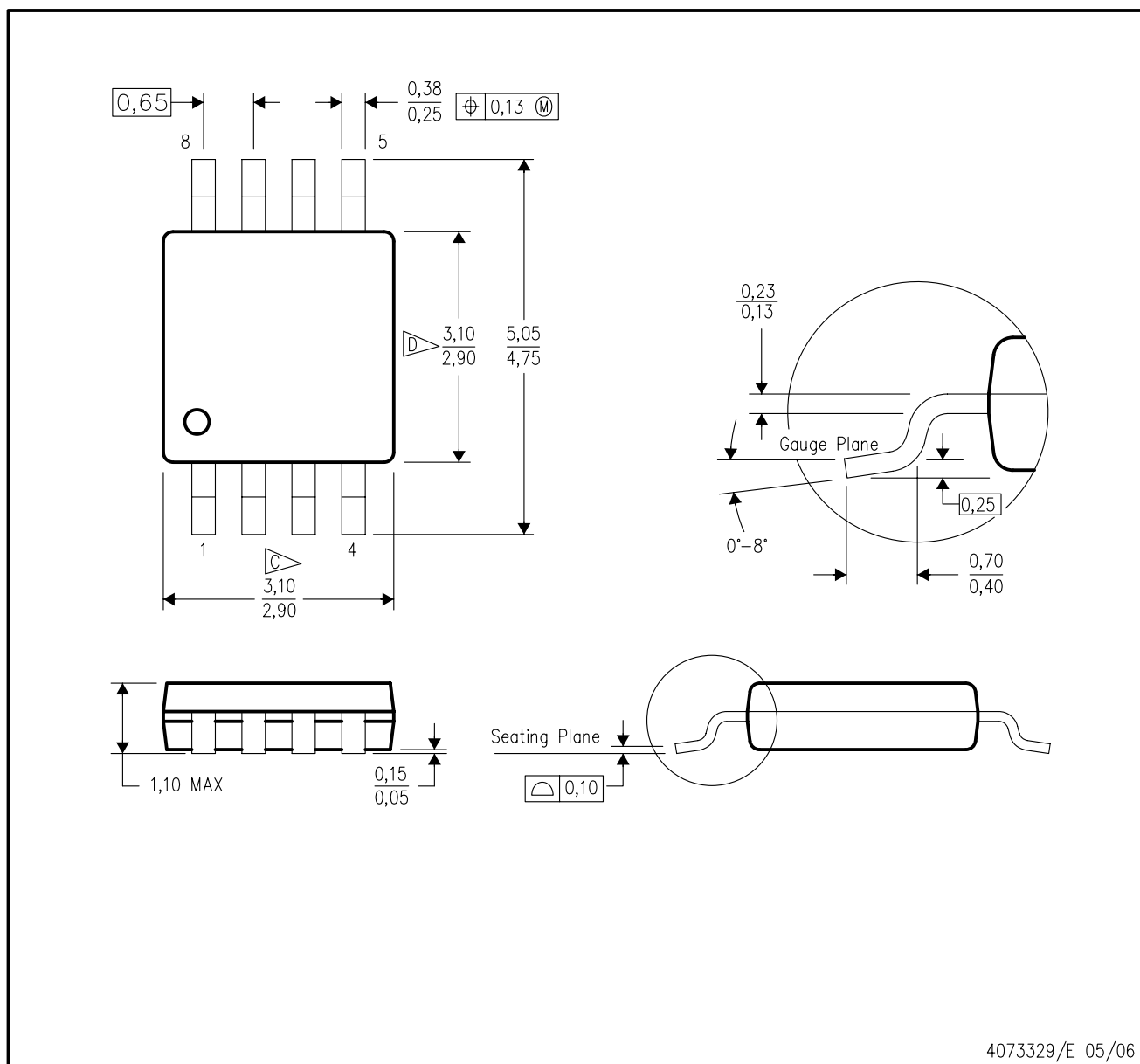
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

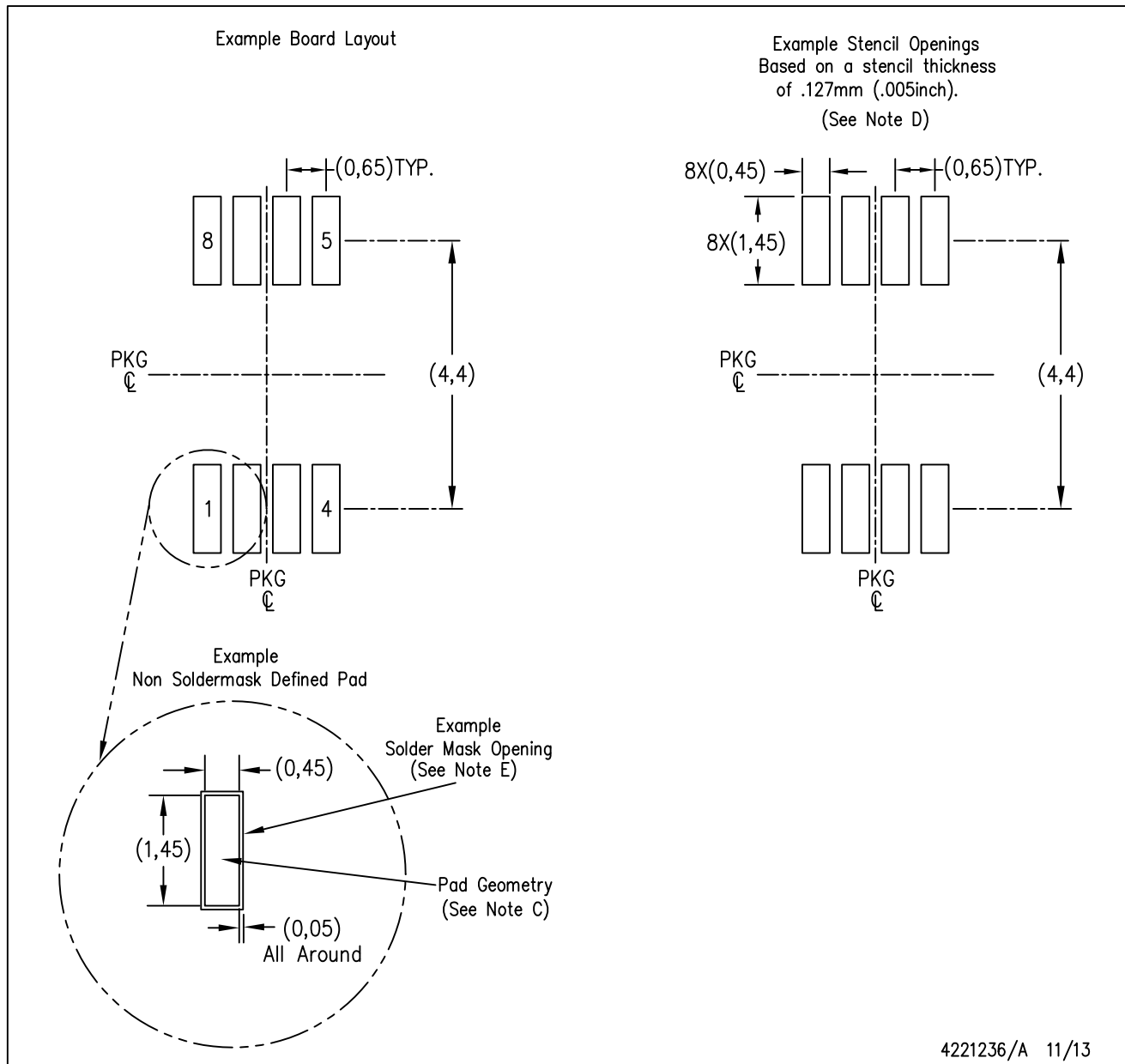
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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