

# TLV9051/TLV9052/TLV9054 5MHz 15V/μs 高压摆率 RRIO 运算放大器

## 1 特性

- 高压摆率：15V/μs
- 低静态电流：330μA
- 轨至轨输入和输出
- 低输入失调电压：±0.33mV
- 单位增益带宽：5MHz
- 低宽带噪声：15nV/√Hz
- 低输入偏置电流：2pA
- 单位增益稳定
- 内置 RFI 和 EMI 滤波器
- 可扩展 CMOS 运算放大器系列，适用于低成本应用
- 可在电源电压低至 1.8V 的情况下运行
- 工作温度范围：-40°C 至 125°C

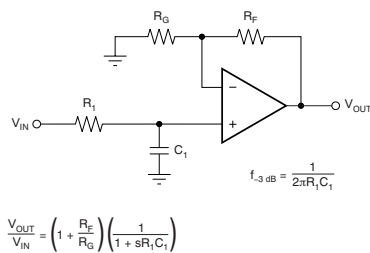
## 2 应用

- HVAC：暖通空调
- 光电二极管放大器
- 用于实现直流电机控制的电流分流监控
- 白色家电（冰箱、洗衣机等）
- 传感器信号调节
- 有源滤波器
- 低侧电流检测

## 3 说明

TLV9051、TLV9052 和 TLV9054 器件分别为单通道、双通道和四通道的运算放大器。这些器件经过优化，可在低至 1.8V 至 5.5V 的电压下运行。它们可以在非常高的压摆率下实现轨至轨输入和输出。这些器件非常适合需要高工作电压、高压摆率和低静态电流的成本受限型应用。TLV905x 系列的容性负载驱动器具有 150pF 的电容，而电阻式开环输出阻抗使其能够在更高的容性负载下更轻松地实现稳定。

### 单极低通滤波器



TLV905xS 器件具有关断模式，允许放大器切换至典型电流消耗低于 1μA 的待机模式。

TLV905x 系列易于使用，因为它具有稳定的单位增益，集成了 RFI 和 EMI 滤波器，且不会在过驱动情况下出现相位反转。

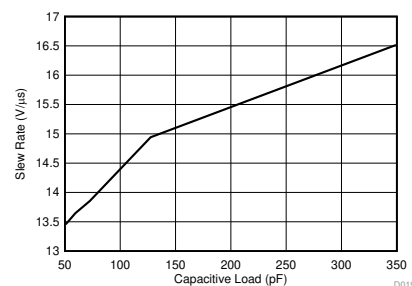
### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸（标称值）
TLV9051	SOT-23 (5)	1.60mm × 2.90mm
	SC70 (5)	1.25mm × 2.00mm
	SOT553 (5) <sup>(2)</sup>	1.65mm × 1.20mm
	X2SON (5)	0.80mm × 0.80mm
TLV9051S	SOT-23 (6)	1.60mm × 2.90mm
TLV9052	SOIC (8)	3.91mm × 4.90mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
	SOT-23 (8)	1.60mm × 2.90mm
	WSON (8)	2.00mm × 2.00mm
TLV9052S	VSSOP (10)	3.00mm × 3.00mm
	X2QFN (10)	1.50mm × 2.00mm
TLV9054	SOIC (14)	8.65mm × 3.91mm
	TSSOP (14)	4.40mm × 5.00mm
	X2QFN (14)	2.00mm × 2.00mm
	WQFN (16)	3.00mm × 3.00mm
TLV9054S	WQFN (16)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装仅供预览。

### 压摆率与负载电容间的关系



## 目录

<b>1</b>	<b>特性</b> .....	<b>1</b>	8.3	Feature Description .....	<b>24</b>
<b>2</b>	<b>应用</b> .....	<b>1</b>	8.4	Device Functional Modes .....	<b>27</b>
<b>3</b>	<b>说明</b> .....	<b>1</b>	<b>9</b>	<b>Application and Implementation</b> .....	<b>28</b>
<b>4</b>	<b>修订历史记录</b> .....	<b>2</b>	9.1	Application Information .....	<b>28</b>
<b>5</b>	<b>Device Comparison Table</b> .....	<b>4</b>	9.2	Typical Low-Side Current Sense Application .....	<b>28</b>
<b>6</b>	<b>Pin Configuration and Functions</b> .....	<b>5</b>	<b>10</b>	<b>Power Supply Recommendations</b> .....	<b>30</b>
<b>7</b>	<b>Specifications</b> .....	<b>12</b>	<b>11</b>	<b>Layout</b> .....	<b>31</b>
7.1	Absolute Maximum Ratings .....	<b>12</b>	11.1	Layout Guidelines .....	<b>31</b>
7.2	ESD Ratings .....	<b>12</b>	11.2	Layout Example .....	<b>32</b>
7.3	Recommended Operating Conditions .....	<b>12</b>	<b>12</b>	<b>器件和文档支持</b> .....	<b>33</b>
7.4	Thermal Information for Single Channel .....	<b>12</b>	12.1	文档支持 .....	<b>33</b>
7.5	Thermal Information for Dual Channel .....	<b>13</b>	12.2	相关链接 .....	<b>33</b>
7.6	Thermal Information for Quad Channel .....	<b>13</b>	12.3	接收文档更新通知 .....	<b>33</b>
7.7	Electrical Characteristics: $V_S$ (Total Supply Voltage) = ( $V_+$ ) – ( $V_-$ ) = 1.8 V to 5.5 V .....	<b>14</b>	12.4	社区资源 .....	<b>33</b>
7.8	Typical Characteristics .....	<b>16</b>	12.5	商标 .....	<b>33</b>
<b>8</b>	<b>Detailed Description</b> .....	<b>23</b>	12.6	静电放电警告 .....	<b>33</b>
8.1	Overview .....	<b>23</b>	12.7	Glossary .....	<b>33</b>
8.2	Functional Block Diagram .....	<b>23</b>	<b>13</b>	<b>机械、封装和可订购信息</b> .....	<b>34</b>

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision G (September 2019) to Revision H	Page
Added new human-body model and charged-device model ratings for TLV9051 X2SON package to the <i>ESD Ratings</i> ...	<b>12</b>
已添加 <i>Packages With an Exposed Thermal Pad</i> section to <i>Feature Description</i> section .....	<b>25</b>

Changes from Revision F (June 2019) to Revision G	Page
已删除 删除了所有 TLV9051 封装的预览标签 .....	<b>1</b>
已删除 删除了 TLV9052 SOT-23 (8) - DDF 封装的预览标签 .....	<b>1</b>
Added link to <i>Shutdown Function</i> section in all of the $\overline{\text{SHDN}}$ pin function rows .....	<b>6</b>
已添加 <i>EMI Rejection</i> section to <i>Feature Description</i> section .....	<b>24</b>
已添加 clarification to the <i>Shutdown Function</i> section .....	<b>26</b>

Changes from Revision E (May 2019) to Revision F	Page
已删除 在器件信息 中删除了 TLV9052S 器件的封装预览符号 .....	<b>1</b>
Deleted package preview notation for TLV9052S devices under <i>Device Comparison Table</i> .....	<b>4</b>
Deleted package preview notation for TLV9052S devices in <i>Device Comparison Table</i> .....	<b>4</b>
Deleted package preview notation for TLV9052S in <i>Pin Configuration and Functions</i> section .....	<b>8</b>
Deleted package preview notation for TLV9052S under <i>Thermal Information for Dual Channel</i> .....	<b>13</b>

Changes from Revision D (April 2019) to Revision E	Page
Added DDF (SOT-23) information to <i>Thermal Information for Dual Channel</i> table .....	<b>13</b>

---

**Changes from Revision C (April 2019) to Revision D**
**Page**


---

• 已删除 在器件信息 中删除了 TLV9054/S 器件的预览符号 .....	1
• Deleted preview notations for TLV9054 devices in <i>Device Comparison Table</i> .....	4
• Deleted preview notations for TLV9054S device in <i>Device Comparison Table</i> .....	4
• Deleted preview notations for TLV9054 packages in <i>Pin Configurations and Functions</i> section .....	9
• Deleted preview notation for TLV9054S RTE package in <i>Pin Configurations and Functions</i> section .....	11
• Deleted preview notation for TLV9054/S packages in <i>Thermal Information for Quad Channel</i> .....	13

---



---

**Changes from Revision B (March 2019) to Revision C**
**Page**


---

• Added TLV9051 thermal information for DPW, DBV, and DCK packages .....	12
--	----

---



---

**Changes from Revision A (December 2018) to Revision B**
**Page**


---

• 已添加 在说明 部分中添加了关断器件注意事项.....	1
• 已添加 向器件信息 添加了 SOT-23 (8) 封装.....	1
• 已添加 向器件信息 中添加了关断器件 .....	1
• 已添加 向 TLV9054 器件信息 中添加了 X2QFN (RUC) 封装 .....	1
• Added DDF package information to <i>Device Comparison Table</i> .....	4
• Added Shutdown devices (TLV9051S/TLV9052S/TLV9054S) and packages (DGS/RUG/RTE) to <i>Device Comparison Table</i> .....	4
• Added TLV9051S pinout information to <i>Pin Configurations and Functions</i> section.....	6
• Added DDF (SOT-23) package .....	7
• Added TLV9052S pinout information to <i>Pin Configurations and Functions</i> section.....	8
• Added TLV9054S and TLV9054 X2QFN (RUC) pinout information to <i>Pin Configurations and Functions</i> section.....	9
• Added TLV9051 and TLV9051S thermal information to <i>Thermal Information for Single Channel</i> .....	12
• Added TLV9052S thermal info to <i>Thermal Information for Dual Channel</i> .....	13
• Added DDF (SOT-23) package to <i>Thermal Information for Dual Channel</i> .....	13
• Added TLV9054 and TLV9054S thermal information to <i>Thermal Information for Quad Channel</i> .....	13
• 已添加 Shutdown Function information in <i>Feature Description</i> section .....	26
• 已添加 向相关链接 中添加了“S”后缀以反映新增了关断器件.....	33

---



---

**Changes from Original (August 2018) to Revision A**
**Page**


---

• 已更改 将器件状态从高级信息 更改为生产数据.....	1
-------------------------------	---

---

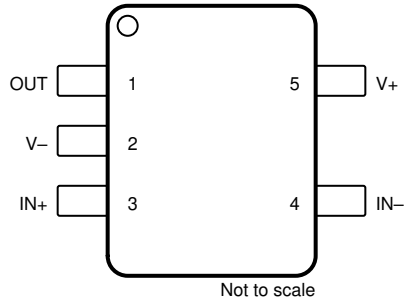
## 5 Device Comparison Table

DEVICE	NO. OF CH.	PACKAGE LEADS												
		SC70 DCK	SOT-23 DBV	SOT-553 <sup>(1)</sup> DRL	X2SON DPW	SOIC D	WSO DSG	VSSOP DGK	TSSOP PW	SOT-23 DDF	VSSOP DGS	X2QFN RUG	X2QFN RUC	WQFN RTE
TLV9051	1	5	5	5	5	—	—	—	—	—	—	—	—	—
TLV9051S		—	6	—	—	—	—	—	—	—	—	—	—	—
TLV9052	2	—	—	—	—	8	8	8	8	8	—	—	—	—
TLV9052S		—	—	—	—	—	—	—	—	—	10	10	—	—
TLV9054	4	—	—	—	—	14	—	—	14	—	—	—	14	16
TLV9054S		—	—	—	—	—	—	—	—	—	—	—	—	16

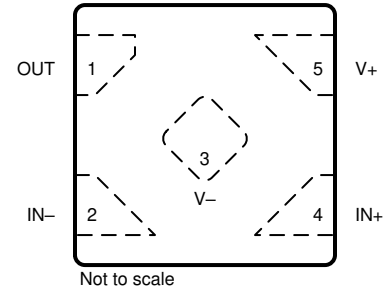
(1) Package is for preview only.

## 6 Pin Configuration and Functions

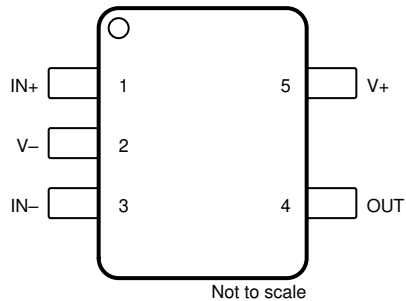
**TLV9051 DBV, DRL Packages**  
**5-Pin SOT-23, SOT-553**  
**Top View**



**TLV9051 DPW Package**  
**5-Pin X2SON**  
**Top View**

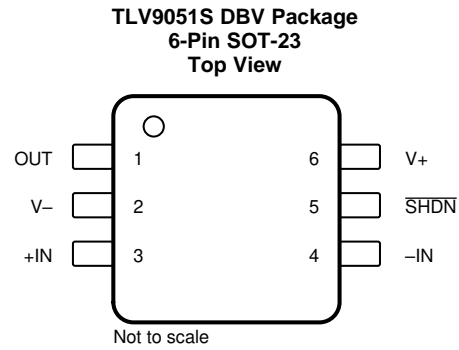


**TLV9051 DCK Package**  
**5-Pin SC70**  
**Top View**



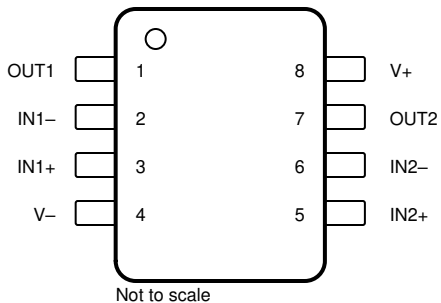
**Pin Functions: TLV9051**

NAME	PIN			I/O	DESCRIPTION
	SOT-23, SOT-553	SC-70	X2SON		
IN–	4	3	2	I	Inverting input
IN+	3	1	4	I	Noninverting input
OUT	1	4	1	O	Output
V–	2	2	3	—	Negative (low) supply or ground (for single-supply operation)
V+	5	5	5	—	Positive (high) supply

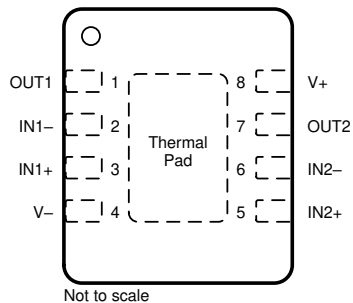

**Pin Functions: TLV9051S**

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN	4	I	Inverting input
+IN	3	I	Noninverting input
OUT	1	O	Output
$\overline{\text{SHDN}}$	5	I	Shutdown: low = amp disabled, high = amp enabled. See <a href="#">Shutdown Function</a> section for more information.
V-	2	—	Negative (lowest) supply or ground (for single-supply operation).
V+	6	—	Positive (highest) supply

**TLV9052 D, DGK, PW, DDF Packages  
8-Pin SOIC, VSSOP, TSSOP, SOT-23  
Top View**



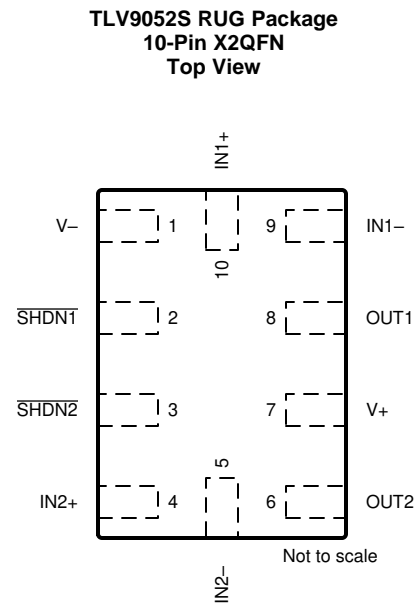
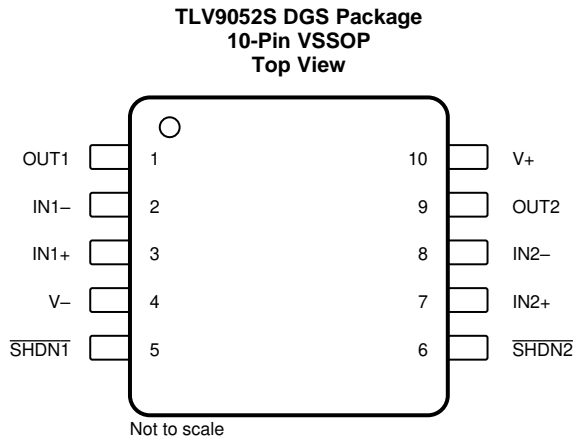
**TLV9052 DSG Package  
8-Pin WSON With Exposed Thermal Pad  
Top View**



Connect exposed thermal pad to V-. See [Packages With an Exposed Thermal Pad](#) section for more information.

**Pin Functions: TLV9052**

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	—	Negative (low) supply or ground (for single-supply operation)
V+	8	—	Positive (high) supply

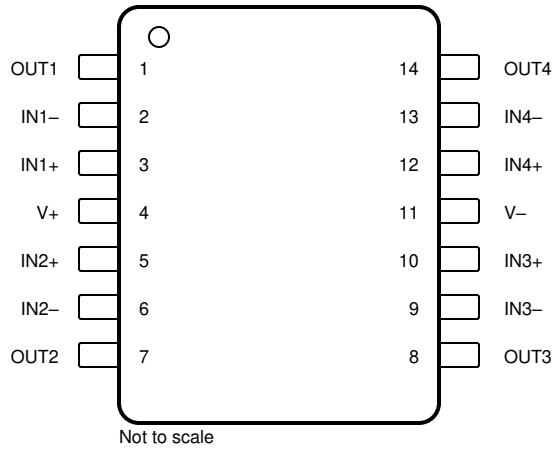


### Pin Functions: TLV9052S

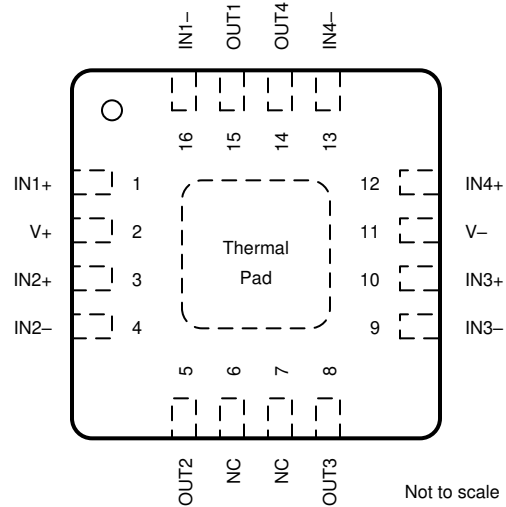
PIN			I/O	DESCRIPTION
NAME	VSSOP	X2QFN		
IN1–	2	9	I	Inverting input, channel 1
IN1+	3	10	I	Noninverting input, channel 1
IN2–	8	5	I	Inverting input, channel 2
IN2+	7	4	I	Noninverting input, channel 2
OUT1	1	8	O	Output, channel 1
OUT2	9	6	O	Output, channel 2
$\overline{\text{SHDN1}}$	5	2	I	Shutdown: low = amp disabled, high = amp enabled, channel 1. See <a href="#">Shutdown Function</a> section for more information.
$\overline{\text{SHDN2}}$	6	3	I	Shutdown: low = amp disabled, high = amp enabled, channel 2. See <a href="#">Shutdown Function</a> section for more information.
V–	4	1	—	Negative (low) supply or ground (for single-supply operation)
V+	10	7	—	Positive (high) supply



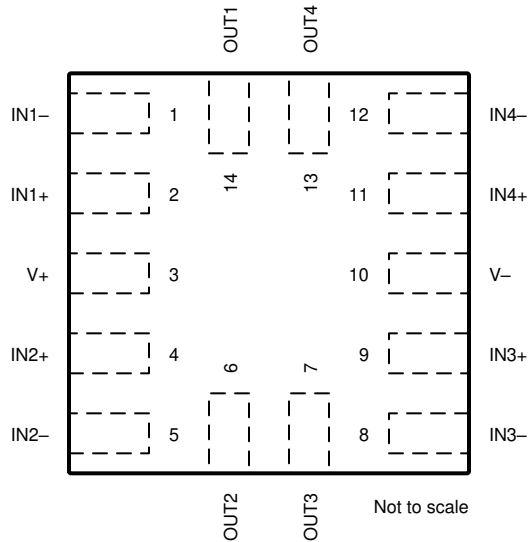
**TLV9054 D, PW Packages  
14-Pin SOIC, TSSOP  
Top View**



**TLV9054 RTE Package  
16-Pin WQFN With Exposed Thermal Pad  
Top View**



**TLV9054 RUC Package  
14-Pin X2QFN  
Top View**



Connect exposed thermal pad to V-. See [Packages With an Exposed Thermal Pad](#) section for more information.

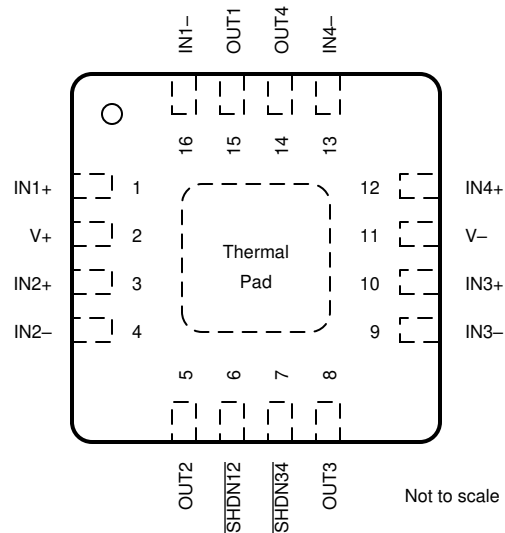
### Pin Functions: TLV9054

NAME	PIN			I/O	DESCRIPTION
	SOIC, TSSOP	WQFN	X2QFN		
IN1-	2	16	1	I	Inverting input, channel 1
IN1+	3	1	2	I	Noninverting input, channel 1
IN2-	6	4	5	I	Inverting input, channel 2
IN2+	5	3	4	I	Noninverting input, channel 2
IN3-	9	9	8	I	Inverting input, channel 3
IN3+	10	10	9	I	Noninverting input, channel 3
IN4-	13	13	12	I	Inverting input, channel 4
IN4+	12	12	11	I	Noninverting input, channel 4

**Pin Functions: TLV9054 (continued)**

PIN				I/O	DESCRIPTION
NAME	SOIC, TSSOP	WQFN	X2QFN		
NC	—	6, 7	—	—	No internal connection
OUT1	1	15	14	O	Output, channel 1
OUT2	7	5	6	O	Output, channel 2
OUT3	8	8	7	O	Output, channel 3
OUT4	14	14	13	O	Output, channel 4
V–	11	11	10	—	Negative (low) supply or ground (for single-supply operation)
V+	4	2	3	—	Positive (high) supply

**TLV9054S RTE Package  
16-Pin WQFN With Exposed Thermal Pad  
Top View**



Connect exposed thermal pad to V<sub>-</sub>. See [Packages With an Exposed Thermal Pad](#) section for more information.

**Pin Functions: TLV9054S**

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	1	I	Noninverting input, channel 1
IN1–	16	I	Inverting input, channel 1
IN2+	3	I	Noninverting input, channel 2
IN2–	4	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3–	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4–	13	I	Inverting input, channel 4
$\overline{\text{SHDN12}}$	6	I	Shutdown: low = amp disabled, high = amp enabled, channel 1 and 2. See <a href="#">Shutdown Function</a> section for more information.
$\overline{\text{SHDN34}}$	7	I	Shutdown: low = amp disabled, high = amp enabled, channel 3 and 4. See <a href="#">Shutdown Function</a> section for more information.
OUT1	15	O	Output, channel 1
OUT2	5	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	—	Negative (low) supply or ground (for single-supply operation)
V+	2	—	Positive (high) supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating junction temperature (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$				6	V
Signal input pins	Voltage <sup>(2)</sup>	Common-mode	$(V-) - 0.5$	$(V+) + 0.5$	V
		Differential		$V_S + 0.2$	V
	Current <sup>(2)</sup>		–10	10	mA
Output short-circuit <sup>(3)</sup>			Continuous		
Operating ambient temperature, $T_A$			–40	150	°C
Junction temperature, $T_J$				150	°C
Storage temperature, $T_{stg}$			–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

### 7.2 ESD Ratings

			VALUE	UNIT
TLV9051 X2SON PACKAGE				
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	
ALL OTHER PACKAGES				
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_S$	Supply voltage, $V_S = (V+) - (V-)$	1.8	5.5	V
$V_{IN}$	Input pin voltage	$(V-) - 0.1$	$(V+) + 0.1$	V
	Specified temperature	–40	125	°C

### 7.4 Thermal Information for Single Channel

THERMAL METRIC <sup>(1)</sup>		TLV9051, TLV9051S					UNIT
		DPW (X2SON)	DBV (SOT-23)		DCK (SC70)	DRL (SOT553) <sup>(2)</sup>	
		5 PINS	5 PINS	6 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	470.0	228.1	210.8	231.2	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	211.9	152.1	152.1	144.4	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	334.8	97.7	92.3	78.6	TBD	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	29.8	74.1	76.2	51.3	TBD	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) This package option is for preview only.

## Thermal Information for Single Channel (continued)

THERMAL METRIC <sup>(1)</sup>		TLV9051, TLV9051S					UNIT
		DPW (X2SON)	DBV (SOT-23)		DCK (SC70)	DRL (SOT553) <sup>(2)</sup>	
		5 PINS	5 PINS	6 PINS	5 PINS	5 PINS	
$\Psi_{JB}$	Junction-to-board characterization parameter	333.2	97.3	92.1	78.3	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	N/A	TBD	°C/W

## 7.5 Thermal Information for Dual Channel

THERMAL METRIC <sup>(1)</sup>		TLV9052, TLV9052S							UNIT
		D (SOIC)	DGK (VSSOP)	DSG (WSON)	PW (TSSOP)	DDF (SOT-23)	DGS (VSSOP)	RUG (X2QFN)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	155.4	208.8	102.3	205.1	184.4	170.4	197.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	95.5	93.3	120.0	93.7	112.8	84.9	93.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.9	130.7	68.2	135.7	99.9	113.5	123.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	41.9	26.1	15.1	25.0	18.7	16.4	3.7	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	98.1	128.9	68.2	134.0	99.3	112.3	120.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	43.6	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.6 Thermal Information for Quad Channel

THERMAL METRIC <sup>(1)</sup>		TLV9054, TLV9054S					UNIT
		D (SOIC)	PW (TSSOP)	RTE (WQFN)		RUC (X2SQFN)	
		14 PINS	14 PINS	14 PINS	16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.0	147.2	65.5	65.6	209.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	71.1	67.2	70.6	70.6	68.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.0	91.6	40.5	40.5	153.3	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	29.7	16.6	5.8	5.8	3.0	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	70.6	90.7	40.5	40.5	152.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	24.5	24.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.7 Electrical Characteristics: $V_S$ (Total Supply Voltage) = $(V_+) - (V_-) = 1.8\text{ V to }5.5\text{ V}$

For  $V_S = (V_+) - (V_-) = 1.8\text{ V to }5.5\text{ V}$  ( $\pm 0.9\text{ V to } \pm 2.75\text{ V}$ ) at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V <sub>OS</sub>	Input offset voltage	V <sub>S</sub> = 5 V		±0.33		±1.6	mV
		V <sub>S</sub> = 5 V	T <sub>A</sub> = −40°C to 125°C			±2	
dV <sub>OS</sub> /dT	Drift	V <sub>S</sub> = 5 V		±0.5			μV/°C
PSRR	Power-supply rejection ratio	V <sub>S</sub> = 1.8 V – 5.5 V, V <sub>CM</sub> = (V−)		±13		±80	μV/V
	Channel separation, DC	At DC		100			dB
INPUT BIAS CURRENT							
I <sub>B</sub>	Input bias current			±2			pA
I <sub>OS</sub>	Input offset current			±1			pA
NOISE							
E <sub>n</sub>	Input voltage noise (peak-to-peak)	V <sub>S</sub> = 5 V, f = 0.1 Hz to 10 Hz		6			μV <sub>PP</sub>
e <sub>n</sub>	Input voltage noise density	V <sub>S</sub> = 5 V, f = 10 kHz		15			nV/√Hz
		V <sub>S</sub> = 5 V, f = 1 kHz		20			
i <sub>n</sub>	Input current noise density	f = 1 kHz		18			fA/√Hz
INPUT VOLTAGE RANGE							
V <sub>CM</sub>	Common-mode voltage range	V <sub>S</sub> = 1.8 V to 5.5 V		(V−) − 0.1	(V+) + 0.1		V
CMRR	Common-mode rejection ratio	V <sub>S</sub> = 5.5 V, (V−) − 0.1 V < V <sub>CM</sub> < (V+) − 1.4 V	T <sub>A</sub> = −40°C to 125°C	80	96		dB
		V <sub>S</sub> = 5.5 V, V <sub>CM</sub> = −0.1 V to 5.6 V	T <sub>A</sub> = −40°C to 125°C	62	79		
		V <sub>S</sub> = 1.8 V, (V−) − 0.1 V < V <sub>CM</sub> < (V+) − 1.4 V	T <sub>A</sub> = −40°C to 125°C		88		
		V <sub>S</sub> = 1.8 V, V <sub>CM</sub> = −0.1 V to 1.9 V	T <sub>A</sub> = −40°C to 125°C		72		
INPUT CAPACITANCE							
C <sub>ID</sub>	Differential			2			pF
C <sub>IC</sub>	Common-mode			4			pF
OPEN-LOOP GAIN							
A <sub>OL</sub>	Open-loop voltage gain	V <sub>S</sub> = 1.8 V, (V−) + 0.04 V < V <sub>O</sub> < (V+) − 0.04 V, R <sub>L</sub> = 10 kΩ		106			dB
		V <sub>S</sub> = 5.5 V, (V−) + 0.05 V < V <sub>O</sub> < (V+) − 0.05 V, R <sub>L</sub> = 10 kΩ		104	128		
		V <sub>S</sub> = 1.8 V, (V−) + 0.06 V < V <sub>O</sub> < (V+) − 0.06 V, R <sub>L</sub> = 2 kΩ		108			
		V <sub>S</sub> = 5.5 V, (V−) + 0.15 V < V <sub>O</sub> < (V+) − 0.15 V, R <sub>L</sub> = 2 kΩ		130			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product	V <sub>S</sub> = 5.5 V, G = +1		5			MHz
φ <sub>m</sub>	Phase margin	V <sub>S</sub> = 5.5 V, G = +1		60			°
SR	Slew rate	V <sub>S</sub> = 5.5 V, G = +1, C <sub>L</sub> = 130 pF		15			V/μs
t <sub>S</sub>	Settling time	To 0.1%, V <sub>S</sub> = 5.5 V, 2-V step, G = +1, C <sub>L</sub> = 100 pF		0.75			μs
		To 0.01%, V <sub>S</sub> = 5.5 V, 2-V step, G = +1, C <sub>L</sub> = 100 pF		1			
t <sub>OR</sub>	Overload recovery time	V <sub>S</sub> = 5 V, V <sub>IN</sub> × gain > V <sub>S</sub>		0.3			μs
THD + N	Total harmonic distortion + noise <sup>(1)</sup>	V <sub>S</sub> = 5.5 V, V <sub>CM</sub> = 2.5 V, V <sub>O</sub> = 1 V <sub>RMS</sub> , G = +1, f = 1 kHz		0.0006%			

(1) Third-order filter; bandwidth = 80 kHz at -3 dB.

**Electrical Characteristics:  $V_S$  (Total Supply Voltage) =  $(V_+) - (V_-) = 1.8\text{ V to }5.5\text{ V}$  (continued)**

For  $V_S = (V_+) - (V_-) = 1.8\text{ V to }5.5\text{ V}$  ( $\pm 0.9\text{ V to } \pm 2.75\text{ V}$ ) at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V <sub>O</sub>	Voltage output swing from rail	Positive rail headroom, V <sub>S</sub> = 5.5 V	R <sub>L</sub> = 2 kΩ			40	mV
			R <sub>L</sub> = 10 kΩ			16	
		Negative rail headroom, V <sub>S</sub> = 5.5 V	R <sub>L</sub> = 2 kΩ			40	
			R <sub>L</sub> = 10 kΩ			16	
I <sub>SC</sub>	Short-circuit current	V <sub>S</sub> = 5 V		±50			mA
Z <sub>O</sub>	Open-loop output impedance	V <sub>S</sub> = 5 V, f = 5 MHz		250			Ω
POWER SUPPLY							
I <sub>Q</sub>	Quiescent current per amplifier	V <sub>S</sub> = 5.5 V, I <sub>O</sub> = 0 mA		330		450	μA
		V <sub>S</sub> = 5.5 V, I <sub>O</sub> = 0 mA	T <sub>A</sub> = −40°C to 125°C		475		
SHUTDOWN							
I <sub>QSD</sub>	Quiescent current per amplifier	V <sub>S</sub> = 1.8 V to 5.5 V, all amplifiers disabled, $\overline{\text{SHDN}}$ = V <sub>S</sub> −		0.35		1	μA
Z <sub>SHDN</sub>	Output impedance during shutdown	V <sub>S</sub> = 1.8 V to 5.5 V, amplifier disabled		10    8			GΩ    pF
V <sub>IH</sub>	High voltage (amplifier enabled)	V <sub>S</sub> = 1.8 V to 5.5 V, amplifier enabled		(V−) + 0.9		(V−) + 1.1	V
V <sub>IL</sub>	Low voltage (amplifier disabled)	V <sub>S</sub> = 1.8 V to 5.5 V, amplifier disabled		(V−) + 0.2		(V−) + 0.7	V
t <sub>ON</sub>	Amplifier enable time (full shutdown) <sup>(2)(3)</sup>	V <sub>S</sub> = 1.8 V to 5.5 V, full shutdown; G = 1, V <sub>OUT</sub> = 0.9 × V <sub>S</sub> / 2		35			μs
	Amplifier enable time (partial shutdown) <sup>(2)(3)</sup>	V <sub>S</sub> = 1.8 V to 5.5 V, partial shutdown; G = 1, V <sub>OUT</sub> = 0.9 × V <sub>S</sub> / 2		10			
t <sub>OFF</sub>	Amplifier disable time <sup>(2)</sup>	V <sub>S</sub> = 1.8 V to 5.5 V, G = 1, V <sub>OUT</sub> = 0.1 × V <sub>S</sub> / 2		6			μs
	$\overline{\text{SHDN}}$ pin input bias current (per pin)	V <sub>S</sub> = 1.8 V to 5.5 V, V+ ≥ $\overline{\text{SHDN}}$ ≥ (V+) − 0.8 V		40			nA
		V <sub>S</sub> = 1.8 V to 5.5 V, V− ≤ $\overline{\text{SHDN}}$ ≤ (V−) + 0.8 V		160			

- (2) Disable time ( $t_{OFF}$ ) and enable time ( $t_{ON}$ ) are defined as the time interval between the 50% point of the signal applied to the  $\overline{\text{SHDN}}$  pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
- (3) Full shutdown refers to the dual TLV9052S having both channels 1 and 2 disabled ( $\overline{\text{SHDN}}_1 = \overline{\text{SHDN}}_2 = V_-$ ) and the quad TLV9054S having all channels 1 to 4 disabled ( $\overline{\text{SHDN}}_{12} = \overline{\text{SHDN}}_{34} = V_-$ ). For partial shutdown, only one  $\overline{\text{SHDN}}$  pin is exercised; in this mode, the internal biasing circuitry remains operational and the enable time is shorter.

## 7.8 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

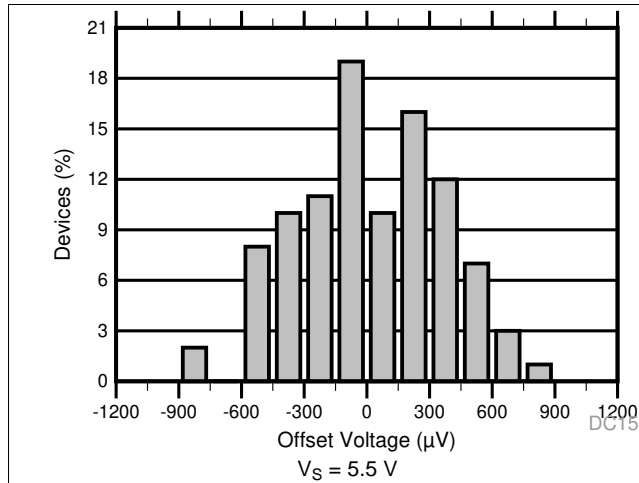


图 1. Offset Voltage Production Distribution

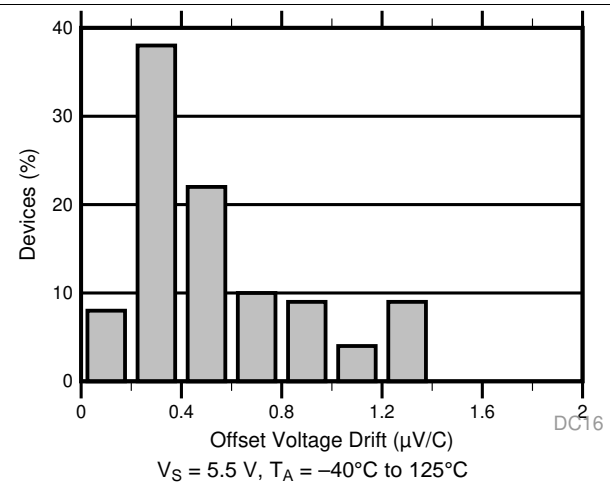


图 2. Offset Voltage Drift Distribution

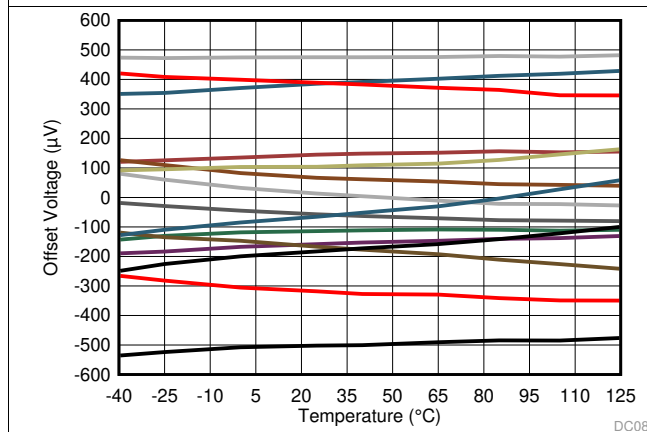


图 3. Offset Voltage vs Temperature

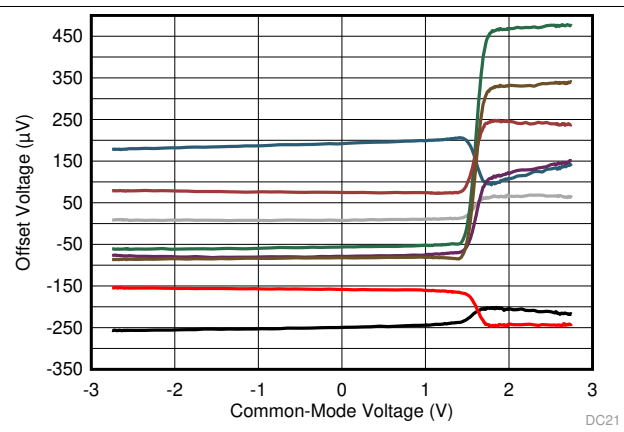


图 4. Offset Voltage vs Common-Mode Voltage

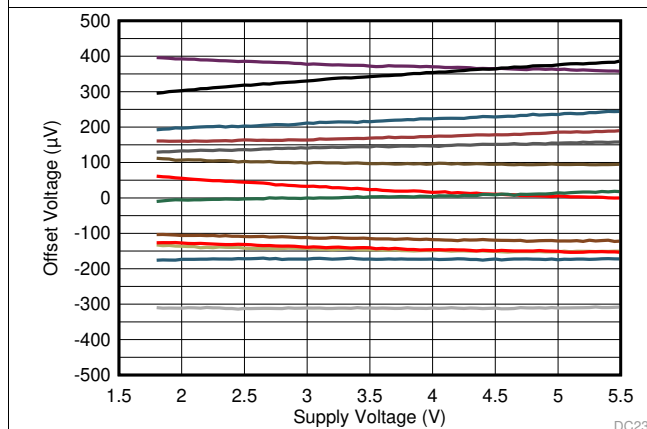


图 5. Offset Voltage vs Power Supply

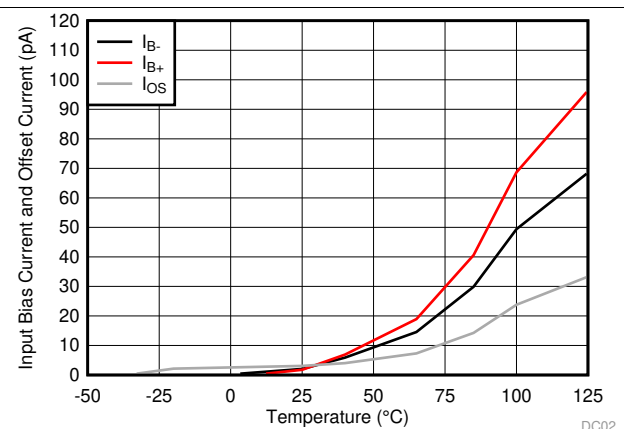


图 6. Input Bias Current vs Temperature



## Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

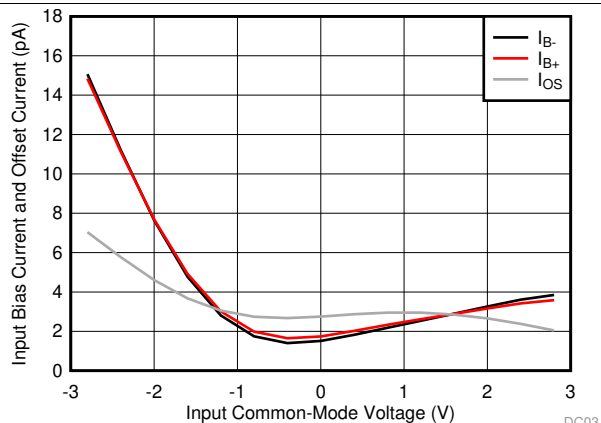


图 7. Input Bias Current and Offset Current vs Common-Mode Voltage

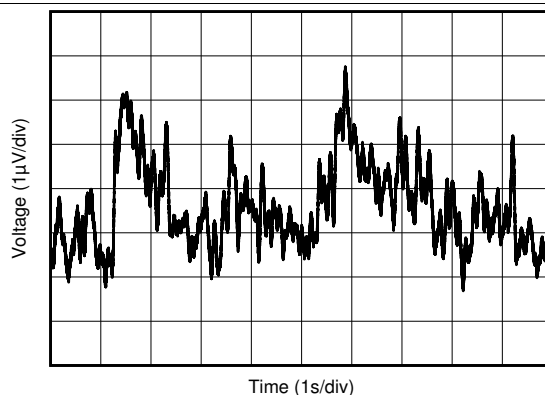


图 8. 0.1-Hz to 10-Hz Input Voltage Noise

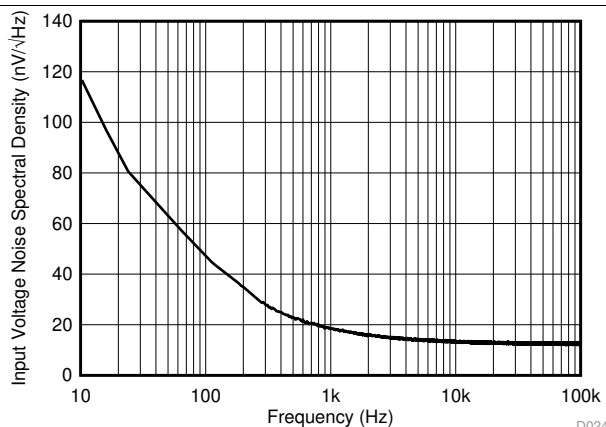


图 9. Input Voltage Noise Spectral Density vs Frequency

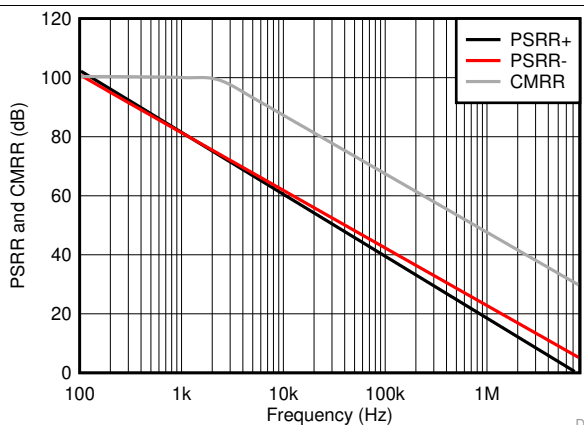


图 10. CMRR and PSRR vs Frequency (Referred to Input)

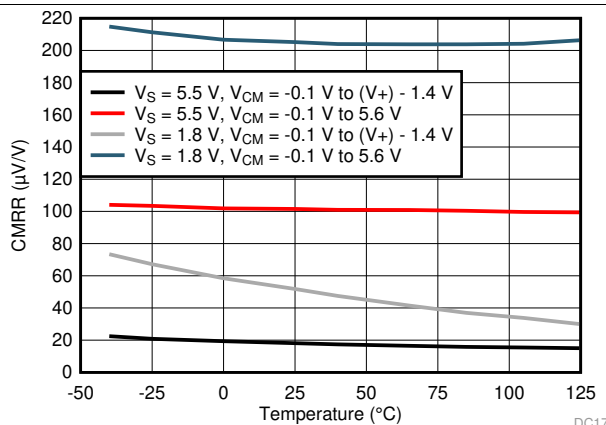


图 11. CMRR vs Temperature

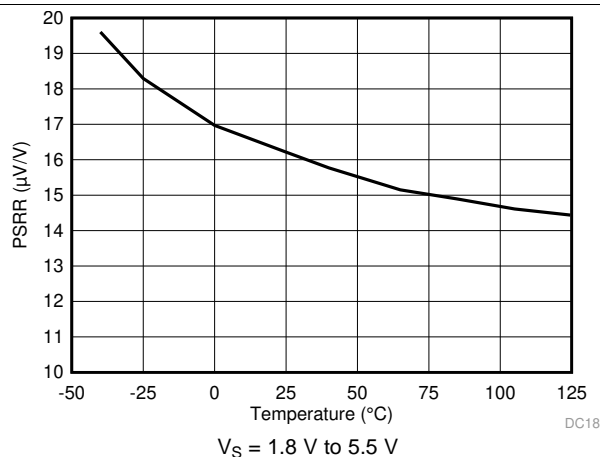


图 12. PSRR vs Temperature

## Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

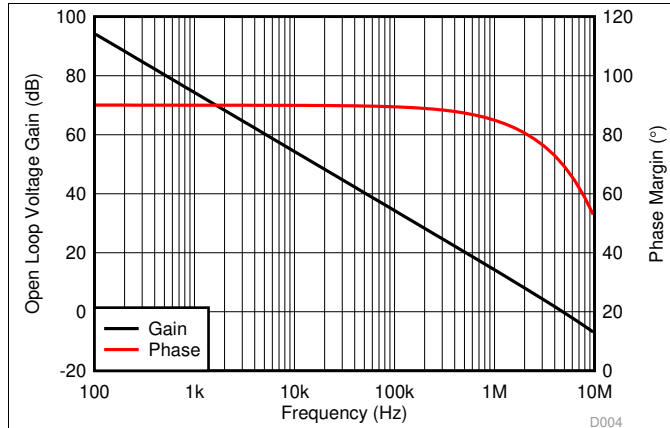


图 13. Open Loop Voltage Gain and Phase vs Frequency

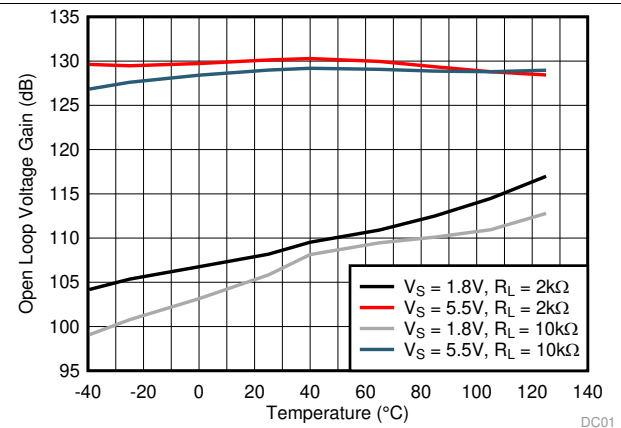


图 14. Open Loop Voltage Gain vs Temperature

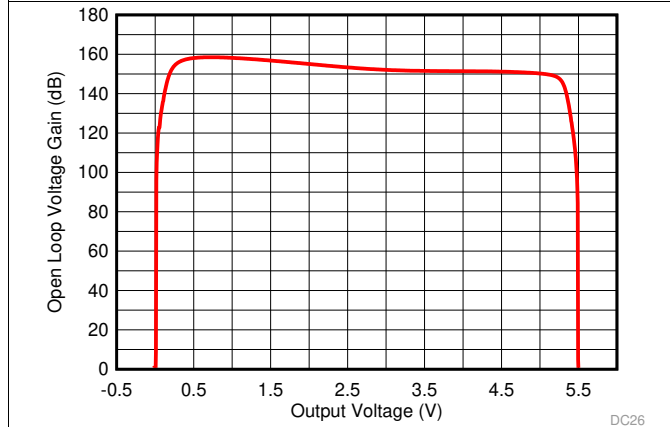


图 15. Open Loop Voltage Gain vs Output Voltage

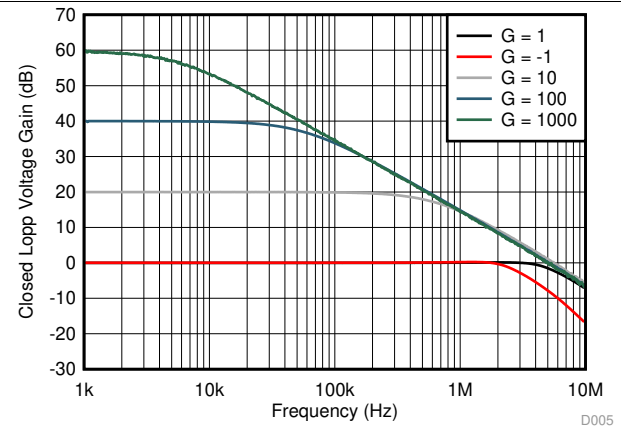


图 16. Closed Loop Voltage Gain vs Frequency

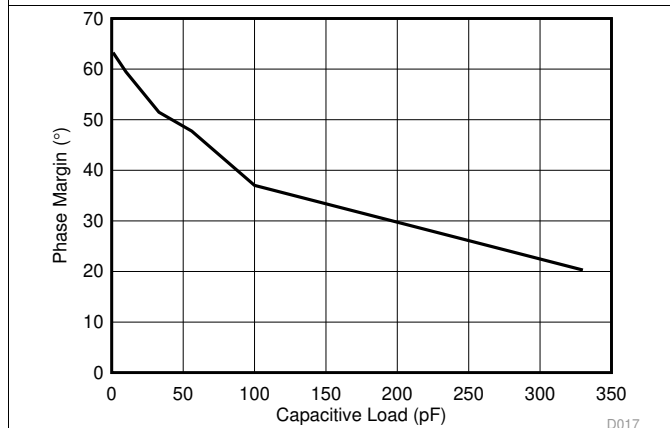


图 17. Phase Margin vs Capacitive Load

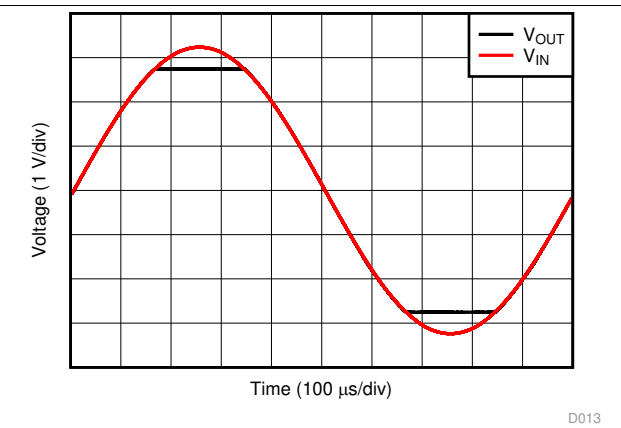


图 18. No Phase Reversal

## Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

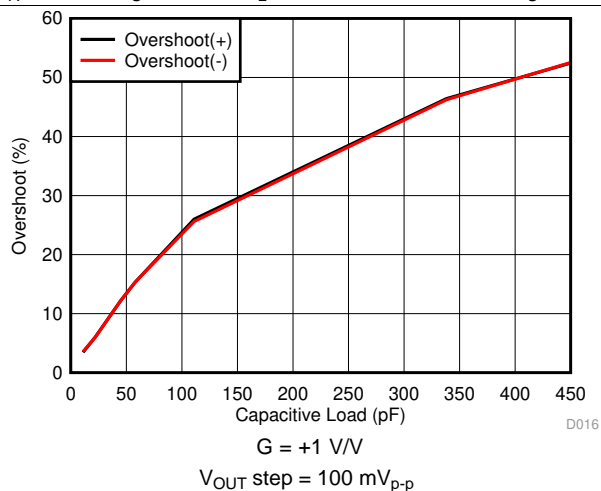


图 19. Small-Signal Overshoot vs Load Capacitance

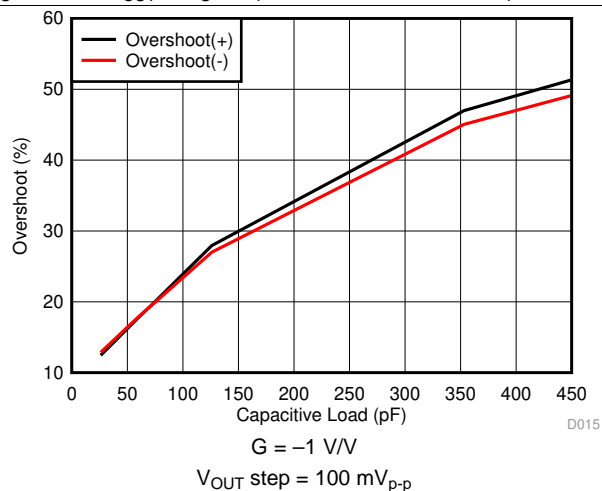


图 20. Small-Signal Overshoot vs Load Capacitance

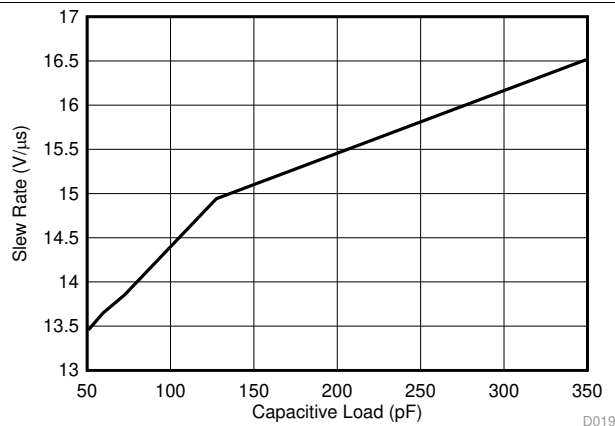


图 21. Slew Rate vs Capacitive Load

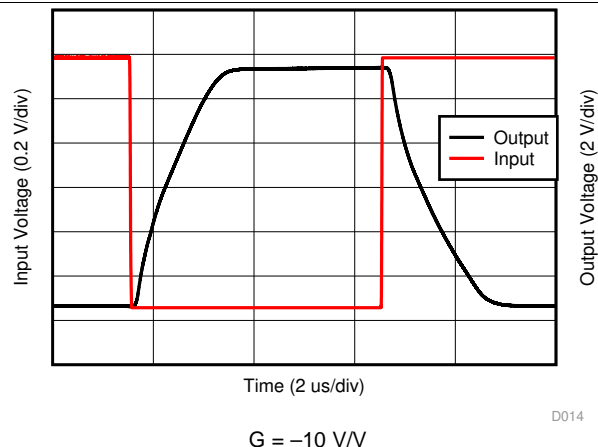


图 22. Overload Recovery

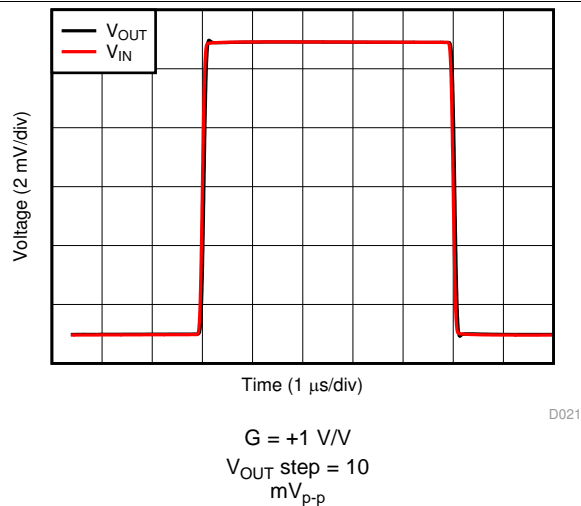


图 23. Small-Signal Step Response

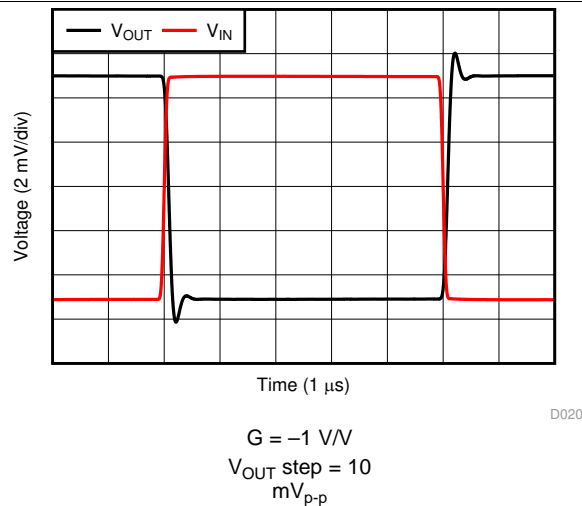
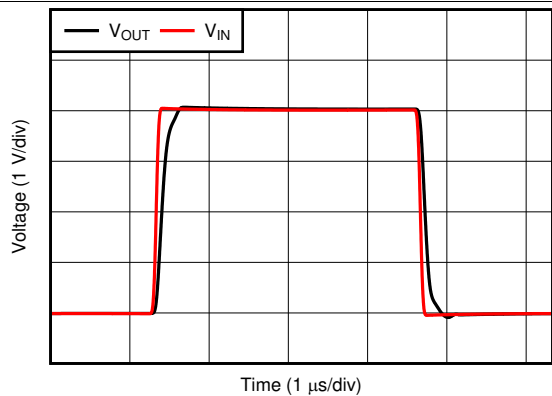


图 24. Small-Signal Step Response

## Typical Characteristics (接下页)

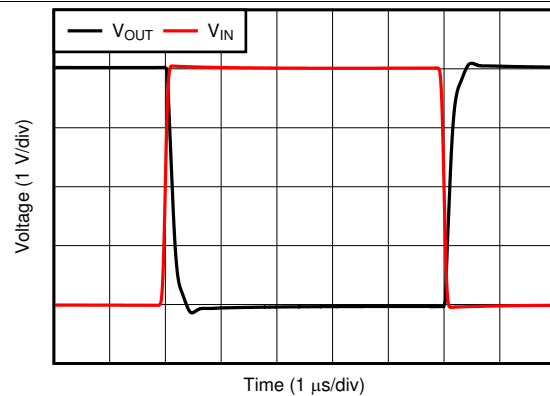
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



$G = +1\text{ V/V}$   
 $V_{OUT}\text{ step} = 4\text{ V}_{p-p}$

D012

图 25. Large-Signal Step Response



$G = -1\text{ V/V}$   
 $V_{OUT}\text{ step} = 4\text{ V}_{p-p}$

D011

图 26. Large-Signal Step Response

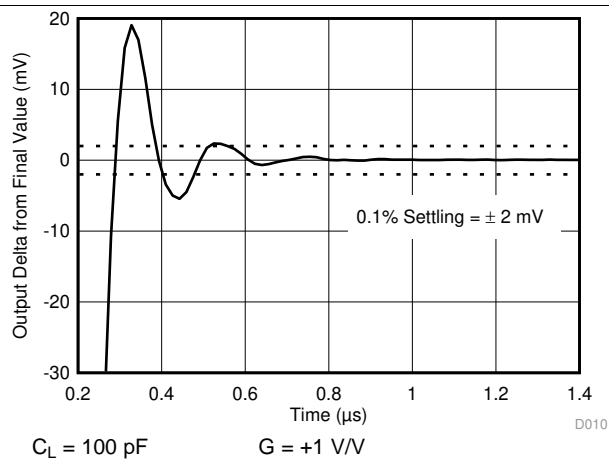


图 27. Positive Large-Signal Settling Time

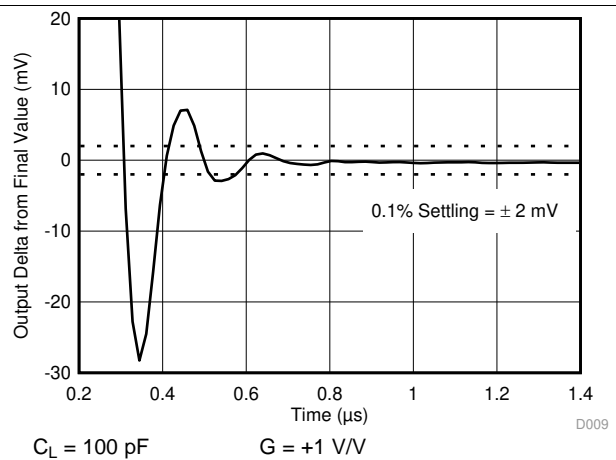


图 28. Negative Large-Signal Settling Time

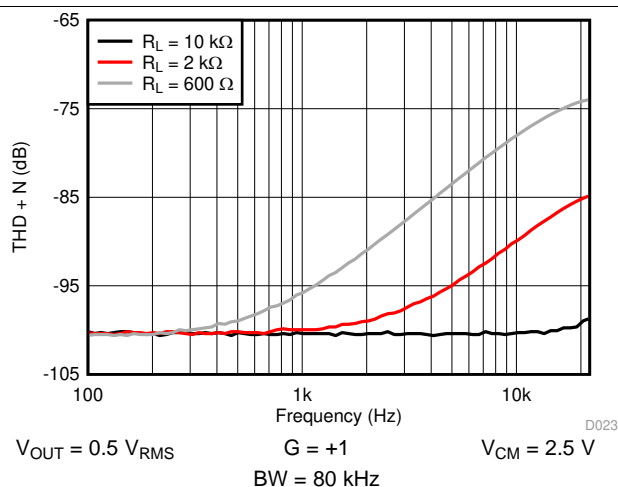


图 29. THD + N vs Frequency

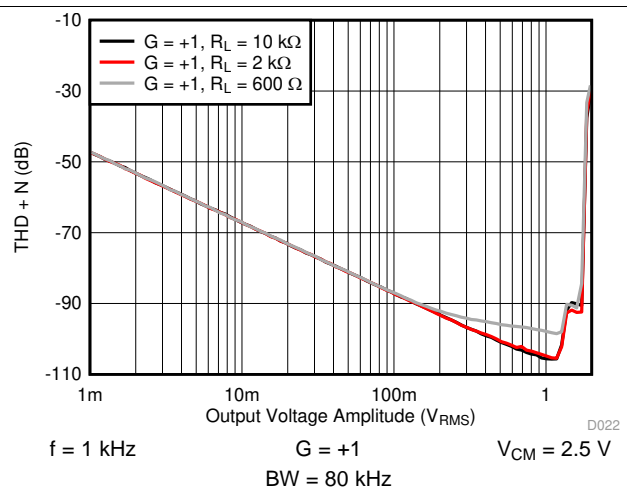


图 30. THD + N vs Amplitude

## Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

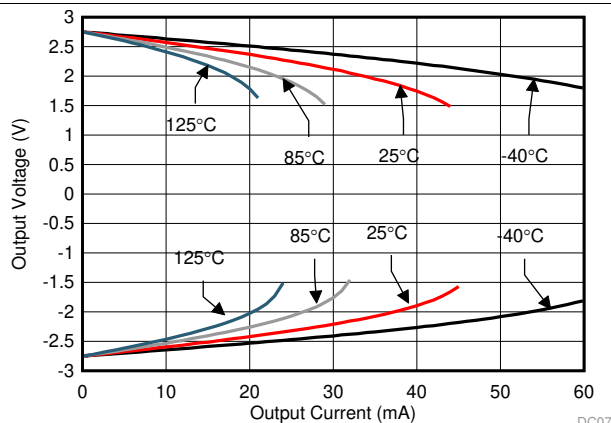


图 31. Output Voltage Swing vs Output Current

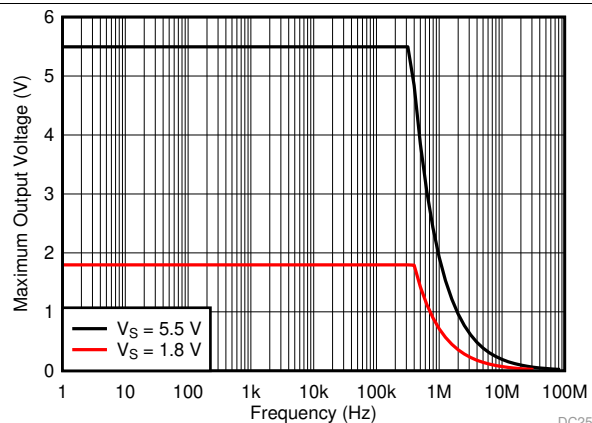


图 32. Maximum Output Voltage vs Frequency and Supply Voltage

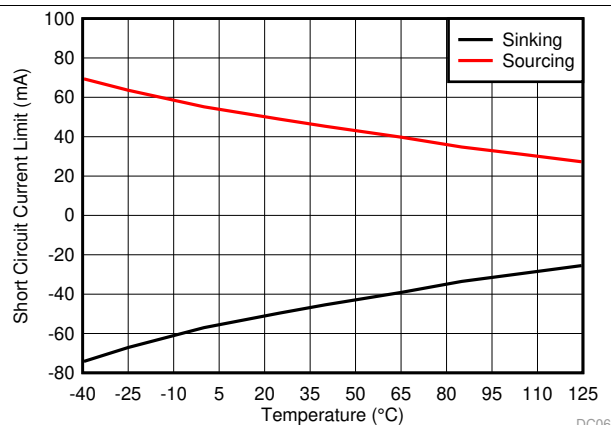


图 33. Short-Circuit Current vs Temperature

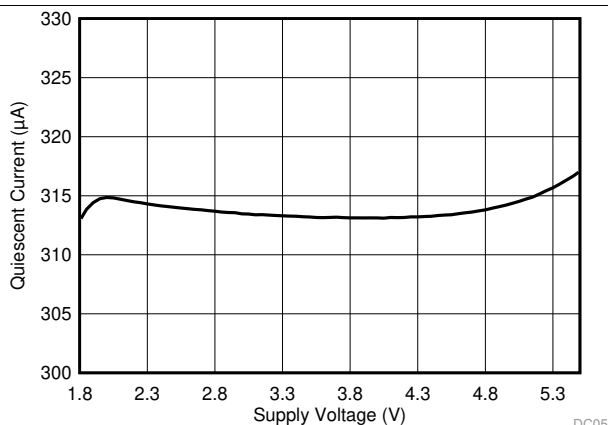


图 34. Quiescent Current vs Supply Voltage

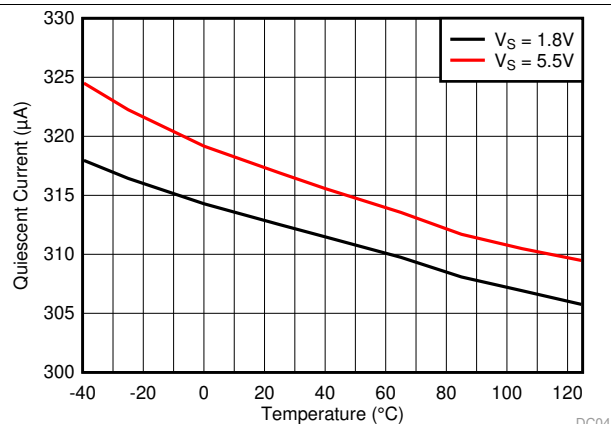


图 35. Quiescent Current vs Temperature

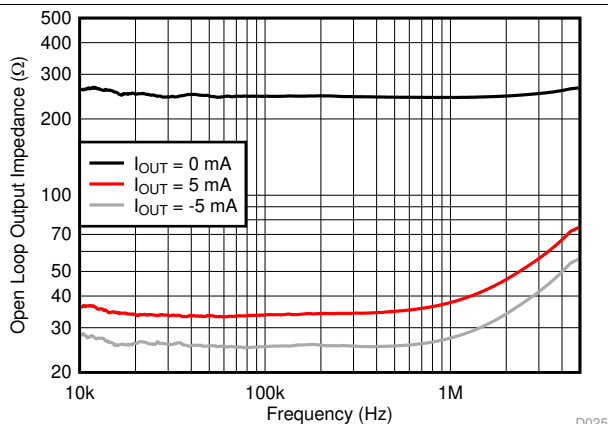


图 36. Open-Loop Output Impedance vs Frequency

## Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

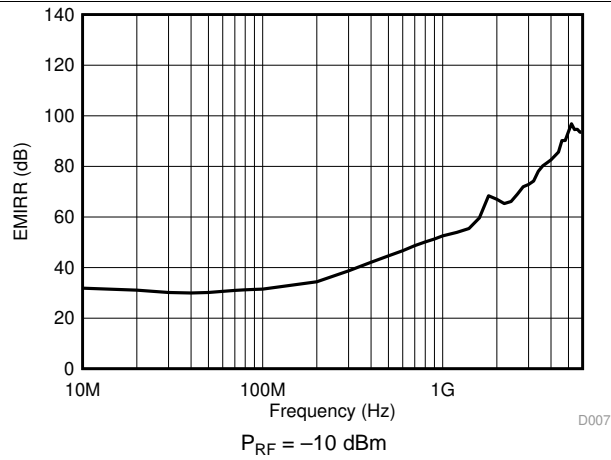


图 37. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

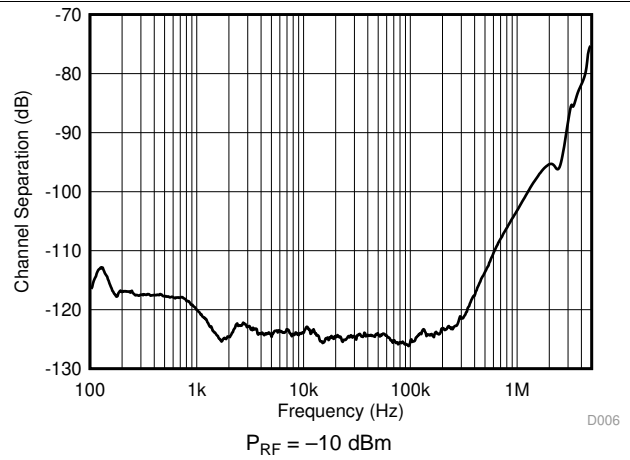


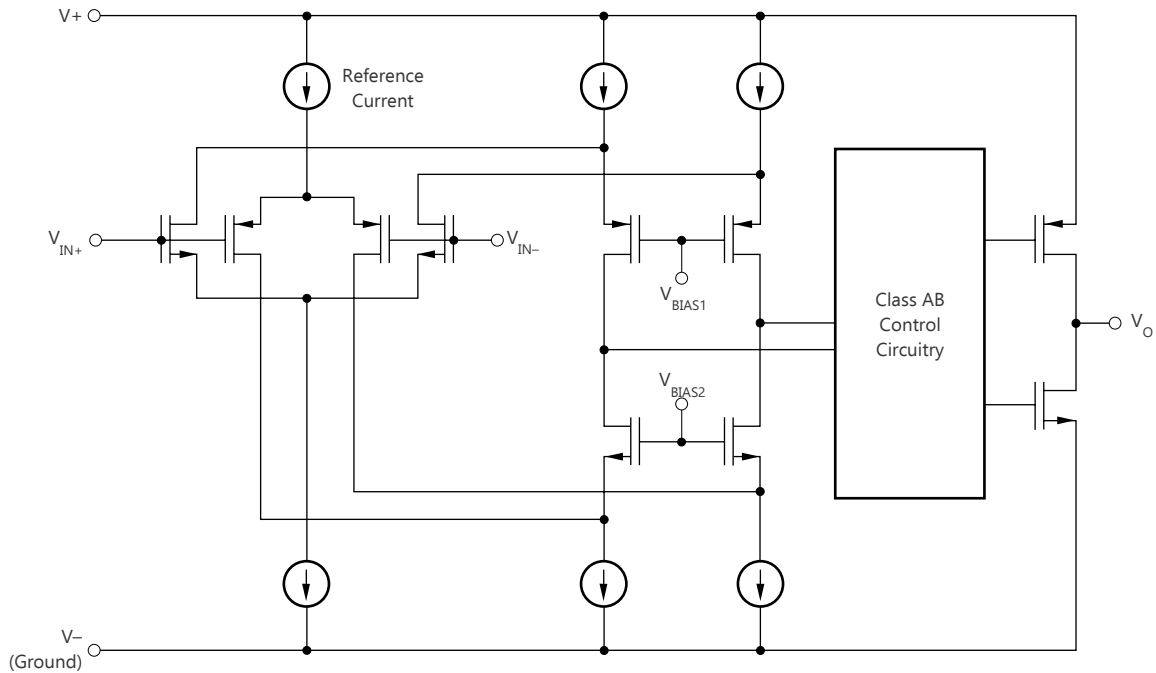
图 38. Channel Separation vs Frequency

## 8 Detailed Description

### 8.1 Overview

The TLV905x devices are a 5-MHz family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV905x family to be used in virtually any single-supply application. The unique combination of a high slew rate and low quiescent current makes this family a potential choice for battery-powered motor-drive applications. Rail-to-rail input and output swing significantly increase dynamic range, especially in low-supply applications.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Operating Voltage

The TLV905x family of op amps is specified for operation from 1.8 V to 5.5 V. In addition, many specifications apply from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Parameters that vary significantly with operating voltages or temperature are illustrated in the [Typical Characteristics](#) section.

### 8.3.2 Rail-to-Rail Input

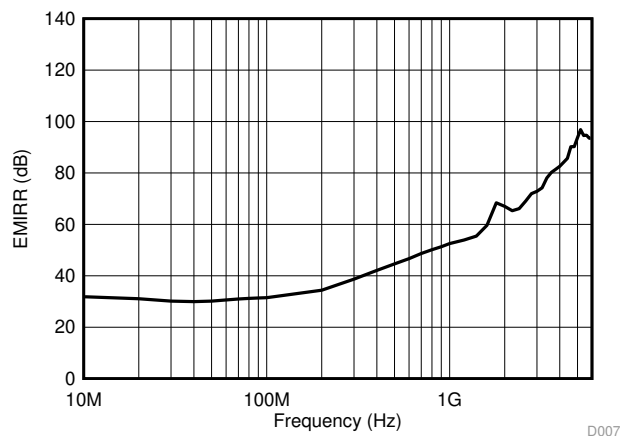
The input common-mode voltage range of the TLV905x family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the [Functional Block Diagram](#). The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 1.4\text{ V}$  to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately  $(V+) - 1.4\text{ V}$ . There is a small transition region, typically  $(V+) - 1.2\text{ V}$  to  $(V+) - 1\text{ V}$ , in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from  $(V+) - 1.4\text{ V}$  to  $(V+) - 1.2\text{ V}$  on the low end, and up to  $(V+) - 1\text{ V}$  to  $(V+) - 0.8\text{ V}$  on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

### 8.3.3 Rail-to-Rail Output

Designed as low-power, low-voltage operational amplifiers, the TLV905x family delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 k $\Omega$ , the output swings to within 16 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

### 8.3.4 EMI Rejection

The TLV905x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV905x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. [图 39](#) shows the results of this testing on the TLV905x. [表 1](#) shows the EMIRR IN+ values for the TLV905x at particular frequencies commonly encountered in real-world applications. The [EMI Rejection Ratio of Operational Amplifiers](#) application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from [www.ti.com](http://www.ti.com).



**图 39. EMIRR Testing**



## Feature Description (接下页)

**表 1. TLV905x EMIRR IN+ for Frequencies of Interest**

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	68.9 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	77.8 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	78.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	87.6 dB

### 8.3.5 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. After the device enters the saturation region, the output devices require time to return to the linear operating state. After the output devices return to their linear operating state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV905x family is approximately 300 ns.

### 8.3.6 Packages With an Exposed Thermal Pad

The TLV905x family is available in packages such as the WSON-8 (DSG) and WQFN-16 (RTE) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V– or left floating. Attaching the thermal pad to a potential other than V– is not allowed, and the performance of the device is not assured when doing so.

### 8.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 40 shows the ESD circuits contained in the TLV905x devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

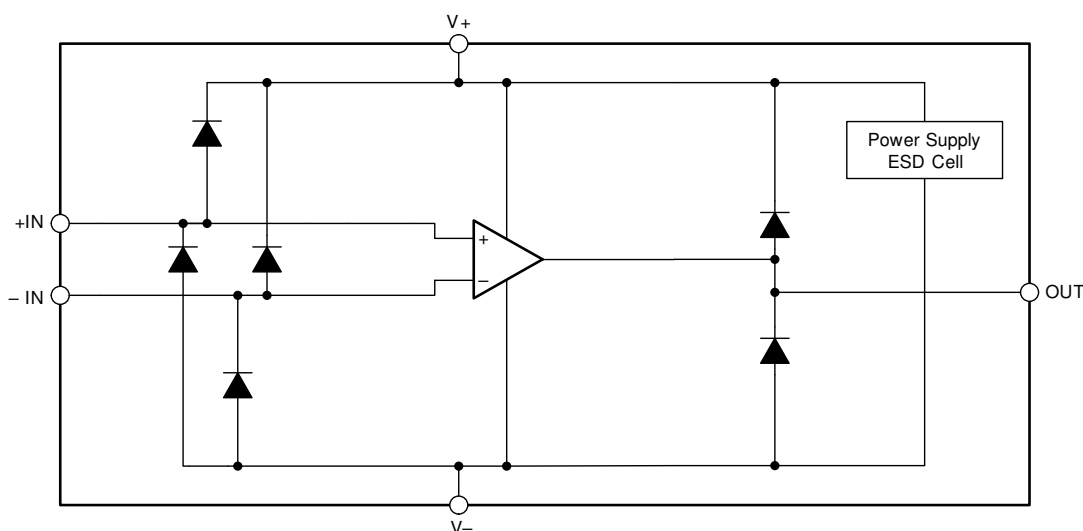


图 40. Equivalent Internal ESD Circuitry

### 8.3.8 Input Protection

The TLV905x family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as shown in the [Absolute Maximum Ratings](#). 图 41 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

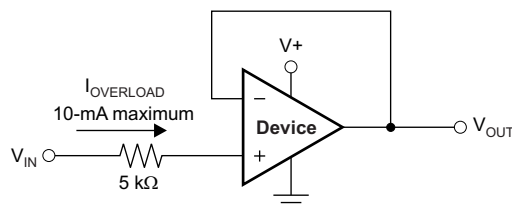


图 41. Input Current Protection

### 8.3.9 Shutdown Function

The TLV905xS devices feature  $\overline{\text{SHDN}}$  pins that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes less than 1  $\mu\text{A}$ . The  $\overline{\text{SHDN}}$  pins are active low, meaning that shutdown mode is enabled when the input to the  $\overline{\text{SHDN}}$  pin is a valid logic low.

The  $\overline{\text{SHDN}}$  pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the  $\overline{\text{SHDN}}$  pins should be driven with valid logic signals. A valid logic low is defined as a voltage between  $V_-$  and  $V_- + 0.4\text{ V}$ . A valid logic high is defined as a voltage between  $V_- + 1.2\text{ V}$  and  $V_+$ . The shutdown pin circuitry includes a pull-up resistor, which will inherently pull the voltage of the pin to the positive supply rail if not driven. Thus, to enable the amplifier, the  $\overline{\text{SHDN}}$  pins should either be left floating or driven to a valid logic high. To disable the amplifier, the  $\overline{\text{SHDN}}$  pins must be driven to a valid logic low. While we highly recommend that the shutdown pin be connected to a valid high or a low voltage or driven, we have included a pull-up resistor connected to VCC. The maximum voltage allowed at the  $\overline{\text{SHDN}}$  pins is  $(V_+) + 0.5\text{ V}$ . Exceeding this voltage level will damage the device.

The  $\overline{\text{SHDN}}$  pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 35  $\mu\text{s}$  for full shutdown of all channels; disable time is 6  $\mu\text{s}$ . When disabled, the output assumes a high-impedance state. This architecture allows the TLV905xS to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time ( $t_{\text{OFF}}$ ) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-k $\Omega$  load to midsupply ( $V_{\text{S}} / 2$ ) is required. If using the TLV905xS without a load, the resulting turnoff time is significantly increased.

## 8.4 Device Functional Modes

The TLV905x family is operational when the power-supply voltage is between 1.8 V ( $\pm 0.9$  V) and 5.5 V ( $\pm 2.75$  V).

The TLV905xS devices feature a shutdown mode and are shutdown when a valid logic low is applied to the shutdown pin.

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TLV905x family features 5-MHz bandwidth and very high slew rate of 15 V/ $\mu$ s with only 330  $\mu$ A of supply current per channel, providing excellent AC performance at very low-power consumption. DC applications are well served with a very low input noise voltage of 15 nV/ $\sqrt{\text{Hz}}$  at 10 kHz, low input bias current, and a typical input offset voltage of 0.33 mV.

### 9.2 Typical Low-Side Current Sense Application

图 42 shows the TLV905x configured in a low-side current sensing application.

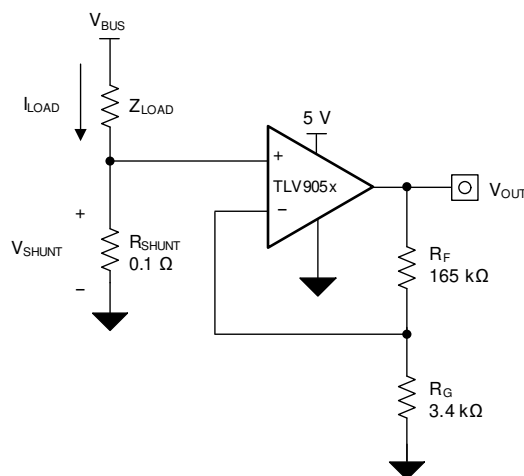


图 42. TLV905x in a Low-Side, Current-Sensing Application

#### 9.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

## Typical Low-Side Current Sense Application (接下页)

### 9.2.2 Detailed Design Procedure

The transfer function of the circuit in 图 42 is given in 公式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

The load current ( $I_{LOAD}$ ) produces a voltage drop across the shunt resistor ( $R_{SHUNT}$ ). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using 公式 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega \quad (2)$$

Using 公式 2,  $R_{SHUNT}$  equals 100 mΩ. The voltage drop produced by  $I_{LOAD}$  and  $R_{SHUNT}$  is amplified by the TLV905x device to produce an output voltage of approximately 0 V to 4.95 V. 公式 3 calculates the gain required for the TLV905x device to produce the required output voltage.

$$\text{Gain} = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (3)$$

Using 公式 3, the required gain equals 49.5 V/V, which is set with the  $R_F$  and  $R_G$  resistors. 公式 4 sizes the  $R_F$  and  $R_G$  resistors to set the gain of the TLV905x device to 49.5 V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Selecting  $R_F$  to equal 165 kΩ and  $R_G$  to equal 3.4 kΩ provides a combination that equals approximately 49.5 V/V. 图 43 shows the measured transfer function of the circuit shown in 图 42.

### 9.2.3 Application Curve

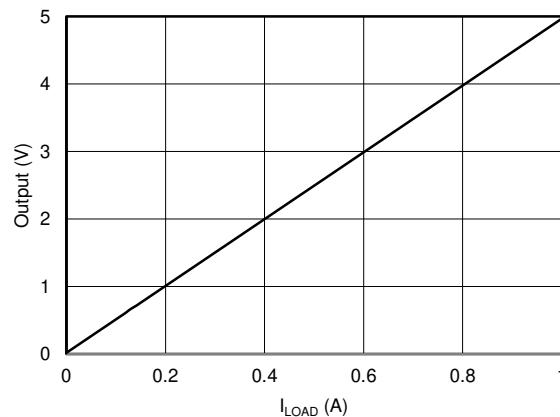


图 43. Low-Side, Current-Sense Transfer Function

## 10 Power Supply Recommendations

The TLV905x family is specified for operation from 1.8 V to 5.5 V ( $\pm 0.9$  V to  $\pm 2.75$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

### CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the [Absolute Maximum Ratings](#) table.

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more-detailed information on bypass capacitor placement, see the [Layout Example](#) section.

## 11 Layout

### 11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Circuit Board Layout Techniques](#).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [图 45](#), keeping R<sub>F</sub> and R<sub>G</sub> close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

## 11.2 Layout Example

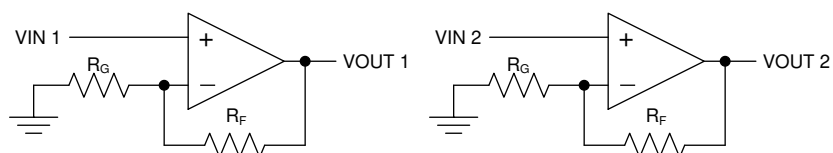


图 44. Schematic Representation for 图 45

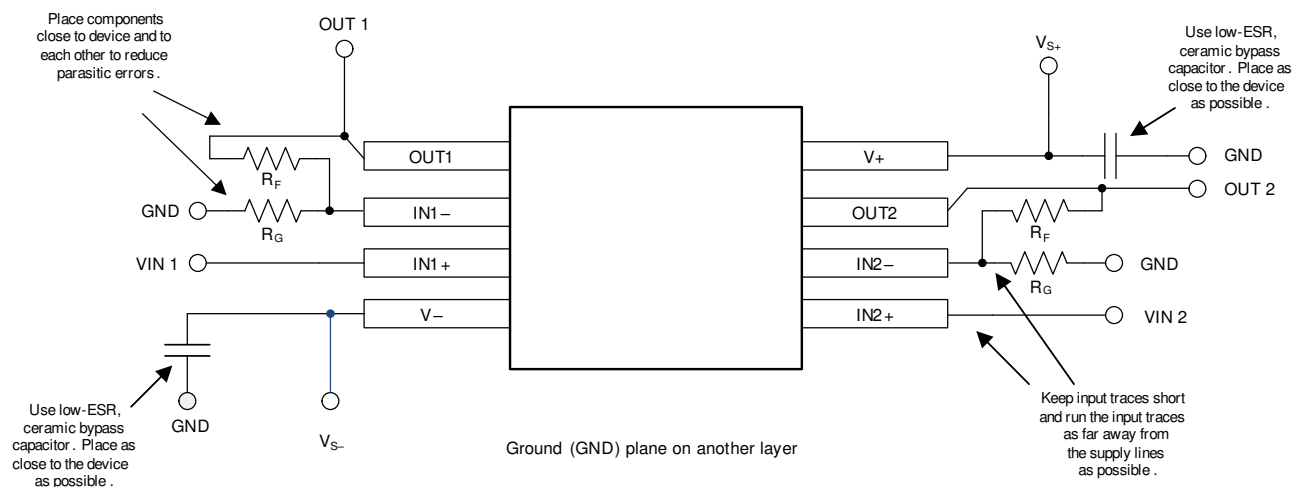


图 45. Layout Example



## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

德州仪器 (TI), 《适用于成本敏感型系统的 [TLVx313](#) 低功耗、轨至轨输入/输出、[500 \$\mu\$ V](#) 典型失调电压、[1MHz](#) 运算放大器》

德州仪器 (TI), 《[TLVx314 3MHz](#)、低功耗、内置 [EMI](#) 滤波器、[RRIO](#) 运算放大器》

德州仪器 (TI), 《运算放大器的 [EMI](#) 抑制比》

德州仪器 (TI), 《[QFN/SON PCB 连接](#)》

德州仪器 (TI), 《四方扁平封装无引线逻辑封装》

德州仪器 (TI), 《电路板布局技巧》

德州仪器 (TI), 《单端输入至差分输出转换电路参考设计》

### 12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 2. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TLV9051/S	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
TLV9052/S	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
TLV9054/S	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>

### 12.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.4 社区资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.5 商标

E2E is a trademark of Texas Instruments.

Bluetooth is a registered trademark of Bluetooth SIG, Inc.

All other trademarks are the property of their respective owners.

### 12.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

### **13 机械、封装和可订购信息**

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航面板。

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9051IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T51D	<a href="#">Samples</a>
TLV9051IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T51	<a href="#">Samples</a>
TLV9051IDPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	FH	<a href="#">Samples</a>
TLV9051SIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T51S	<a href="#">Samples</a>
TLV9052IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T052	<a href="#">Samples</a>
TLV9052IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1PWX	<a href="#">Samples</a>
TLV9052IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL9052	<a href="#">Samples</a>
TLV9052IDSGR	ACTIVE	WSO	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	9052	<a href="#">Samples</a>
TLV9052IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL9052	<a href="#">Samples</a>
TLV9052SIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T052	<a href="#">Samples</a>
TLV9052SIRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	FPF	<a href="#">Samples</a>
TLV9054IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9054D	<a href="#">Samples</a>
TLV9054IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T9054PW	<a href="#">Samples</a>
TLV9054IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T54RT	<a href="#">Samples</a>
TLV9054IRUCR	ACTIVE	QFN	RUC	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1FF	<a href="#">Samples</a>
TLV9054SIRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9054S	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9051IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9051IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9051DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV9051SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9052IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9052IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9052IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9052IDSGR	WSOP	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9052IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9052SIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9052SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1
TLV9054IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9054IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9054IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV9054IRUCR	QFN	RUC	14	3000	180.0	9.5	2.16	2.16	0.5	4.0	8.0	Q2
TLV9054SIRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9051IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9051IDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV9051IDPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV9051SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9052IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9052IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9052IDR	SOIC	D	8	2500	853.0	449.0	35.0
TLV9052IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9052IPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TLV9052SIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TLV9052SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0
TLV9054IDR	SOIC	D	14	2500	853.0	449.0	35.0
TLV9054IPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
TLV9054IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TLV9054IRUCR	QFN	RUC	14	3000	205.0	200.0	30.0
TLV9054SIRTER	WQFN	RTE	16	3000	367.0	367.0	35.0

## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE

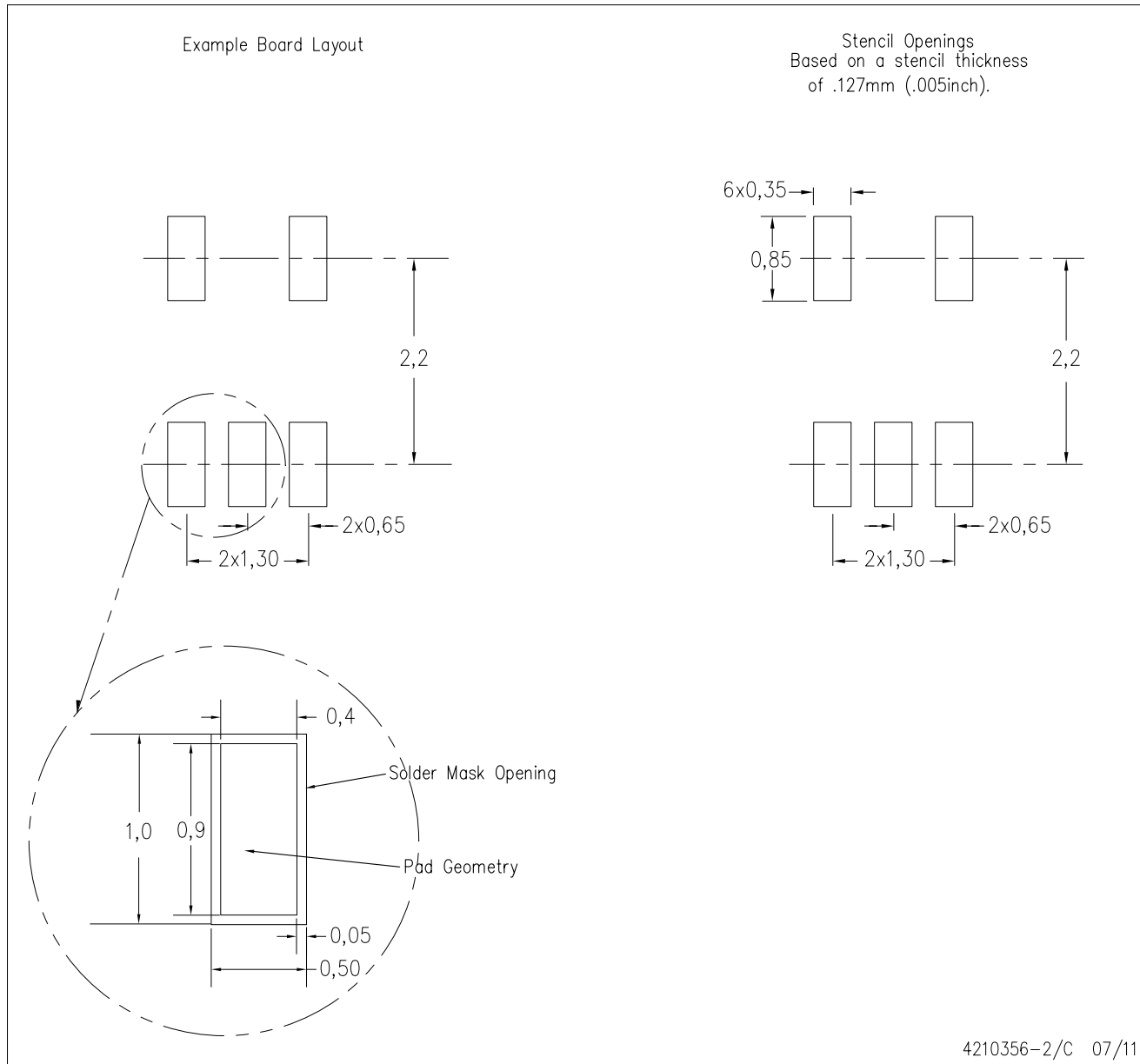


4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-203 variation AA.

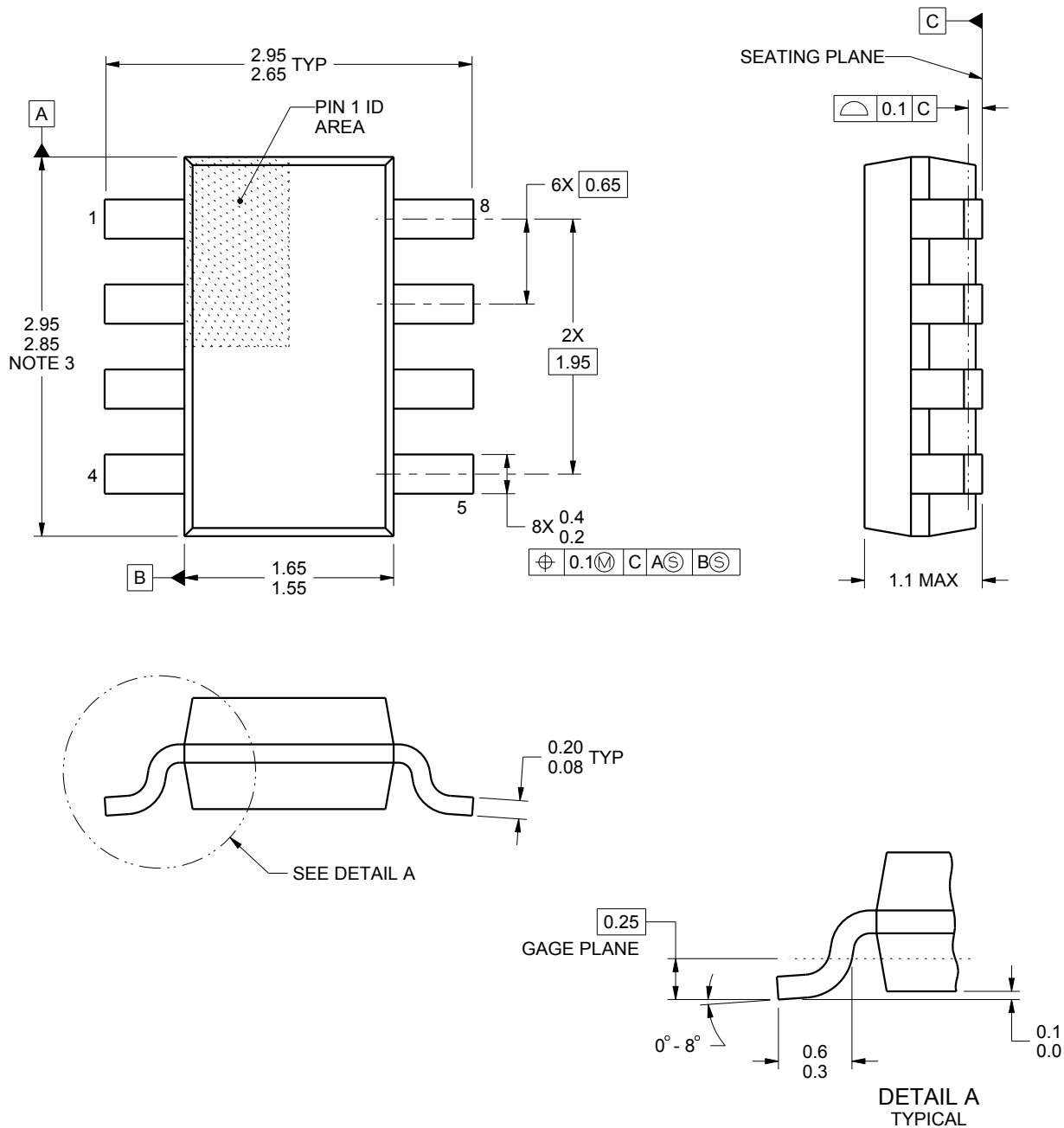
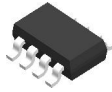
DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.





4222047/B 11/2015

## NOTES:

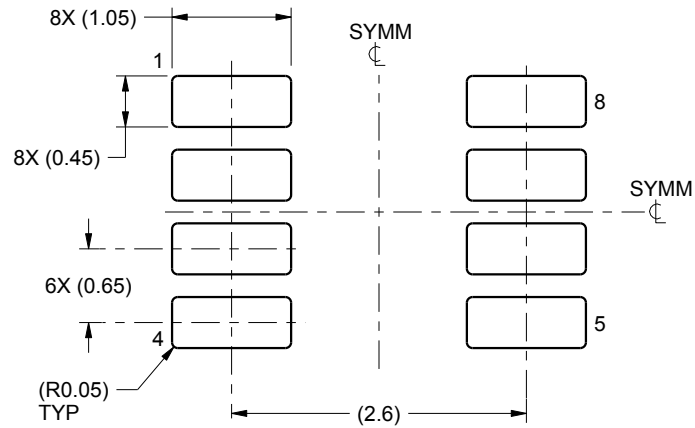
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

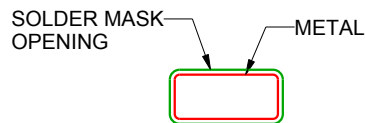
DDF0008A

SOT-23 - 1.1 mm max height

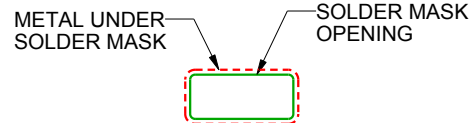
PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:15X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

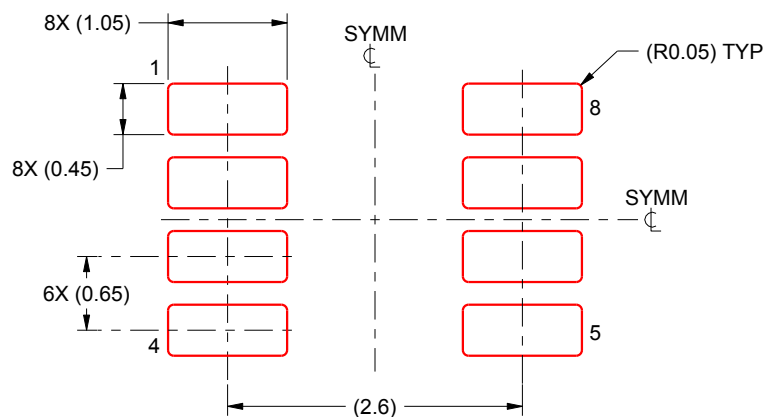
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

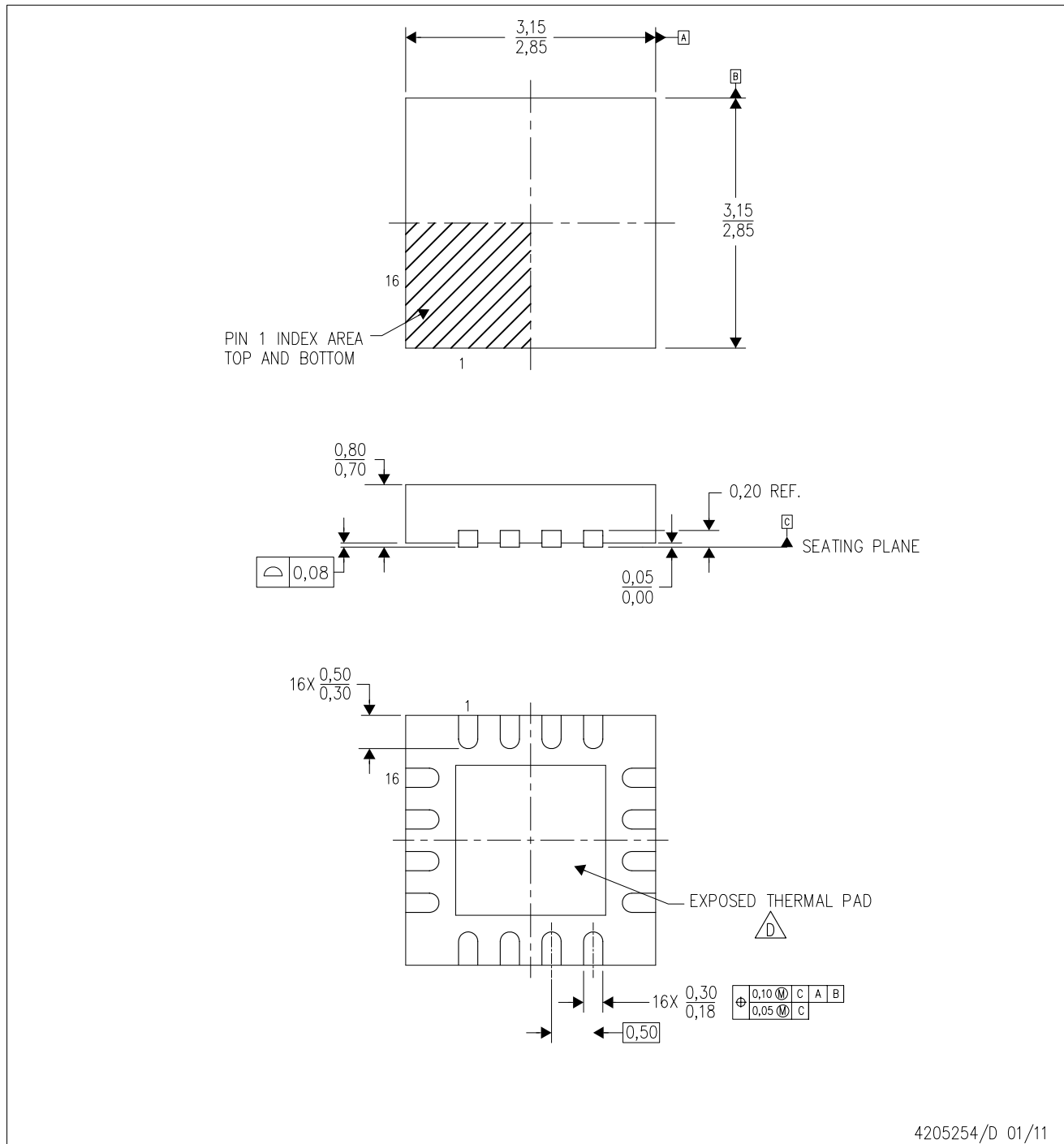
4222047/B 11/2015

NOTES: (continued)


6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4205254/D 01/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

RTE (S-PWQFN-N16)

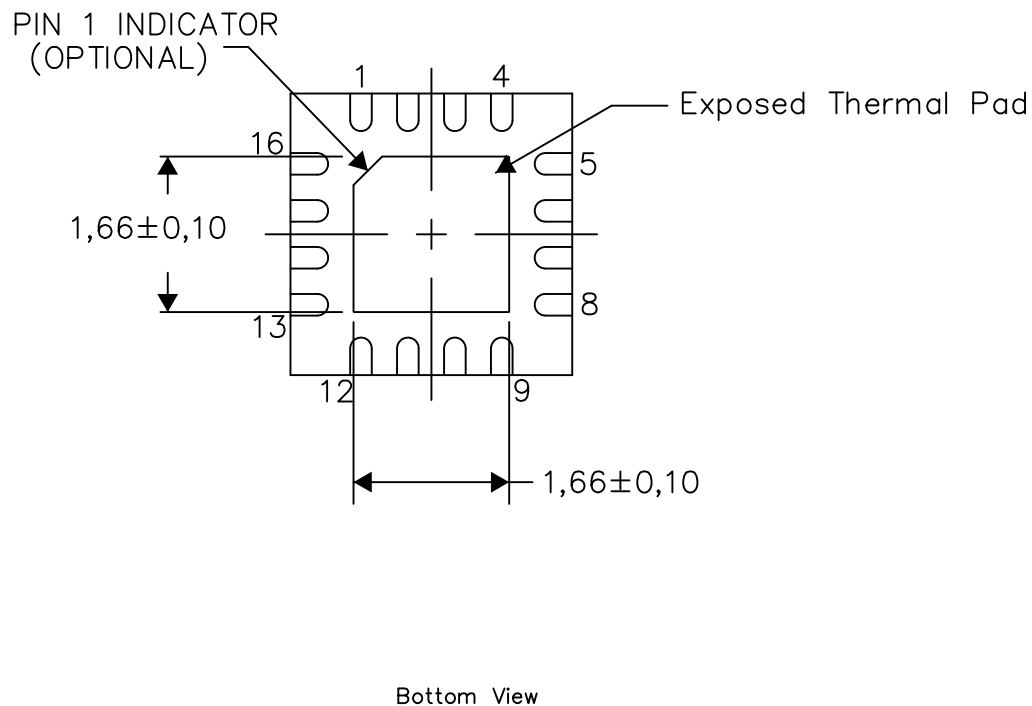
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



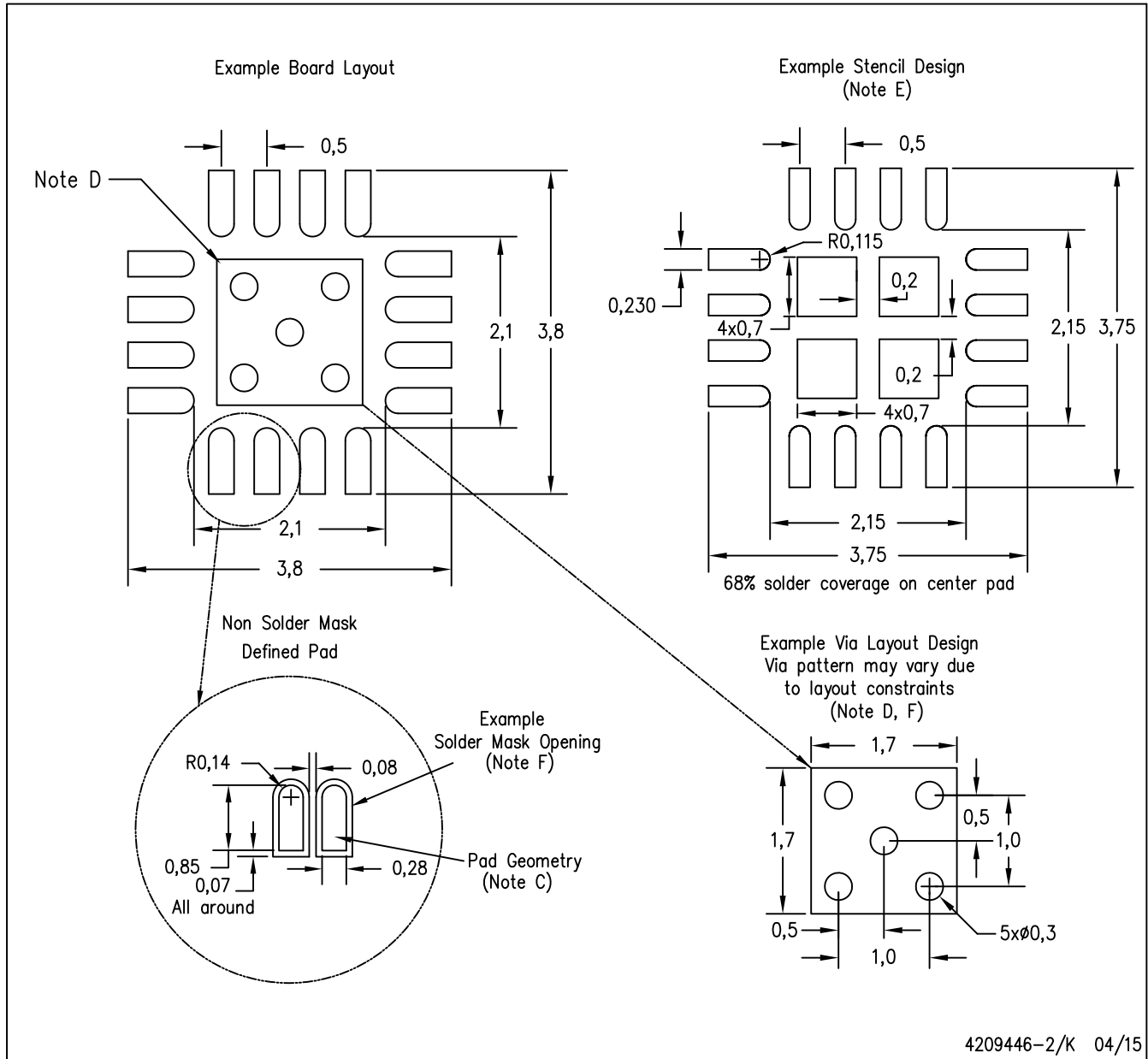
Exposed Thermal Pad Dimensions

4206446-8/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



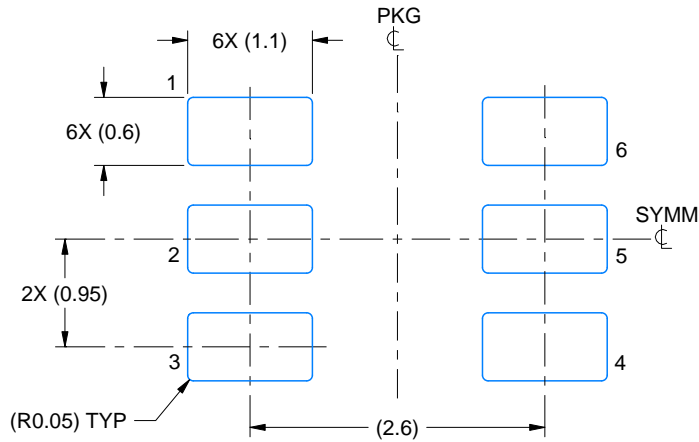
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

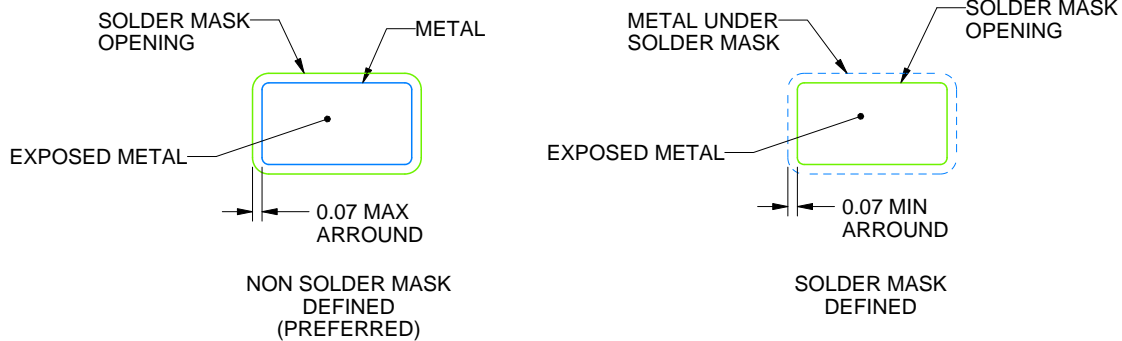
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

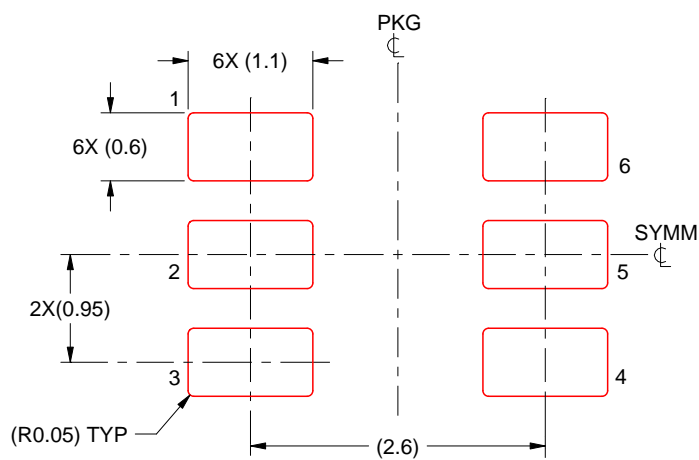


## EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## SOT-23 - 1.45 mm max height

## SMALL OUTLINE TRANSISTOR



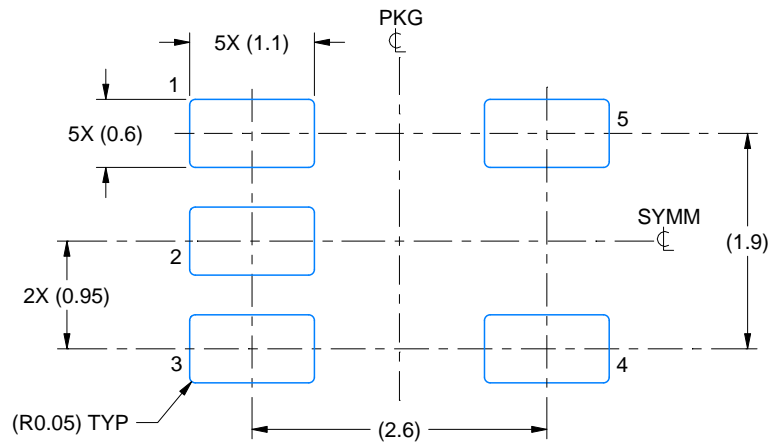
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

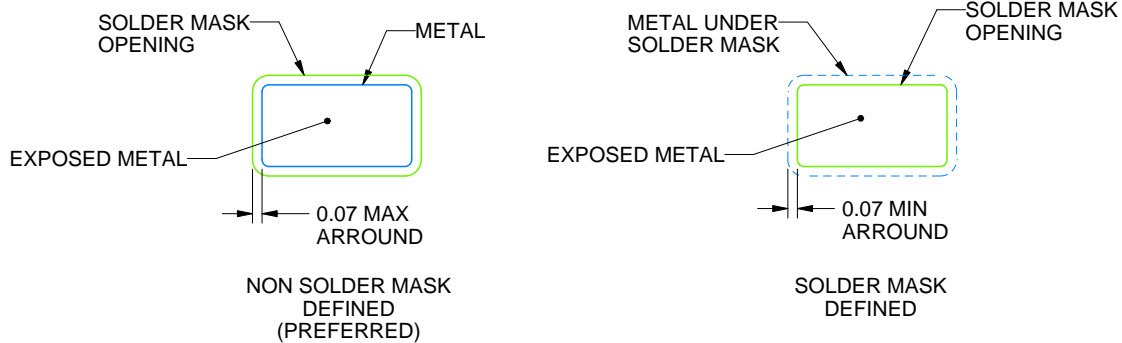
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

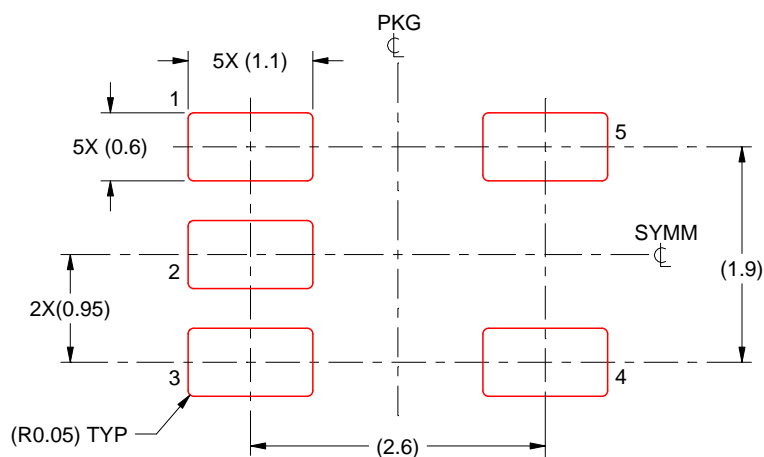
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**DBV0005A**

## SOT-23 - 1.45 mm max height

## SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4221984/A 05/2015

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

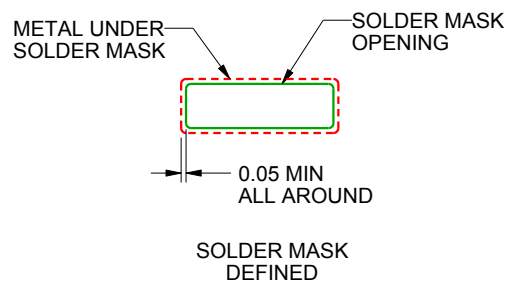
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**DPW 5**

**X2SON - 0.4 mm max height**

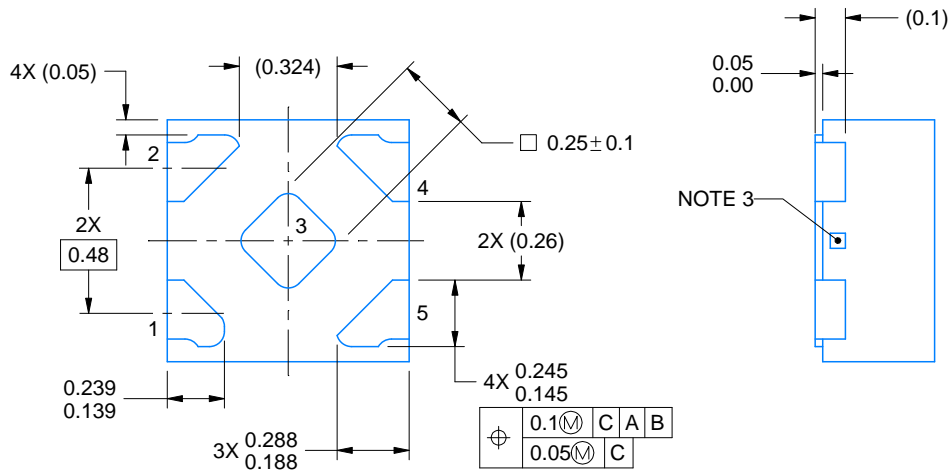
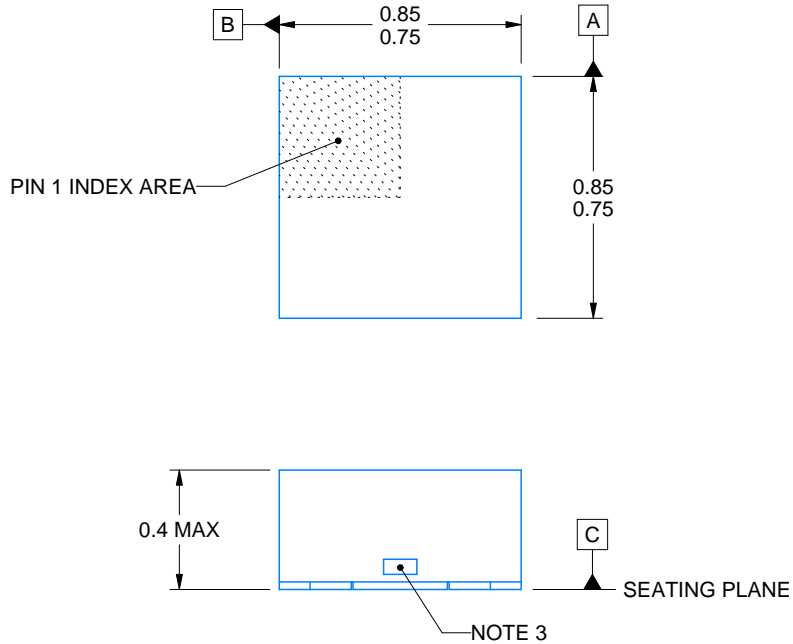
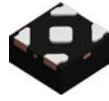
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211218-3/D





4223102/C 06/2021

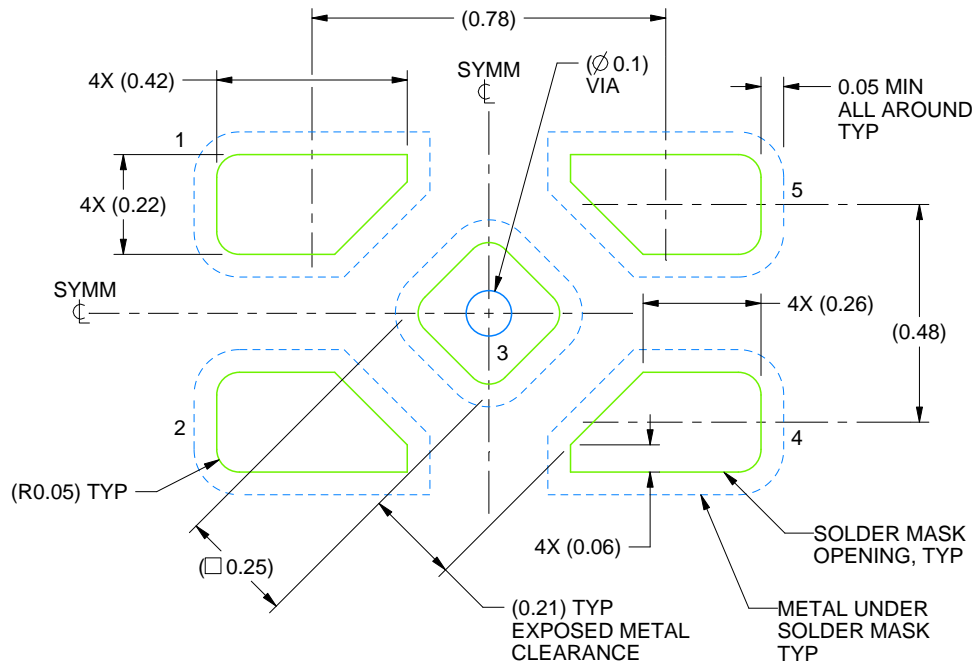
**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

**DPW0005A**

**X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:60X

4223102/C 06/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3  
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:100X

4223102/C 06/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

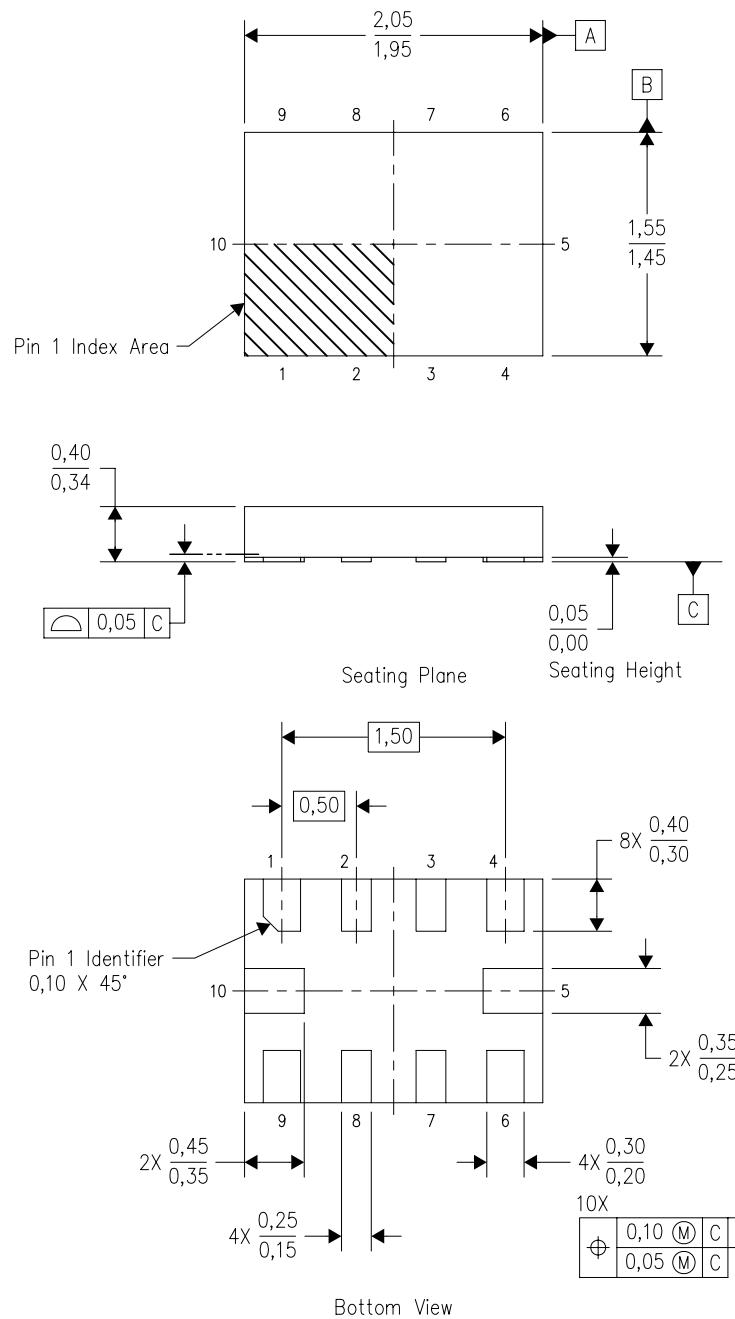
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RUG (R-PQFP-N10)

PLASTIC QUAD FLATPACK

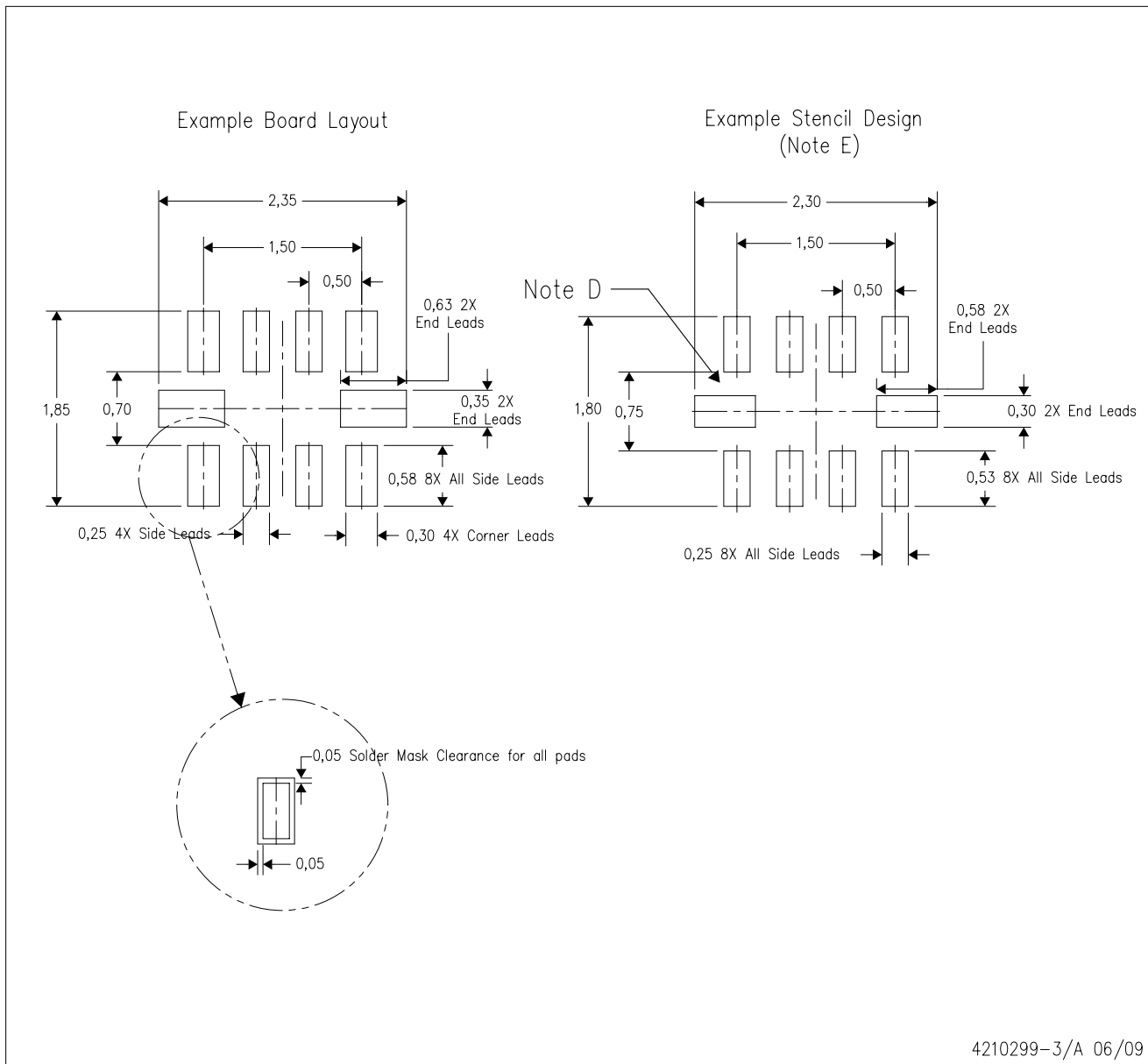


4208528-3/B 04/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. This package complies to JEDEC MO-288 variation X2EFD.



RUG (R-PQFP-N10)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

**D0008A**

## SOIC - 1.75 mm max height

## SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



## SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

## NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## GENERIC PACKAGE VIEW

**DSG 8**

**WSON - 0.8 mm max height**

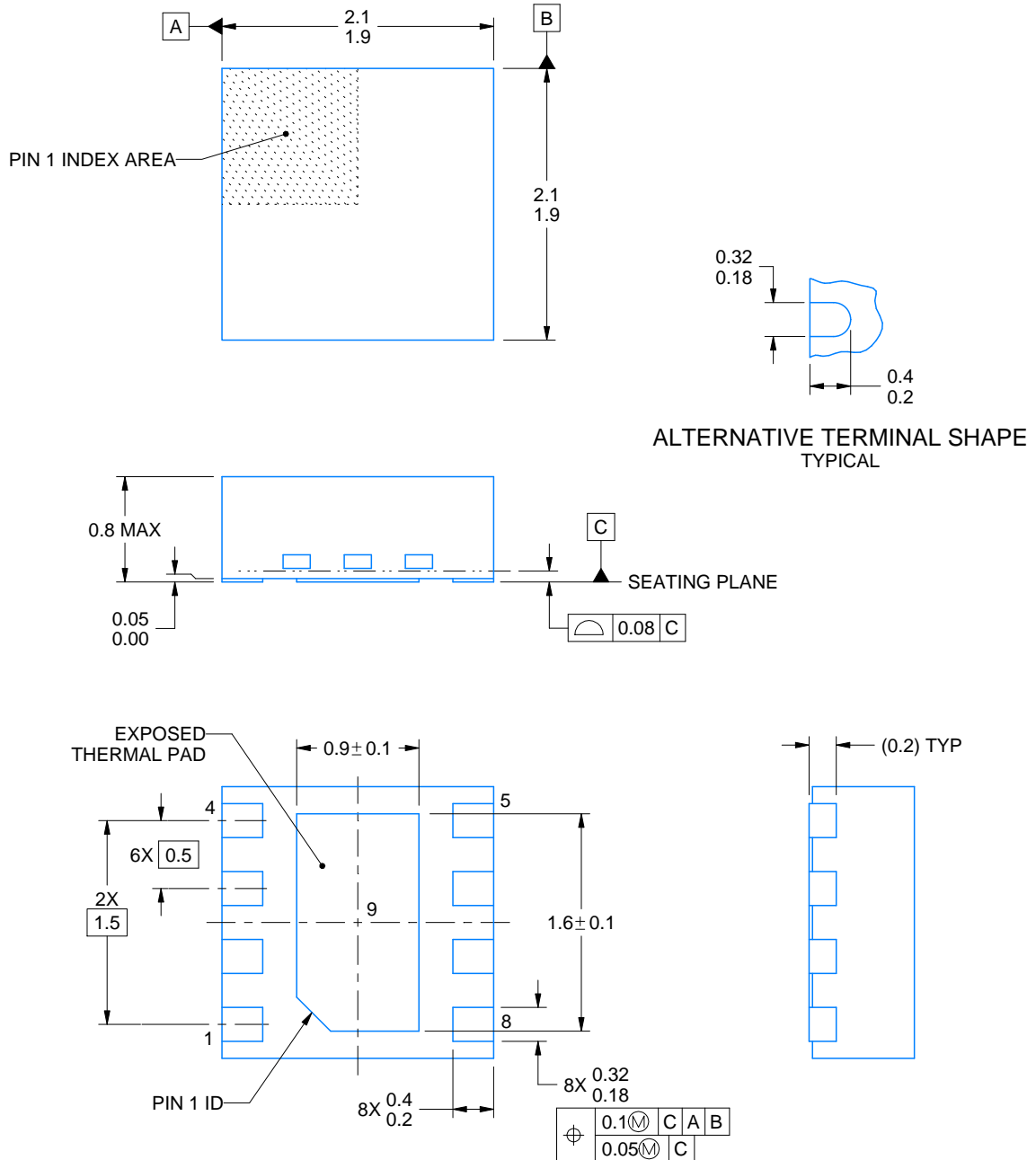
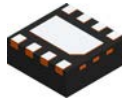
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224783/A



4218900/D 04/2020

## NOTES:

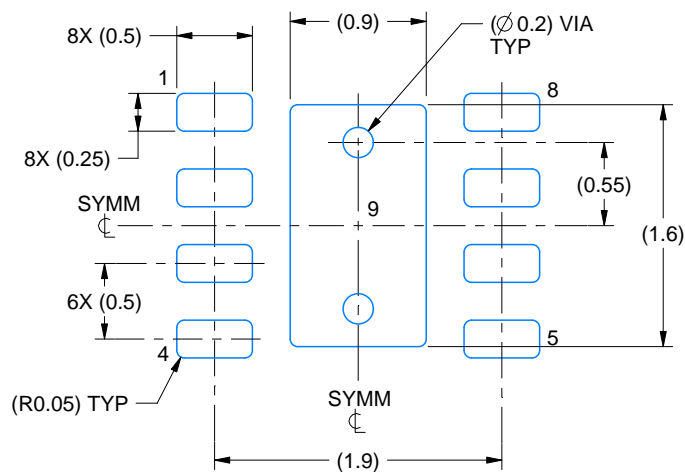
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



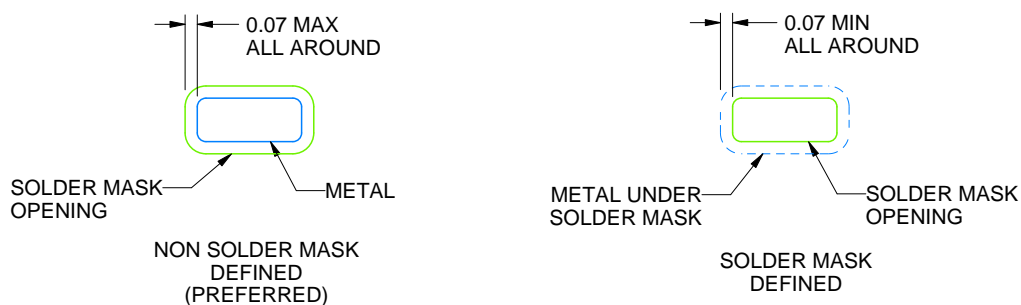
**DSG0008A**

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



## SOLDER MASK DETAILS

4218900/D 04/2020

NOTES: (continued)

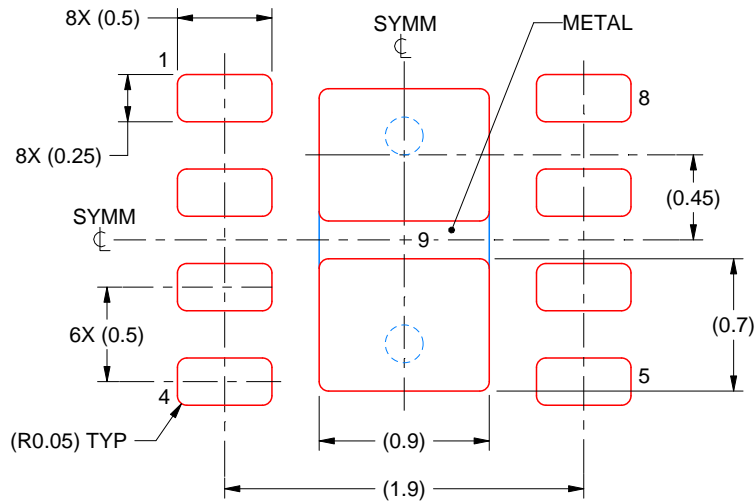
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

DSG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4218900/D 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

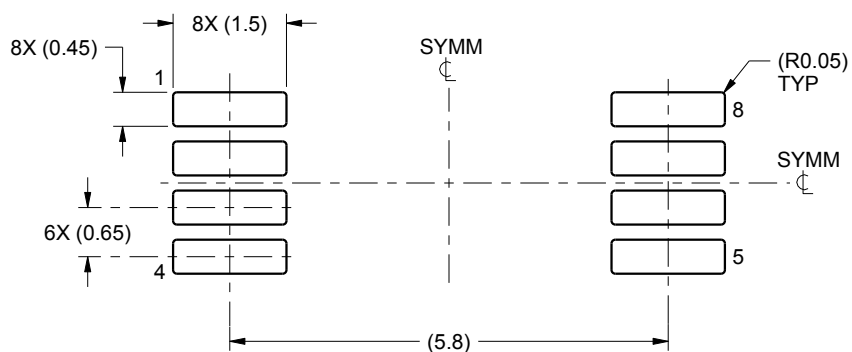


# EXAMPLE BOARD LAYOUT

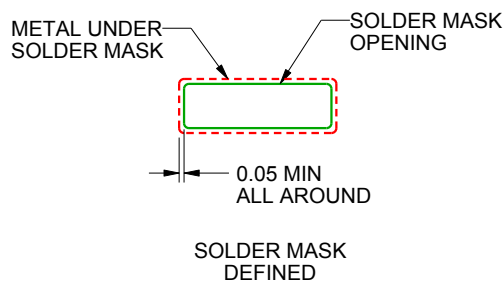
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

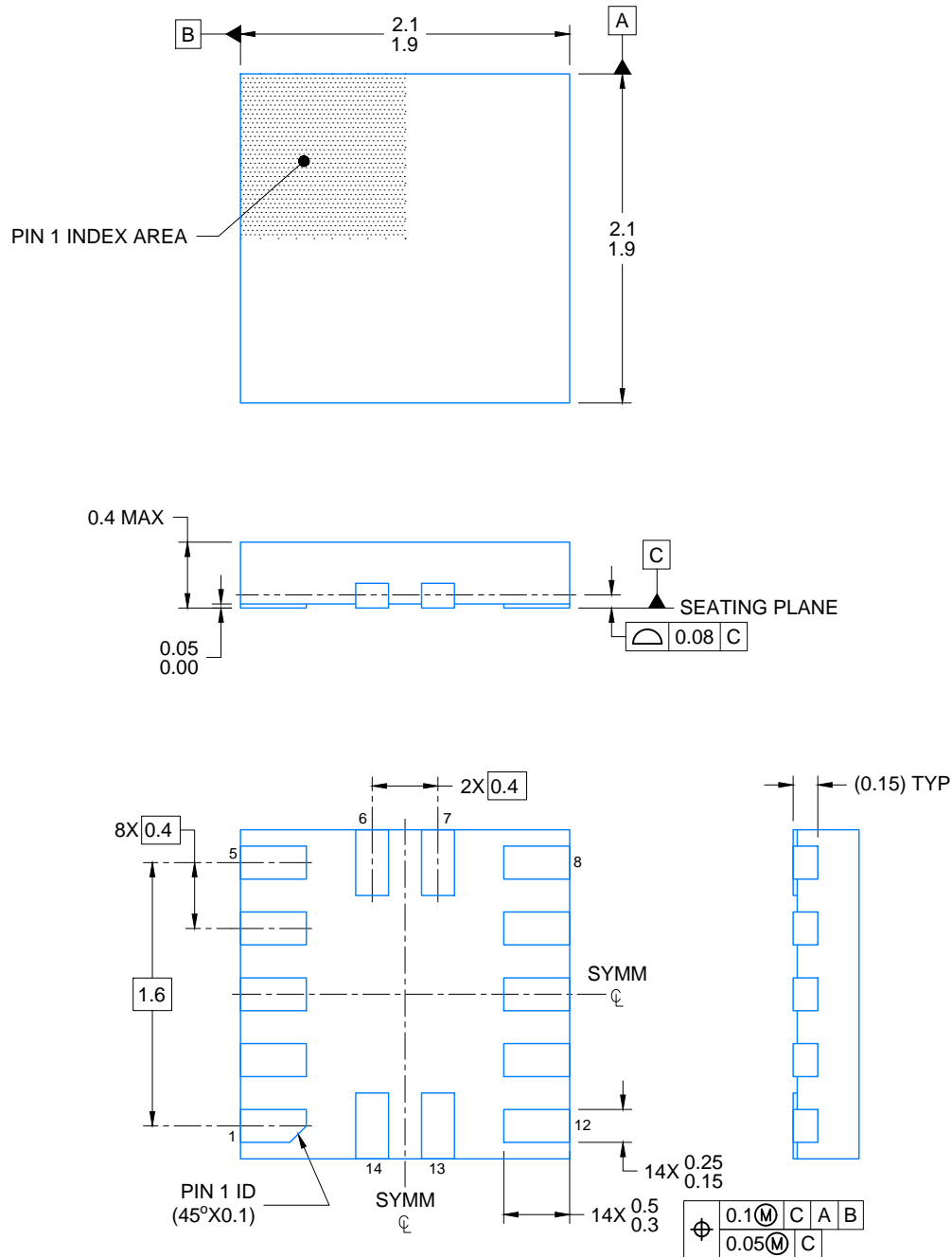


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

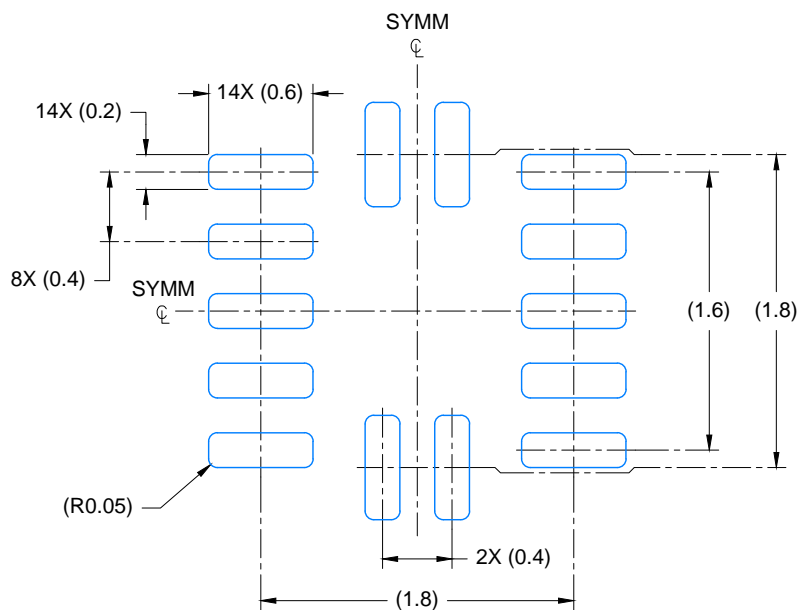
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



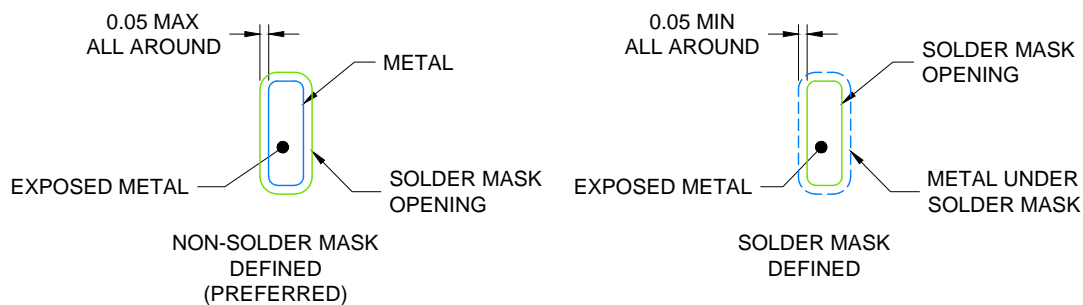
4220584/A 05/2019

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 23X



SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

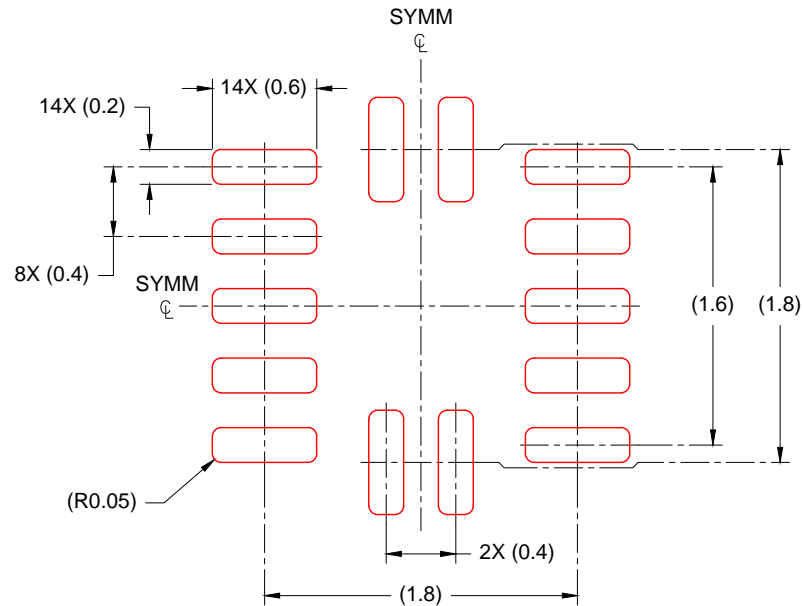
- For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

RUC0014A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.100mm THICK STENCIL  
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



## 重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (<https://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 或 [ti.com.cn](https://www.ti.com.cn) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2021 德州仪器半导体技术（上海）有限公司