TEXAS INSTRUMENTS
TLV9002-Q1, TLV9004-Q1
ZHCSJN6B – MAY 2019 – REVISED MARCH 2021

TLV900x-Q1 低功耗 RRIO 1MHz 汽车运算放大器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C 至 +125°C，T_A
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 可扩展 CMOS 放大器，适用于低成本应用
- 轨至轨输入和输出
- 低输入失调电压：±0.4mV
- 单位带宽增益积：1MHz
- 低宽带噪声：27nV/$\sqrt{Hz}$
- 低输入偏置电流：5pA
- 低静态电流：60μA/通道
- 单位增益稳定
- 内置 RFI 和 EMI 滤波器
- 可在电源电压低至 1.8V 的情况下运行
- 由于具有电阻式开环输出阻抗，因此可在更高的容性负载下更轻松地实现稳定
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档

2 应用

- 针对 AEC-Q100 1 级应用进行了优化
- 信息娱乐系统与仪表组
- 被动安全
- 车身电子装置和照明
- 混合动力汽车/电动汽车逆变器和电机控制
- 车载充电器 (OBC) 和无线充电器
- 动力总成电流传感器
- 高级驾驶辅助系统 (ADAS)
- 单电源、低侧、单向电流感应电路

3 说明

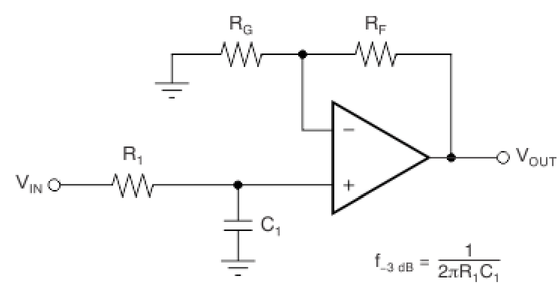
TLV900x-Q1 系列包括双通道 (TLV9002-Q1) 和四通道 (TLV9004-Q1) 低压（1.8V 至 5.5V）运算放大器，具有轨至轨输入和输出摆幅功能。这些运算放大器为空间受限、需要低压运行和高容性负载驱动的汽车应用（例如信息娱乐系统和照明）提供了一种具有成本效益的解决方案。TLV900x-Q1 系列的容性负载驱动器具有 500pF 的电容，并且电阻式开环输出阻抗使其能够在更高的容性负载下更轻松地实现稳定。这些运算放大器专为低工作电压（1.8V 至 5.5V）而设计，性能规格类似于 TLV600x-Q1 器件。

TLV900x-Q1 系列稳健的设计可简化电路设计。这些运算放大器具有单位增益稳定性，集成了 RFI 和 EMI 抑制滤波器，并且在过驱情况下不会出现相位反转。

器件信息

器件型号 (1)	封装	封装尺寸（标称值）
TLV9002-Q1	SOIC (8)	3.91mm × 4.90mm
	TSSOP (8)(2)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
TLV9004-Q1	SOT-23 (14)(2)	4.20mm × 1.90mm
	SOIC (14)	8.65mm × 3.91mm
	TSSOP (14)(2)	4.40mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 仅表示封装为预发布。



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

单极低通滤波器

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (June 2020) to Revision B (March 2021) **Page**

- 更新了整个文档的表、图和交叉参考的编号格式........ 1
- 向*特性* 部分添加了提供功能安全和文档的链接........ 1
- 删除了*器件信息* 部分中 VSSOP (8) 的预发布标签........ 1
- Added note 4 to differential input voltage in *Absolute Maximum Ratings* table 6
- Added Thermal Information for DGK package........ 6
- Added Thermal Information for DYY package........ 7

Changes from Revision * (May 2019) to Revision A (June 2020) **Page**

- 将器件状态从*预告信息* 更改为*量产数据* 1
- 向*应用* 部分添加了终端设备链接........ 1
- 删除了*器件信息* 部分中 SOIC (8) 的预发布标签........ 1
- 向*器件信息* 部分添加了 SOT-23 (14)........ 1
- 删除了*器件信息* 部分中 SOIC (14) 的预发布标签........ 1
- Added SOT-23 (DYY) package in *Device Comparison Table* section 3
- Added DYY (SOT-23) in *Pin Functions: TLV9004-Q1* section 4

5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS			
		SOIC D	TSSOP PW	VSSOP DGK	SOT-23 DYY
TLV9002-Q1	2	8	8	8	—
TLV9004-Q1	4	14	14	—	14

6 Pin Configuration and Functions

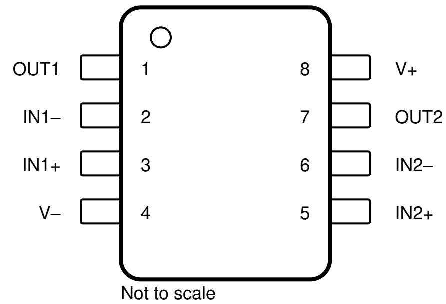


图 6-1. TLV9002-Q1 D, DGK, PW Packages 8-Pin SOIC, VSSOP, TSSOP Top View

表 6-1. Pin Functions: TLV9002-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1 –	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2 –	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V –	4	I or —	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

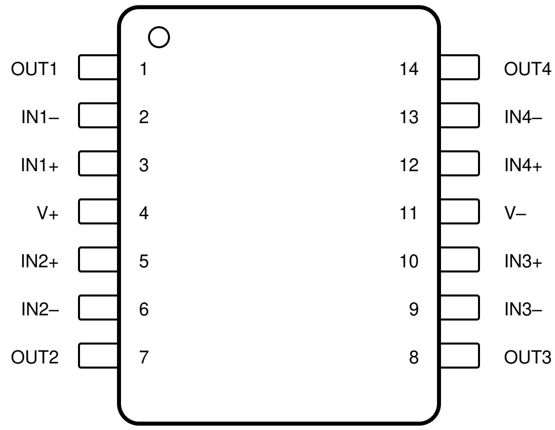


图 6-2. TLV9004-Q1 D, PW, DYY Packages 14-Pin SOIC, TSSOP, SOT-23 Top View

表 6-2. Pin Functions: TLV9004-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1 –	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2 –	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3 –	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4 –	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
NC	—	—	No internal connection
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V –	11	I or —	Negative (low) supply or ground (for single-supply operation)
V+	4	I	Positive (high) supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Supply voltage ([V+] – [V–])			0	6	V
Signal input pins	Voltage[2]	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential [4]		(V+) – (V–) + 0.2	V
	Current[2]		–10	10	mA
Output short-circuit[3]			Continuous		mA
Operating, T_A			–55	150	°C
Junction, T_J				150	°C
Storage, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.
(4) Differential input voltages greater than 0.5 V applied continuously can result in a shift to the input offset voltage and quiescent current above the maximum specifications of these parameters. The magnitude of this effect increases as the ambient operating temperature rises.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with ANSI/ESDA/JEDEC JS-001 Specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	1.8	5.5	V
T_A	Specified temperature	–40	125	°C

7.4 Thermal Information for Dual Channel

THERMAL METRIC [1]		TLV9002-Q1			UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.9	196.6	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.0	86.2	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	95.4	118.3	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	40.2	23.2	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	94.7	116.7	TBD	°C/W

(1) For more information about traditional and new thermalmetrics, see Semiconductor and ICPackage Thermal Metrics application report.

7.5 Thermal Information for Quad Channel

THERMAL METRIC [1]		TLV9004-Q1			UNIT
		D (SOIC)	DYY (SOT-23)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.1	154.3	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.2	86.8	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.1	67.9	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.6	10.1	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.7	67.5	TBD	°C/W

(1) For more information about traditional and new thermalmetrics, see Semiconductor and ICPackage Thermal Metrics application report.

7.6 Electrical Characteristics

For V_S = (V+) – (V –) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V), T_A = 25 °C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	Vs = 5 V		±0.4	±1.85	mV
		Vs = 5 V, T_A = – 40°C to 125°C			±2	mV
dV_{OS}/dT	V_{OS} vs temperature	T_A = – 40°C to 125°C		±0.6		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 to 5.5 V, V_{CM} = (V –)	80	105		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	(V –) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (V –) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = – 40°C to 125°C		86		dB
		V_S = 5.5 V, (V –) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = – 40°C to 125°C		95		dB
		V_S = 5.5 V, (V –) – 0.1 V < V_{CM} < (V+) + 0.1 V, T_A = – 40°C to 125°C	63	77		dB
		V_S = 1.8 V, (V –) – 0.1 V < V_{CM} < (V+)+ 0.1 V, T_A = – 40°C to 125°C		68		dB
INPUT BIAS CURRENT						
I_B	Input bias current	Vs = 5 V		±5		pA
I_{OS}	Input offset current			±2		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz, Vs = 5 V		4.7		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz, Vs = 5 V		30		$nV/\sqrt{Hz}$
		f = 10 kHz, Vs = 5 V		27		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz, Vs = 5 V		23		$fA/\sqrt{Hz}$
INPUT CAPACITANCE						
C_{ID}	Differential			1.5		pF
C_{IC}	Common-mode			5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 5.5 V, (V –) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ	104	117		dB
		V_S = 1.8 V, (V –) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10 kΩ		100		dB
		V_S = 1.8 V, (V –) + 0.1 V < V_O < (V+) – 0.1 V, R_L = 2 kΩ		115		dB
		V_S = 5.5 V, (V –) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ		130		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	Vs = 5 V		1		MHz
ϕ_m	Phase margin	V_S = 5.5 V, G = 1		78		degrees
SR	Slew rate	Vs = 5 V		2		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2 V Step , G = +1, C_L = 100 pF		2.5		µs
		To 0.01%, V_S = 5 V, 2 V Step , G = +1, C_L = 100 pF		3		µs
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		0.85		µs
THD+N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz, 80 kHz measurement BW		0.004		%
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ		10	20	mV
		V_S = 5.5 V, R_L = 2 kΩ		35	55	mV
I_{SC}	Short-circuit current	Vs = 5.5 V		±40		mA

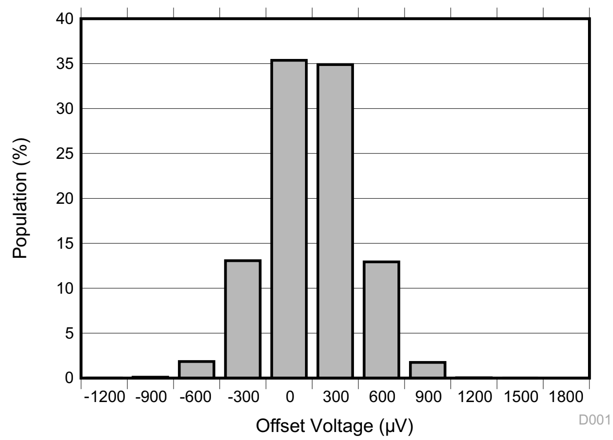
7.6 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V), T_A = 25 °C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_O	Open-loop output impedance	Vs = 5 V, f = 1 MHz		1200		Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	I_O = 0 mA, V_S = 5.5 V		60	80	µA
		I_O = 0 mA, V_S = 5.5 V, T_A = –40°C to 125°C			85	µA
	Power-on time	V_S = 0 V to 5 V, to 90% I_Q level		50		µs

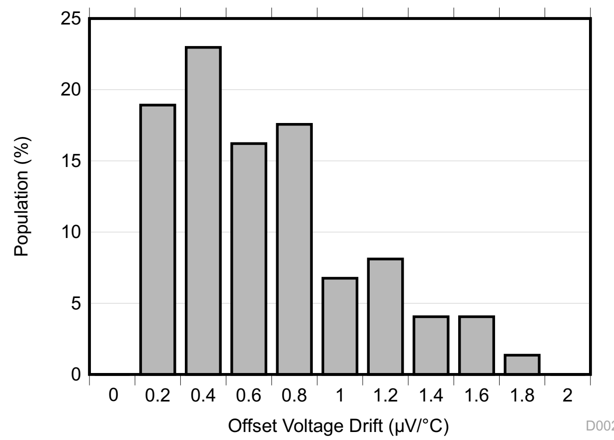
7.7 Typical Characteristics

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5 V

图 7-1. Offset Voltage Distribution Histogram



V_S = 5 V, T_A = –40°C to +125°C

图 7-2. Offset Voltage Drift Distribution Histogram

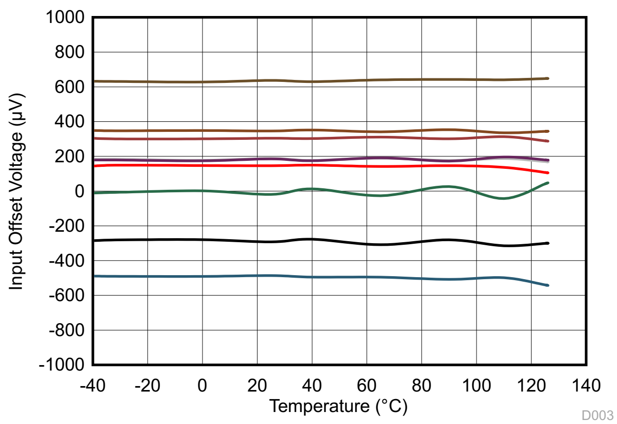


图 7-3. Input Offset Voltage vs Temperature

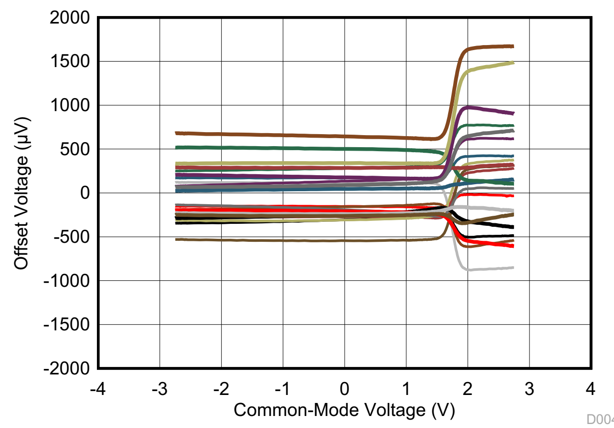


图 7-4. Offset Voltage vs Common-Mode

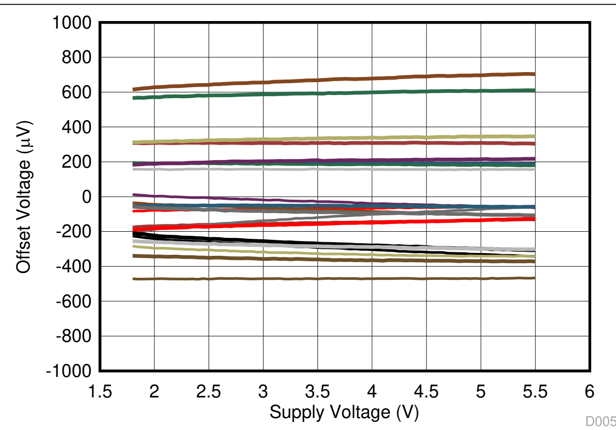


图 7-5. Offset Voltage vs Supply Voltage

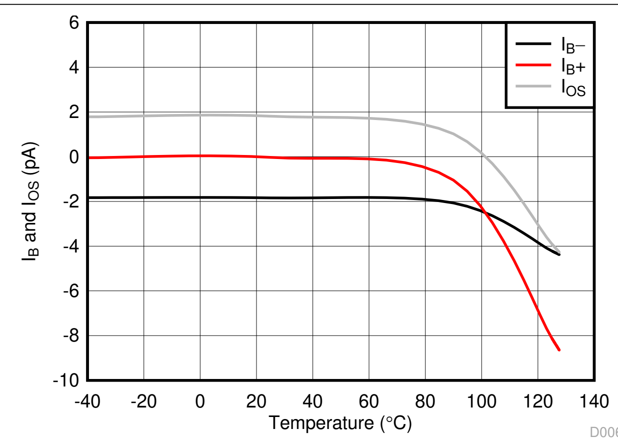


图 7-6. I_B and I_{OS} vs Temperature

7.7 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

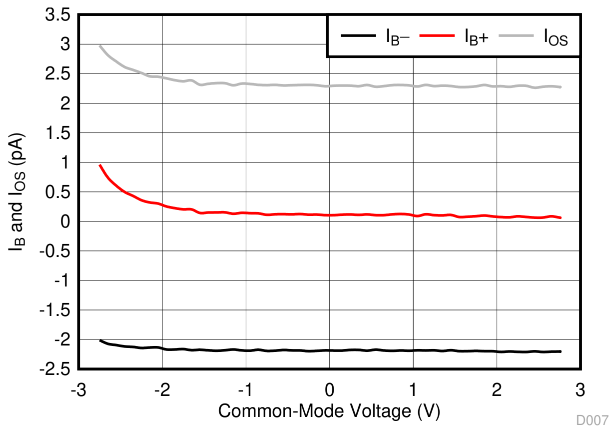


图 7-7. I_B and I_{OS} vs Common-Mode Voltage

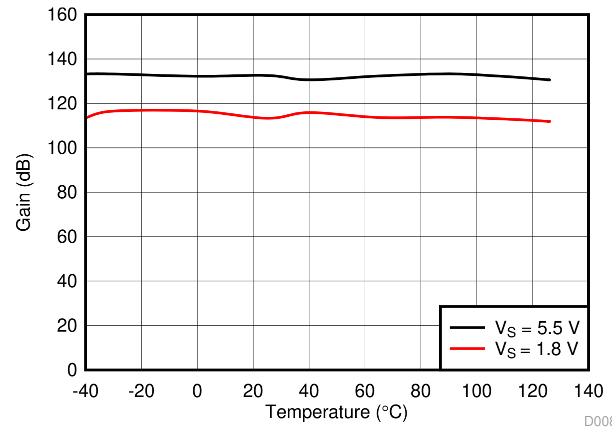
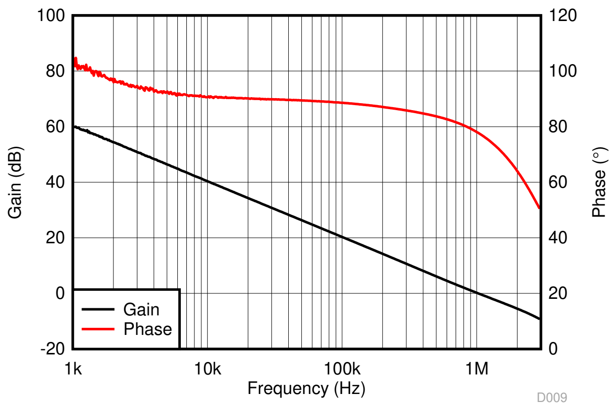


图 7-8. Open-Loop Gain vs Temperature



C_L = 10 pF

图 7-9. Open-Loop Gain and Phase vs Frequency

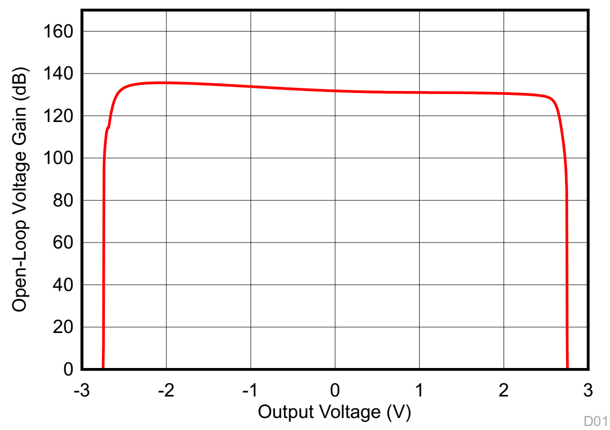
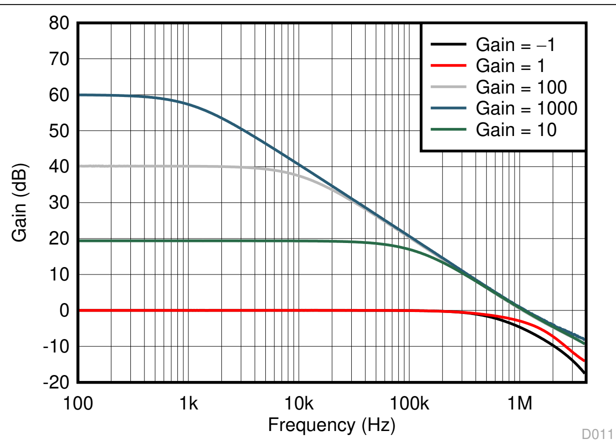


图 7-10. Open-Loop Gain vs Output Voltage



C_L = 10 pF

图 7-11. Closed-Loop Gain vs Frequency

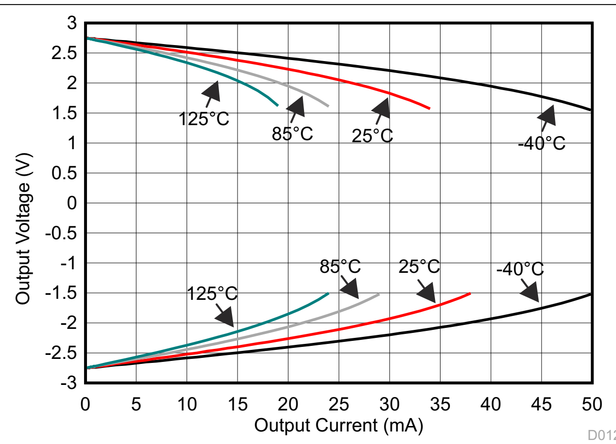


图 7-12. Output Voltage vs Output Current (Claw)

7.7 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

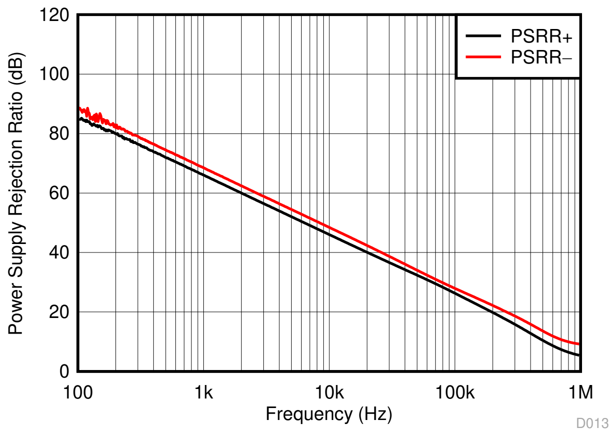
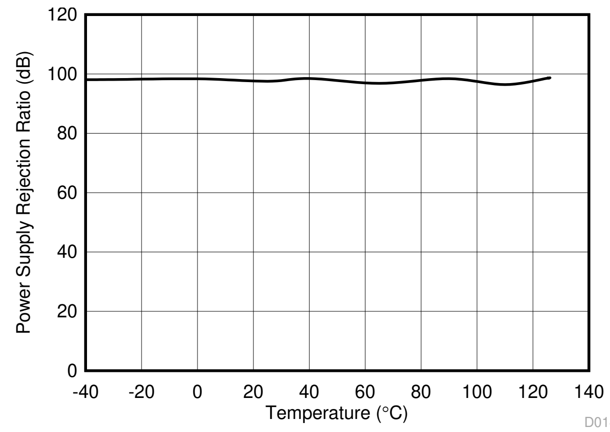


图 7-13. PSRR vs Frequency



V_S = 1.8 V to 5.5 V

图 7-14. DC PSRR vs Temperature

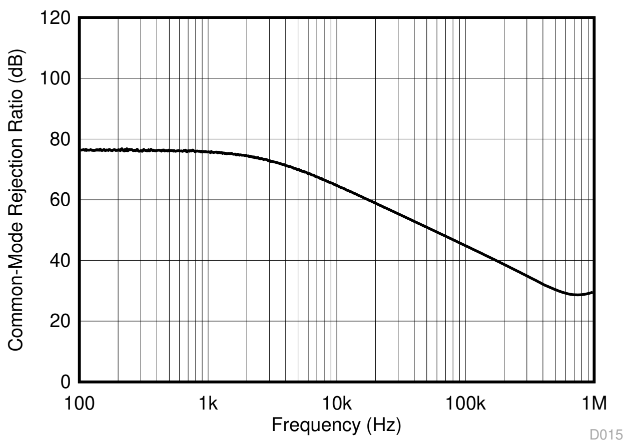
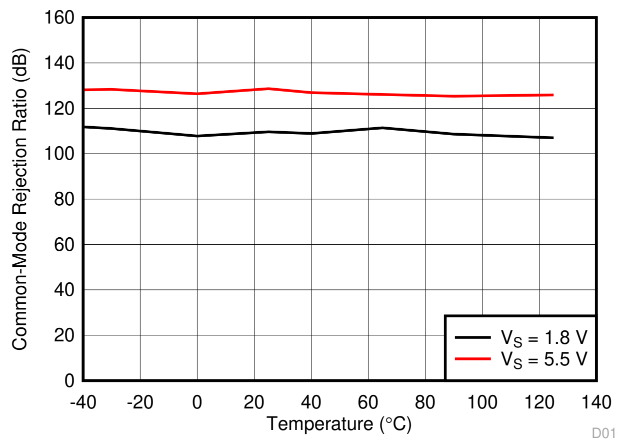


图 7-15. CMRR vs Frequency



V_{CM} = (V–) – 0.1 V to (V+) – 1.4 V

图 7-16. DC CMRR vs Temperature

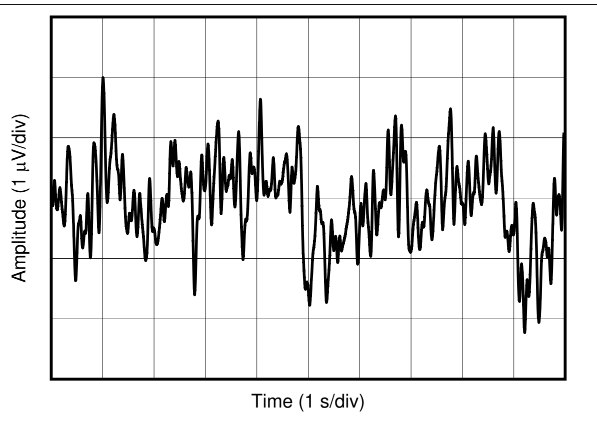


图 7-17. 0.1 Hz to 10 Hz Integrated Voltage Noise

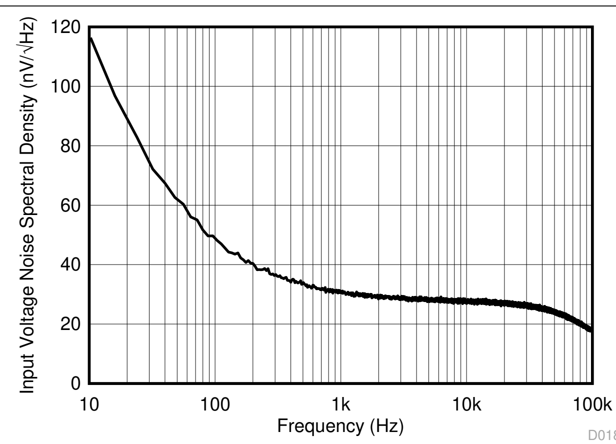
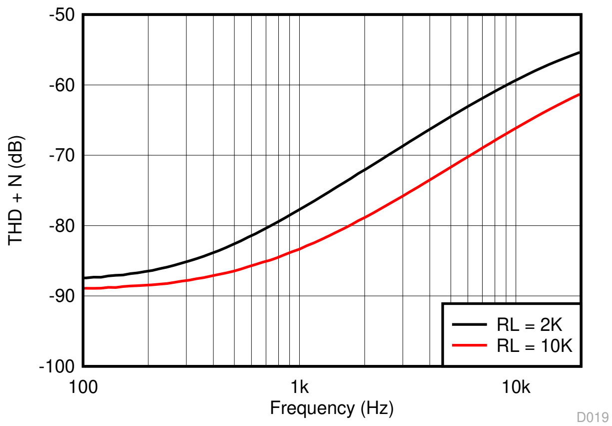


图 7-18. Input Voltage Noise Spectral Density

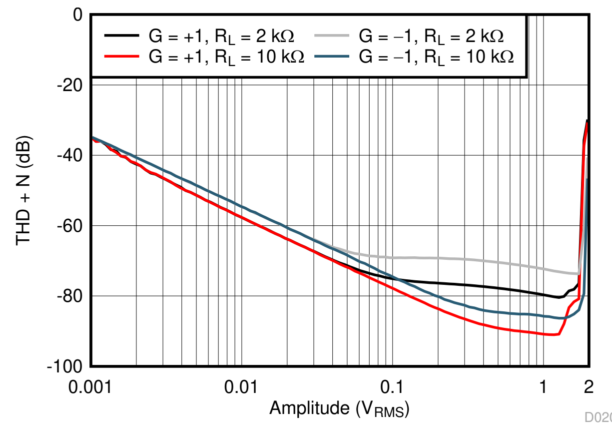
7.7 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5.5 V V_{CM} = 2.5 V G = 1
BW = 80 kHz V_{OUT} = 0.5 V_{RMS}

图 7-19. THD + N vs Frequency



V_S = 5.5 V V_{CM} = 2.5 V f = 1 kHz
G = 1 BW = 80 kHz

图 7-20. THD + N vs Amplitude

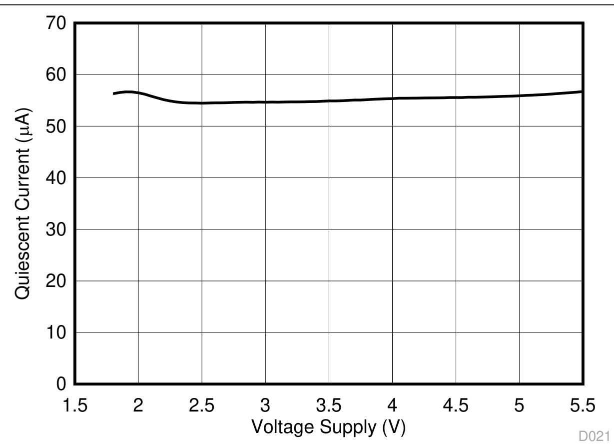


图 7-21. Quiescent Current vs Supply Voltage

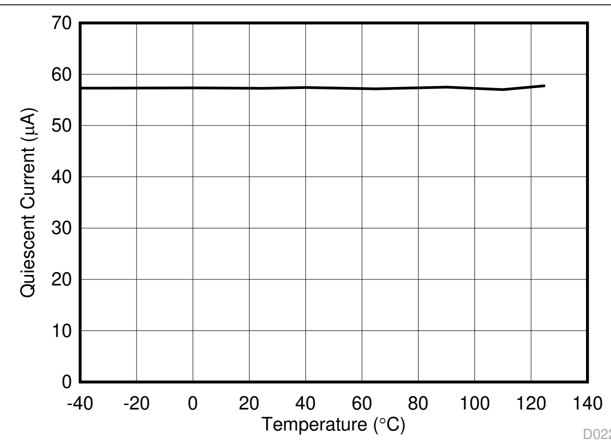


图 7-22. Quiescent Current vs Temperature

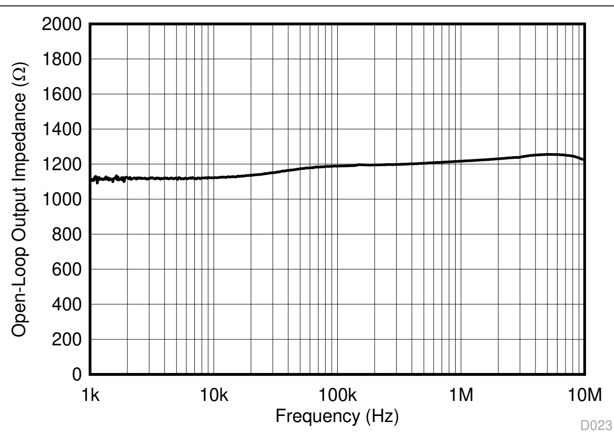
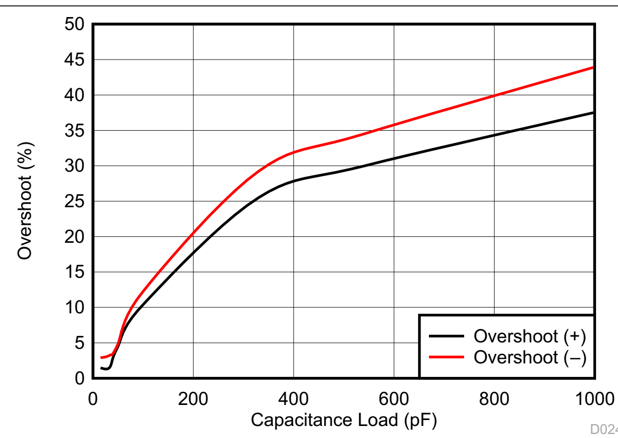


图 7-23. Open-Loop Output Impedance vs Frequency

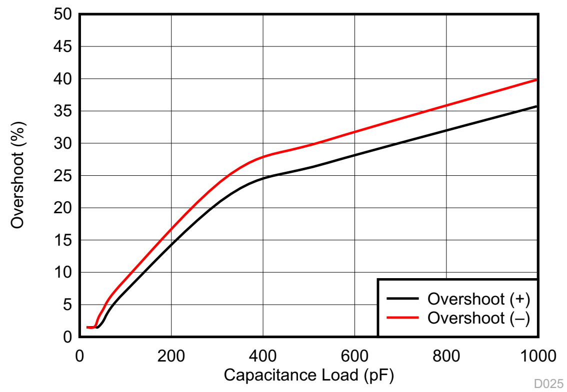


G = 1 V_{IN} = 100 mVpp

图 7-24. Small Signal Overshoot vs Capacitive Load

7.7 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = –1 V_{IN} = 100 mVpp

图 7-25. Small Signal Overshoot vs Capacitive Load

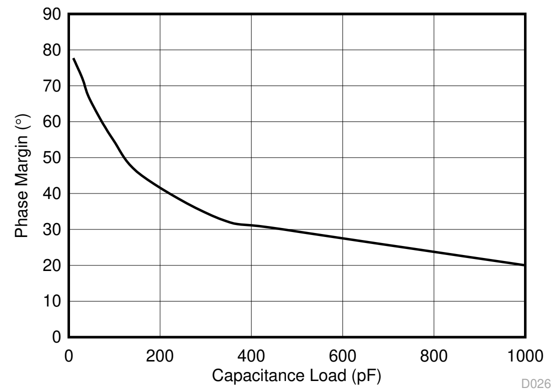
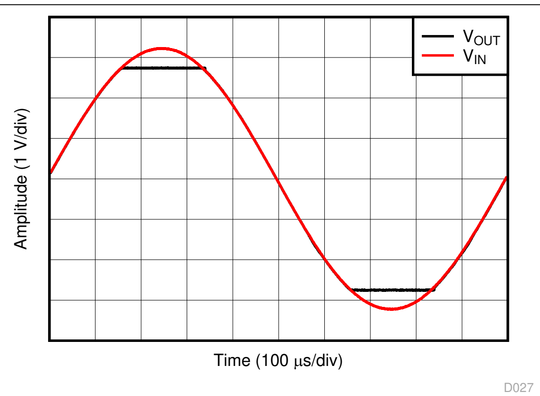
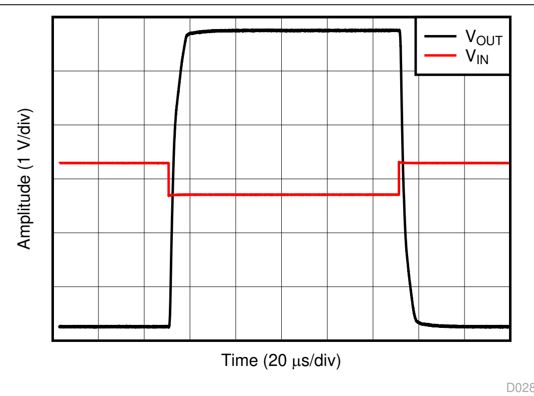


图 7-26. Phase Margin vs Capacitive Load



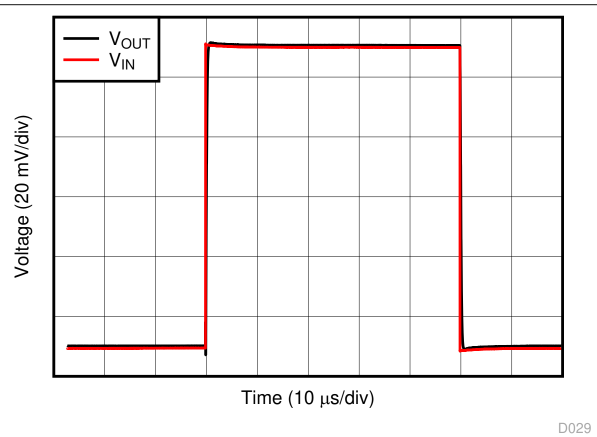
G = 1 V_{IN} = 6.5 V_{PP}

图 7-27. No Phase Reversal



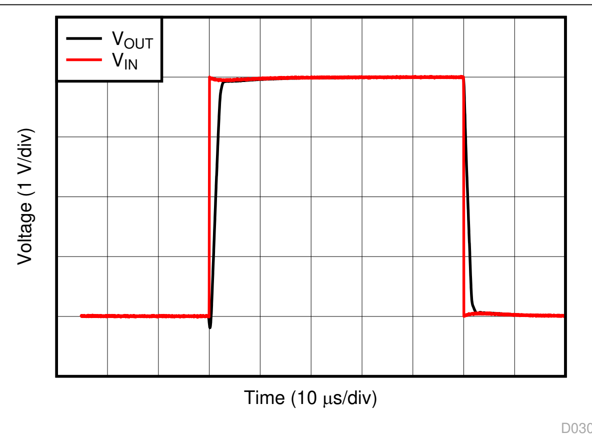
G = –10 V_{IN} = 600 mV_{PP}

图 7-28. Overload Recovery



G = 1 V_{IN} = 100 mV_{PP} C_L = 10 pF

图 7-29. Small-Signal Step Response

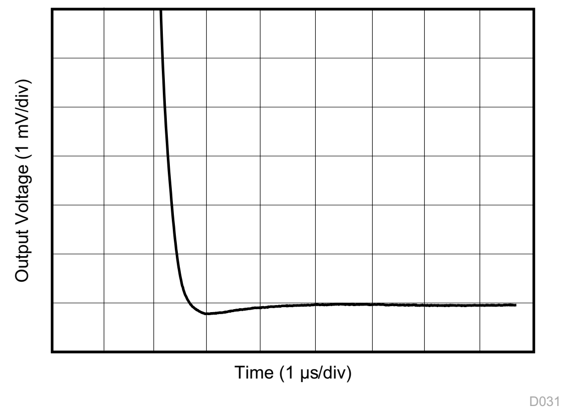


G = 1 V_{IN} = 4 V_{PP} C_L = 10 pF

图 7-30. Large-Signal Step Response

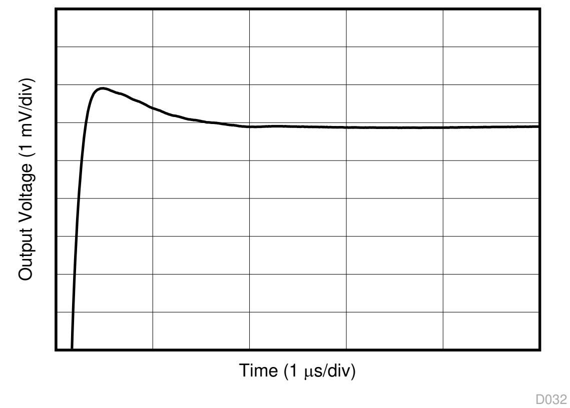
7.7 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = 1 C_L = 100 pF 2-V step

图 7-31. Large-Signal Settling Time (Negative)



G = 1 C_L = 100 pF 2-V step

图 7-32. Large-Signal Settling Time (Positive)

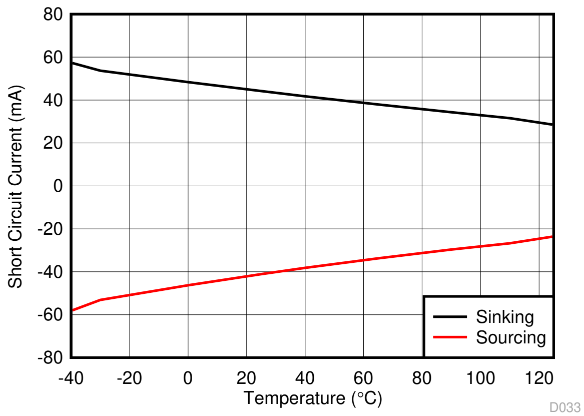


图 7-33. Short-Circuit Current vs Temperature

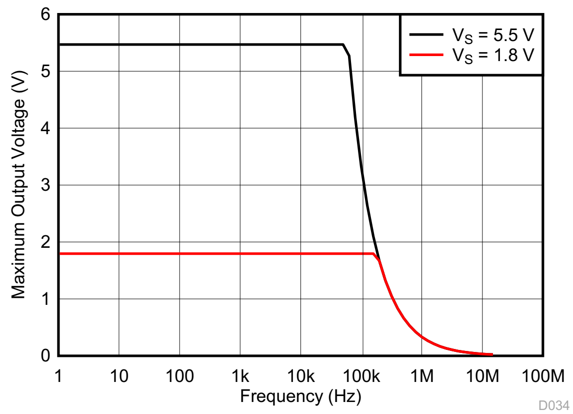


图 7-34. Maximum Output Voltage vs Frequency

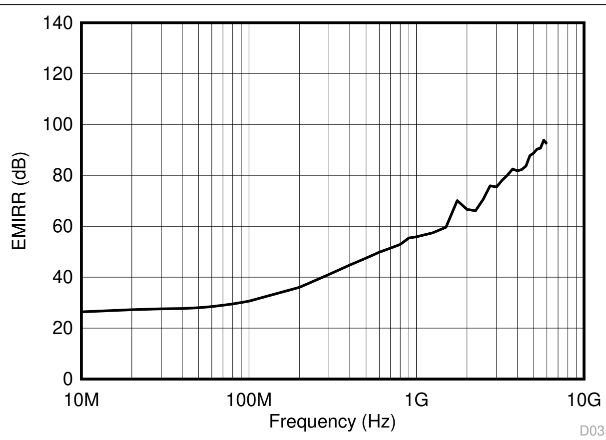


图 7-35. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

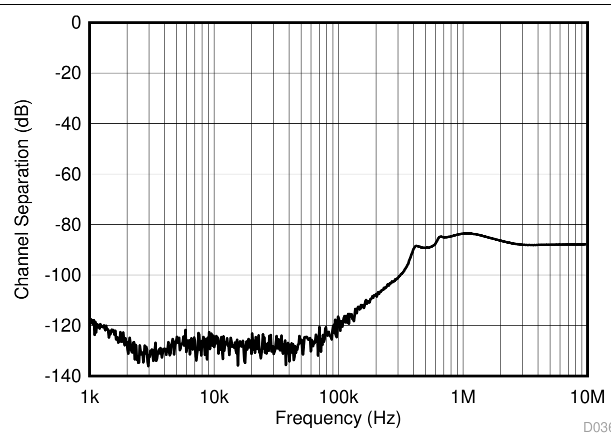


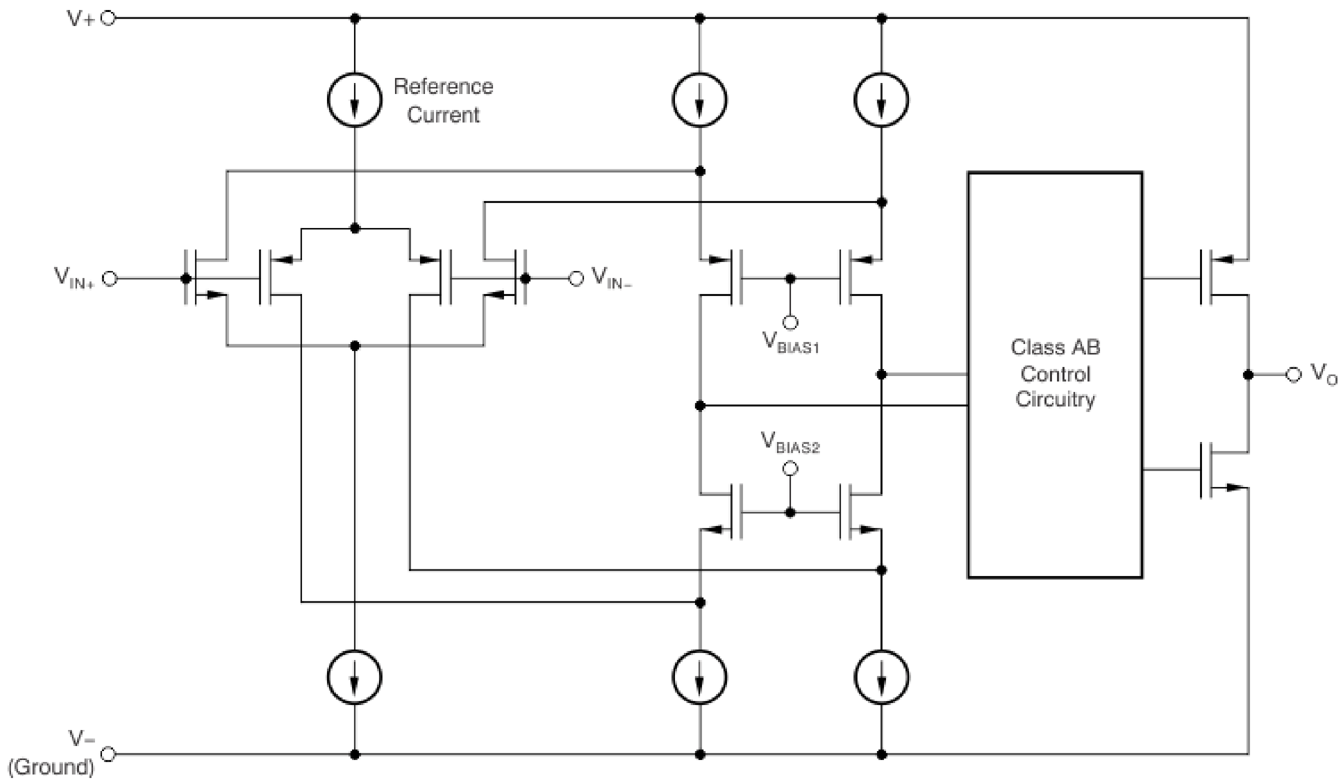
图 7-36. Channel Separation

8 Detailed Description

8.1 Overview

The TLV900x-Q1 is a family of automotive qualified, low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV900x-Q1 family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them suitable for driving sampling analog-to-digital converters (ADCs).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The TLV900x-Q1 family of op amps are for operation from 1.8 V to 5.5 V. In addition, many specifications such as input offset voltage, quiescent current, offset current, and short circuit current apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are shown in the typical characteristics section.

8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV900x-Q1 family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram* section. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 100 mV above the positive supply, whereas the P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 100-mV transition region can vary up to 100 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

8.3.3 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV900x-Q1 family delivers a robust output drive capability. A class-AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within 20 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.4 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV900x-Q1 family is approximately 850 ns.

8.4 Device Functional Modes

The TLV900x-Q1 family has a single functional mode. The devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TLV900x-Q1 family of low-power, rail-to-rail input and output operational amplifiers is specifically designed for portable applications. The devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving less than or equal to 10-kΩ loads connected to any point between V+ and V－. The input common-mode voltage range includes both rails, and allows the TLV900x-Q1 devices to be used in any single-supply application.

9.2 Typical Application

9.2.1 TLV900x-Q1 Low-Side, Current Sensing Application

图 9-1 shows the TLV900x-Q1 configured in a low-side current sensing application.

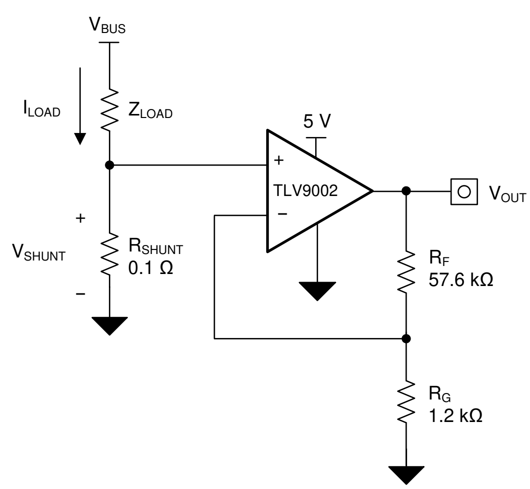


图 9-1. TLV900x-Q1 in a Low-Side, Current-Sensing Application

9.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

9.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 图 9-1 is given in 方程式 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is shown using 方程式 2:

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \tag{2}$$

Using 方程式 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV900x-Q1 to produce an output voltage of approximately 0 V to 4.9 V. The gain needed by the TLV900x-Q1 to produce the necessary output voltage is calculated using 方程式 3:

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \tag{3}$$

Using 方程式 3, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. 方程式 4 sizes the resistors R_F and R_G, to set the gain of the TLV900x-Q1 to 49 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \tag{4}$$

Selecting R_F as 57.6 kΩ and R_G as 1.2 kΩ provides a combination that equals 49 V/V. 图 9-2 shows the measured transfer function of the circuit shown in 图 9-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

9.2.1.3 Application Curve

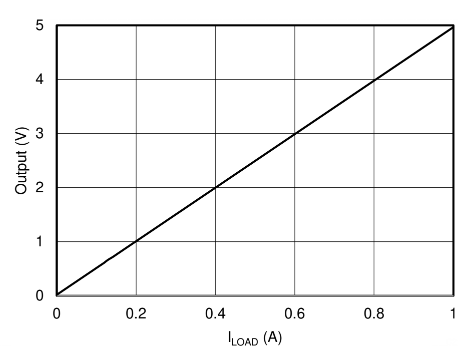


图 9-2. Low-Side, Current-Sense Transfer Function

9.2.2 Single-Supply Photodiode Amplifier

Photodiodes are used in many applications to convert light signals to electrical signals. The current through the photodiode is proportional to the photon energy absorbed, and is commonly in the range of a few hundred picoamps to a few tens of microamps. An amplifier in a transimpedance configuration is typically used to convert the low-level photodiode current to a voltage signal for processing in an MCU. The circuit shown in 图 9-3 is an example of a single-supply photodiode amplifier circuit using the TLV9002-Q1.

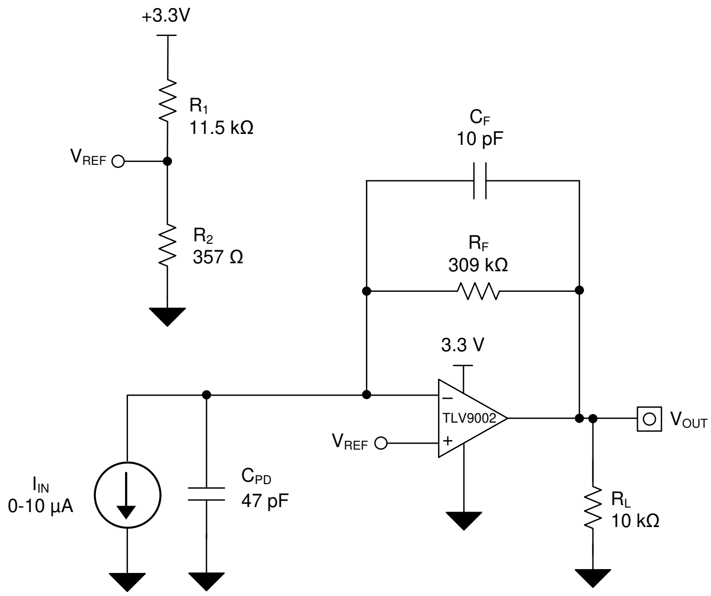


图 9-3. Single-Supply Photodiode Amplifier Circuit

9.2.2.1 Design Requirements

The design requirements for this design are:

- Supply voltage: 3.3 V
- Input: 0 µA to 10 µA
- Output: 0.1 V to 3.2 V
- Bandwidth: 50 kHz

9.2.2.2 Detailed Design Procedure

The transfer function between the output voltage (V_{OUT}), the input current, (I_{IN}) and the reference voltage (V_{REF}) is defined in 方程式 5.

$$V_{OUT} = I_{IN} \times R_F + V_{REF} \tag{5}$$

Where:

$$V_{REF} = V_{+} \times \left(\frac{R_1 \times R_2}{R_1 + R_2} \right) \tag{6}$$

Set V_{REF} to 100 mV to meet the minimum output voltage level by setting R1 and R2 to meet the required ratio calculated in 方程式 7.

$$\frac{V_{REF}}{V_{+}} = \frac{0.1\ V}{3.3\ V} = 0.0303 \tag{7}$$

The closest resistor ratio to meet this ratio sets R1 to 11.5 kΩ and R2 to 357 Ω.

The required feedback resistance can be calculated based on the input current and desired output voltage.

$$R_F = \frac{V_{OUT} - V_{REF}}{I_{IN}} = \frac{3.2\ V - 0.1\ V}{10\ \mu A} = 310 \frac{kV}{A} \approx 309\ k\Omega \tag{8}$$

Calculate the value for the feedback capacitor based on R_F and the desired –3-dB bandwidth, (f_{-3dB}) using 方程式 9.

$$C_F = \frac{1}{2 \times \pi \times R_F \times f_{-3dB}} = \frac{1}{2 \times \pi \times 309\ k\Omega \times 50\ kHz} = 10.3\ pF \approx 10\ pF \tag{9}$$

The minimum op amp bandwidth required for this application is based on the value of R_F, C_F, and the capacitance on the INx– pin of the TLV9002-Q1 which is equal to the sum of the photodiode shunt capacitance, (CPD) the common-mode input capacitance, (CCM) and the differential input capacitance (CD) as 方程式 10 shows.

$$C_{IN} = C_{PD} + C_{CM} + C_D = 47\ pF + 5\ pF + 1\ pF = 53\ pF \tag{10}$$

The minimum op amp bandwidth is calculated in 方程式 11.

$$f_{=BGW} \geq \frac{C_{IN} + C_F}{2 \times \pi \times R_F \times C_F^2} \geq 324\ kHz \tag{11}$$

The 1-MHz bandwidth of the TLV900x-Q1 meets the minimum bandwidth requirement and remains stable in this application configuration.

9.2.2.3 Application Curves

The measured current-to-voltage transfer function for the photodiode amplifier circuit is shown in 图 9-4. The measured performance of the photodiode amplifier circuit is shown in 图 9-5.

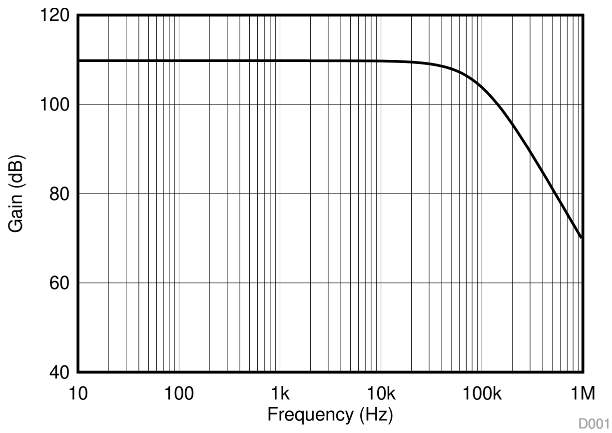


图 9-4. Photodiode Amplifier Circuit AC Gain Results

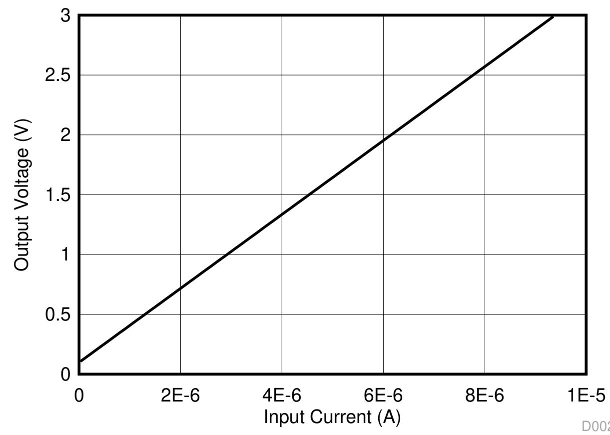


图 9-5. Photodiode Amplifier Circuit DC Results

10 Power Supply Recommendations

The TLV900x-Q1 family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V may permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

10.1 Input and ESD Protection

The TLV900x-Q1 family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA. 图 10-1 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

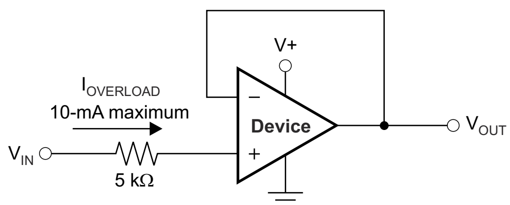


图 10-1. Input Current Protection

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in 图 11-2. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

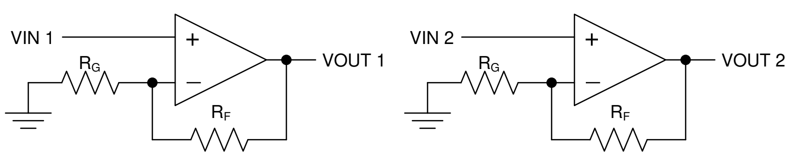


图 11-1. Schematic Representation for Figure 11-2

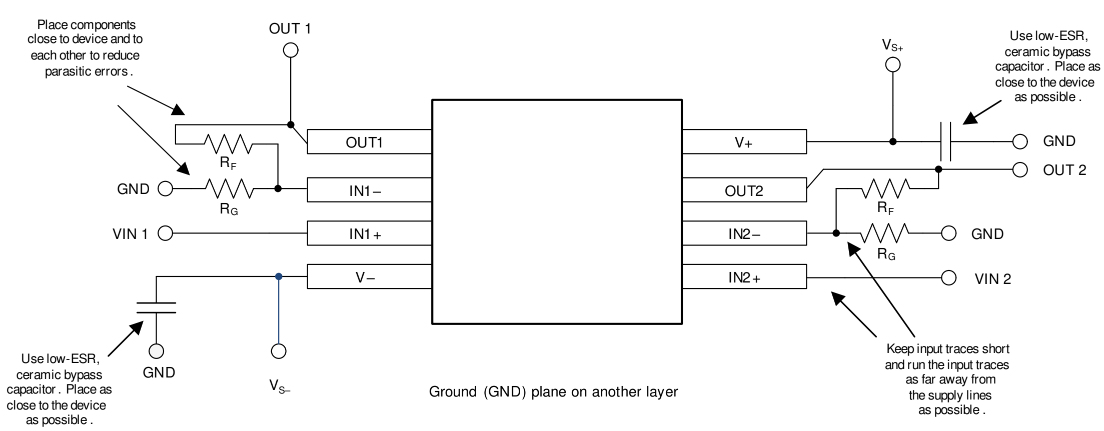


图 11-2. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers*

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV9002-Q1	Click here	Click here	Click here	Click here	Click here
TLV9004-Q1	Click here	Click here	Click here	Click here	Click here

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV9004QDYYRQ1	ACTIVE	SOT-23-THN	DYY	14	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples
TLV9002QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27DT	Samples
TLV9002QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9002Q	Samples
TLV9004QDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV9004Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

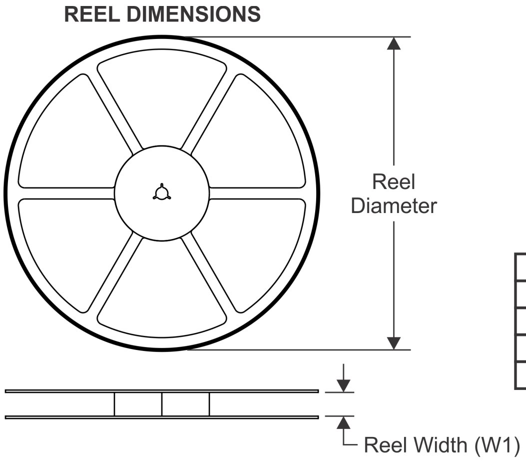
OTHER QUALIFIED VERSIONS OF TLV9002-Q1, TLV9004-Q1 :

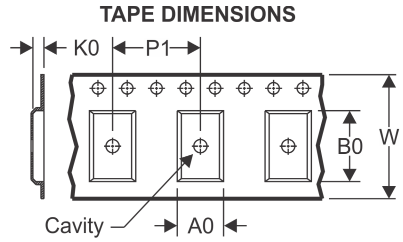
- Catalog : TLV9002, TLV9004

NOTE: Qualified Version Definitions:

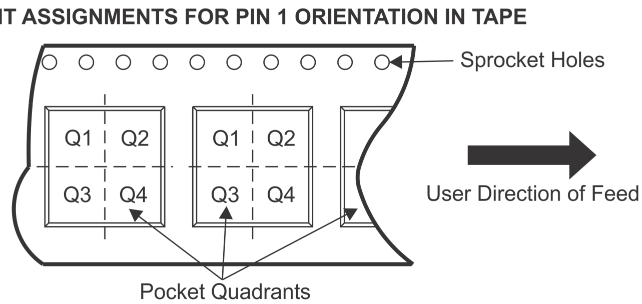
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





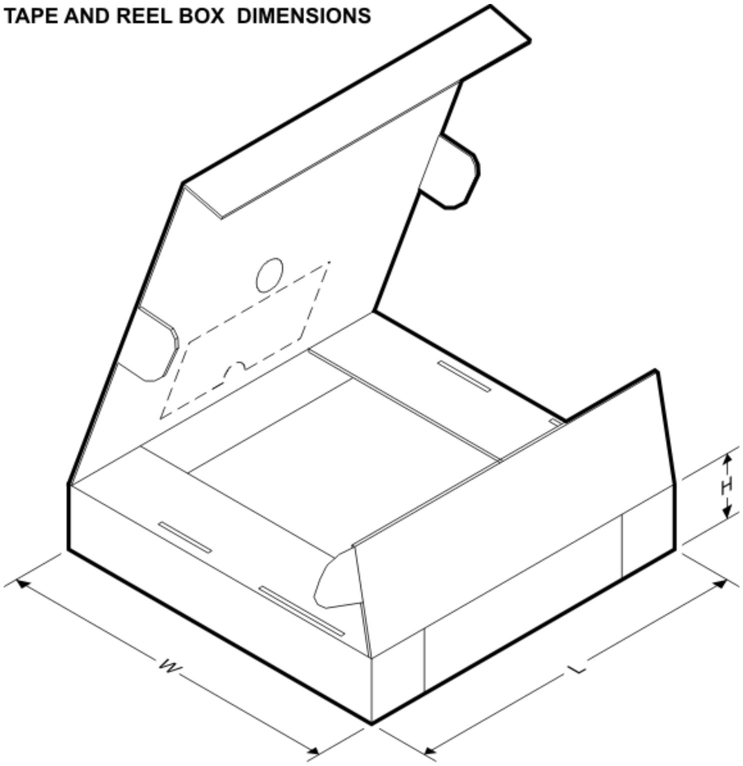
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9002QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9002QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9004QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

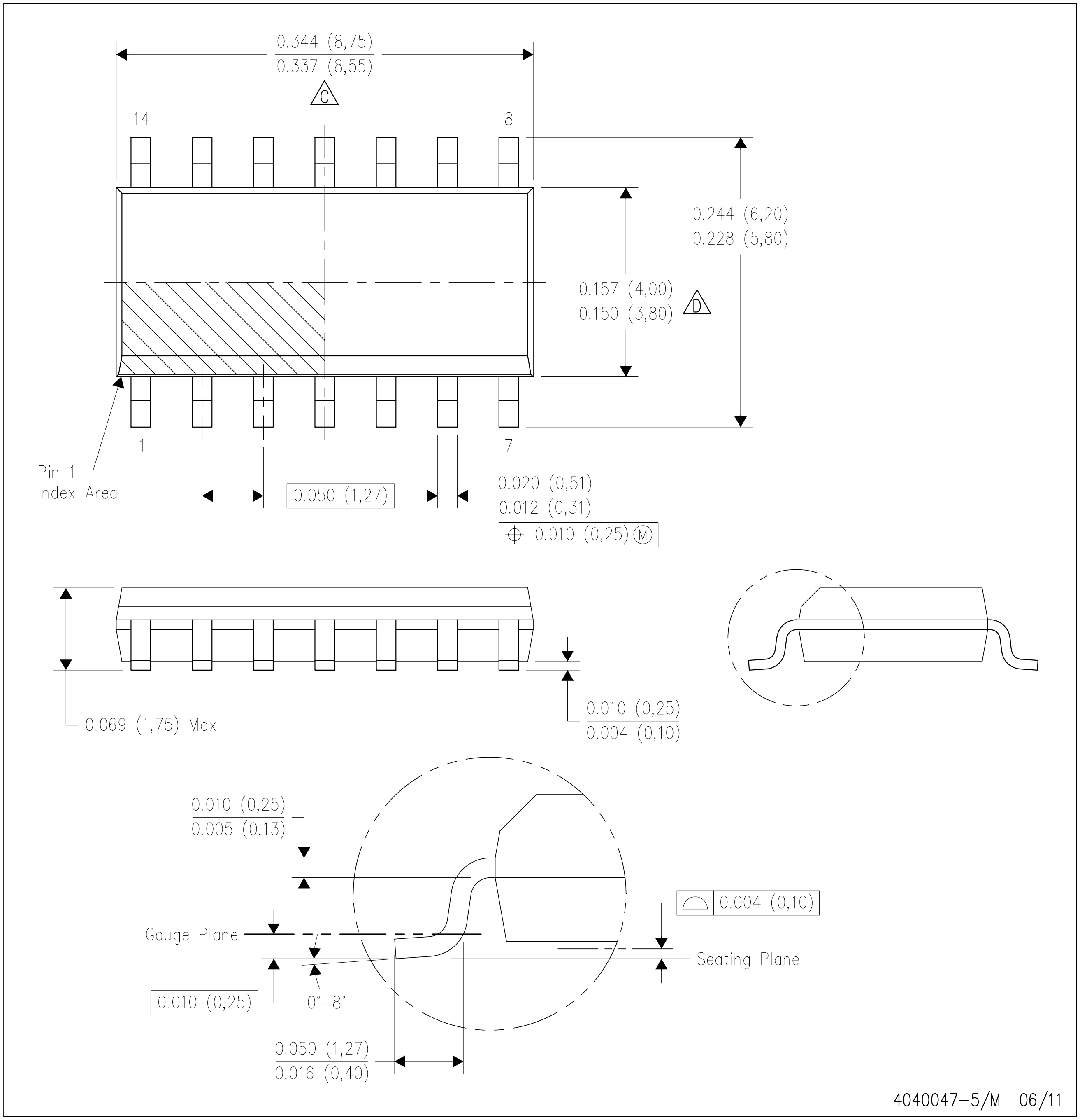
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

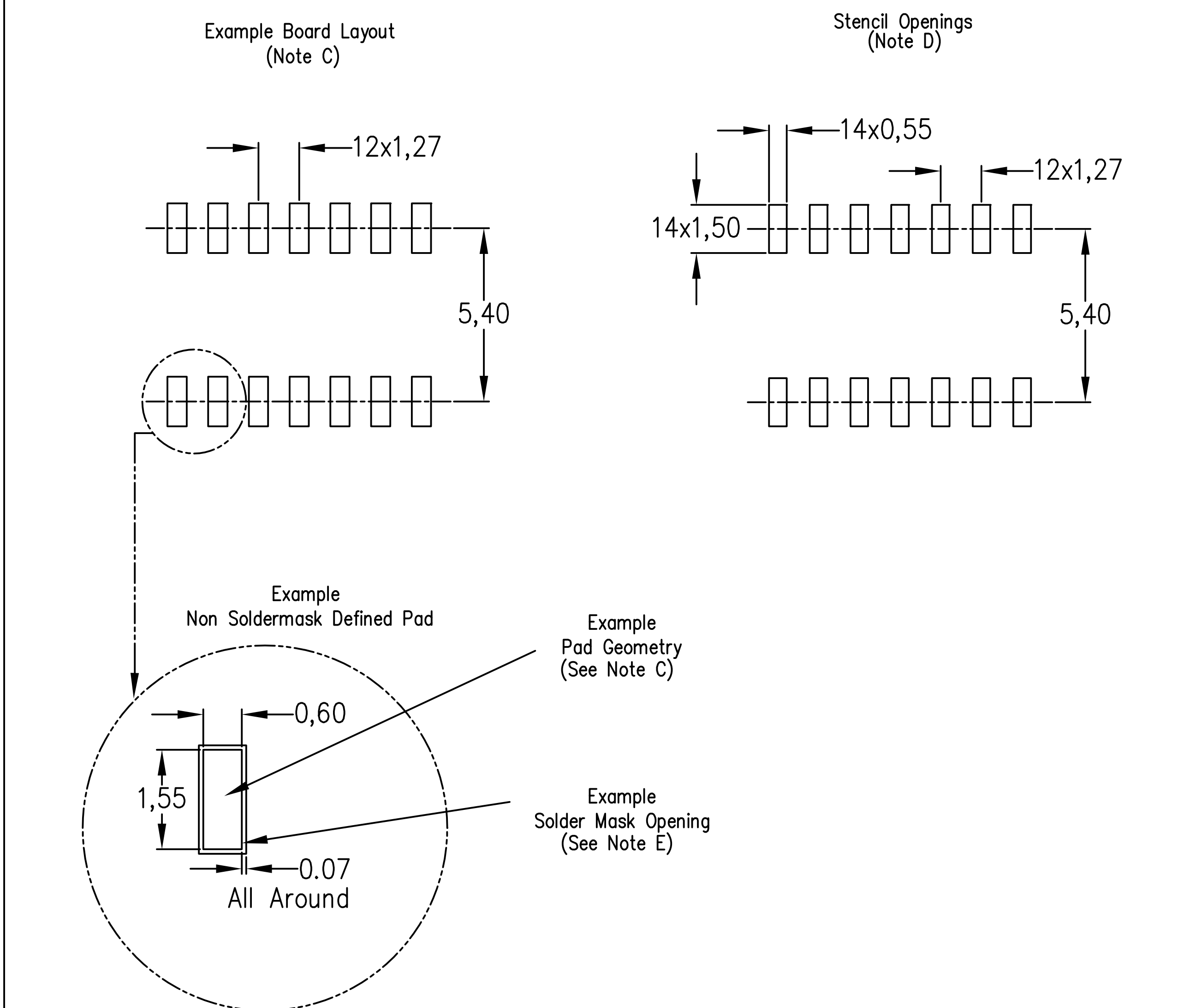
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9002QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9002QDRQ1	SOIC	D	8	2500	853.0	449.0	35.0
TLV9004QDRQ1	SOIC	D	14	2500	853.0	449.0	35.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



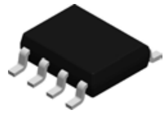
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



4211283-3/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

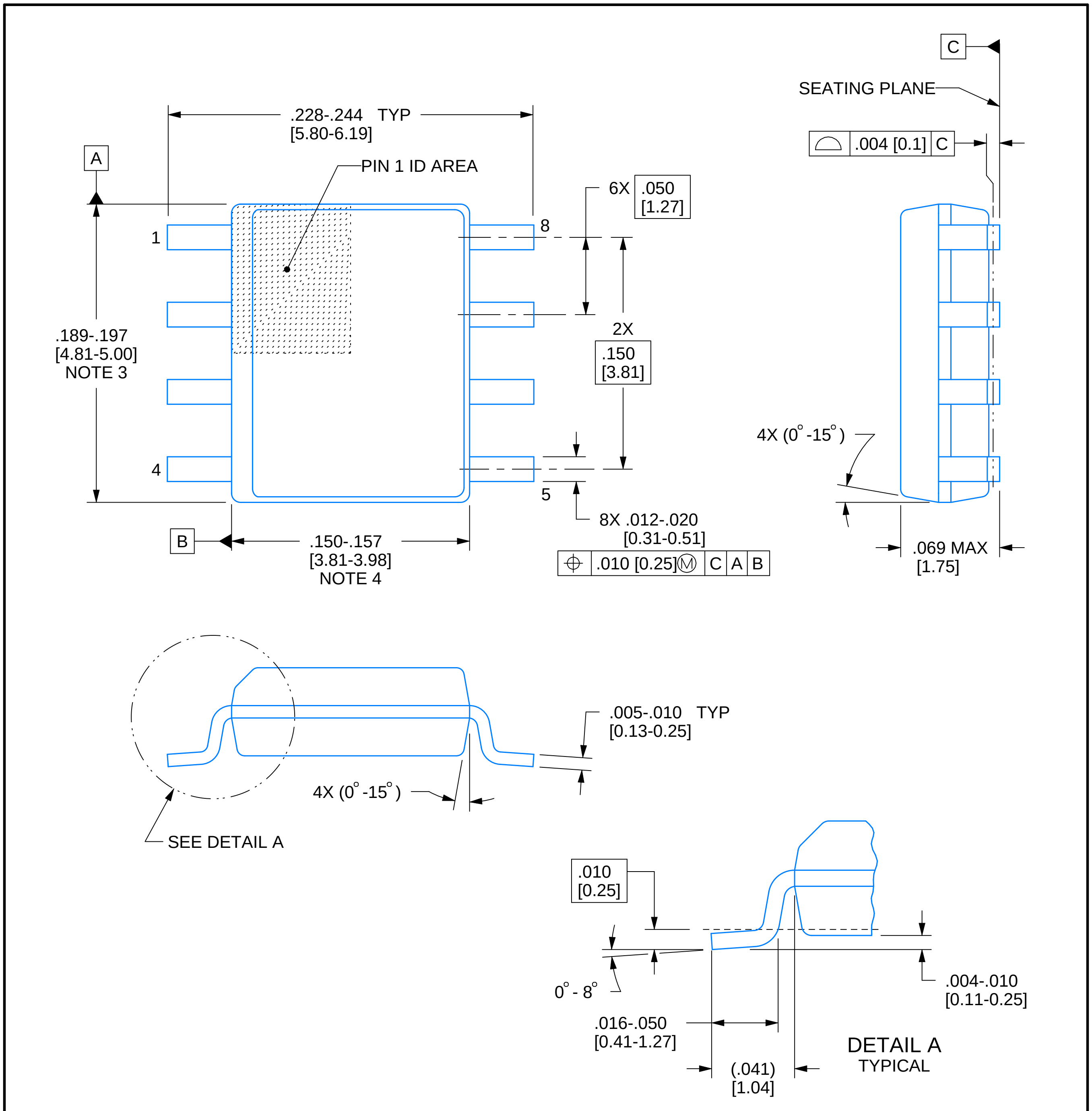


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

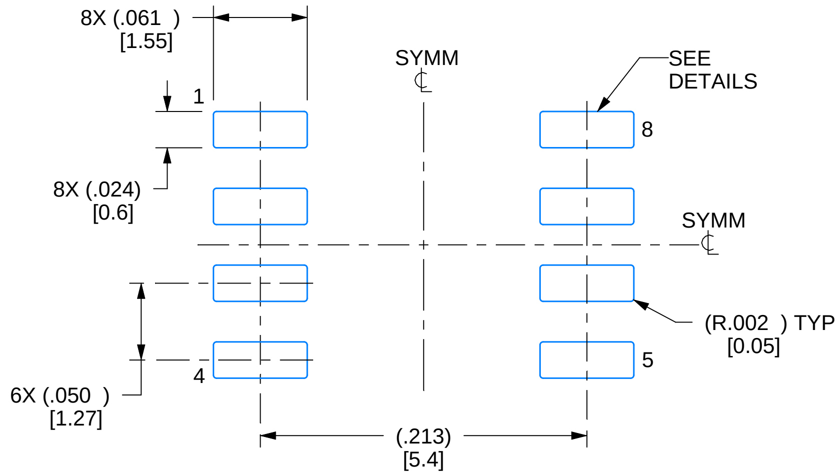
SMALL OUTLINE INTEGRATED CIRCUIT



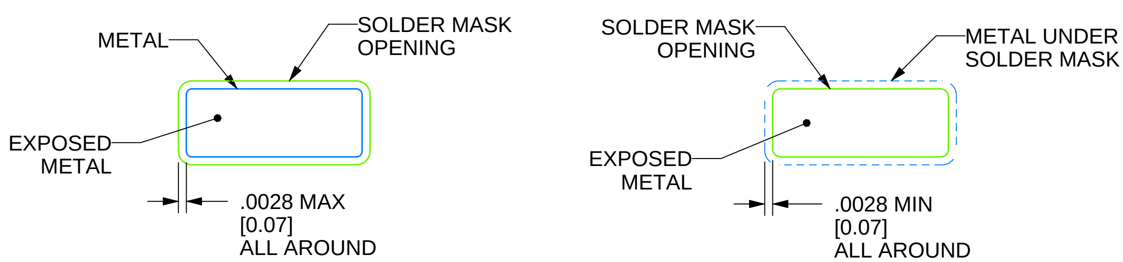
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

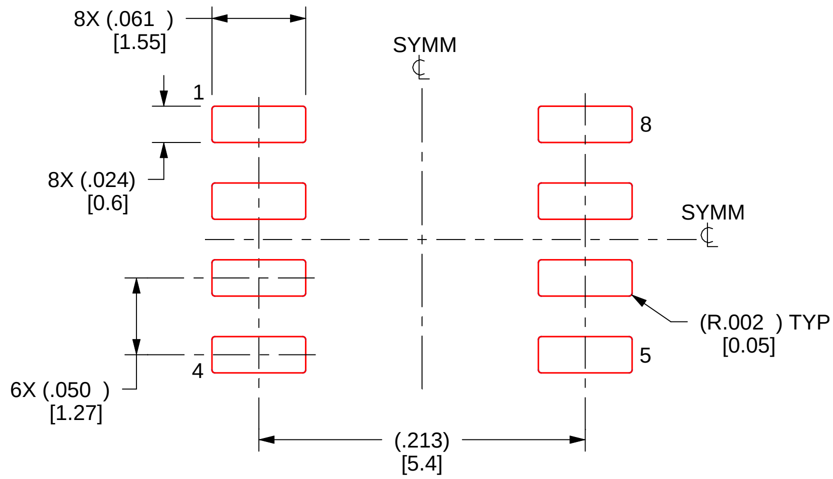
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

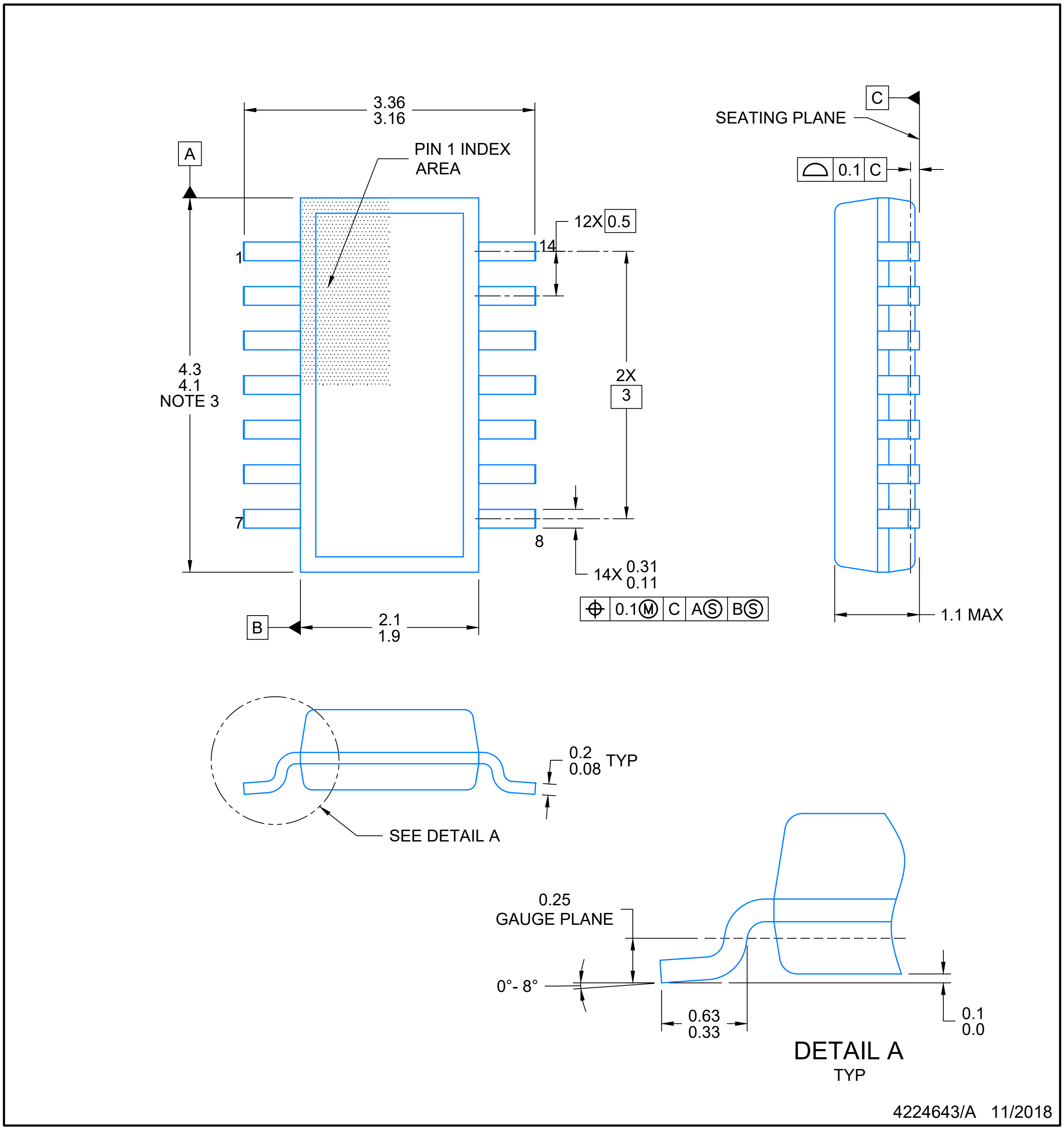


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

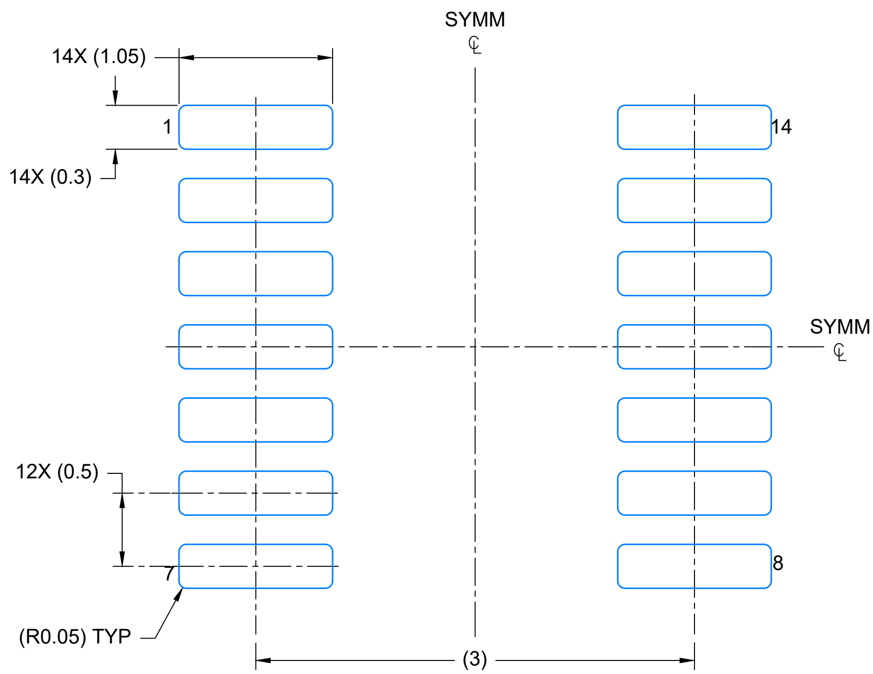
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

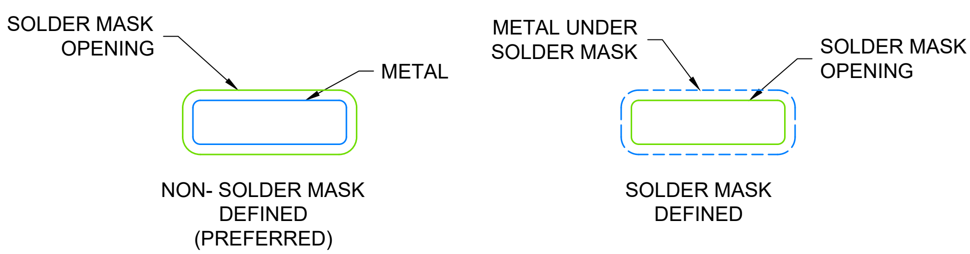


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

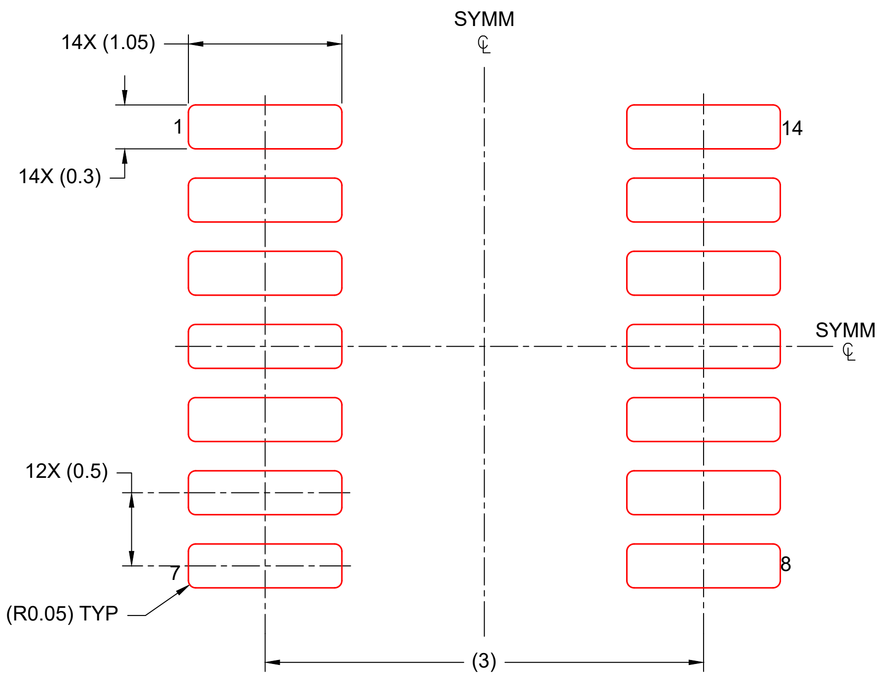


SOLDER MASK DETAILS

4224643/A 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



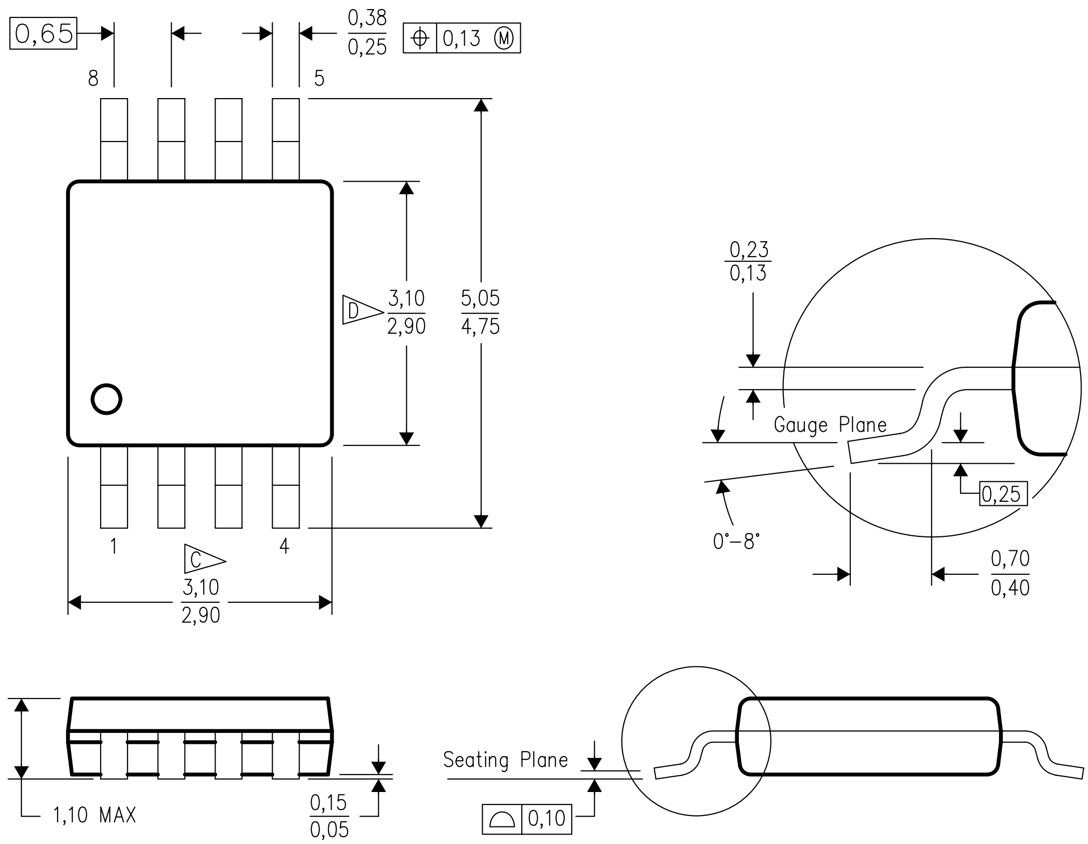
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/A 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

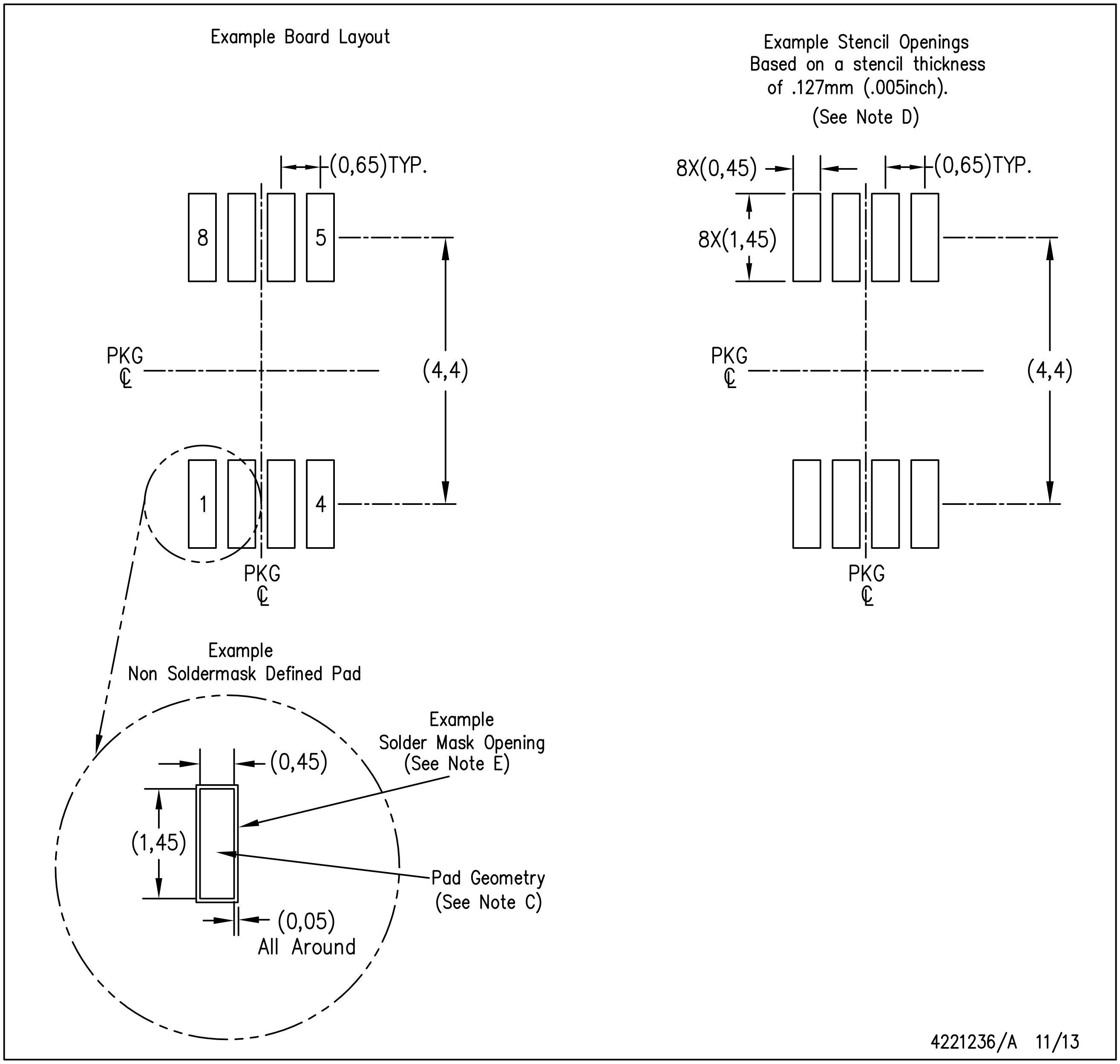
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122