LM53603-Q1 (3A)、LM53602-Q1 (2A) 面向汽车类应用的 3.5V 至 36V 宽 V_{IN} 同步 2.1MHz 降压转换器

1 特性

- 3A 或 2A 最大负载电流
- 输入电压范围：3.5V 至 36V，瞬态电压可达 42V
- 输出电压选项：5V 或 3.3V (ADJ)
- 2.1MHz 固定开关频率
- ±2% 输出电压容差
- 结温范围：-40°C 至 150°C
- 1.7μA 关断电流（典型值）
- 无负载时的输入电源电流为 24μA（典型值）
- 5V 或 3.3V 输出无需外部反馈分压器
- 具有滤波和延迟功能的复位输出
- 可提高效率的自动轻负载模式
- 用户可选的强制脉宽调制模式 (FPWM)
- 内置环路补偿、软启动、电流限制、热关断、欠压锁定 (UVLO) 以及外部频率同步功能
- 耐热增强型 16 引脚封装：
  5mm x 4.4mm x 1mm
- LM53603-Q1 和 LM53602-Q1 均为符合 AEC-Q1 标准的汽车级产品

2 应用

- 导航/全球定位系统 (GPS)
- 仪表板
- 高级驾驶员辅助系统 (ADAS)、信息娱乐、平视显示器 (HUD)

3 说明

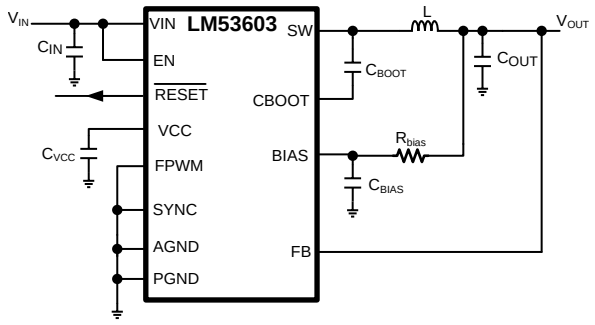
LM53603-Q1、LM53602-Q1 降压稳压器专为汽车类应用而设计，可通过最高 36V 的输入电压提供 5V/3A 或 3.3V/2A（通过 ADJ 选项选择）输出。当输入电压高达 20V 时，该器件可利用高级高速电路得以稳压，同时以 2.1MHz 的开关频率提供 5V 输出。 该器件采用创新型架构，在输入电压仅为 3.5V 时也可提供 3.3V 稳压输出。该产品针对汽车客户进行了全方位优化。器件的输入电压最高可达 36V，容许的最高瞬态电压达 42V，这简化了输入浪涌保护设计。 开漏复位输出具有滤波和延迟功能，可提供正确的系统状态指示。凭借这一特性，器件无需使用附加监控组件，这节省了成本和电路板空间。 该器件可在 PWM 和脉频调制 (PFM) 两种模式之间无缝切换，并且无负载条件下的工作电流仅为 24μA，这确保了其在所有负载条件下均可展现高效率和出色的瞬态响应。

器件信息(1)

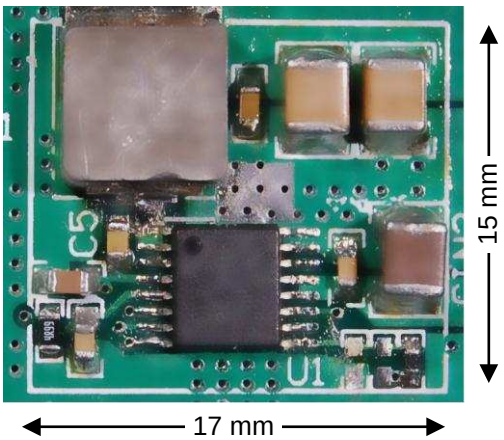
器件型号	封装	封装尺寸（标称值）
LM53603-Q1 LM53602-Q1	HTSSOP (16)	5.00mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



汽车电源（5V/3A 输出）



目录

4 修订历史记录

Changes from Original (June 2015) to Revision A **Page**

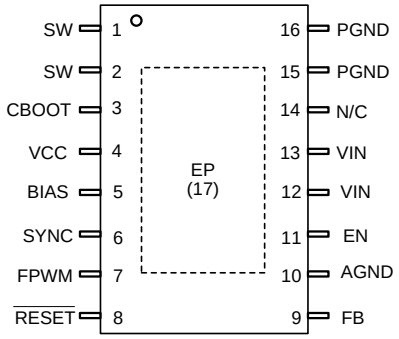
- 已更改 产品预览至完整数据表 ... 1

5 Device Comparison Table

PART NUMBER	PACKAGE	MAXIMUM OUTPUT CURRENT
LM53603-Q1	HTSSOP (16)	3 A
LM53602-Q1	HTSSOP (16)	2 A

6 Pin Configuration and Functions

PWP Package
16-Lead HTSSOP
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
SW	1,2	P	Regulator switch node. Connect to power inductor. Connect pins 1 and 2 directly together at the PCB.
CBOOT	3	P	Bootstrap supply input for gate drivers. Connect a high quality 470 nF capacitor from this pin to SW.
VCC	4	O	Internal 3.15 V regulator output. Used as supply to internal control circuits. Do not connect to any external loads. Can be used as logic supply for control inputs. Connect a high quality 3.3 µF capacitor from this pin to GND.
BIAS	5	P	Input to internal voltage regulator. Connect to output voltage point. Do not ground. Connect a high quality 0.1 µF capacitor from this pin to GND.
SYNC	6	I	Synchronization input to regulator. Used to synchronize the regulator switching frequency to the system clock. When not used connect to GND; do not float.
FPWM	7	I	Mode control input to regulator. High = forced PWM (FPWM). Low = auto mode; automatic transition between PFM and PWM. Do not float.
$\overline{\text{RESET}}$	8	O	Open drain reset output. Connect to suitable voltage supply through a current limiting resistor. High = power OK. Low = fault. $\overline{\text{RESET}}$ will go low when EN = low.
FB	9	I	Feedback input to regulator. Connect to output voltage sense point for fixed 5 V and 3.3 V output. Connect to feedback divider tap point for ADJ option. Do not float or ground.
AGND	10	G	Analog ground for regulator and system. All electrical parameters are measured with respect to this pin. Connect to EP and PGND on PCB.
EN	11	I	Enable input to the regulator. High = ON. Low = OFF. Can be connected directly to VIN. Do not float.
VIN	12, 13	P	Input supply to the regulator. Connect a high quality bypass capacitor(s) from this pin to PGND. Connect pins 12 and 13 directly together at the PCB.
N/C	14	-	This pin has no connection to the device.
PGND	15, 16	G	Power ground to internal low side MOSFET. Connect to AGND and system ground. Connect pins 15 and 16 directly together at the PCB.
EP	17	G	Exposed die attach paddle. Connect to ground plane for adequate heat sinking and noise reduction.

(1) O = Output, I = Input, G = Ground, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

PARAMETER	MIN	MAX	UNIT
VIN to AGND, PGND(2)	–0.3	40	V
SW to AGND, PGND(3)	–0.3	V_{IN} + 0.3	V
CBOOT to SW	–0.3	3.6	V
EN to AGND, PGND(2)	–0.3	40	V
BIAS to AGND, PGND	–0.3	16	V
FB to AGND, PGND : fixed 5 V and 3.3 V	–0.3	16	V
FB to AGND, PGND : ADJ	–0.3	5.5	V
$\overline{\text{RESET}}$ to AGND, PGND	–0.3	8	V
SYNC, FPWM, to AGND, PGND	–0.3	5.5	V
VCC to AGND, PGND	–0.3	4.2	V
$\overline{\text{RESET}}$ Pin Current(4)	–0.1	1.2	mA
AGND to PGND(5)	–0.3	0.3	V
Storage temperature, T_{stg}	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Values given are D.C.
(2) A maximum of 42 V can be sustained at this pin for a duration of ≤ 500 ms at a duty cycle of ≤ 0.01%.
(3) Transients on this pin, not exceeding –3 V or +40 V, can be tolerated for a duration of ≤ 100 ns. For transients between 40 V and 42 V, see note (2).
(4) Positive current flows into this pin.
(5) A transient voltage of ±2 V can be sustained for ≤1 µs.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	VIN, SW, CBOOT	±1500	V
		EN, BIAS, $\overline{\text{RESET}}$, FB, SYNC, PWM, VCC	±2500	
	Charged-device model (CDM), per AEC Q100-011	CBOOT, VCC, BIAS, SYNC, FPWM, EN, VIN	±750	
		SW, $\overline{\text{RESET}}$, FB, PGND	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Input voltage(2)	3.9		36	V
Output voltage : Fixed 5 V(3)	0	5		V
Output voltage : Fixed 3.3 V(3)	0	3.3		V
Output voltage adjustment range: ADJ(3)(4)	3.3		6	V
Output current for LM53603-Q1	0		3	A
Output current for LM53602-Q1	0		2	A
$\overline{\text{RESET}}$ pin current	0		1	mA
Operating junction temperature(5)	–40		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See *System Characteristics* for details of input voltage range.
(3) Under no conditions should the output voltage be allowed to fall below zero volts.
(4) The maximum recommended output voltage is 6 V. An extended output voltage range to 10 V is possible with changes to the typical application schematic. Also, some system specifications will not be achieved for output voltages greater than 6 V. Consult the factory for further information.
(5) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.4 Thermal Information

THERMAL METRIC(1)		LM53603-Q1, LM63602-Q1	UNIT
		PWP (HTSSOP)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information please see the *Maximum Ambient Temperature* section. For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953, and the *Using New Thermal Metrics* applications report, SBVA025.

7.5 Electrical Characteristics

Limits apply to the recommended operating junction temperature range of –40°C to 150°C, unless otherwise noted. Minimum and maximum limits are verified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
V_{FB}	Initial reference voltage accuracy for 5 V and 3.3 V options	V_{IN} = 3.8 V to 36 V, FPWM, T_J = 25°C	–1%		1%	
		V_{IN} = 3.8 V to 36 V, FPWM	–1.25%		1.25%	
V_{REF}	Reference voltage for ADJ option	V_{IN} = 3.8 V to 36 V, FPWM, T_J = 25°C	0.993	1	1.007	V
		V_{IN} = 3.8 V to 36 V, FPWM, T_J = -40°C to 125°C	0.99	1	1.01	
$V_{IN\text{-}operate}$	Minimum input voltage to operate(2)	Rising	3.2		3.95	V
		Falling	2.9		3.55	
		Hysteresis, below	0.34			
I_Q	Operating quiescent current; measured at VIN pin.(3)(4)	V_{BIAS} = 5 V, T_J = -40°C to 125°C		8	13	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin.	EN ≤ 0.4 V, T_J = 25°C		1.7		µA
		EN ≤ 0.4 V, T_J = 85°C			2.8	
		EN ≤ 0.4 V, T_J = 125°C			3.5	
I_B	Current into the BIAS pin(4)	V_{BIAS} = 5 V, FPWM = 3.3 V		47	78	µA
I_{EN}	Current into EN pin	V_{IN} = V_{EN} = 13.5 V		2.3		µA
R_{FB}	Resistance from FB to AGND	5 V option		1.5		MΩ
	Resistance from FB to AGND	3.3 V option		1		MΩ
I_{FB}	Bias current into FB pin	ADJ option		10		nA
V_{RESET}	$\overline{\text{RESET}}$ upper threshold voltage	Rising, % of nominal V_{out}	105%	107%	110%	
	$\overline{\text{RESET}}$ lower threshold voltage	Falling, % of nominal V_{out}	92%	94%	96.5%	
	$\overline{\text{RESET}}$ lower threshold voltage with respect to output voltage	Falling, % actual V_{out}	–4.3%			
$V_{RESET\text{-}Hyst}$	$\overline{\text{RESET}}$ hysteresis as a percent of output voltage set point			1.5%		
V_{MIN}	Minimum input voltage for proper $\overline{\text{RESET}}$ function	50 µA pull-up to $\overline{\text{RESET}}$ pin, V_{EN} = 0 V, T_J = 25°C			1.5	V
V_{OL}	Low level $\overline{\text{RESET}}$ pin output voltage	50 µA pull-up to $\overline{\text{RESET}}$ pin, V_{in} = 1.5 V, EN = 0 V			0.4	V
		0.5 mA pull-up to $\overline{\text{RESET}}$ pin, V_{in} = 13.5 V, EN = 0 V			0.4	
		1 mA pull-up to $\overline{\text{RESET}}$ pin, V_{in} = 13.5 V, EN = 3.3 V			0.4	
V_{EN}	Enable input threshold voltage	Rising	1.7		2	V
		Hysteresis, below	0.45		0.55	
$V_{EN\text{-}off}$	Enable input threshold for full shutdown(5)	EN input voltage required for complete shutdown of the regulator, falling.	0.8			V
V_{LOGIC}	Logic input levels on FPWM and SYNC pins	V_{IH}	1.5			V
		V_{IL}			0.4	
I_{HS}	High side switch current limit	LM53603-Q1	4.5		6.2	A
		LM53602-Q1	2.4		4.4	

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range are verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) This is the input voltage at which the device will start to operate ("rising"). The device will shutdown when the input voltage goes below this value minus the hysteresis.
(3) This is the current used by the device, open loop. It does not represent the total input current of the system when in regulation. See "I_{supply}" in *System Characteristics*
(4) The FB pin is set to 5.5 V for this test.
(5) Below this voltage on the EN input, the device will shut down completely.

Electrical Characteristics (continued)

Limits apply to the recommended operating junction temperature range of –40°C to 150°C, unless otherwise noted. Minimum and maximum limits are verified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
I_{LS}	Low side switch current limit(6)	LM53603-Q1	3	3.6	4.3	A
		LM53602-Q1	2	2.4	2.8	
I_{ZC}	Zero-cross current limit	FPWM = 0 V		-0.02		A
I_{NEG}	Negative current limit	FPWM = 3.3 V		-1.5		A
R_{dson}	Power switch on-resistance	High side MOSFET resistance		135	290	mΩ
		Low side MOSFET resistance		60	125	
F_{SW}	Switching frequency	V_{IN} = 3.8 V to 18 V	1.85	2.1	2.35	MHz
		V_{IN} = 36 V		1.2		
F_{SYNC}	Synchronizing frequency range		1.9	2.1	2.3	MHz
V_{CC}	Internal V_{CC} voltage	V_{BIAS} = 3.3 V		3.15		V
T_{SD}	Thermal shutdown thresholds	Rising	162		178	°C
		Hysteresis, below	18			

(6) See the *Current Limit* section for an explanation of valley current limit.

7.6 System Characteristics

The following specifications apply only to the typical application circuit, shown in Figure 15 with nominal component values. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. The parameters in this table are not guaranteed.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN-MIN}	Minimum input voltage for V_{out} to stay within ±2% of regulation. (1)	V_{OUT} = 3.3 V, I_{OUT} = 3 A		3.9		V
		V_{OUT} = 3.3 V, I_{OUT} = 1 A		3.55		
Regulation	Line Regulation	**V_{OUT} = 5 V**, V_{IN} = 8 V to 36 V, I_{OUT} = 3 A		7		mV
		V_{OUT} = 3.3 V, V_{IN} = 6 V to 36 V, I_{OUT} = 3 A		5		
	Load Regulation : Auto Mode	**V_{OUT} = 5 V**, V_{IN} = 12 V, I_{OUT} = 10 µA to 3 A		77		mV
		V_{OUT} = 3.3 V, V_{IN} = 12 V, I_{OUT} = 10 µA to 3 A		53		
	Load Regulation : FPWM Mode	**V_{OUT} = 5 V**, V_{IN} = 12 V, I_{OUT} = 10 µA to 3 A		12		mV
		V_{OUT} = 3.3 V, V_{IN} = 12 V, I_{OUT} = 10 µA to 3 A		9		
I_{SUPPLY}	Input supply current when in regulation. (2)	V_{IN} = 13.5 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A		24		µA
		V_{IN} = 13.5 V, V_{OUT} = 5 V, I_{OUT} = 0 A		34		
V_{DROP}	Dropout voltage (V_{IN} – V_{OUT})	**5 V Option:** V_{OUT} = 4.95 V, I_{OUT} = 3 A, F_{SW} < 1.85 MHz		0.7		V
		5 V Option: V_{OUT} = 5 V, I_{OUT} = 3 A, F_{SW} = 1.85 MHz		1.8		
		3.3 V Option: V_{OUT} = 3.27 V, I_{OUT} = 3 A, F_{SW} < 1.85 MHz		0.65		
		3.3 V Option: V_{OUT} = 3.3 V, I_{OUT} = 3 A, F_{SW} = 1.85 MHz		1.8		

(1) This parameter is valid once the input voltage has risen above $V_{IN-operate}$ and the device has started up.
(2) Includes current into the EN pin. See *Input Supply Current* section.

7.7 Timing Characteristics

		MIN	NOM	MAX	UNIT
T_{ON}	Minimum switch on-time, V_{IN} = 20 V		50	80	ns
T_{OFF}	Minimum switch off-time, V_{IN} = 3.8 V		125	200	ns
$T_{RESET\text{-}act}$	Delay time to $\overline{RESET}$ high signal	2	3	4	ms
$T_{RESET\text{-}filter}$	Glitch filter time for $\overline{RESET}$ function	12	25	45	µs
T_{SS}	Soft-start time	1	2	3	ms
T_{EN}	Turn-on delay, C_{VCC} = 1 µF(1)		0.7	0.8	ms
T_W	Short circuit wait time. ("Hiccup" time)		5.5		ms

(1) This is the time from the rising edge of EN to the time that the soft-start ramp begins.

7.8 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, T_A = 25°C. Specified temperatures are ambient.

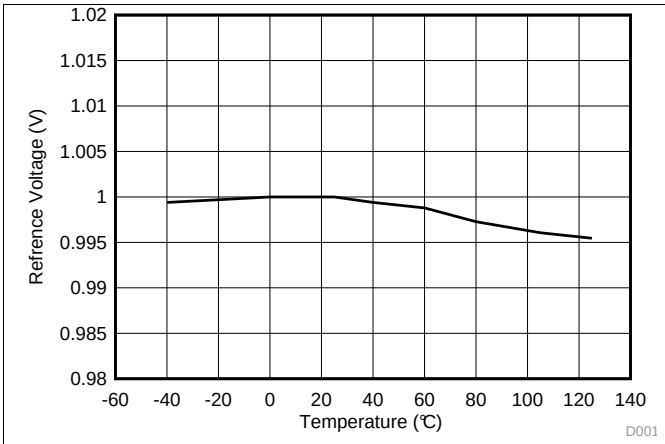


Figure 1. Reference Voltage for ADJ Device

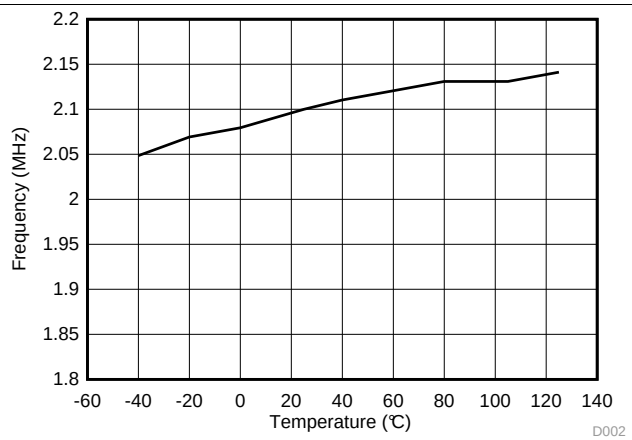


Figure 2. Switching Frequency

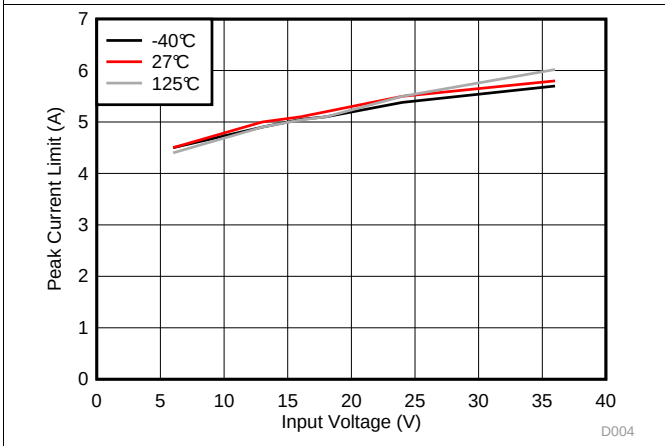


Figure 3. High Side Peak Current Limit for LM53603-Q1

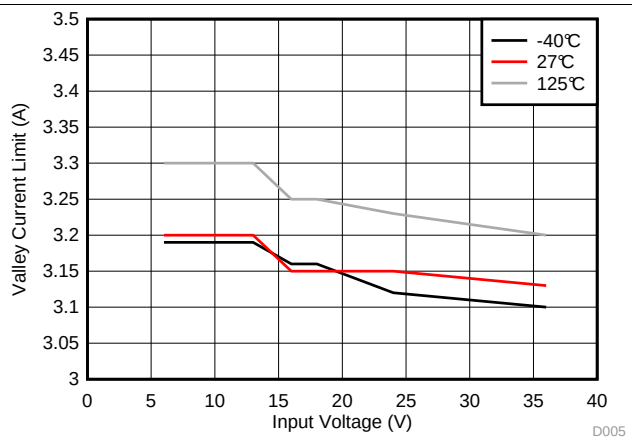


Figure 4. Low Side Valley Current Limit for LM53603-Q1

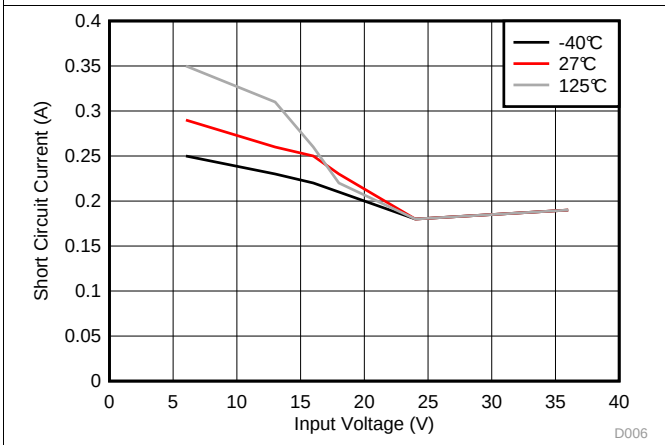


Figure 5. Short Circuit Output Current for LM53603-Q1

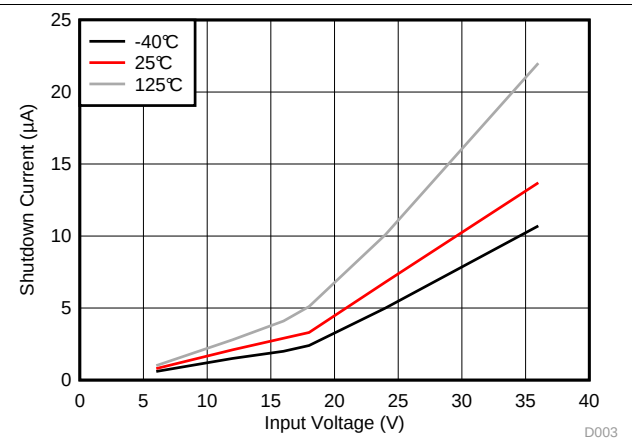


Figure 6. Shutdown Current

8 Detailed Description

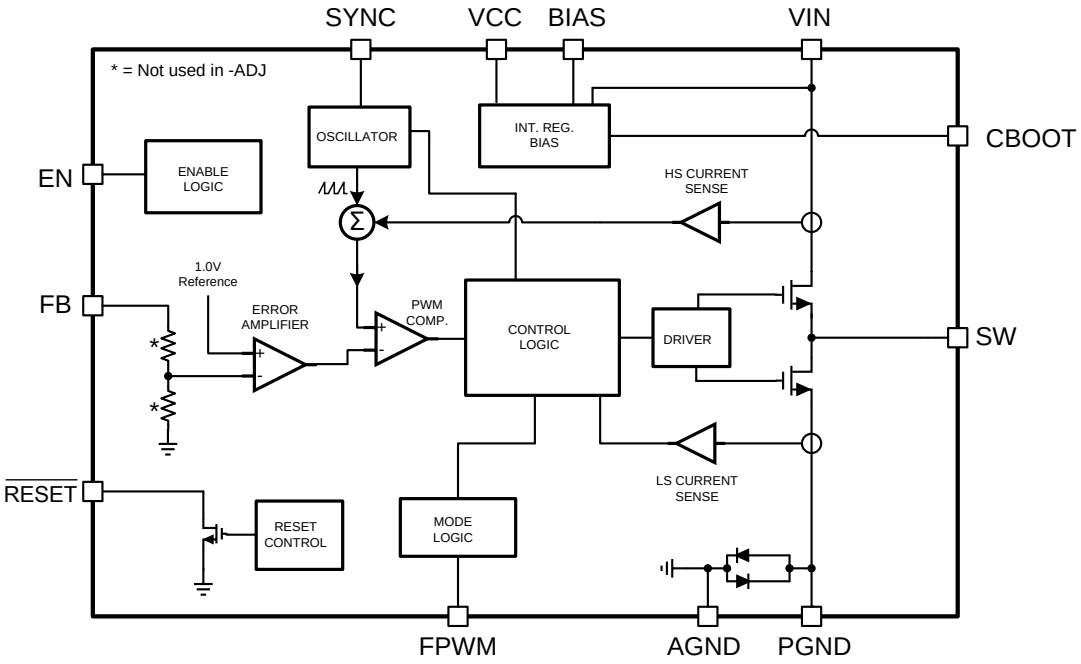
8.1 Overview

The LM5360x family of devices are synchronous current mode buck regulators designed specifically for the automotive market. The regulator automatically switches between PWM and PFM depending on load. At heavy loads the device operates in PWM at a switching frequency of 2.1 MHz. The regulator's oscillator can also be synchronized to an external system clock. At input voltages above about 20 V, the switching frequency reduces to maintain regulation during conditions of abnormally high battery voltage. At light loads the mode changes to PFM, with diode emulation allowing DCM. This reduces input supply current and keeps the efficiency high. The user can also choose to lock the mode in PWM (FPWM) so that the switching frequency remains constant regardless of load.

A $\overline{\text{RESET}}$ flag is provided to indicate when the output voltage is near its regulation point. This feature includes filtering and a delay before asserting. This helps to prevent false flag operation during output voltage transients.

Please note that, throughout this data sheet, references to the LM53603-Q1 apply equally to the LM53602-Q1. The difference between the two devices is the maximum output current and specified MOSFET current limits.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 $\overline{\text{RESET}}$ Flag Output

The $\overline{\text{RESET}}$ function, built-in to the LM53603-Q1, has special features not found in the ordinary power-good function. A glitch filter prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Furthermore, there is a delay between the point at which the output voltage is within specified limits and the flag asserts "power-good". Since the $\overline{\text{RESET}}$ comparator and the regulation loop share the same reference, the thresholds will track with the output voltage. This allows the LM53603-Q1 to be specified with a 96.5% maximum threshold, while at the same time specifying a 95% threshold with respect to the actual output voltage for that device. This allows tighter tolerance than is possible with an external supervisor device. The net result is a more accurate power-good function while expanding the system allowance for transients, etc. $\overline{\text{RESET}}$ operation can best be understood by reference to Figure 7 and Figure 8. The values for the various filter and delay times can be found in the *Timing Characteristics* table. Output voltage excursions lasting less than $T_{\text{RESET-filter}}$, will not trip $\overline{\text{RESET}}$. Once the output voltage is within the prescribed limits, a delay of $T_{\text{RESET-act}}$ is imposed before $\overline{\text{RESET}}$ goes high.

Feature Description (continued)

This output consists of an open drain NMOS; requiring an external pull-up resistor to a suitable logic supply. It can also be pulled-up to either VCC or V_{OUT}, through an appropriate resistor, as desired. If this function is not needed, the pin should be left floating or grounded. When EN is pulled low, the flag output will also be forced low. With EN low, $\overline{\text{RESET}}$ will remain valid as long as the input voltage is ≥ 1.5 V. The maximum current into this pin should be limited to 1 mA, while the maximum voltage should be less than 8 V.

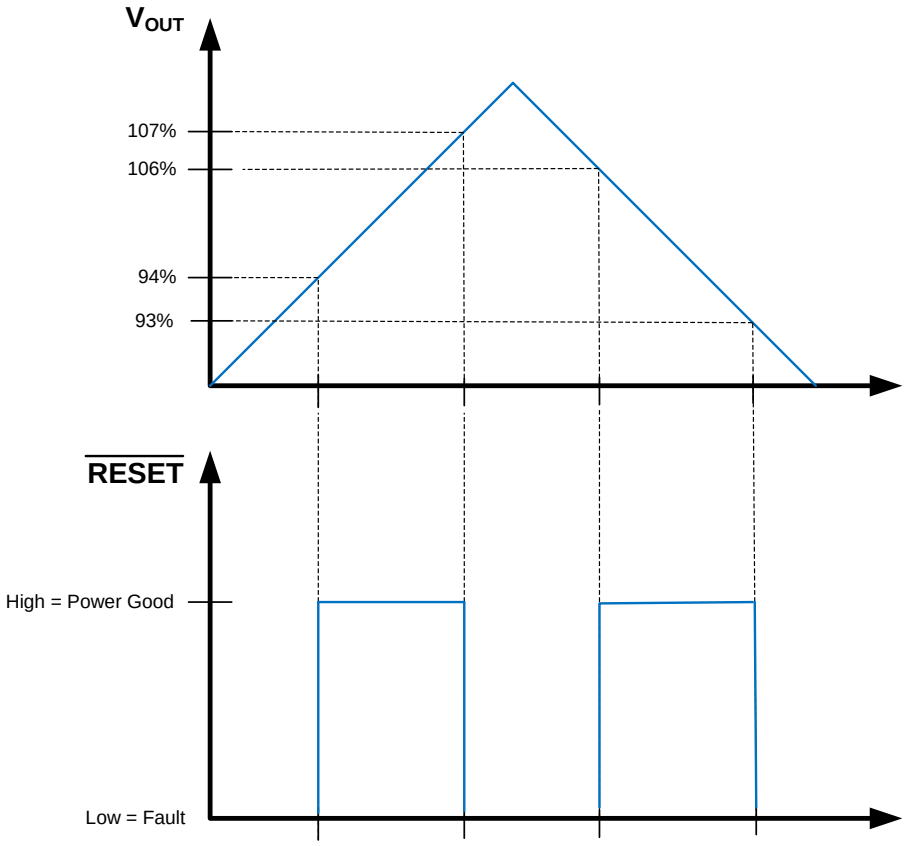


Figure 7. Static $\overline{\text{RESET}}$ Operation

Feature Description (continued)

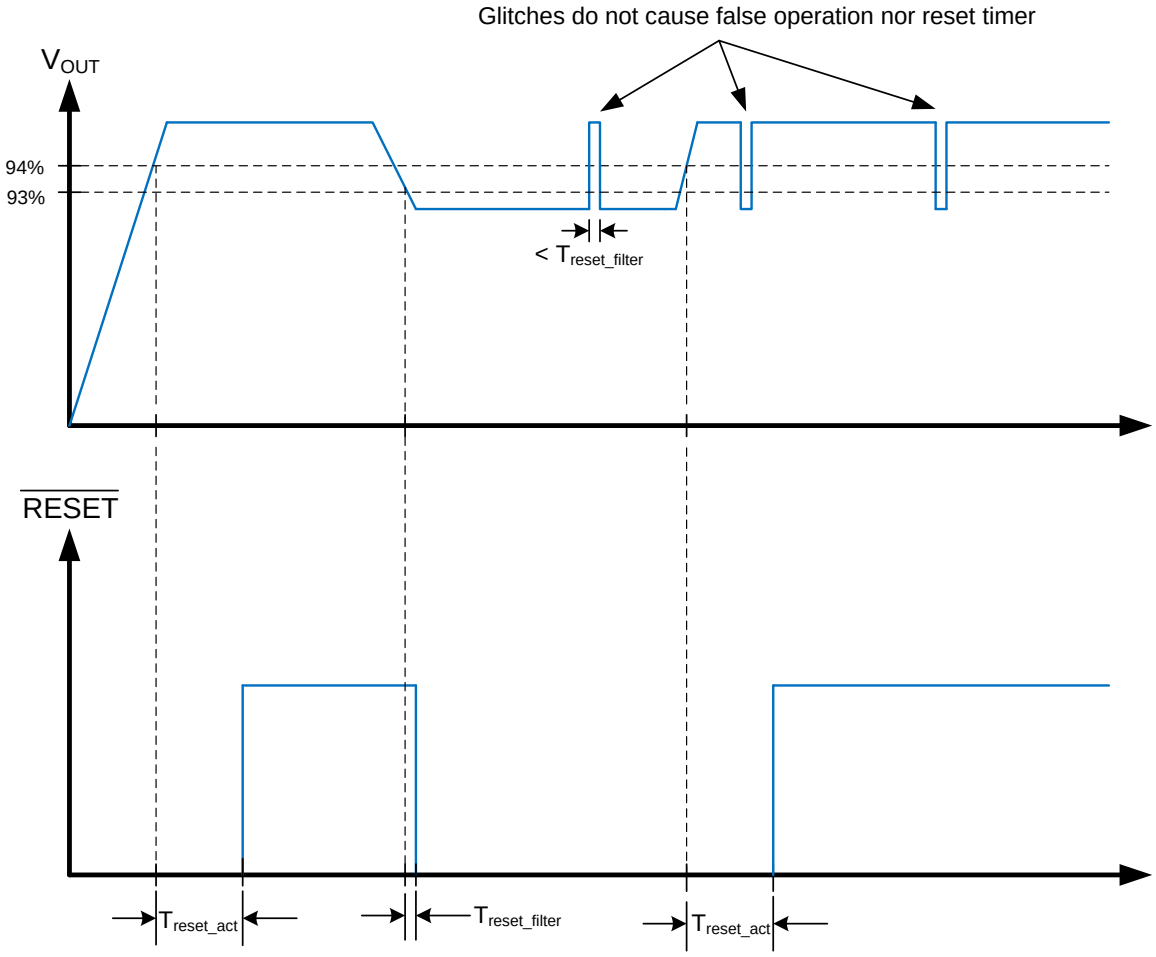


Figure 8. $\overline{\text{RESET}}$ Timing Behavior

8.3.2 Enable and Start-up

Start-up and shutdown of the LM53603-Q1 are controlled by the EN input. Applying a voltage of ≥ 2V will activate the device, while a voltage of ≤ 0.8V is required to shut it down. The EN input may also be connected directly to the input voltage supply, if this feature is not needed. This input must not be left floating. The LM53603-Q1 utilizes a reference based soft-start, that prevents output voltage overshoots and large inrush currents as the regulator is starting-up. A typical start-up waveform is shown in Figure 9 along with typical timings.

Feature Description (continued)

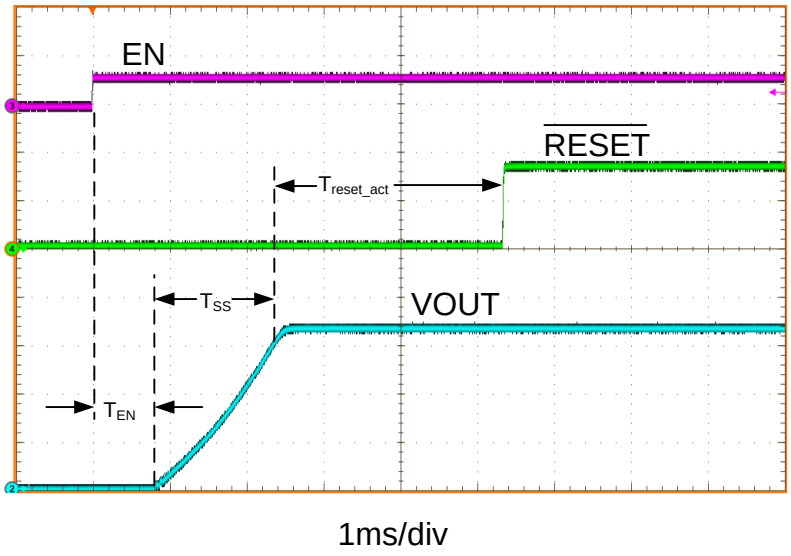


Figure 9. Typical Start-up Waveform

8.3.3 Current Limit

The LM53603-Q1 incorporates valley current limit for normal overloads and for short circuit protection. In addition, the low side switch is also protected from excessive negative current when the device is in FPWM mode. Finally, a high side peak current limit is employed for protection of the top NMOS FET.

During overloads the low side current limit, I_{LS} (see *Electrical Characteristics*), determines the maximum load current that the LM53603-Q1 can supply. When the low side switch turns on, the inductor current begins to ramp down. If the current does not fall below I_{LS} , before the next turn-on cycle, then that cycle is skipped and the low side FET is left on until the current falls below I_{LS}. This is somewhat different than the more typical peak current limit, and results in Equation 1 for the maximum load current.

$$I_{OUT}|_{max} = I_{LS} + \frac{(V_{IN} - V_{OUT})}{2 \cdot F_S \cdot L} \cdot \frac{V_{OUT}}{V_{IN}} \quad (1)$$

If the above situation persists for more than about 64 clock cycles, the device turns off both high and low side switches for approximately 5.5 ms (see T_W in *Timing Characteristics*). If the overload is still present after the "hiccup" time, another 64 cycles is counted and the process is repeated. If the current limit is not tripped for two consecutive clock cycles, the counter is reset. Figure 10 shows the inductor current with a hard short on the output. The "hiccup" time allows the inductor current to fall to zero, resetting the inductor volt-second balance. This is the method used for short circuit protection and keeps the power dissipation low during a fault. Of course the output current is greatly reduced in this condition (see *Typical Characteristics*). A typical short circuit transient and recovery is shown in Figure 11.

Feature Description (continued)

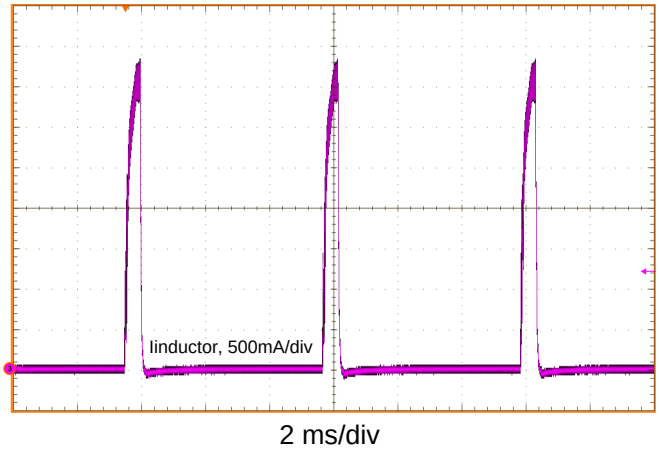


Figure 10. Inductor Current Bursts in Short Circuit

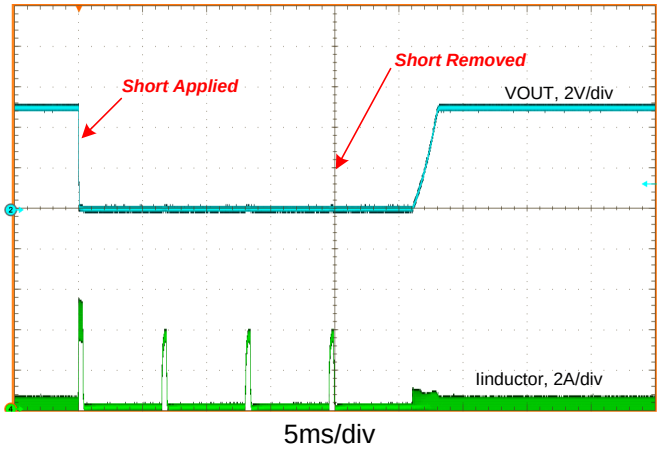


Figure 11. Short Circuit Transient and Recovery

The high side current limit trips when the peak inductor current reaches I_{HS} (see *Electrical Characteristics*). This is a cycle-by-cycle current limit and does not produce any frequency or current fold-back. It is meant to protect the high side MOSFET from excessive current. Under some conditions, such as high input voltage, this current limit may trip before the low side protection. The peak value of this current limit will vary with duty-cycle.

In FPWM mode, the inductor current is allowed to go negative. Should this current exceed I_{NEG}, the low side switch is turned off until the next clock cycle. This is used to protect the low side switch from excessive negative current. When the device is in AUTO mode, the negative current limit is increased to about 0 A; I_{ZC}. This allows the device to operate in DCM.

8.3.4 Synchronizing Input

The internal clock of the LM53603-Q1 can be synchronized to a system clock through the SYNC input. This input recognizes a valid high level as that ≥ 1.5 V, and a valid low as that ≤ 0.4 V. The frequency synchronization signal should be in the range of 1.9 MHz to 2.3 MHz with a duty cycle of from 10% to 90%. The internal clock is synced to the rising edge of the external clock. If this input is not used, it should be grounded. The maximum voltage on this input is 5.5 V; and should not be allowed to float. See the *Device Functional Modes* section to determine which modes are valid for synchronizing the clock.

8.3.5 Input Supply Current

The LM53603-Q1 is designed to have very low input supply current when regulating light loads. One way this is achieved is by powering much of the internal circuitry from the output. The BIAS pin is the input to the LDO that powers the majority of the control circuits. By connecting the BIAS input to the output of the regulator, this current acts as a small load on the output. This current is reduced by the ratio of V_{OUT}/V_{IN}, just like any other load. Another advantage of the LM53603-Q1 is that the feed-back divider is integrated into the device. This allows the use of much larger resistors than can be used externally; >> 100 kΩ. This results in much lower divider current than is possible with external resistors. Equation 2 can be used to estimate the total input supply current when the device is regulating with no external loads. The terms of the equation are as follows:

- I_{IN}: Input supply current with no load.
- I_Q: Device quiescent current, see *Electrical Characteristics*.
- I_{EN}: Current into EN pin; see *Electrical Characteristics*.
- I_B: Current into BIAS pin; see *Electrical Characteristics*.
- K: ≈ 0.9

$$I_{IN} = I_Q + I_{EN} + \frac{V_{OUT}}{V_{IN} \cdot K} \cdot \left(I_B + \frac{V_{OUT}}{R_{FB}} \right) \quad (2)$$

Feature Description (continued)

Equation 2 can be used as a guide to indicate how the various terms affect the input supply current. The *Application Curves* show measured values for the input supply current for both 3.3 V and 5 V output voltage versions.

8.3.6 UVLO and TSD

The LM53603-Q1 incorporates an input undervoltage lockout (UVLO) function. The device will accept an EN command when the input voltage rises above about 3.64 V and shuts down when the input falls below about 3.3 V. See the *Electrical Characteristics* table under "$V_{IN\text{-}operate}$" for detailed specifications.

Thermal shutdown is provided to protect the device from excessive temperature. When the junction temperature reaches about 162°C, the device will shut down; re-start occurs at a temperature of about 144ºC.

8.4 Device Functional Modes

Please refer to Table 1 and the following paragraphs for a detailed description of the functional modes for the LM53603-Q1. These modes are controlled by the FPWM input as shown in Table 1. This input can be controlled by any compatible logic, and the mode changed while the regulator is operating. If it is desired to lock the mode for a given application, the input can be either connected to ground, a logic supply, or the VCC pin, as desired. The maximum input voltage on this pin is 5.5 V; and it should not be allowed to float.

Table 1. Mode Selection

FPWM INPUT VOLTAGE	OPERATING MODE
> 1.5 V	**Forced PWM**: The regulator operates as a constant frequency, current mode, full-synchronous converter for all loads; without diode emulation.
< 0.4 V	**AUTO**: The regulator will move between PFM and PWM as the load current changes, utilizing diode-emulation-mode to allow DCM (see the *Glossary*).

8.4.1 AUTO Mode

In AUTO mode the device moves between PWM and PFM as the load changes. At light loads the regulator operates in PFM . At higher loads the mode changes to PWM. The load currents for which the devices moves from PWM to PFM can be found in the *Application Curves*.

In PWM , the converter operates as a constant frequency, current mode, full synchronous converter using PWM to regulate the output voltage. While operating in this mode the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple. When in PWM the converter will synchronize to any valid clock signal on the SYNC input (see *Drop-Out* and *Input Voltage Frequency Fold-Back*).

In PFM the high side FET is turned on in a burst of one or more cycles to provide energy to the load. The frequency of these bursts is adjusted to regulate the output, while diode emulation is used to maximize efficiency (see the). This mode provides high light load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads*Glossary*. This trades off very good light load efficiency for larger output voltage ripple and variable switching frequency. Also, a small increase in the output voltage will occur in PFM. The actual switching frequency and output voltage ripple will depend on the input voltage, output voltage, and load. Typical switching waveforms for PFM are shown in Figure 12 . See the *Application Curves* for output voltage variation in AUTO mode. The SYNC input is ignored during PFM operation.

A unique feature of this device, is that a minimum input voltage is required for the regulator to switch from PWM to PFM at light load. This feature is a consequence of the advanced architecture employed to provide high efficiency at light loads. Figure 13 indicates typical values of input voltage required to switch modes at no-load. Also, once the regulator switches to PFM, at light load, it will remain in that mode if the input voltage is reduced.

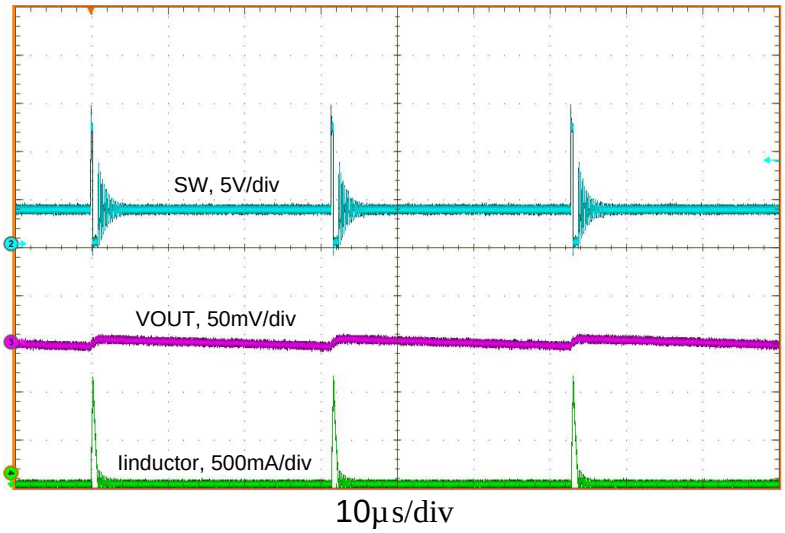


Figure 12. Typical PFM Switching Waveforms

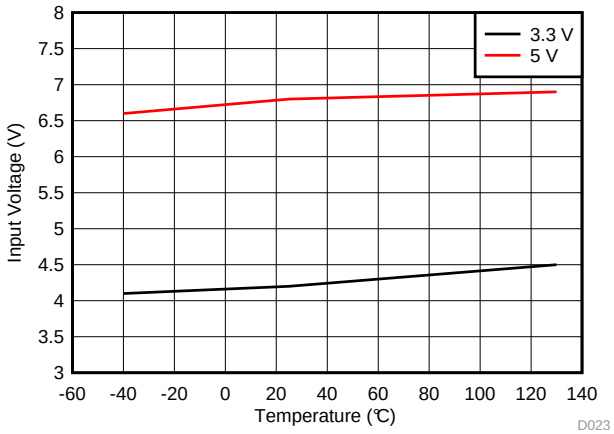


Figure 13. Input Voltage for Mode Change

8.4.2 FPWM Mode

With a logic high on the FPWM input, the device is locked in PWM mode. This operation is maintained, even at no-load, by allowing the inductor current to reverse its normal direction. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency. In this mode, a negative current limit of I_{NEG} is imposed to prevent damage to the regulators low side FET. When in FPWM the converter will synchronize to any valid clock signal on the SYNC input (see *Drop-Out* and *Input Voltage Frequency Fold-Back*).

8.4.3 Drop-Out

One of the parameters that influences the drop-out performance of a buck regulator is the minimum off-time. As the input voltage is reduced, to near the output voltage, the off-time of the high side switch starts to approach the minimum value (see *Timing Characteristics*). Beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the LM53603-Q1 automatically reduces the switching frequency to increase the effective duty cycle. This results in two specifications regarding drop-out

voltage, as shown in the *System Characteristics* table. One specification indicates when the switching frequency drops to 1.85 MHz; avoiding the A.M. radio band. The other specification indicates when the output voltage has fallen to 1% of nominal. See the *Application Curves* for typical values of drop-out. The overall drop-out characteristic for the 5 V option, can be seen in Figure 14. The SYNC input is ignored during frequency fold-back in drop-out.

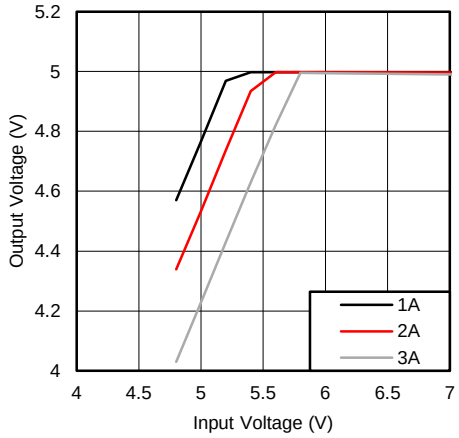


Figure 14. Overall Drop-out Characteristic
V_{OUT} = 5V

8.4.4 Input Voltage Frequency Fold-Back

At higher input voltages the on-time of the high side switch becomes small. When the minimum is reached (see *Timing Characteristics*), the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this behavior, the LM53603-Q1 automatically reduces the switching frequency at input voltages above about 20 V (see *Application Curves*). In this way the device avoids the minimum on-time restriction and maintains regulation at abnormally high battery voltages. The SYNC input is ignored during frequency fold-back at high input voltages.

9 Application and Implementation

9.1 Application Information

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining the suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

The LM53603-Q1 and LM53602-Q1 are step-down DC-DC converters, typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of either 3 A or 2 A. The following design procedure can be used to select components for the LM53603-Q1 or LM53602-Q1. Alternately, the WEBENCH® Design Tool may be used to generate a complete design. This tool utilizes an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various design options.

9.2 Typical Applications

Figure 15 shows the minimum required application circuit for the fixed output voltage versions, while Figure 16 shows the connections for complete processor control of the LM53603-Q1. Please refer to these figures while following the design procedures. Table 2 provides an example of typical design requirements.

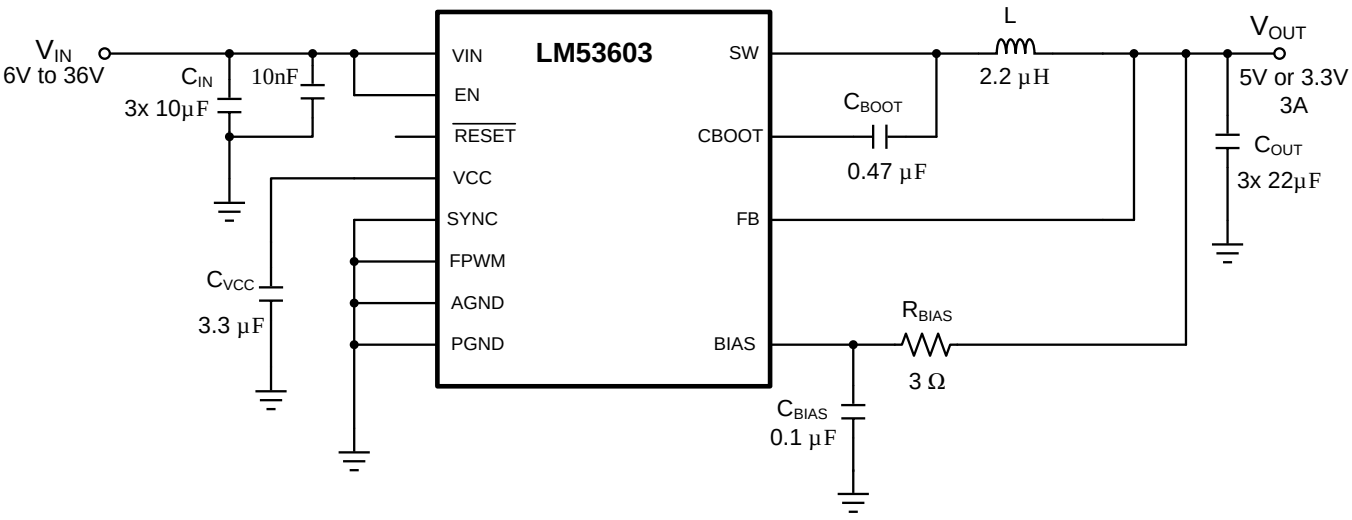


Figure 15. Typical Automotive Power Supply Schematic

Typical Applications (continued)

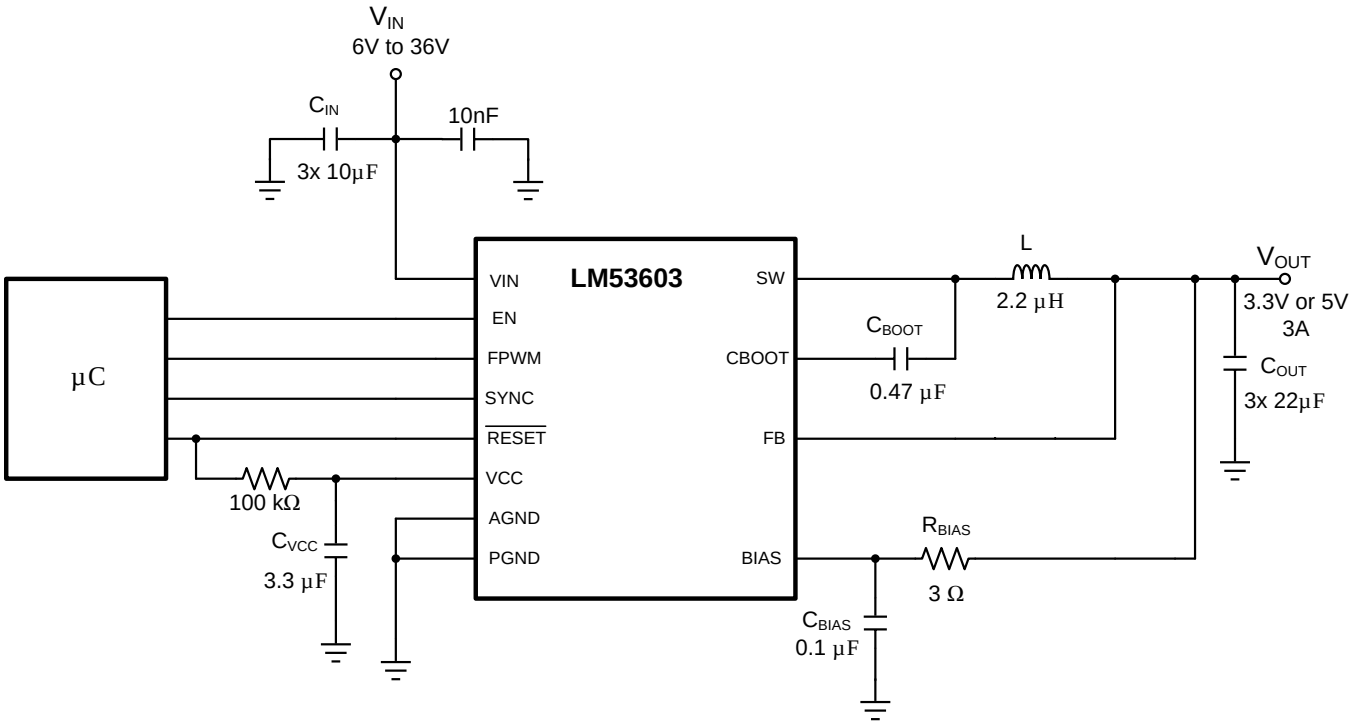


Figure 16. Full Featured Automotive Power Supply Schematic

9.2.1 Design Parameters

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V
Output voltage	5 V
Maximum output current	3A

9.2.2 Detailed Design Procedure

The following detailed design procedure applies to Figure 15, Figure 16, and Figure 43.

9.2.2.1 Setting the Output Voltage

For the fixed output voltage versions, the FB input is connected directly to the output voltage node. Preferably, near the top of the output capacitor. If the feed-back point is located further away from the output capacitors (that is, remote sensing), then a small 100 nF capacitor may be needed at the sensing point.

For output voltages other than 5 V or 3.3 V, a feed-back divider is required. For the ADJ version of the device, the regulator holds the FB pin at 1.0 V. The range of adjustable output voltage can be found in the *Recommended Operating Conditions*. Equation 3 can be used to determine R_{FBB} for a desired output voltage and a given R_{FBT}. Usually R_{FBT} is limited to a maximum value of 100 kΩ.

$$R_{FBB} = R_{FBT} \cdot \left[\frac{1V}{V_{OUT} - 1V} \right] \quad (3)$$

In addition a feed-forward capacitor C_{FF} may be required to optimize the transient response. For output voltages greater than 6 V, the WEBENCH Design Tool can be used to optimize the design.

9.2.2.2 Output Capacitors

The LM53603-Q1 is designed to work with low ESR ceramic capacitors. The *effective* value of these capacitors is defined as the actual capacitance under voltage bias and temperature. All ceramic capacitors have a large voltage coefficient, in addition to normal tolerances and temperature coefficients. Under D.C. bias, the capacitance value drops considerably. Larger case sizes and/or higher voltage capacitors are better in this regard. To help mitigate these effects, multiple small capacitors can be used in parallel to bring the minimum *effective* capacitance up to the desired value. This can also ease the RMS current requirements on a single capacitor. Table 3 shows the nominal and minimum values of total output capacitance recommended for the LM53603-Q1. The values shown also provide a starting point for other output voltages, when using the ADJ option. Also shown are the measured values of *effective* capacitance for the indicated capacitor. More output capacitance can be used to improve transient performance and reduce output voltage ripple.

In practice, the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and Bode plots are the best way to validate any given design, and should always be completed before the application goes into production. A careful study of temperature and bias voltage variation of any candidate ceramic capacitor should be made in order to ensure that the minimum value of *effective* capacitance is provided. The best way to obtain an optimum design is to use the Texas Instruments WEBENCH Design Tool.

In ADJ applications the feed-forward capacitor, C_{FF}, provides another degree of freedom when stabilizing and optimizing the design. Application report *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* (SLVA289) should prove helpful when adjusting the feed-forward capacitor.

In addition to the capacitance shown in Table 3, a small ceramic capacitor placed on the output can help to reduce high frequency noise. Small case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing spikes on the output caused by inductor parasitics.

The maximum value of total output capacitance should be limited to between 300 µF and 400 µF. Large values of output capacitance can prevent the regulator from starting-up correctly and adversely effect the loop stability. If values in the range given above, or greater, are to be used, then a careful study of start-up at full load and loop stability must be performed.

Table 3. Recommended Output Capacitors

OUTPUT VOLTAGE	NOMINAL OUTPUT CAPACITANCE		MINIMUM OUTPUT CAPACITANCE		PART NUMBER (MANUFACTURER)
	RATED CAPACITANCE	MEASURED CAPACITANCE(1)	RATED CAPACITANCE	MEASURED CAPACITANCE(1)	
3.3 V	3 x 22 µF	63 µF	2 x 22 µF	42 µF	C3225X7R1C226M250AC (TDK)
5 V	3 x 22 µF	60 µF	2 x 22 µF	40 µF	C3225X7R1C226M250AC (TDK)
6 V	3 x 22 µF	59 µF	2 x 22 µF	39 µF	C3225X7R1C226M250AC (TDK)
10 V(2)	3 x 22 µF	48 µF	2 x 22 µF	32 µF	C3225X7R1C226M250AC (TDK)

(1) Measured at indicated V_{OUT} at 25°C.
(2) The following components were used: C_{FF} = 47 pF, R_{FBT} = 100 kΩ, R_{FBB} = 11 kΩ, L = 4. 7 µH.

9.2.2.3 Input Capacitors

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying ripple current and isolating switching noise from other circuits. Table 4 shows the nominal and minimum values of total input capacitance recommenced for the LM53603-Q1. Also shown are the measured values of *effective* capacitance for the indicated capacitor. In addition, small high frequency bypass capacitors connected directly between the VIN and PGND pins are very helpful in reducing noise spikes and aid in reducing conducted EMI. It is recommenced that a small case size 10 nF ceramic capacitor be placed across the input, as close as possible to the device (see Figure 45). Additional high frequency capacitors can be used to help manage conducted EMI or voltage spike issues that may be encountered.

Table 4. Recommended Input Capacitors

NOMINAL INPUT CAPACITANCE		MINIMUM INPUT CAPACITANCE		PART NUMBER (MANUFACTURER)
RATED CAPACITANCE	MEASURED CAPACITANCE (1)	RATED CAPACITANCE	MEASURED CAPACITANCE(1)	
3 x 10 µF	22.5 µF	2 x 10 µF	15 µF	CL32B106KBJNNNE (Samsung)

(1) Measured at 14V and 25°C.

Many times it is desirable to use an electrolytic capacitor on the input, in parallel with the ceramics. This is especially true if longs leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by long power leads. The use of this additional capacitor will also help with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor(s). The approximate RMS value of this current can be calculated from Equation 4 and should be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{4}$$

9.2.2.4 Inductor

The LM53603-Q1 and LM53602-Q1 are optimized for a nominal inductance of 2.2 µH for the 5 V and 3.3 V versions. This gives a ripple current that is approximately 20% to 30% of the full load current of 3 A. For output voltages greater than 5 V, a proportionally larger inductor can be used. This will keep the ratio of inductor current slope to internal compensating slope constant.

The most important inductor parameters are saturation current and parasitic resistance. Inductors with a saturation current of between 5 A and 6 A are appropriate for most applications, when using the LM53603-Q1. For the LM53602-Q1, inductors with a saturation current of between 4 A and 5 A are appropriate. Of course the inductor parasitic resistance should be as low as possible to reduce losses at heavy loads. Table 5 gives a list of several possible inductors that can be used with the LM53603-Q1.

Table 5. Recommenced Inductors

MANUFACTURER	PART NUMBER	SATURATION CURRENT	D.C. RESISTANCE
Würth	7440650022	6 A	15 mΩ
Coilcraft	DO3316T-222MLB	7.8 A	11 mΩ
Coiltronics	MPI4040R3-2R2-R	7.9 A	48 mΩ
Vishay	IHLP2525CZER2R2M01	8 A	18 mΩ
Vishay	IHLP2525BDER2R2M01	6.5 A	28 mΩ
Coilcraft	XAL6030-222ME	16 A	13 mΩ

9.2.2.5 VCC

The VCC pin is the output of the internal LDO, used to supply the control circuits of the LM53603-Q1. This output requires a 3.3 µF, 10 V ceramic capacitor connected from VCC to GND for proper operation. In general this output should not be loaded with any external circuitry. However, it can be used to supply a logic level to the FPWM input, or for the pull-up resistor used with the $\overline{\text{RESET}}$ output (see Figure 16). The nominal output of the LDO is 3.15 V.

9.2.2.6 BIAS

The BIAS pin is the input to the internal LDO. As mentioned in *Input Supply Current*, this input is connected to V_{OUT} in order to provide the lowest possible supply current at light loads. Since this input is connected directly to the output, it should be protected from negative voltage transients. Such transients may occur when the output is shorted at the end of a long PCB trace or cable. If this is likely, in a given application, then a small resistor should be placed in series between the BIAS input and V_{OUT}, as shown in Figure 15. The resistor should be sized to limit the current out of the BIAS pin to <100 mA. Values in the range of 2 Ω to 5 Ω are usually sufficient. Values greater than 5 Ω are not recommended. As a rough estimate, assume that the full negative transient will appear across R_{BIAS}, and design for a current of < 100 mA. In severe cases, a Schottky diode can be placed in parallel with the output to limit the transient voltage and current.

9.2.2.7 CBOOT

The LM53603-Q1 requires a "boot-strap" capacitor between the CBOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A ceramic capacitor of 0.47 µF, ≥6.3 V is required.

9.2.2.8 Maximum Ambient Temperature

As with any power conversion device, the LM53603-Q1 will dissipate internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter, above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss and the effective thermal resistance, $R_{\theta JA}$ of the device and PCB combination. The maximum internal die temperature for the LM53603-Q1 is 150°C, thus establishing a limit on the maximum device power dissipation and therefore load current at high ambient temperatures. Equation 5 shows the relationships between the important parameters.

$$I_{OUT} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \tag{5}$$

It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ will reduce the maximum available output current. As stated in SPRA953, the values given in the *Thermal Information* table are not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are never obtained in an actual application. The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as power dissipation, air temperature, PCB area, copper heat-sink area, number of thermal vias under the package, air flow, and adjacent component placement. The LM53603-Q1 utilizes an advanced package with a heat spreading pad (EP) on the bottom. This must be soldered directly to the PCB copper ground plane to provide an effective heat-sink, as well as a proper electrical connection. The resources found in Table 8 can be used as a guide to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment. A typical example of $R_{\theta JA}$ versus copper board area is shown in Figure 17. The copper area in this graph is that for each layer of a four layer board; the inner layers are 1 oz. (35µm), while the outer layers are 2 oz. (70µm). A typical curve of maximum load current versus ambient temperature, for both the LM53603-Q1 and LM53602-Q1, is shown in Figure 18. This data was taken with the device soldered to a PCB with an $R_{\theta JA}$ of about 17°C/W and an input voltage of 12 V. It must be remembered that the data shown in these graphs are for illustration only and the actual performance in any given application will depend on all of the factors mentioned above.

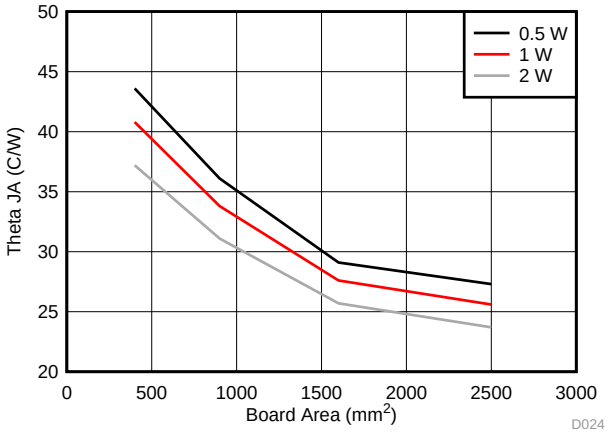


Figure 17. $R_{\theta JA}$ versus Copper Board Area

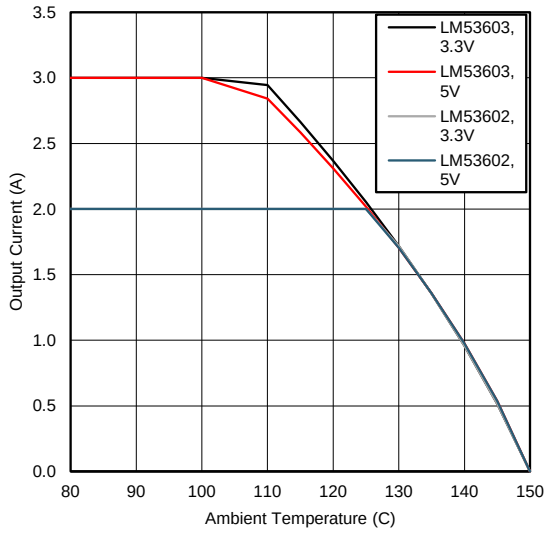
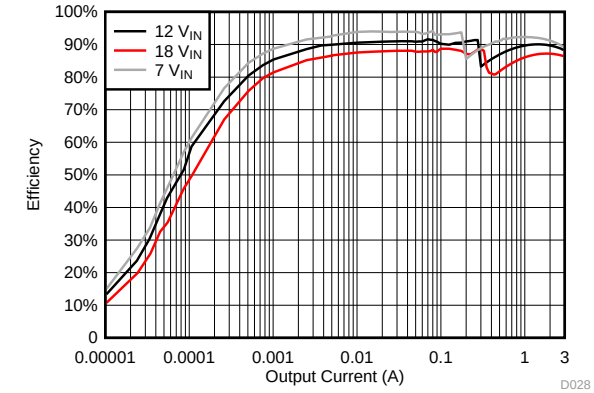


Figure 18. Maximum Output Current versus Ambient Temperature $R_{\theta JA}$ = 17°C/W, VIN = 12V

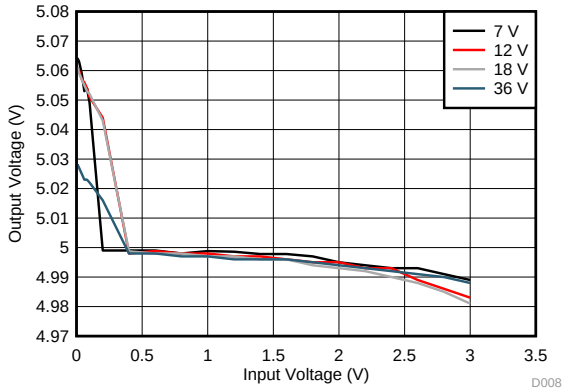
9.2.3 Application Curves

The following characteristics apply only to the circuit of Figure 15. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C.



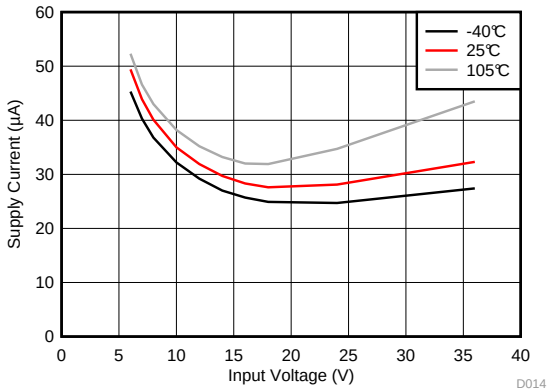
V_{OUT} = 5 V AUTO
Inductor = XAL6030-222ME

Figure 19. Efficiency



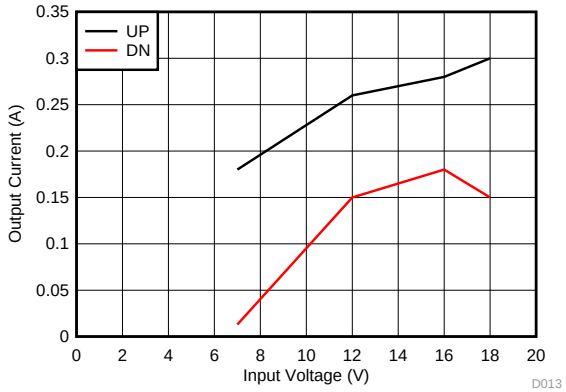
V_{OUT} = 5 V AUTO

Figure 20. Load and Line Regulation



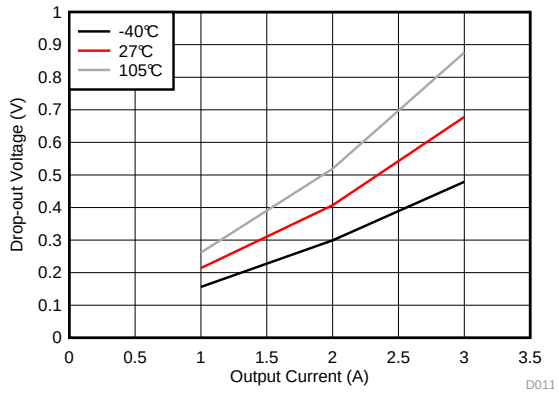
V_{OUT} = 5 V AUTO I_{OUT} = 0 A

Figure 21. Input Supply Current



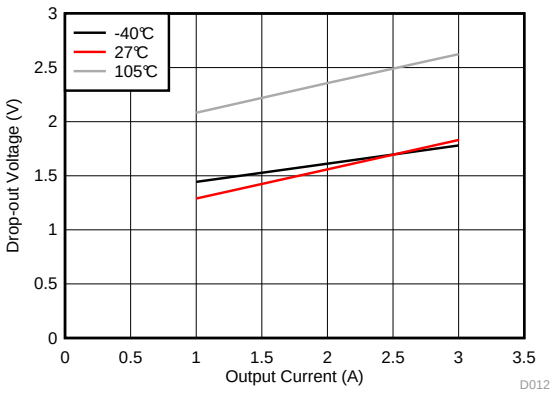
V_{OUT} = 5 V

Figure 22. Load Current for Mode Change



V_{OUT} = 5 V

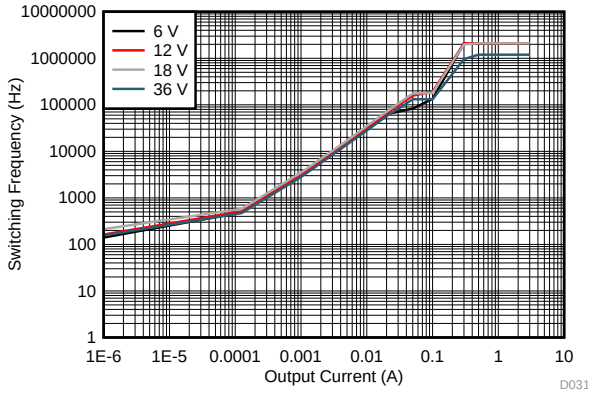
Figure 23. Drop-out for –1% Regulation



V_{OUT} = 5 V

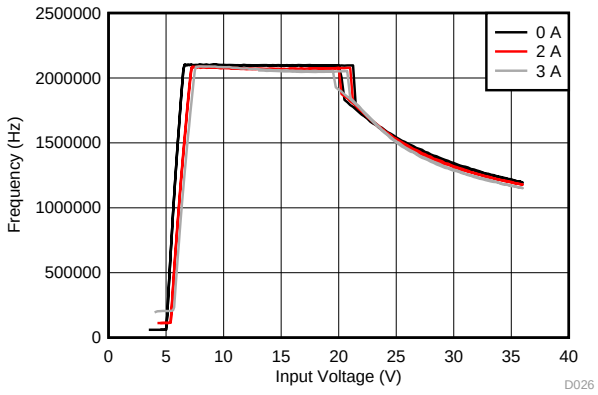
Figure 24. Drop-out for ≥ 1.85 MHz

The following characteristics apply only to the circuit of Figure 15. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C.



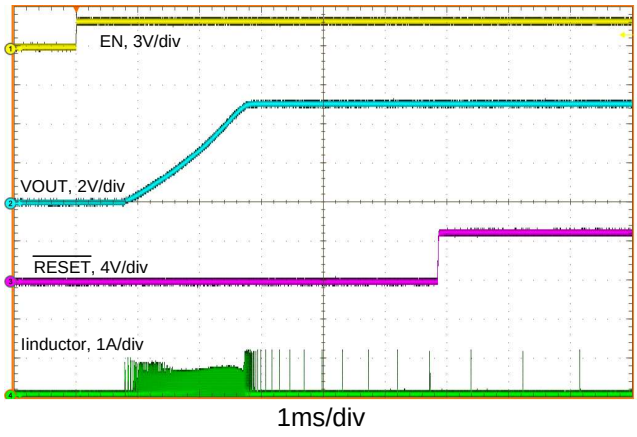
V_{OUT} = 5 V AUTO

Figure 25. Switching Frequency vs. Load Current



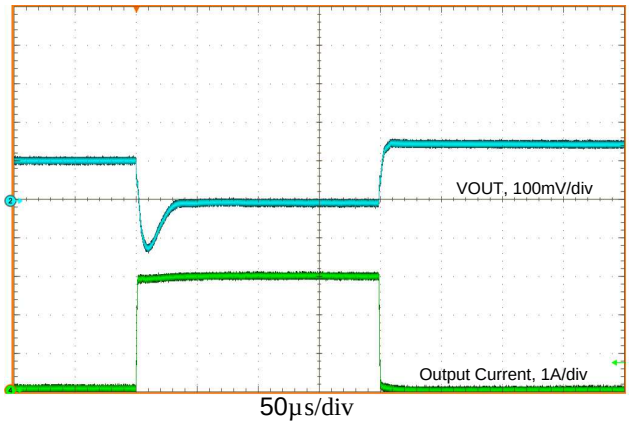
V_{OUT} = 5 V FPWM

Figure 26. Switching Frequency vs. Input Voltage



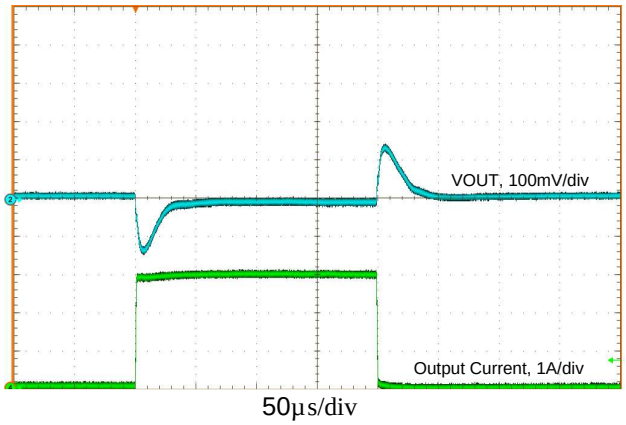
V_{OUT} = 5 V I_{OUT} = 0 A AUTO

Figure 27. Start-up



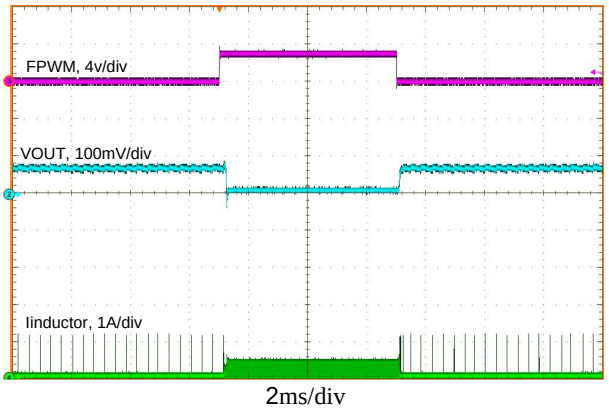
V_{OUT} = 5 V I_{OUT} = 0 A to 3 A, T_R = T_F = 1 µs AUTO

Figure 28. Load Transients



V_{OUT} = 5 V I_{OUT} = 0 A to 3 A, T_R = T_F = 1 µs FPWM

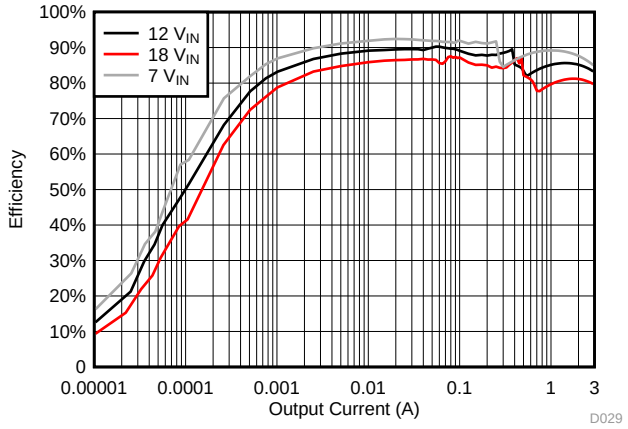
Figure 29. Load Transient



V_{OUT} = 5 V I_{OUT} = 1 mA

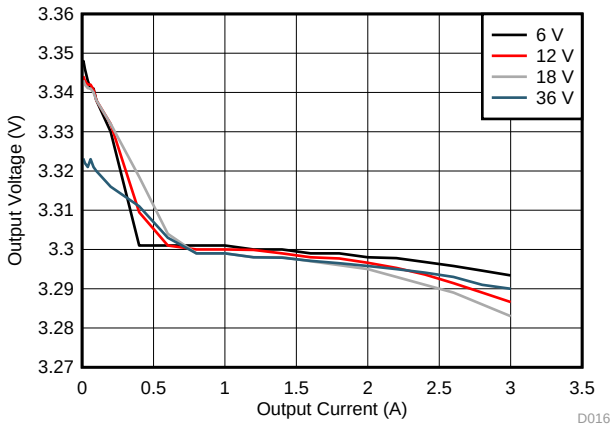
Figure 30. Mode Change Transient

The following characteristics apply only to the circuit of Figure 15. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C.



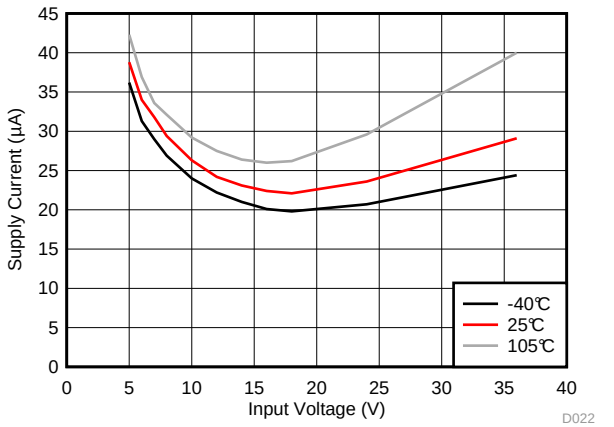
V_{OUT} = 3.3 V AUTO
Inductor = XAL6030-222ME

Figure 31. Efficiency



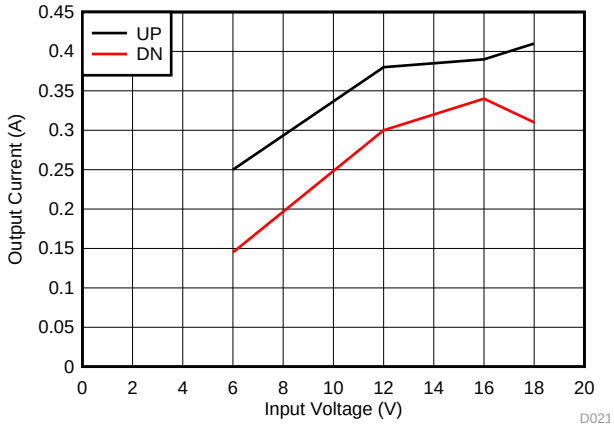
V_{OUT} = 3.3 V AUTO

Figure 32. Load and Line Regulation



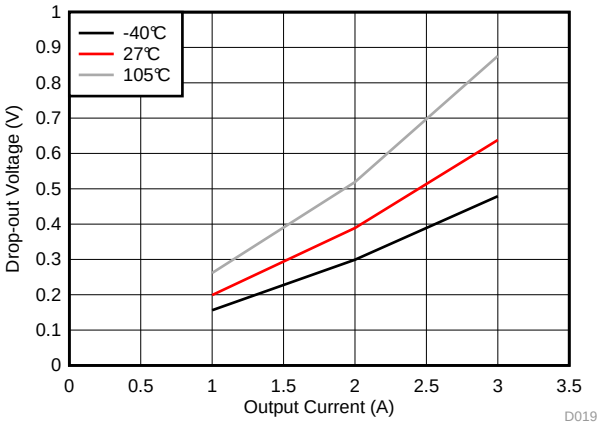
V_{OUT} = 3.3 V AUTO I_{OUT} = 0 A

Figure 33. Input Supply Current



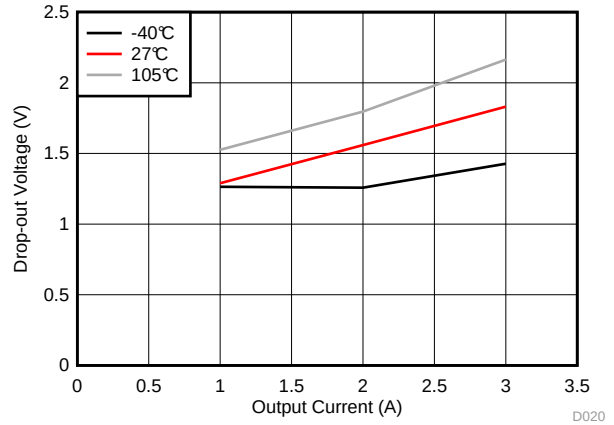
V_{OUT} = 3.3 V

Figure 34. Load Current for Mode Change



V_{OUT} = 3.3 V

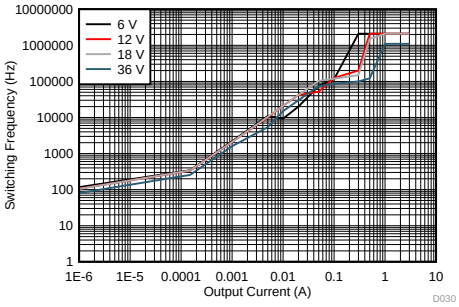
Figure 35. Drop-out for –1% Regulation



V_{OUT} = 3.3 V

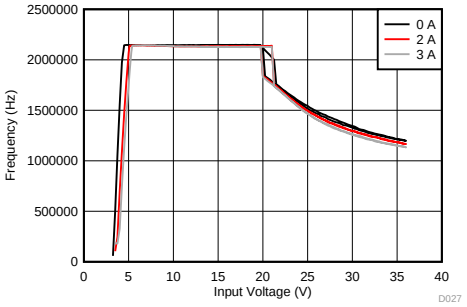
Figure 36. Drop-out for ≥ 1.85 MHz

The following characteristics apply only to the circuit of Figure 15. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C.



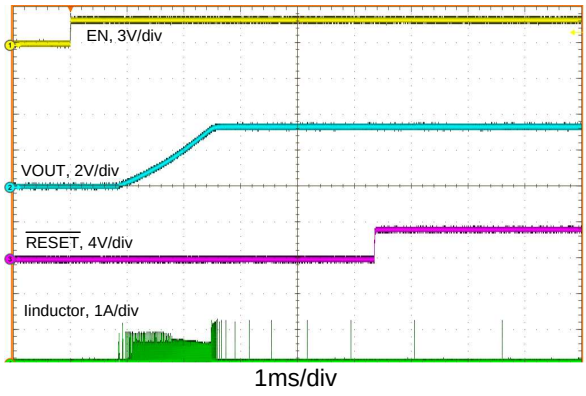
V_{OUT} = 3.3 V AUTO

Figure 37. Switching Frequency vs. Load Current



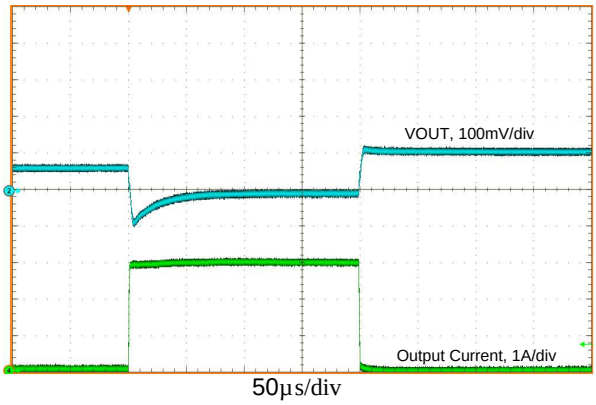
V_{OUT} = 3.3 V FPWM

Figure 38. Switching Frequency vs. Input Voltage



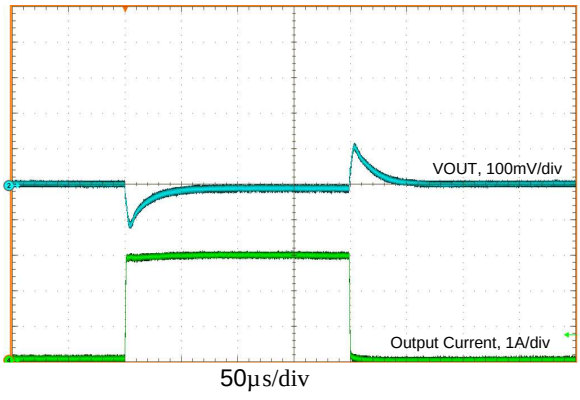
V_{OUT} = 3.3 V AUTO I_{OUT} = 0 A

Figure 39. Start-up



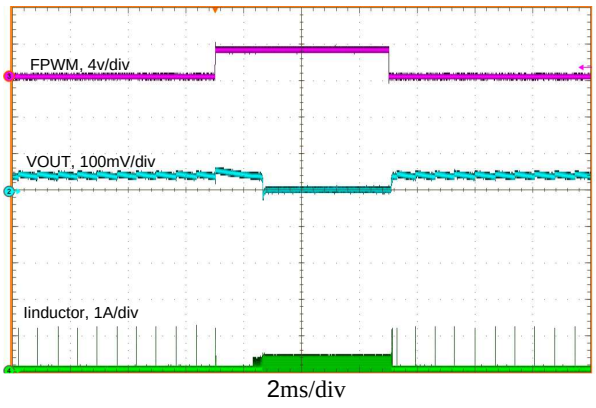
V_{OUT} = 3.3 V I_{OUT} = 0 A to 3 A, T_R = T_F = 1 µs AUTO

Figure 40. Load Transient



V_{OUT} = 3.3 V I_{OUT} = 0 A to 3 A, T_R = T_F = 1 µs FPWM

Figure 41. Load Transient



V_{OUT} = 3.3 V I_{OUT} = 1 mA

Figure 42. Mode Change Transient

9.2.4 Additional Application Circuit

Figure 43 shows a typical example of a design with an output voltage of 10 V; while Table 6 gives typical design parameters. Please refer to *Detailed Design Procedure* for the design procedure.

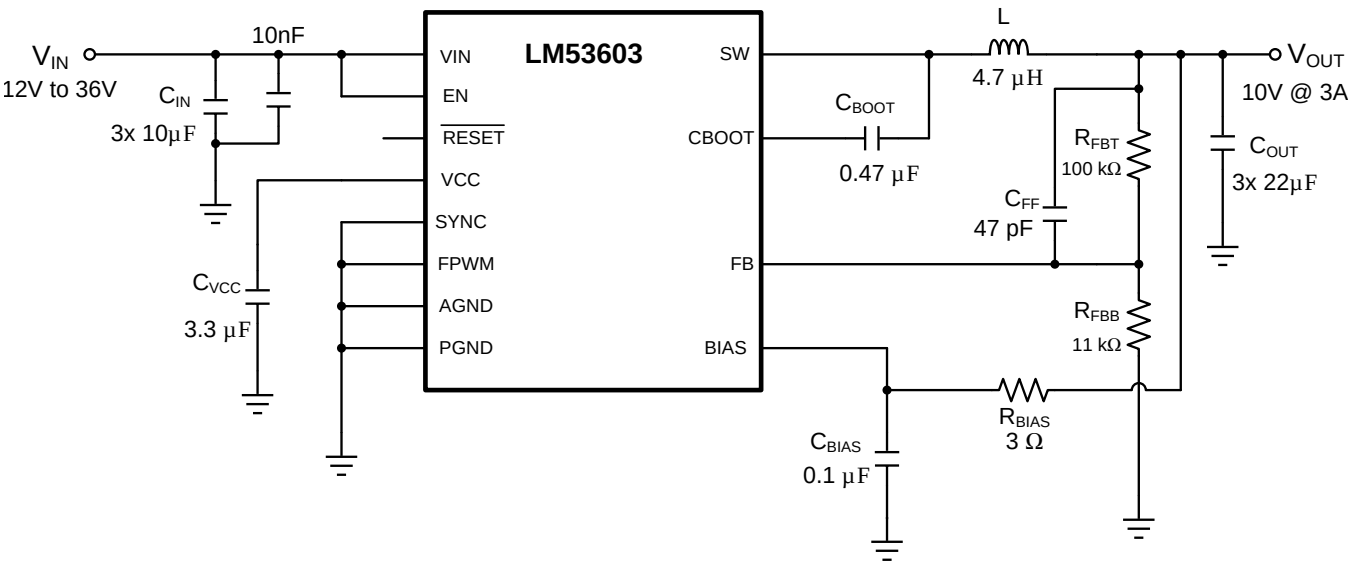


Figure 43. Typical Adjustable Output Automotive Power Supply Schematic CD/DVD/Blu-ray Disc™ Motor Drive Applications V_{OUT} = 10 V

9.2.4.1 Design Parameters for Typical Adjustable Output Automotive Power Supply

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage	12 V
Output Voltage	10 V
Maximum Output Current	3 A

9.3 Do's and Don't's

- **Don't:** Exceed the *Absolute Maximum Ratings*.
- **Don't:** Exceed the *ESD Ratings*.
- **Don't:** Exceed the *Recommended Operating Conditions*.
- **Don't:** Allow the EN, FPWM or SYNC input to float.
- **Don't:** Allow the output voltage to exceed the input voltage, nor go below ground.
- **Don't:** Use the thermal data given in the *Thermal Information* table to design your application.
- **Do:** Follow all of the guidelines and/or suggestions found in this data sheet, before committing your design to production. TI Application Engineers are ready to help critique your design and PCB layout to help make your project a success.
- **Do:** Refer to the helpful documents found in Table 8 and Table 7.

10 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with Equation 6, where η is the efficiency.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \quad (6)$$

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low ESR ceramic input capacitors, can form an under-damped resonant circuit. This circuit may cause over-voltage transients at the VIN pin, each time the input supply is cycled on and off. The parasitic resistance will cause the voltage at the VIN pin to dip when the load on the regulator is switched on, or exhibits a transient. If the regulator is operating close to the minimum input voltage, this dip may cause the device to shutdown and/or reset. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator and/or use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors will help to damp the input resonant circuit and reduce any voltage overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The user guide *Simple Success with Conducted EMI for DC-DC Converters*, SNVA489, provides helpful suggestions when designing an input filter for any switching regulator

In some cases a Transient Voltage Suppressor (TVS) is used on the input of regulators. One class of this device has a "snap-back" V-I characteristic (thyristor type). The use of a device with this type of characteristic is not recommend. When the TVS "fires", the clamping voltage drops to a very low value. If this holding voltage is less than the output voltage of the regulator, the output capacitors will be discharged through the regulator back to the input. This uncontrolled current flow could damage the regulator.

11 Layout

11.1 Layout Guidelines

The PCB layout of any DC-DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout, to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor and power ground, as shown in Figure 44. This loop carries fast transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages will disrupt the proper operation of the converter. Because of this, the traces in this loop should be wide and short, and the loop area as small as possible to reduce the parasitic inductance. Figure 45 shows a recommended layout for the critical components of the LM53603-Q1. This PCB layout is a good guide for any specific application. The following important guidelines should also be followed:

1. **Place the input capacitor(s) CIN as close as possible to the VIN and PGND terminals.** VIN and GND are on the same side of the device, simplifying the input capacitor placement.
2. **Place bypass capacitors for VCC and BIAS close to their respective pins.** These components must be placed close to the device and routed with short/wide traces to the pins and ground. The trace from BIAS to VOUT should be ≥10mils wide.
3. **Use wide traces for the CBOOT capacitor.** CBOOT should be placed close to the device with short/wide traces to the CBOOT and SW pins.
4. **Place the feedback divider as close as possible to the FB pin on the device.** If a feedback divider and C_{FF} are used, they should be close to the device, while the length of the trace from V_{OUT} to the divider can be somewhat longer. However, this latter trace should not be routed near any noise sources that can capacitively couple to the FB input.
5. **Use at least one ground plane in one of the middle layers.** This plane will act as a noise shield and also act as a heat dissipation path.
6. **Connect the EP pad to the GND plane.** This pad acts as a heat-sink connection and a ground connection for the regulator. It must be solidly connected to a ground plane. The integrity of this connection has a direct bearing on the effective $R_{\theta JA}$.
7. **Provide wide paths for VIN, VOUT and GND.** Making these paths as wide as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
8. **Provide enough PCB area for proper heat-sinking.** As stated in the *Maximum Ambient Temperature* section, enough copper area must be used to ensures a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers should be made with two ounce copper; and no less than one ounce. Use an array of heat-sinking vias to connect the exposed pad (EP) to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
9. **Keep switch area small.** The copper area connecting the SW pin to the inductor should be kept as short and wide as possible. At the same time the total area of this node should be minimized to help mitigate radiated EMI.
10. **The resources in Table 7 provide additional important guidelines**

Table 7. PCB Layout Resources

TITLE	LINK
AN-1149 *Layout Guidelines for Switching Power Supplies*	SNVA021
AN-1229 *Simple Switcher PCB Layout Guidelines*	SNVA054
Constructing Your Power Supply- Layout Considerations	SLUP230
SNVA721 *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*	SNVA721

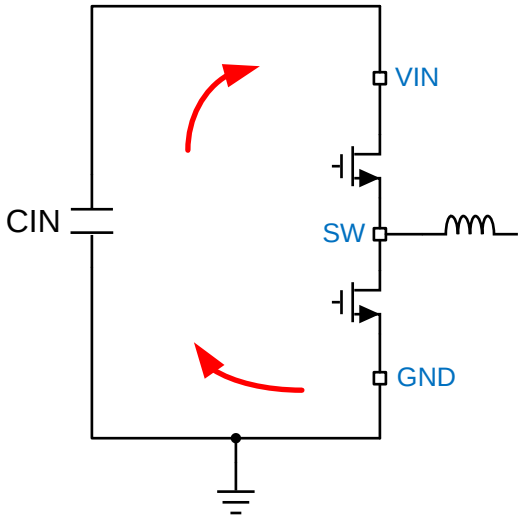


Figure 44. Current Loops with Fast Transients

11.1.1 Ground and Thermal Plane Considerations

As mentioned above, it is recommended to use one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins should be connected to the ground plane using vias right next to the bypass capacitors. PGND pins are connected to the source of the internal low side MOSFET switch. They should be connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and may bounce due to load variations. The PGND trace, as well as PVIN and SW traces, should be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and should be used for sensitive routes.

It is recommended to provide adequate device heat sinking by utilizing the exposed pad (EP) of the IC as the primary thermal path. Use a minimum 4 by 4 array of 10 mil thermal vias to connect the EP to the system ground plane for heat sinking. The vias should be evenly distributed under the exposed pad. Use as much copper as possible for system ground plane on the top and bottom layers for the best heat dissipation. It is recommended to use a four-layer board with the copper thickness, starting from the top, as: 2 oz / 1 oz / 1 oz / 2 oz. A four layer board with enough copper thickness and proper layout provides low current conduction impedance, proper shielding and lower thermal resistance.

Table 8. Resources for Thermal PCB Design

TITLE	LINK
AN-2020 *Thermal Design By Insight, Not Hindsight*	SNVA419
AN-1520 *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*	SNVA183
SPRA953B *Semiconductor and IC Package Thermal Metrics*	SPRA953
SNVA719 *Thermal Design made Simple with LM43603 and LM43602*	SNVA719
SLMA002 *PowerPAD™ Thermally Enhanced Package*	SLMA002
SLMA004 *PowerPAD Made Easy*	SLMA004
SBVA025 *Using New Thermal Metrics*	SBVA025

11.2 Layout Example

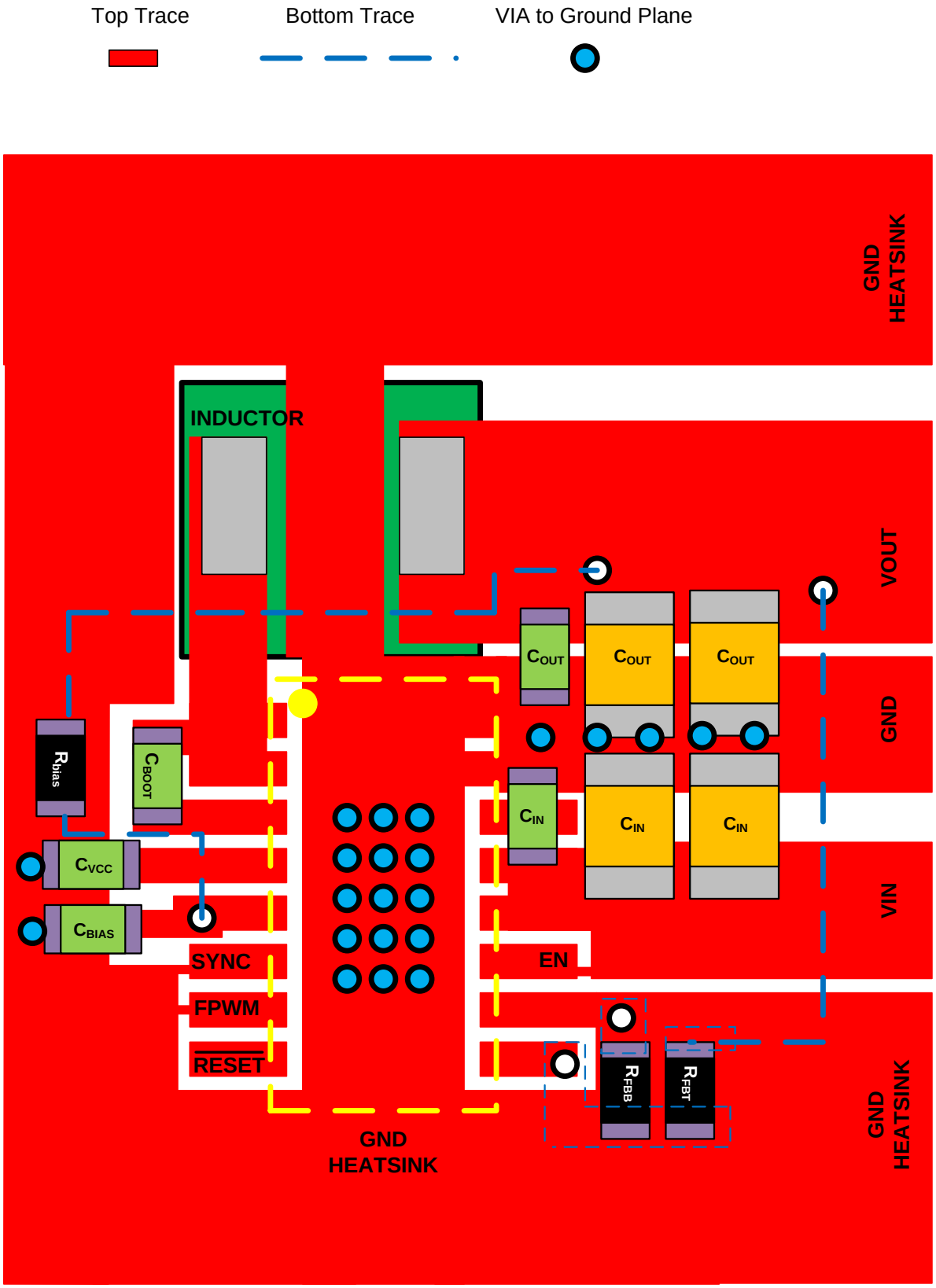


Figure 45. PCB Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 文档支持

12.2.1 相关文档

相关文档如下：

- 应用报告《*使用新的热指标*》（文献编号：SBVA025）。
- 《*采用前馈电容优化内部补偿 DC-DC 转换器的瞬态响应*》（文献编号：SLVA289）。
- 《*轻松抑制 DC-DC 转换器中的传导性 EMI*》（文献编号：SNVA489）。

12.2.2 相关链接

表 9 列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **9.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
LM53602-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LM53603-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
Blu-ray Disc is a trademark of Blu-ray Disk Association.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM536023QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	L536023	Samples
LM536023QPWPTQ1	ACTIVE	HTSSOP	PWP	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	L536023	Samples
LM536025QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	L536025	Samples
LM536025QPWPTQ1	ACTIVE	HTSSOP	PWP	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	L536025	Samples
LM53602AQPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	L53602A	Samples
LM53602AQPWPTQ1	ACTIVE	HTSSOP	PWP	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	L53602A	Samples
LM536033QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	L536033	Samples
LM536033QPWPTQ1	ACTIVE	HTSSOP	PWP	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	L536033	Samples
LM536035QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	L536035	Samples
LM536035QPWPTQ1	ACTIVE	HTSSOP	PWP	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	L536035	Samples
LM53603AQPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	L53603A	Samples
LM53603AQPWPTQ1	ACTIVE	HTSSOP	PWP	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	L53603A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

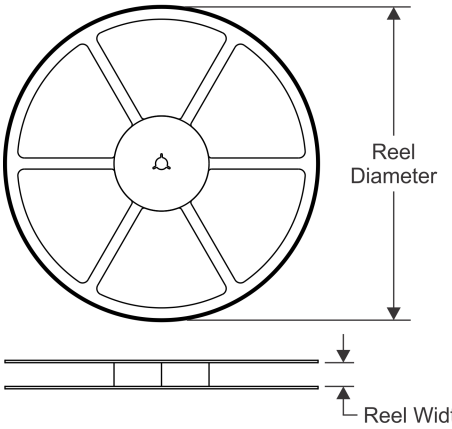
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

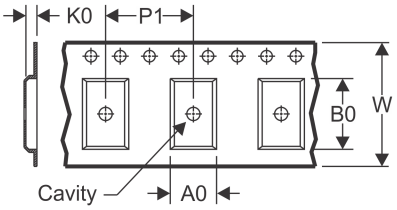
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

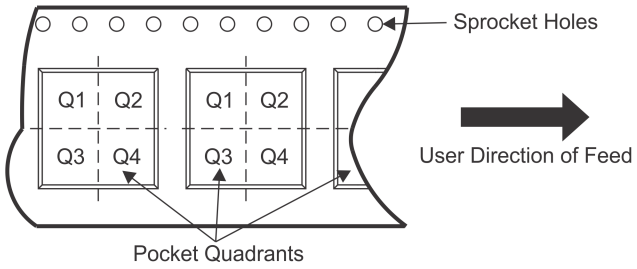


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

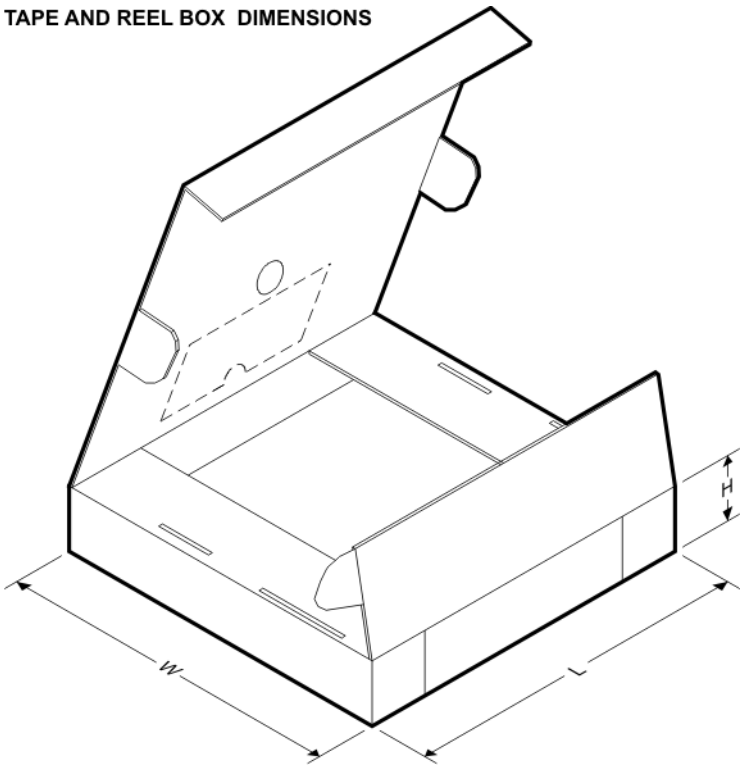
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

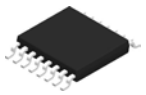
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM536023QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM536023QPWPTQ1	HTSSOP	PWP	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM536025QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM536025QPWPTQ1	HTSSOP	PWP	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM53602AQPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM53602AQPWPTQ1	HTSSOP	PWP	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM536033QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM536033QPWPTQ1	HTSSOP	PWP	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM536035QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM536035QPWPTQ1	HTSSOP	PWP	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM53603AQPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM53603AQPWPTQ1	HTSSOP	PWP	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM536023QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0
LM536023QPWPTQ1	HTSSOP	PWP	16	250	210.0	185.0	35.0
LM536025QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0
LM536025QPWPTQ1	HTSSOP	PWP	16	250	210.0	185.0	35.0
LM53602AQPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0
LM53602AQPWPTQ1	HTSSOP	PWP	16	250	210.0	185.0	35.0
LM536033QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0
LM536033QPWPTQ1	HTSSOP	PWP	16	250	210.0	185.0	35.0
LM536035QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0
LM536035QPWPTQ1	HTSSOP	PWP	16	250	210.0	185.0	35.0
LM53603AQPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0
LM53603AQPWPTQ1	HTSSOP	PWP	16	250	210.0	185.0	35.0

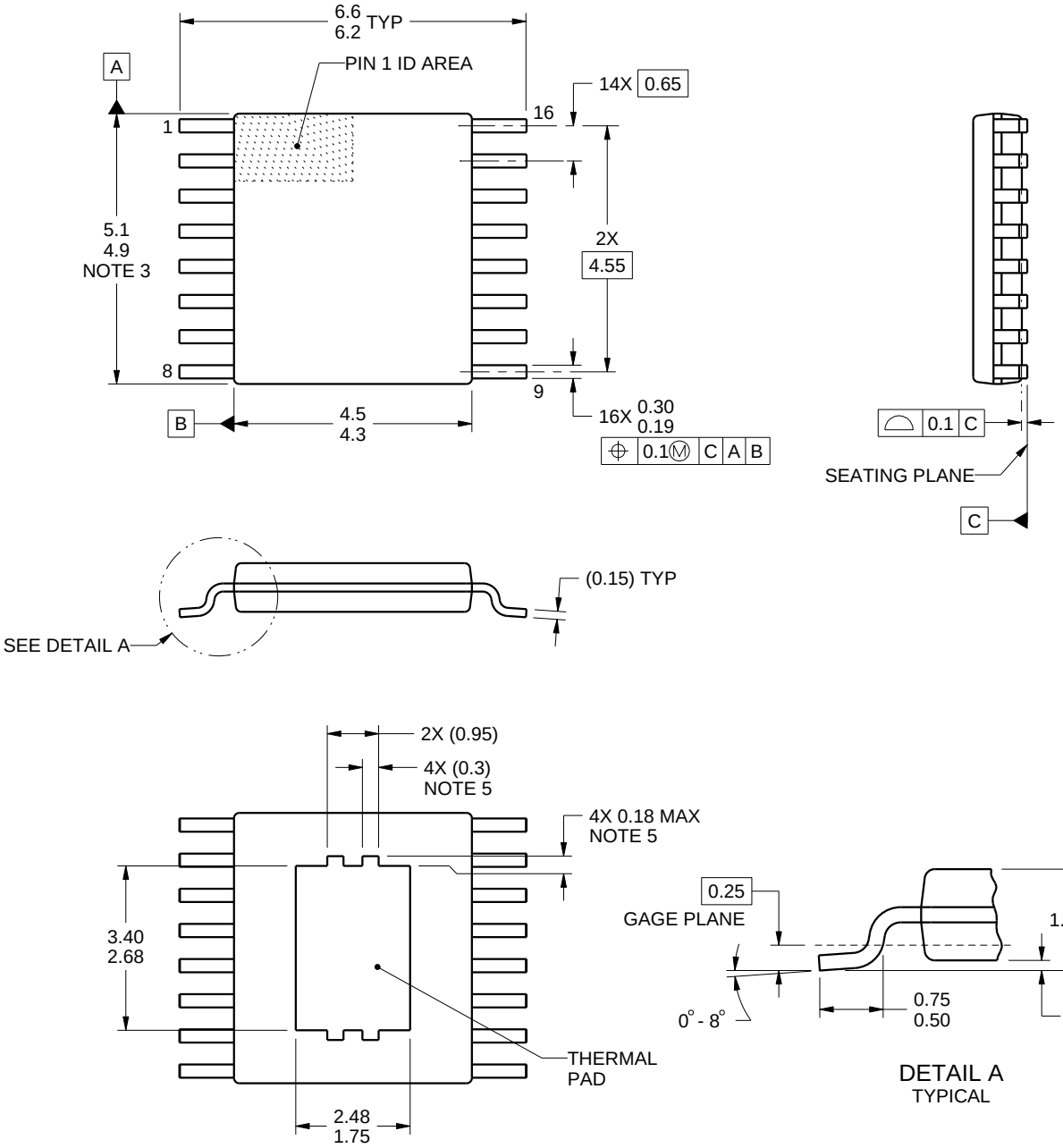


PACKAGE OUTLINE

PWP0016D

PowerPAD™ TSSOP - 1.2 mm max height

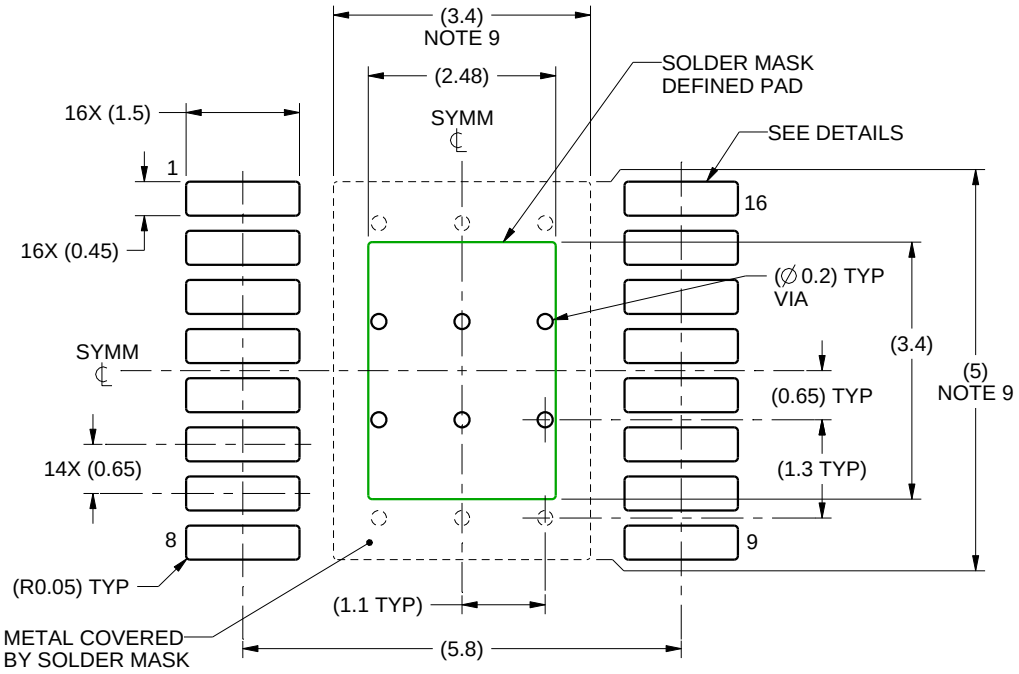
PLASTIC SMALL OUTLINE



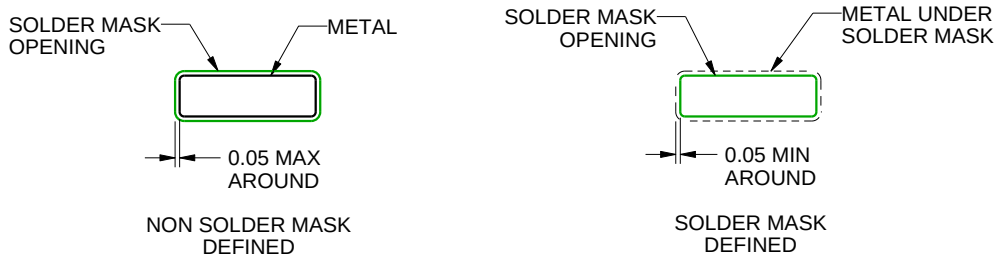
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

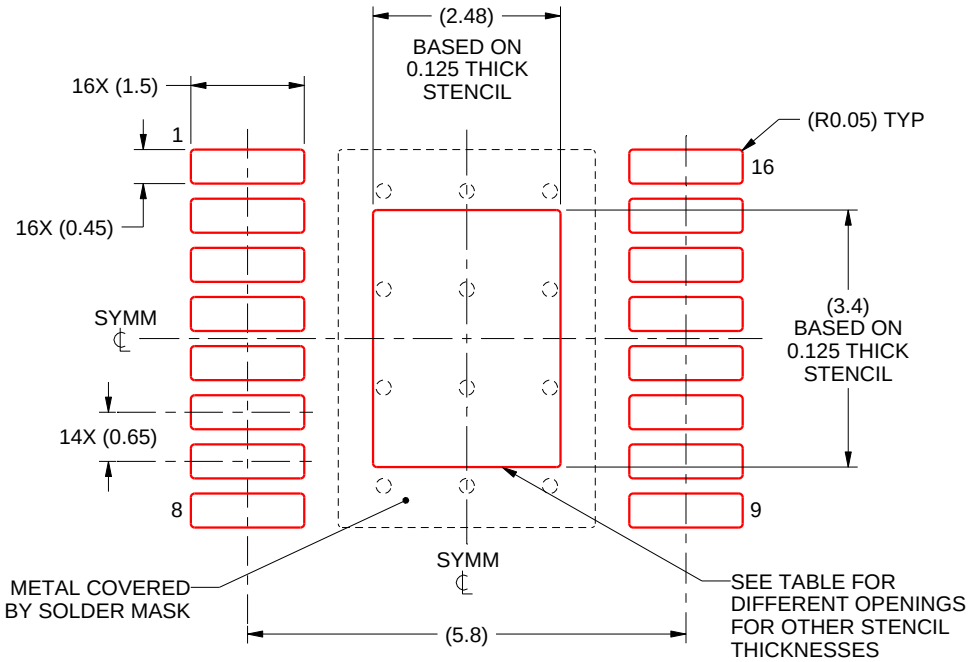


SOLDER MASK DETAILS
NOT TO SCALE

4223219/A 08/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.77 X 3.8
0.125	2.48 X 3.4 (SHOWN)
0.15	2.26 X 3.1
0.175	2.1 X 2.87

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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