

# 10V Drive Nch MOSFET

#### **SP8K80**

#### Structure

Silicon N-channel MOSFET

#### Features

- 1) Built-in G-S protection diode.
- 2) Small surface mount package(SOP8).

#### Application

Switching

Packaging specifications

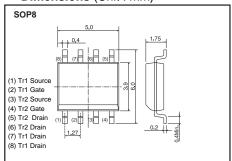
	Package	Taping
Type	Code	ТВ
	Basic ordering unit (pieces)	2500
SP8K80		0

#### ● Absolute maximum ratings (Ta = 25°C)

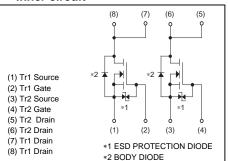
Parameter		Symbol	Limits	Unit
Drain-source voltage		$V_{DSS}$	500	V
Gate-source voltage		$V_{GSS}$	±30	V
Drain current	Continuous	I <sub>D</sub> *3	±0.5	Α
	Pulsed	I <sub>DP</sub> *1	±2	Α
Source current	Continuous	I <sub>S</sub> *3	0.5	Α
(Body Diode)	Pulsed	I <sub>SP</sub> *1	2	Α
Avalanche current		I <sub>AS</sub> *2	0.25	Α
Avalanche energy		E <sub>AS</sub> *2	0.017	mJ
Power dissipation		P <sub>D</sub> *4	2	W
Channel temperature		T <sub>ch</sub>	0.2	°C
Range of storage temperature		$T_{stg}$	-55 to +150	°C

<sup>\*1</sup> Pw $\leq$ 10 $\mu$ s, Duty cycle $\leq$ 1%

#### • Dimensions (Unit : mm)



#### • Inner circuit



<sup>\*2</sup> L  $\stackrel{\bullet}{=}$  500 $\mu$ H, V<sub>DD</sub>=50V, R<sub>G</sub>=25 $\Omega$ , T<sub>ch</sub>=25 $^{\circ}$ C

<sup>\*3</sup> Limited only by maximum channel temperature allowed.

<sup>\*4</sup> Mounted on a ceramic board.

## ● Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Gate-source leakage	$I_{GSS}$		-	±10	μA	$V_{GS}$ =±30V, $V_{DS}$ =0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	1	-	>	I <sub>D</sub> =1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>		-	100	μA	V <sub>DS</sub> =500V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS (th)</sub>	3.0	-	5.0	V	V <sub>DS</sub> =10V, I <sub>D</sub> =1mA
Static drain-source on-state resistance	R <sub>DS (on)</sub> *	-	9.0	11.7	Ω	I <sub>D</sub> =0.25A, V <sub>GS</sub> =10V
Forward transfer admittance	I Y <sub>fs</sub> I*	0.1	-	-	S	V <sub>DS</sub> =10V, I <sub>D</sub> =0.25A
Input capacitance	C <sub>iss</sub>	1	23.5	-	pF	V <sub>DS</sub> =25V
Output capacitance	C <sub>oss</sub>	1	36.5	-	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	$C_{rss}$		2.4	-	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	1	10	-	ns	V <sub>DD</sub> ≒ 250V, I <sub>D</sub> =0.25A
Rise time	t <sub>r</sub> *	1	18	-	ns	V <sub>GS</sub> =10V
Turn-off delay time	t <sub>d(off)</sub> *		25	-	ns	$R_L=1000\Omega$
Fall time	t <sub>f</sub> *	1	170	-	ns	$R_G=10\Omega$
Total gate charge	Q <sub>g</sub> *	-	3.8	-	nC	V <sub>DD</sub> ≒250V
Gate-source charge	Q <sub>gs</sub> *	1	1.3	-	nC	I <sub>D</sub> =0.5A
Gate-drain charge	Q <sub>gd</sub> *	-	1.6	-	nC	V <sub>GS</sub> =10V

<sup>\*</sup>Pulsed

## ●Body diode characteristics (Source-Drain)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub> *	-	-	1.5	V	I <sub>S</sub> =0.25A, V <sub>GS</sub> =0V

<sup>\*</sup>Pulsed

#### ●Electrical characteristic curves (Ta=25°C)

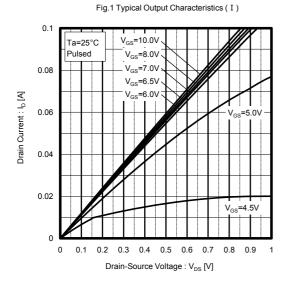


Fig.3 Typical Transfer Characteristics

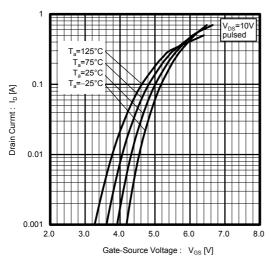


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

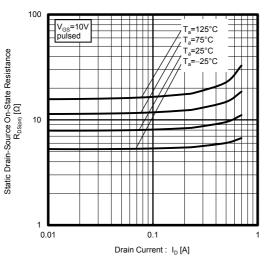


Fig.2 Typical Output Characteristics ( II )

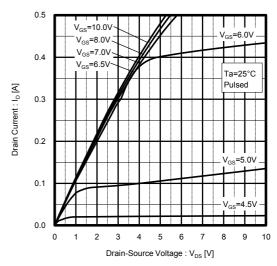


Fig.4 Gate Threshold Voltage vs. Channel Temperature

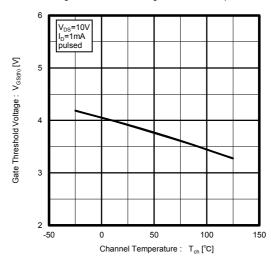


Fig.6 Static Drain-Source On-State Resistance vs. Channel Temperature

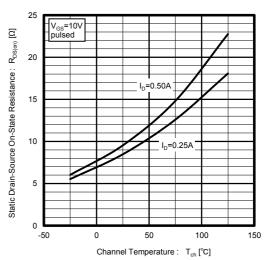
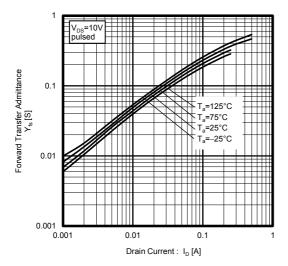


Fig.7 Forward Transfer Admittance vs. Drain Current



Flg.9 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

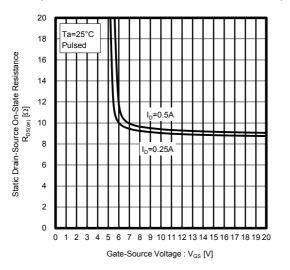


Fig.11 Dynamic Input Characteristics

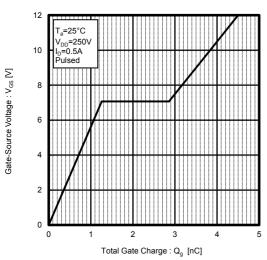


Fig.8 Source Current vs. Source-Drain Voltage

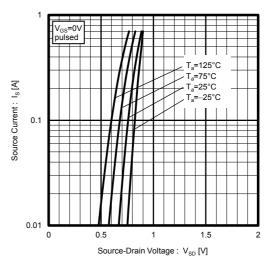


Fig.10 Switching Characteristics

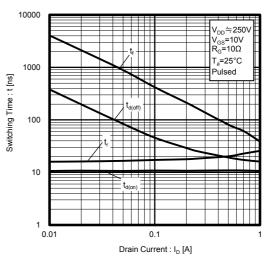


Fig.12 Typical Capacitance vs. Drain-Source Voltage

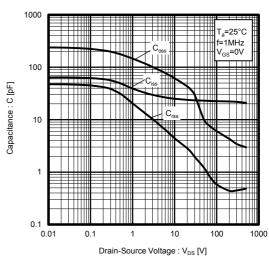


Fig.13 Normalized Transient Thermal Resistance v.s. Pulse Width

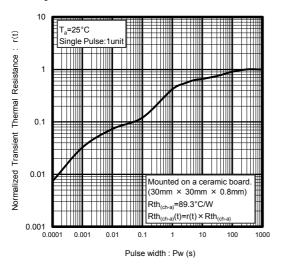


Fig.15 Reverse Recovery Time vs. Source Current

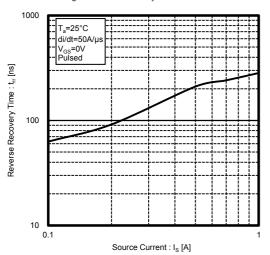
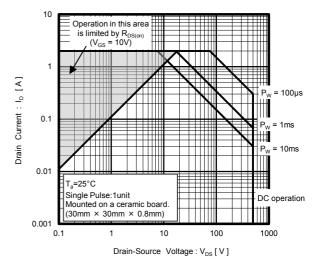


Fig.14 Maximum Safe Operating Area



#### Measurement circuits

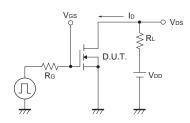


Fig.1-1 Switching Time Measurement Circuit

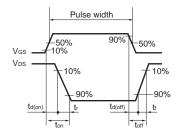


Fig.1-2 Switching Waveforms

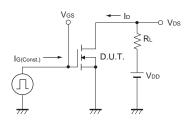


Fig.2-1 Gate Charge Measurement Circuit

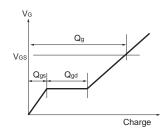


Fig.2-2 Gate Charge Waveform

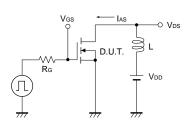


Fig.3-1 Avalanche Measurement Circuit

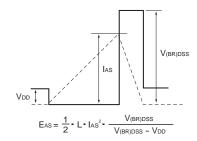


Fig.3-2 Avalanche Waveform

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