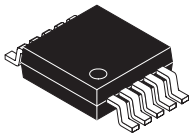


SLUS507D − JANUARY 2002 − REVISED NOVEMBER 2005

LOW-INPUT VOLTAGE-MODE SYNCHRONOUS BUCK CONTROLLER

FEATURES

- Operating Input Voltage 2.25 V to 5.5 V
- Output Voltage as Low as 0.7 V
- 1% Internal 0.7 V Reference
- Predictive Gate Drive™ N-Channel MOSFET Drivers for Higher Efficiency
- Externally Adjustable Soft-Start and Overcurrent Limit
- Source-Only Current or Source/Sink Current
- Versions for Starting Into V_{OUT} Pre-Bias
- 10-Lead MSOP PowerPad™ Package for Higher Performance
- Thermal Shutdown
- Internal Boostrap Diode
- Fixed-Frequency, Voltage-Mode Control
  - TPS40000/1/4 300-kHz
  - TPS40002/3/5 600-kHz

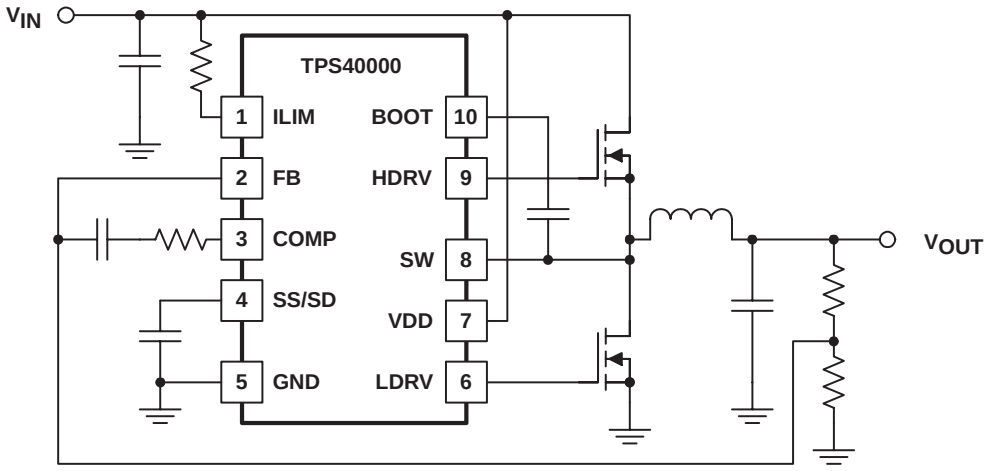
APPLICATIONS

- Networking Equipment
- Telecom Equipment
- Base Stations
- Servers
- DSP Power
- Power Modules

DESCRIPTION

The TPS4000x are controllers for low-voltage, non-isolated synchronous buck regulators. These controllers drive an N-channel MOSFET for the primary buck switch, and an N-channel MOSFET for the synchronous rectifier switch, thereby achieving very high-efficiency power conversion. In addition, the device controls the delays from main switch off to rectifier turn-on and from rectifier turn-off to main switch turn-on in such a way as to minimize diode losses (both conduction and recovery) in the synchronous rectifier with TI's proprietary Predictive Gate Drive™ technology. The reduction in these losses is significant and increases efficiency. For a given converter power level, smaller FETs can be used, or heat sinking can be reduced or even eliminated.

SIMPLIFIED APPLICATION DIAGRAM



UDG−01141

PowerPAD™ and Predictive Gate Drive™ are trademarks of Texas Instruments Incorporated.

DESCRIPTION (continued)

The current-limit threshold is adjustable with a single resistor connected to the device. The TPS4000x controllers implement a closed-loop soft start function. Startup ramp time is set by a single external capacitor connected to the SS/SD pin. The SS/SD pin is also used for shutdown.

ORDERING INFORMATION

T_A	FREQUENCY	PACKAGED DEVICES MSOP(2) (DGQ)		
		APPLICATION		
		SOURCE ONLY	SOURCE/SINK WITH PREBIAS(3)	SOURCE/SINK(3)
−40°C to 85°C	300 kHz	TPS40000DGQ	TPS40001DGQ	TPS40004DGQ
	600 kHz	TPS40002DGQ	TPS40003DGQ	TPS40005DGQ

(2) The DGQ package is available taped and reeled. Add R suffix to device type (e.g. TPS40000DGQR) to order quantities of 2,500 devices per reel and 80 units per tube.

(3) See Application Information section, p. 8.

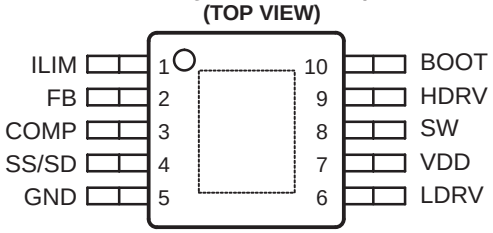
ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS4000x	UNIT
Input voltage range, V_{IN}	BOOT	V_{SW} + 6.5	V
	COMP, FB, ILIM, SS/SD	−0.3 to 6	
	SW	−0.7 to 10.5	
	SW_T (SW transient < 50 ns)	−2.5	
	VDD	6	
Operating junction temperature range, T_J		−40 to 150	°C
Storage temperature, T_{stg}		−55 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DGQ PACKAGE(4).(5)
(TOP VIEW)



ACTUAL SIZE
3,05mm x 4,98mm

(4) See technical brief SLMA002 for PCB guidelines for PowerPAD packages.
(5) PowerPAD™ heat slug can be connected to GND (pin 5).

ELECTRICAL CHARACTERISTICS

over recommended operating temperature range, T_A = −40°C to 85°C, V_{DD} = 5.0 V, all parameters measured at zero power dissipation (unless otherwise noted)

input supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input voltage range		2.25		5.5	V
V_{HGATE}	High-side gate voltage	$V_{BOOT} - V_{SW}$			5.5	V
I_{DD}	Shutdown current	SS/SD = 0 V, Outputs off		0.25	0.45	mA
	Quiescent current	FB = 0.8 V		1.4	2.0	mA
	Switching current	No load at HDRV/LDRV		1.5	4.0	mA
UVLO	Minimum on-voltage		1.95	2.05	2.15	V
	Hysteresis		80	140	200	mV

oscillator

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	TPS40000 TPS40001 TPS40004	2.25 V ≤ V_{DD} ≤ 5.00 V	250	300	350	kHz
		TPS40002 TPS40003 TPS40005		500	600	700	kHz
V_{RAMP}	Ramp voltage		$V_{PEAK} - V_{VALLEY}$	0.80	0.93	1.07	V
	Ramp valley voltage			0.24	0.31	0.41	V

PWM

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Maximum duty cycle(2)	TPS40000 TPS40001 TPS40004	FB = 0 V, V_{DD} = 3.3 V	87%	94%	97%	
		TPS40002 TPS40003 TPS40005		83%	93%	97%	
	Minimum duty cycle					0%	

error amplifier

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	FB input voltage		Line, Temperature	0.689	0.700	0.711	V
		T_A = 25°C		0.693	0.700	0.707	V
	FB input bias current				30	130	nA
V_{OH}	High-level output voltage		FB = 0 V, I_{OH} = 0.5 mA	2.0	2.5		V
V_{OL}	Low-level output voltage		FB = V_{DD}, I_{OL} = 0.5 mA		0.08	0.15	V
I_{OH}	Output source current		COMP = 0.7 V, FB = GND	2	6		mA
I_{OL}	Output sink current		COMP = 0.7 V, FB = V_{DD}	3	8		mA
G_{BW}	Gain bandwidth(1)			5	10		MHz
A_{OL}	Open loop gain			55	85		dB

(1) Ensured by design. Not production tested.
(2) At V_{DD} input voltage of 2.25 V, derate the maximum duty cycle by 3%.

ELECTRICAL CHARACTERISTICS

over recommended operating temperature range, T_A = −40°C to 85°C, V_{DD} = 5.0 V, all parameters measured at zero power dissipation (unless otherwise noted)

current limit

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SINK}	ILIM sink current	V_{DD} = 5 V	11	15	19	µA
		V_{DD} = 2.25 V	9.5	13.0	16.5	
V_{OS}	Offset voltage SW vs ILIM(1)	2.25 V ≤ V_{DD} ≤ 5.00	−20	0	20	mV
V_{ILIM}	Input voltage range		2		VDD	V
t_{ON}	Minimum HDRV pulse time in overcurrent	V_{DD} = 3.3 V		200	300	ns
	SW leading edge blanking pulse in over-current detection			100		ns
t_{SS}	Soft-start capacitor cycles as fault timer(1)			6		

rectifier zero current comparator

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SW}	Sense voltage to turn off rectifier	TPS40000 TPS40002	LDRV output OFF	−15	−7	−2	mV
	SW leading edge blanking pulse in zero current detection				75		ns

predictive delay

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SWP}	Sense threshold to modulate delay time			−350		mV
T_{LDHD}	Maximum delay modulation range time	LDRV OFF − to − HDRV ON	50	75	100	ns
	Predictive counter delay time per bit	LDRV OFF − to − HDRV ON	3.0	4.5	6.2	ns
T_{HDLD}	Maximum delay modulation range	HDRV OFF − to − LDRV ON	40	65	90	ns
	Predictive counter delay time per bit	HDRV OFF − to − LDRV ON	2.4	4.0	5.6	ns

shutdown

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SD}	Shutdown threshold voltage	Outputs OFF	0.09	0.13	0.205	V
V_{EN}	Device active threshold voltage		0.14	0.17	0.235	V

soft start

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SS}	Soft-start source current	Outputs OFF	2.0	3.7	5.4	µA
V_{SS}	Soft-start clamp voltage		1.1	1.5	1.9	V

bootstrap

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{BOOT}	Bootstrap switch resistance	V_{DD} = 3.3 V		50	100	Ω
		V_{DD} = 5 V		35	70	

(1) Ensured by design. Not production tested.

(2) At V_{DD} input voltage of 2.25 V, derate the maximum duty cycle by 3%.

ELECTRICAL CHARACTERISTICS

over recommended operating temperature range, T_A = −40°C to 85°C, V_{DD} = 5.0 V, all parameters measured at zero power dissipation (unless otherwise noted)

output driver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{HDHI}	HDRV pull-up resistance	$V_{BOOT}-V_{SW}$ = 3.3 V, I_{SOURCE} = −100 mA		3	5.5	Ω
R_{HDLO}	HDRV pull-down resistance	$V_{BOOT} - V_{SW}$ = 3.3 V, I_{SINK} = 100 mA		1.5	3	Ω
R_{LDHI}	LDRV pull-up resistance	V_{DD} = 3.3 V, I_{SOURCE} = −100 mA		3	5.5	Ω
R_{LDLO}	LDRV pull-down resistance	V_{DD} = 3.3 V, I_{SINK} = 100 mA		1.0	2.0	Ω
t_{RISE}	LDRV rise time	C_{LOAD} = 1 nF		15	35	ns
t_{FALL}	LDRV fall time	C_{LOAD} = 1 nF		10	25	ns
	HDRV rise time	C_{LOAD} = 1 nF		15	35	ns
	HDRV fall time	C_{LOAD} = 1 nF		10	25	ns

thermal shutdown

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SD}	Shutdown temperature(1)			165		°C
	Hysteresiss(1)			15		°C

sw node

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SW}	Leakage current in shutdown (1)			15		µA

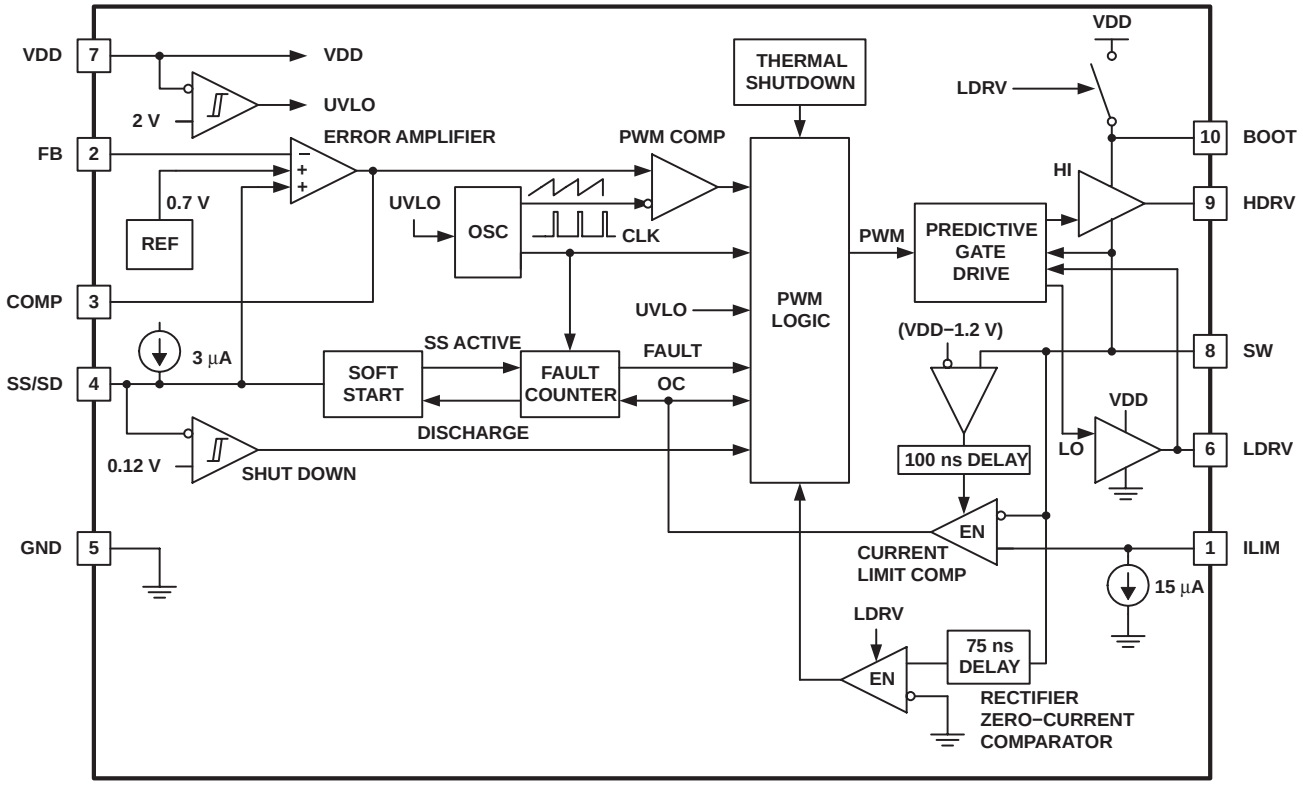
(1) Ensured by design. Not production tested.

(2) At V_{DD} input voltage of 2.25 V, derate the maximum duty cycle by 3%.

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BOOT	10	O	Provides a bootstrapped supply for the topside MOSFET driver, enabling the gate of the topside MOSFET to be driven above the input supply rail
COMP	3	O	Output of the error amplifier
FB	2	I	Inverting input of the error amplifier. In normal operation the voltage at this pin is the internal reference level of 700 mV.
GND	5	−	Power supply return for the device. The power stage ground return on the board requires a separate path from other sensitive signal ground returns.
HDRV	9	O	This is the gate drive output for the topside N-channel MOSFET. HDRV is bootstrapped to near $2\times V_{DD}$ for good enhancement of the topside MOSFET.
ILIM	1	I	A resistor is connected between this pin and VDD to set up the over current threshold voltage. A 15-µA current sink at the pin establishes a voltage drop across the external resistor that represents the drain-to-source voltage across the top side N-channel MOSFET during an over current condition. The ILIM over current comparator is blanked for the first 100 ns to allow full enhancement of the top MOSFET. Set the ILIM voltage level such that it is within 800 mV of V_{DD}; that is, $(V_{DD} - 0.8) \le I_{ILIM} \le V_{DD}$.
LDRV	6	O	Gate drive output for the low-side synchronous rectifier N-channel MOSFET
SS/SD	4	I	Soft-start and overcurrent fault shutdown times are set by charging and discharging a capacitor connected to this pin. A closed loop soft-start occurs when the internal 3-µA current source charges the external capacitor from 0.17 V to 0.70 V. During the soft-start period, the current sink capability of the TPS40001 and TPS40003 is disabled. When the SS/SD voltage is less than 0.12 V, the device is shutdown and the HDRV and LDRV are driven low. In normal operation, the capacitor is charged to 1.5 V. When a fault condition is asserted, the HDRV is driven low, and the LDRV is driven high. The soft-start capacitor goes through six charge/discharge cycles, restarting the converter on the seventh cycle.
SW	8	O	Connect to the switched node on the converter. This pin is used for overcurrent sensing in the topside N-channel MOSFET, zero current sensing in synchronous rectifier N-channel MOSFET, and level sensing for predictive delay circuit. Overcurrent is determined, when the topside N-channel MOSFET is on, by comparing the voltage on SW with respect to VDD and the voltage on the ILIM with respect to VDD. Zero current is sensed, when the rectifier N-channel MOSFET is on, by measuring the voltage on SW with respect to ground. Zero current sensing applies to the TPS40000/2 devices only.
VDD	7	I	Power input for the chip, 5.5-V maximum. Decouple close to the pin with a low-ESR capacitor, 1-µF or larger.

functional block diagram



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APPLICATION INFORMATION

The TPS4000x series of synchronous buck controller devices is optimized for high-efficiency dc-to-dc conversion in non-isolated distributed power systems. A typical application circuit is shown in Figure 1.

The TPS40004 and TPS40005 are the controllers of choice for most general purpose synchronous buck designs. Each operates in two quadrant mode (i.e. source or sink current) full time. This choice provides the best performance for output voltage load transient response over the widest load current range.

The TPS40001 and TPS40003 add an additional feature: They operate in single quadrant mode (i.e. source current only) during converter startup, and then when the converter has reached the regulation point, the controllers change to operate in two quadrant mode. This is useful for applications that have outputs pre-biased at some voltage before the controller is enabled. When the TPS40001 or TPS40003 is enabled, it does not sink current during startup and therefore does not pull current from the pre-biased voltage supply.

The TPS40000 and TPS40002 operate in single quadrant mode (source current only) full time, allowing the paralleling of converters. Single quadrant operation ensures one converter does pull current from a paralleled converter. A converter using one of these controllers emulates a non-synchronous buck converter at light loads. When current in the output inductor attempts to reverse, an internal zero-current detection circuit turns OFF the synchronous rectifier and causes the current flow in the inductor to become discontinuous. At average load currents greater than the peak amplitude of the inductor ripple current, the converter returns to operation as a synchronous buck converter to maximize efficiency.

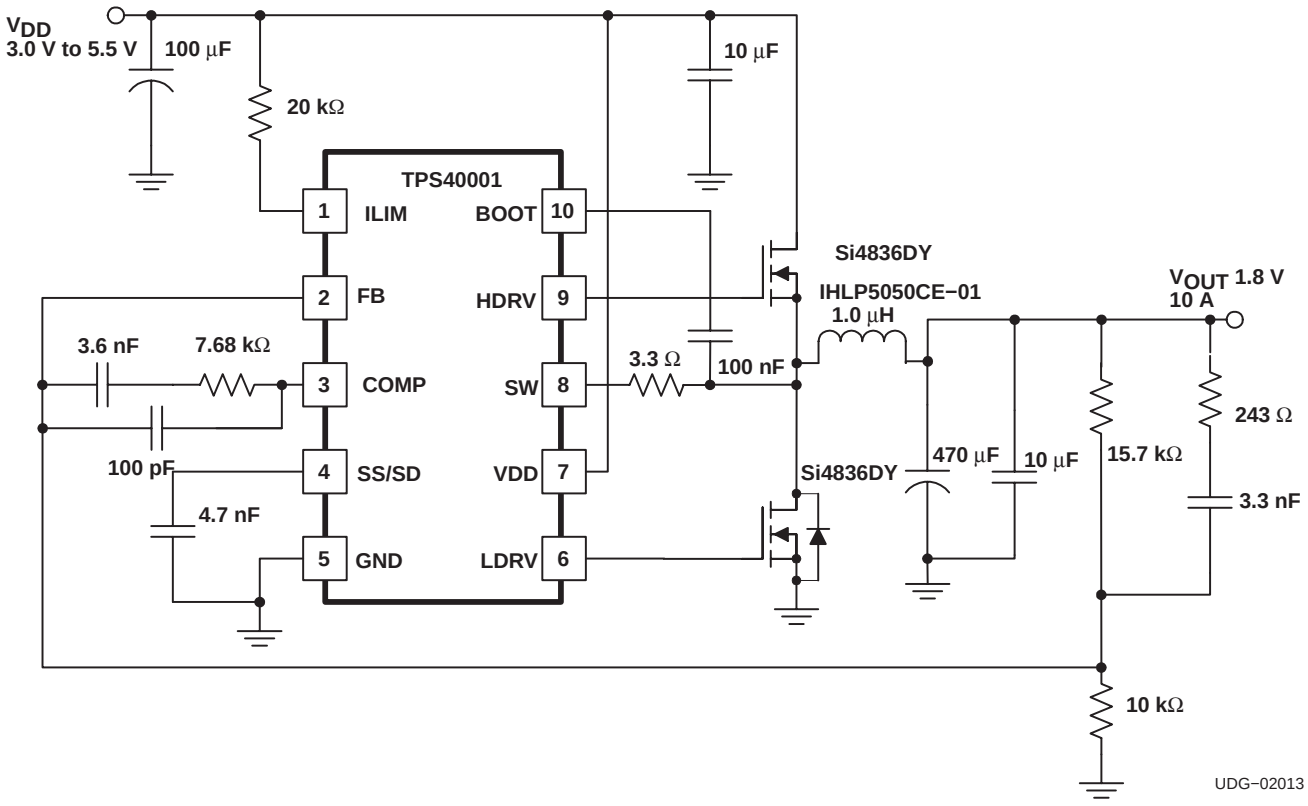


Figure 1. Typical Application Circuit

APPLICATION INFORMATION

error amplifier

The error amplifier has a bandwidth of greater than 5 MHz, with open loop gain of at least 55 dB. The COMP output voltage is clamped to a level above the oscillator ramp in order to improve large-scale transient response.

oscillator

The oscillator uses an internal resistor and capacitor to set the oscillation frequency. The ramp waveform is a triangle at the PWM frequency with a peak voltage of 1.25 V, and a valley of 0.25 V. The PWM duty cycle is limited to a maximum of 95%, allowing the bootstrap capacitor to charge during every cycle.

bootstrap/charge pump

There is an internal switch between VDD and BOOT. This switch charges the external bootstrap capacitor for the floating supply. If the resistance of this switch is too high for the application, an external schottky diode between VDD and BOOT can be used. The peak voltage on the bootstrap capacitor is approximately equal to VDD.

driver

The HDRV and LDRV MOSFET drivers are capable of driving gate-to-source voltages up to 5.5 V. At V_{IN}, = 5 V and using appropriate MOSFETs, a 20-A converter can be achieved. The LDRV driver switches between VDD and ground, while the HDRV driver is referenced to SW and switches between BOOT and SW. The maximum voltage between BOOT and SW is 5.5 V.

synchronous rectification and predictive delay

In a normal buck converter, when the main switch turns off, current is flowing to the load in the inductor. This current cannot be stopped immediately without using infinite voltage. For the current path to flow and maintain voltage levels at a safe level, a rectifier or catch device is used. This device can be either a conventional diode, or it can be a controlled active device if a control signal is available to drive it. The TPS4000x provides a signal to drive an N-channel MOSFET as a rectifier. This control signal is carefully coordinated with the drive signal for the main switch so that there is minimum delay from the time that the rectifier MOSFET turns off and the main switch turns on, and minimum delay from when the main switch turns off and the rectifier MOSFET turns on. This scheme, Predictive Gate Drive™ delay, uses information from the current switching cycle to adjust the delays that are to be used in the next cycle. Figure 2 shows the switch-node voltage waveform for a synchronously rectified buck converter. Illustrated are the relative effects of a fixed-delay drive scheme (constant, pre-set delays for the turn-off to turn-on intervals), an adaptive delay drive scheme (variable delays based upon voltages sensed on the current switching cycle) and the predictive delay drive scheme.

Note that the longer the time spent in diode conduction during the rectifier conduction period, the lower the efficiency. Also, not described in Figure 2 is the fact that the predictive delay circuit can prevent the body diode from becoming forward biased at all while at the same time avoiding cross conduction or shoot through. This results in a significant power savings when the main MOSFET turns on, and minimizes reverse recovery loss in the body diode of the rectifier MOSFET.

APPLICATION INFORMATION

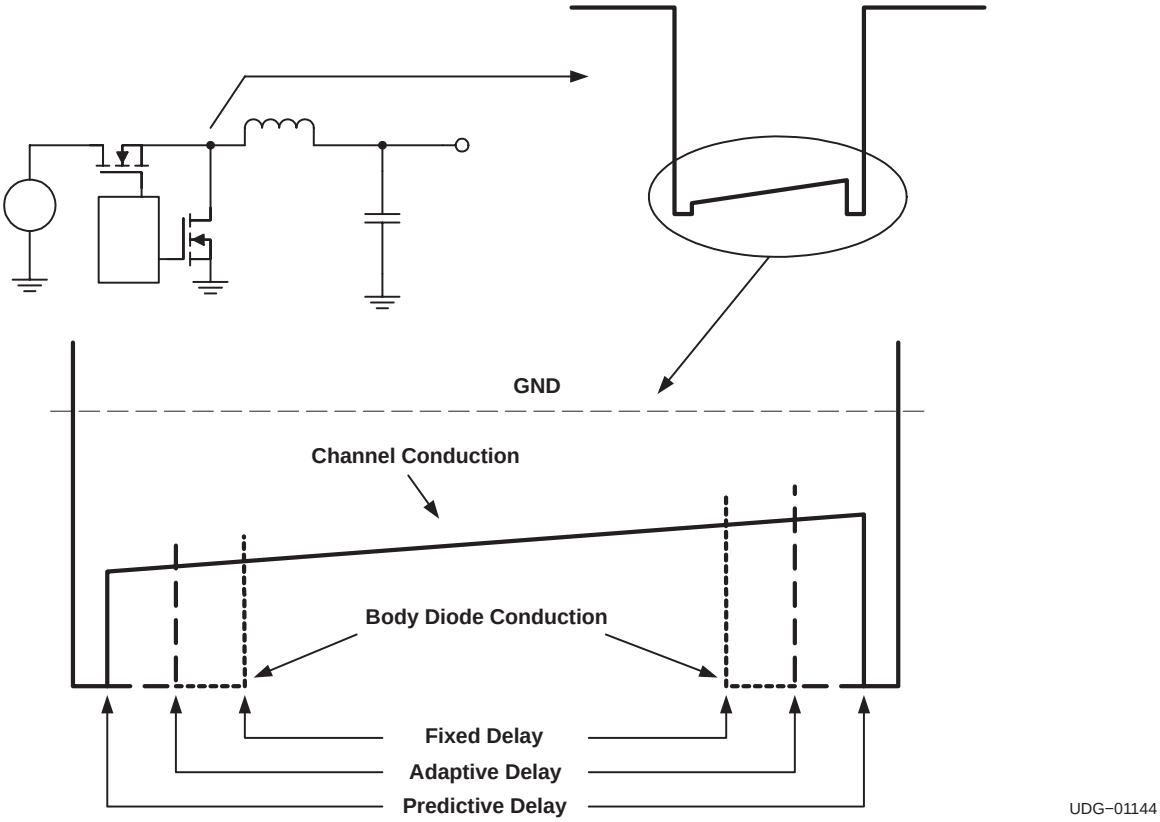


Figure 2. Switch Node Waveforms for Synchronous Buck Converter

overcurrent

Overcurrent conditions in the TPS4000x are sensed by detecting the voltage across the main MOSFET while it is on.

basic description

If the voltage exceeds a pre-set threshold, the current pulse is terminated, and a counter inside the device is incremented. If this counter fills up, a fault condition is declared and the device disables switching for a period of time and then attempts to restart the converter with a full soft-start cycle.

APPLICATION INFORMATION

detailed description

During each switching cycle, a comparator looks at the voltage across the top side MOSFET while it is on. This comparator is enabled after the SW node reaches a voltage greater than (V_{DD}−1.2 V) followed by a 100-ns blanking time. If the voltage across that MOSFET exceeds a programmable threshold voltage, the current-switching pulse is terminated and a 3-bit counter is incremented by one count. If, during the switching cycle, the topside MOSFET voltage does not exceed a preset threshold, then this counter is decremented by one count. (The counter does not wrap around from 7 to 0 or from 0 to 7). If the counter reaches a full count of 7, the device declares that a fault condition exists at the output of the converter. In this fault state, HDRV is turned off and LDRV is turned on and the soft-start capacitor is discharged. The counter is decremented by one by the soft start capacitor (C_{SS}) discharge. When the soft-start capacitor is fully discharged, the discharging circuit is turned off and the capacitor is allowed to charge up at the nominal charging rate. When the soft-start capacitor reaches about 700 mV, it is discharged again and the overcurrent counter is decremented by one count. The capacitor is charged and discharged, and the counter decremented until the count reaches zero (a total of six times). When this happens, the outputs are again enabled as the soft-start capacitor generates a reference ramp for the converter to follow while attempting to restart.

During this soft-start interval (whether or not the controller is attempting to do a fault recovery or starting for the first time), pulse-by-pulse current limiting is in effect, but overcurrent pulses are not counted to declare a fault until the soft-start cycle has been completed. It is possible to have a supply attempt to bring up a short circuit for the duration of the soft start period plus seven switching cycles. Power stage designs should take this into account if it makes a difference thermally. Figure 3 shows the details of the overcurrent operation.

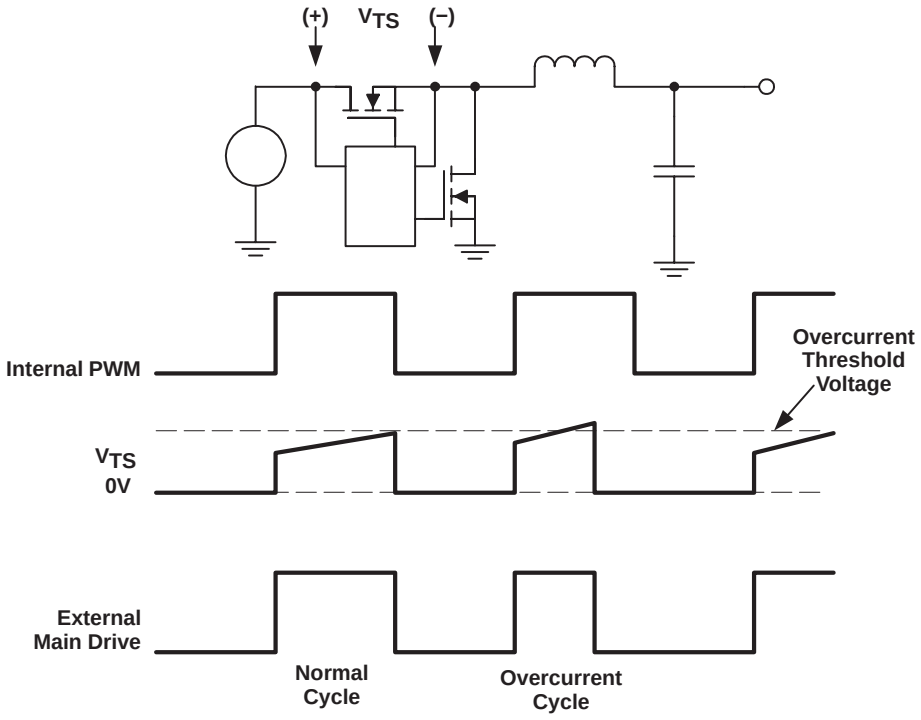


Figure 3. Switch Node Waveforms for Synchronous Buck Converter

APPLICATION INFORMATION

Figure 4 shows the behavior of key signals during initial startup, during a fault and a successfully fault recovery. At time t0, power is applied to the converter. The voltage on the soft-start capacitor (V_{CSS}) begins to ramp up and acts as the reference until it passes the internal reference voltage at t1. At this point the soft-start period is over and the converter is regulating its output at the desired voltage level. From t0 to t1, pulse-by-pulse current limiting is in effect, and from t1 onward, overcurrent pulses are counted for purposes of determining a possible fault condition. At t2, a heavy overload is applied to the converter. This overload is in excess of the overcurrent threshold. The converter starts limiting current and the output voltage falls to some level depending on the overload applied. During the period from t2 to t3, the counter is counting overcurrent pulses, and at time t3 reaches a full count of 7. The soft-start capacitor is then discharged, the counter is decremented, and a fault condition is declared.

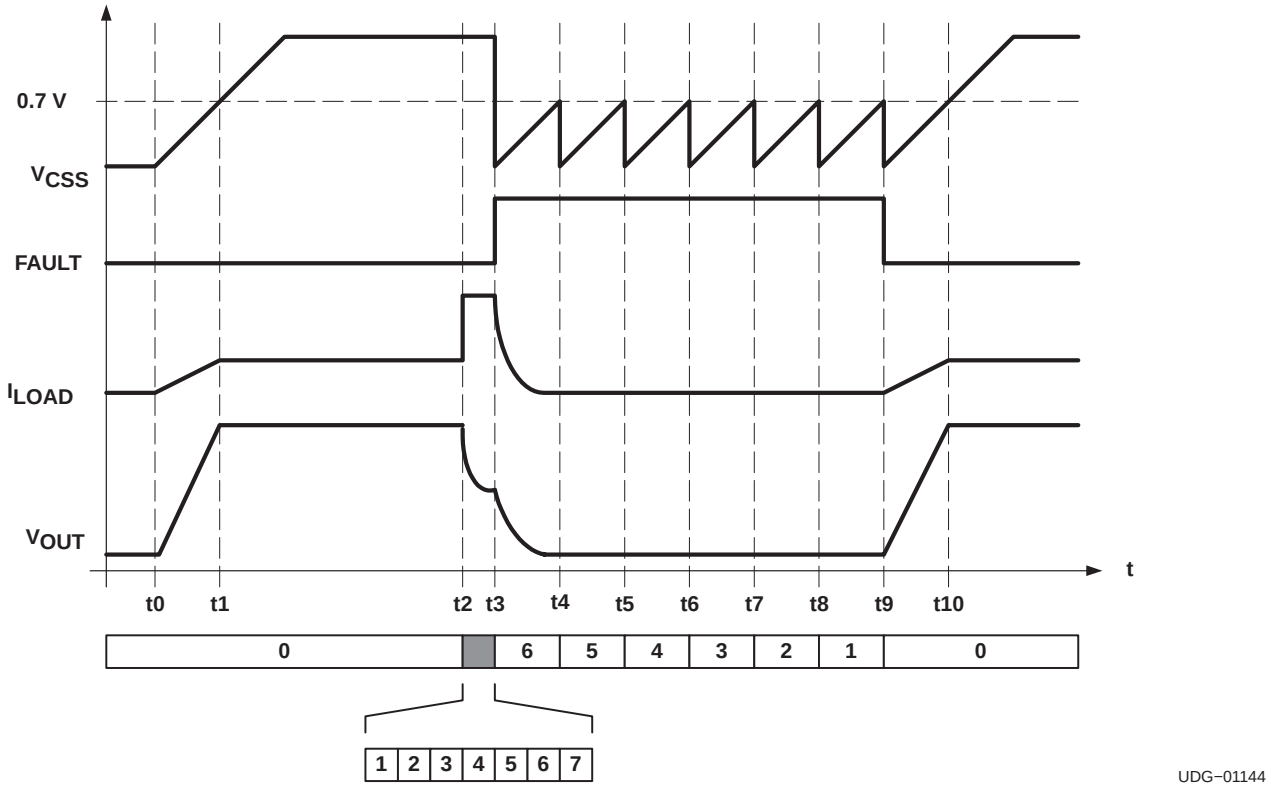


Figure 4. Switch Node Waveforms for Synchronous Buck Converter

When the soft start capacitor is fully discharged, it begins charging again at the same rate that it does on startup, with a nominal 3-µA current source. As the capacitor voltage reaches full charge, it is discharged again and the counter is decremented by one count. These transitions occur at t3 through t9. At t9, the counter has been decremented to 0. The fault logic is then cleared, the outputs are enabled, and the converter attempts to restart with a full soft-start cycle. The converter comes into regulation at t10.

APPLICATION INFORMATION

setting the current limit

Connecting a resistor from VDD to ILIM sets the current limit. A 15-µA current sink internal to the device causes a voltage drop at ILIM that is equal to the overcurrent threshold voltage. Ensure that $(V_{DD}-0.8\ V) \leq V_{ILIM} \leq V_{DD}$. The tolerance of the current sink is too loose to do an accurate current limit. The main purpose is for hard fault protection of the power switches. Given the tolerance of the ILIM sink current, and the $R_{DS(on)}$ range for a MOSFET, it is generally possible to apply a load that thermally damages the converter. This device is intended for embedded converters where load characteristics are defined and can be controlled.

soft-start and shutdown

These two functions are common to the SS/SD pin. The voltage at this pin is the controlling voltage of the error amplifier during startup. This reduces the transient current required to charge the output capacitor at startup, and allows for a smooth startup with no overshoot of the output voltage if done properly. A shutdown feature can be implemented as shown in Figure 5.

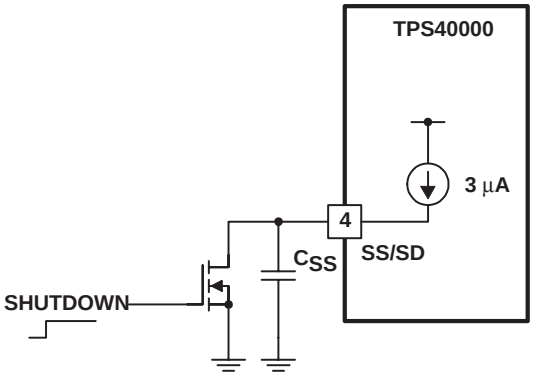


Figure 5. Shutdown Implementation

The device shuts down when the voltage at the SS/SD pin falls below 120 mV. Because of this limitation, it is recommended that a MOSFET be used as the controlling device, as in Figure 5. An open-drain CMOS logic output would work equally well.

rectifier zero-current

Both the TPS40000 and TPS40002 parts are source-only, thus preventing reverse current in the synchronous rectifier. Synchronous rectification is terminated by sensing the voltage, SW with respect to ground, across the low-side MOSFET. When SW node is greater than −7 mV, rectification is terminated and stays off until the next PWM cycle. In order to filter out undesired noise on the SW node, the zero-current comparator is blanked for 75 ns from the time the rectifier is turned on.

The TPS40001 and TPS40003 parts enable the zero-current comparator, (and therefore prevent reverse current), while soft-start is active. However, when the output reaches regulation; that is, at the end of the soft-start time, this comparator is disabled to allow the synchronous rectifier to sink current.

APPLICATION INFORMATION

The following pages include design ideas for a few applications. For more ideas, detailed design information, and helpful hints, visit the TPS40000 resources at http://power.ti.com.

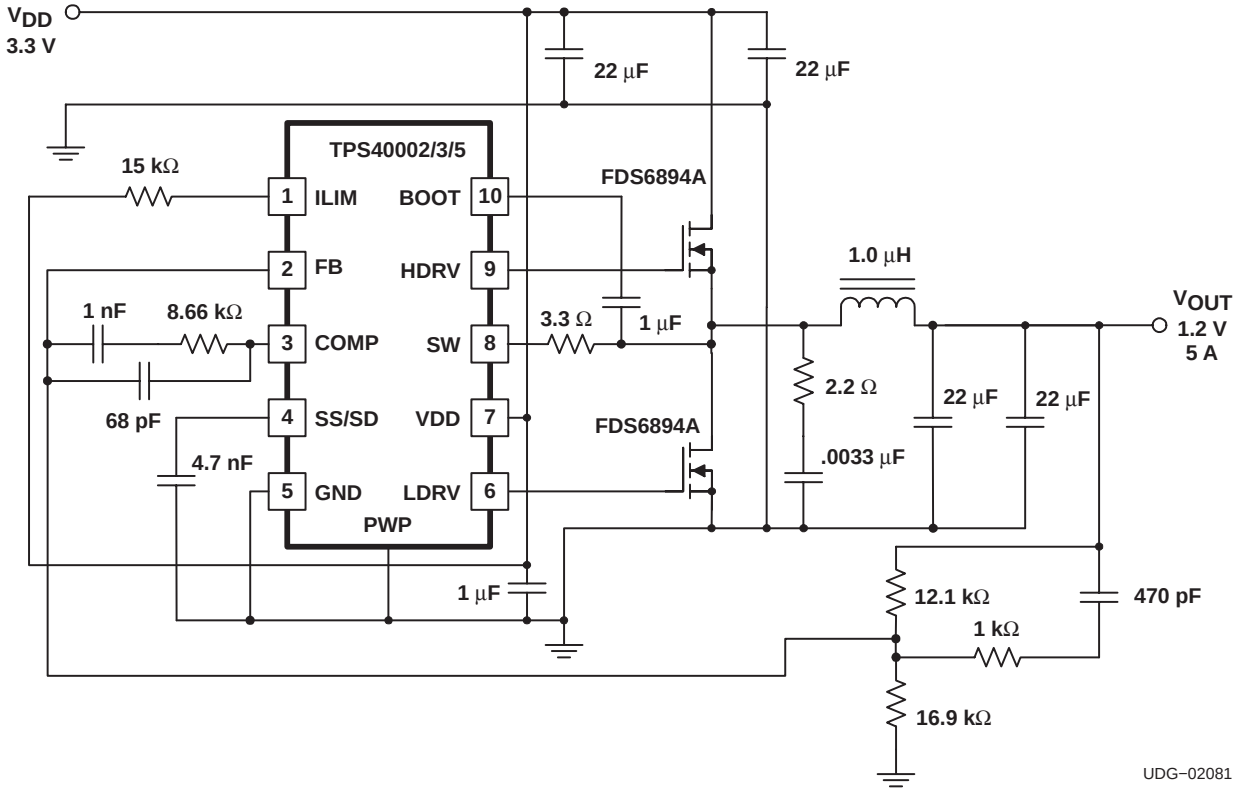


Figure 6. Small-Form Factor Converter for 3.3 V to 1.2 V at 5 A.

APPLICATION INFORMATION

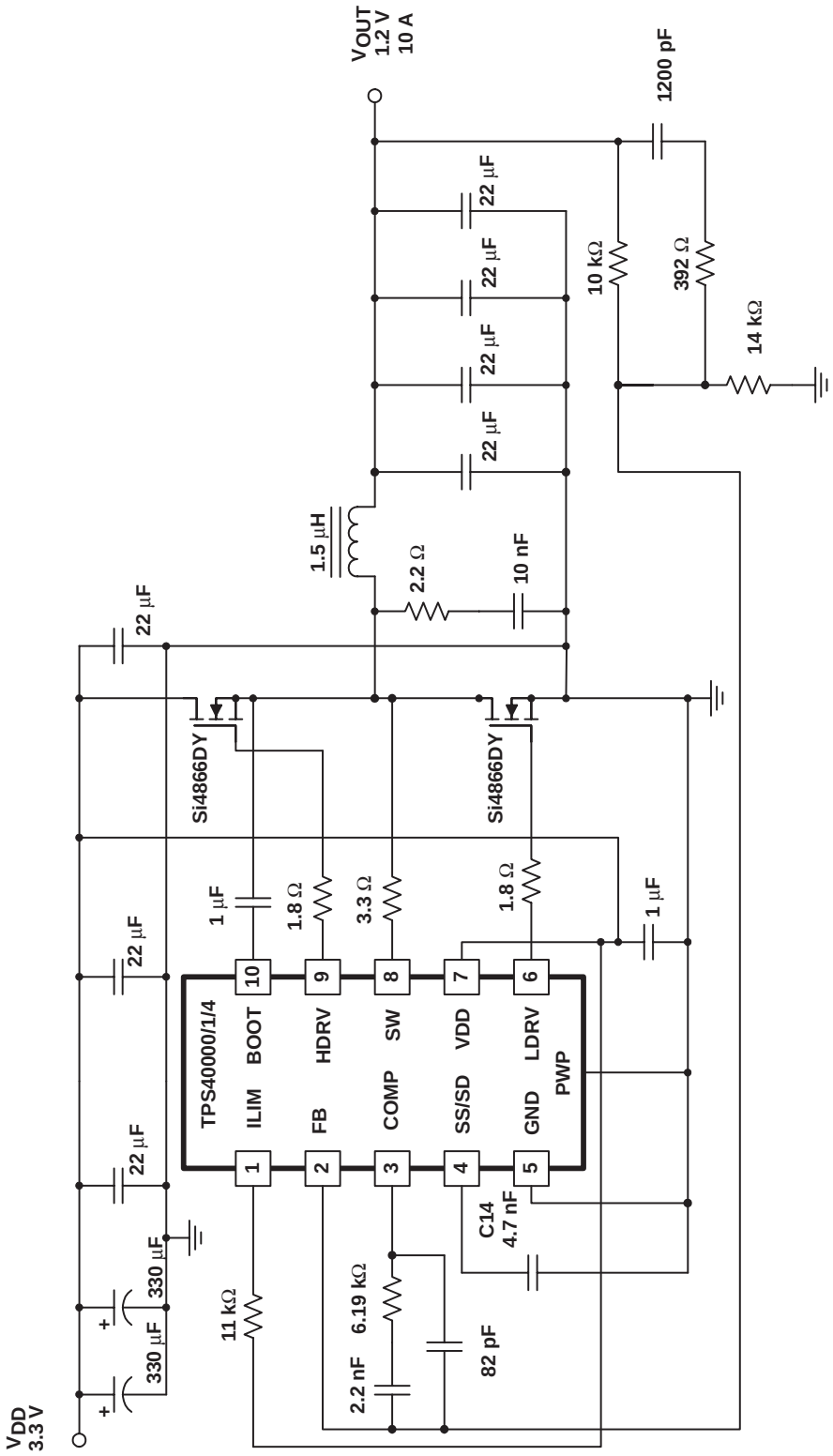


Figure 7. High-Current Converter for 3.3 V to 1.2 V at 10 A.

APPLICATION INFORMATION

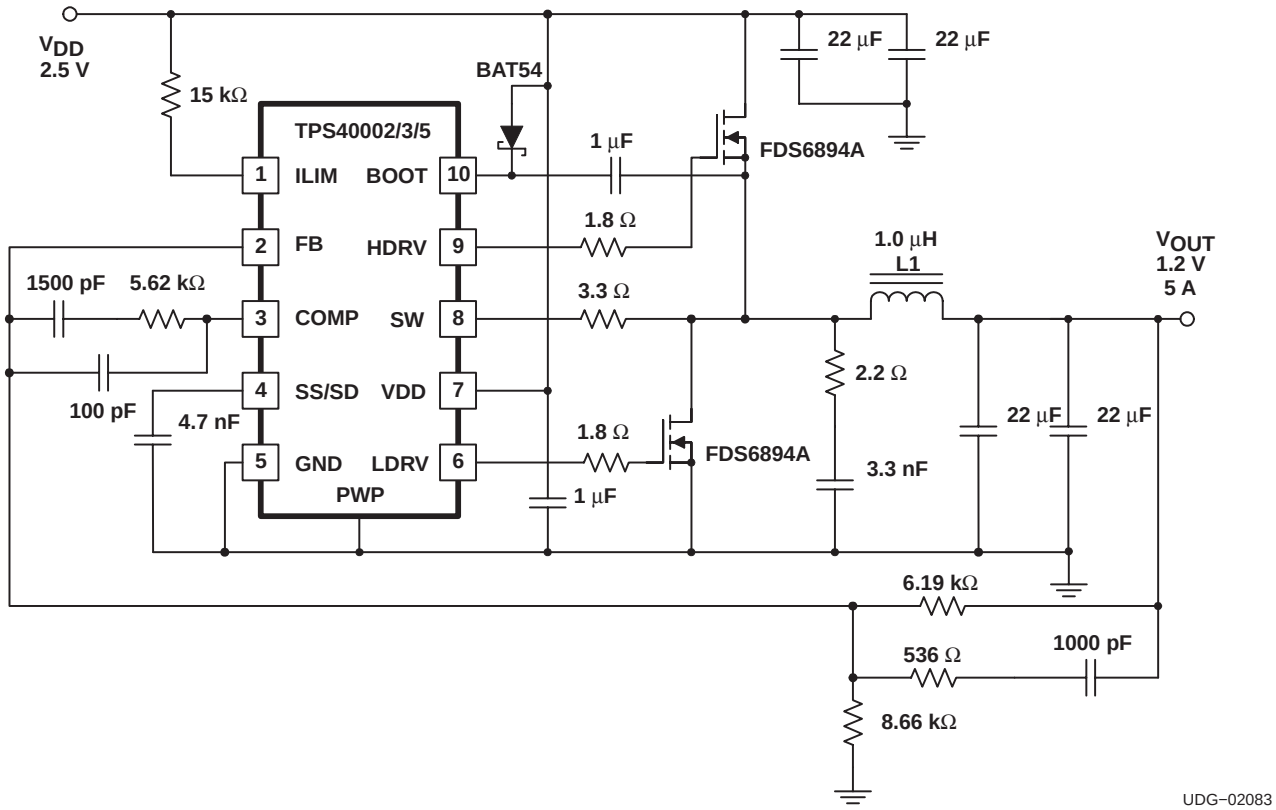


Figure 8. Ultra-Low-Input Voltage Converter for 2.5 V to 1.2 V at 5 A

APPLICATION INFORMATION

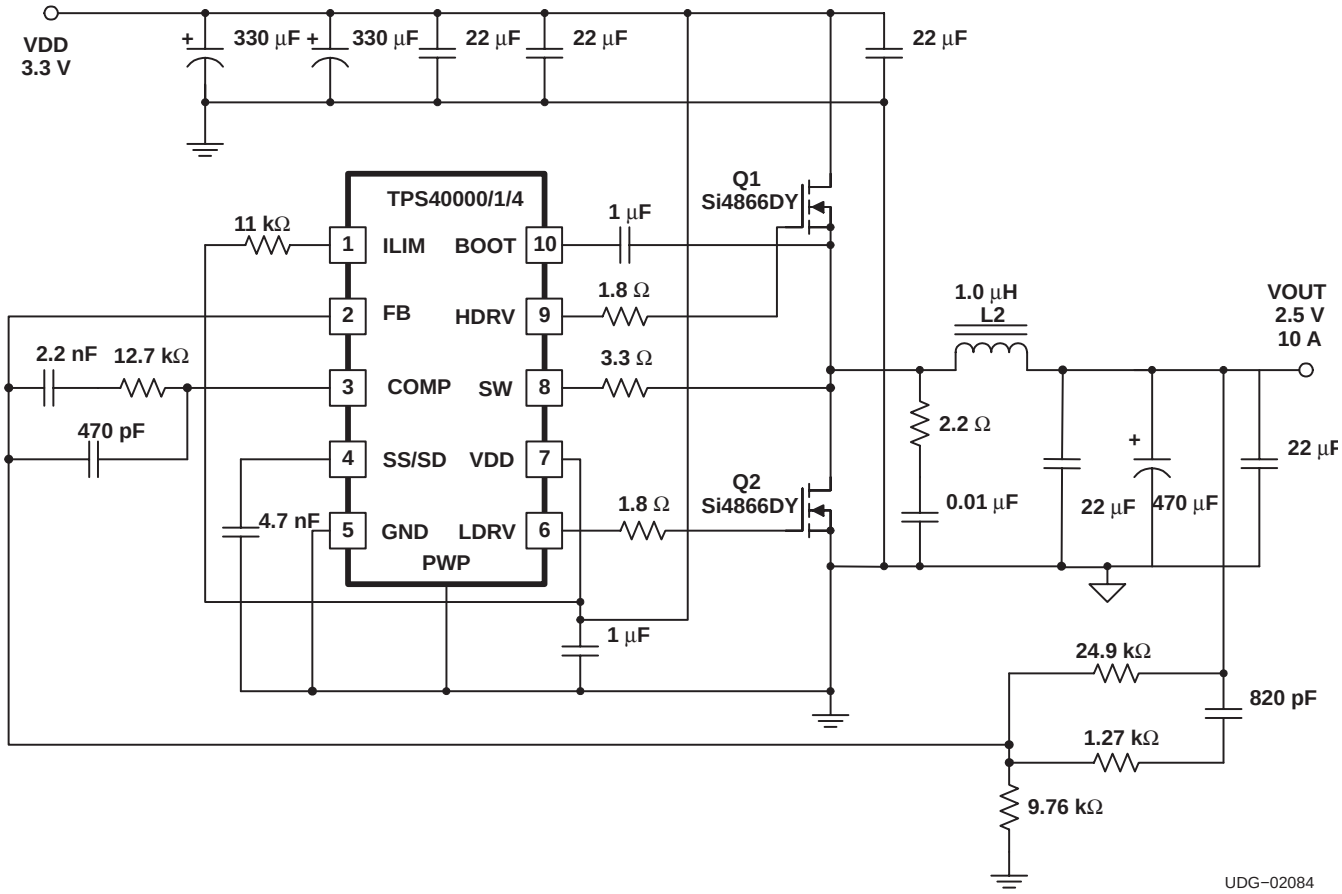


Figure 9. Ultra-High-Efficiency Converter for 3.3 V to 2.5 V at 10 A

TYPICAL CHARACTERISTICS

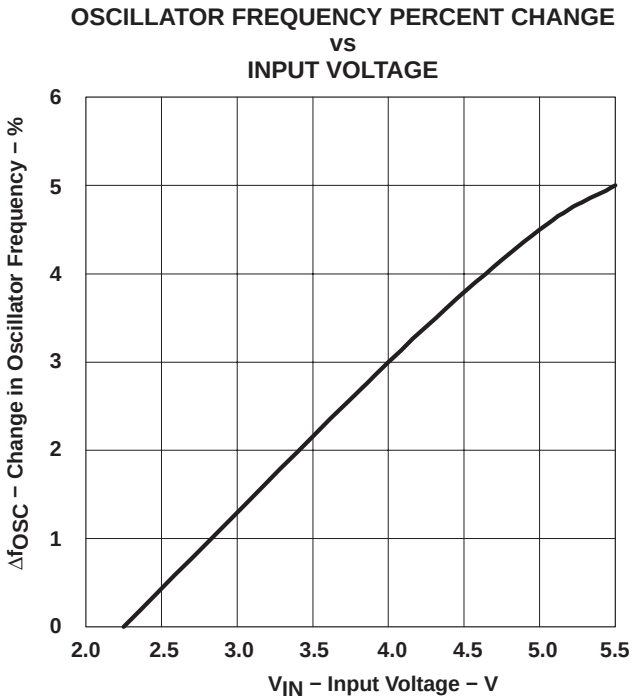


Figure 10

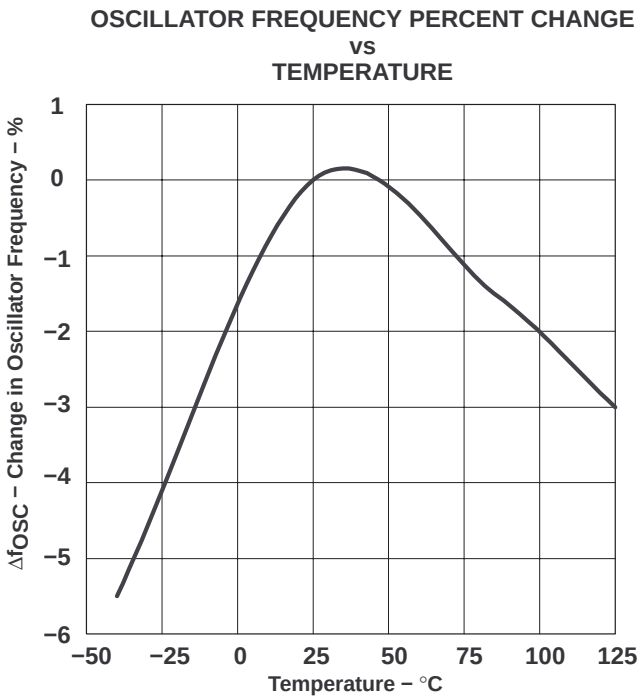


Figure 11

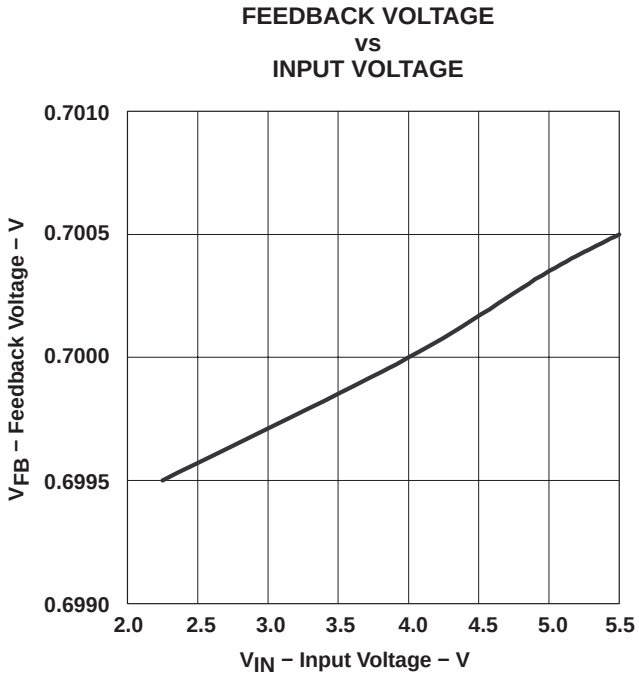


Figure 12

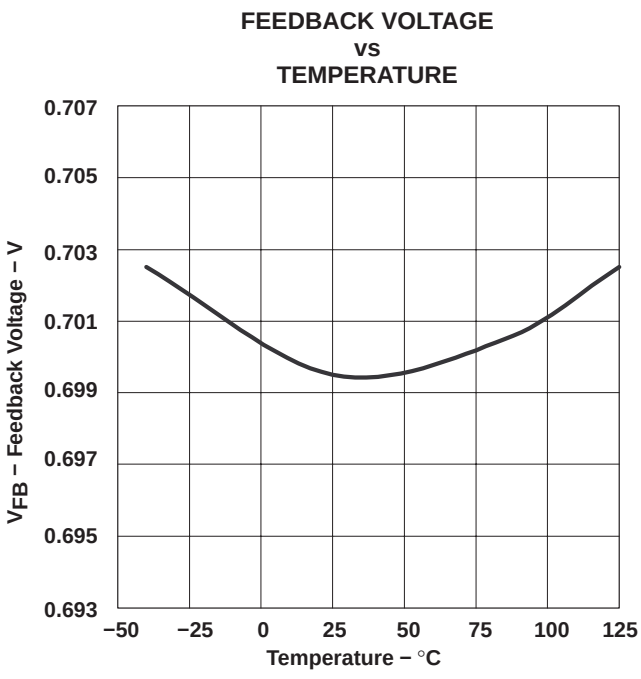


Figure 13

TYPICAL CHARACTERISTICS

CURRENT LIMIT SINK CURRENT vs INPUT VOLTAGE

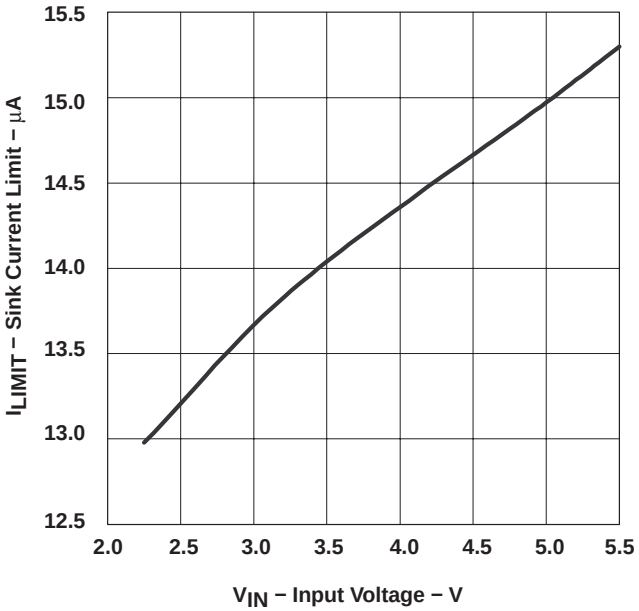


Figure 14

CURRENT LIMIT SINK CURRENT vs TEMPERATURE

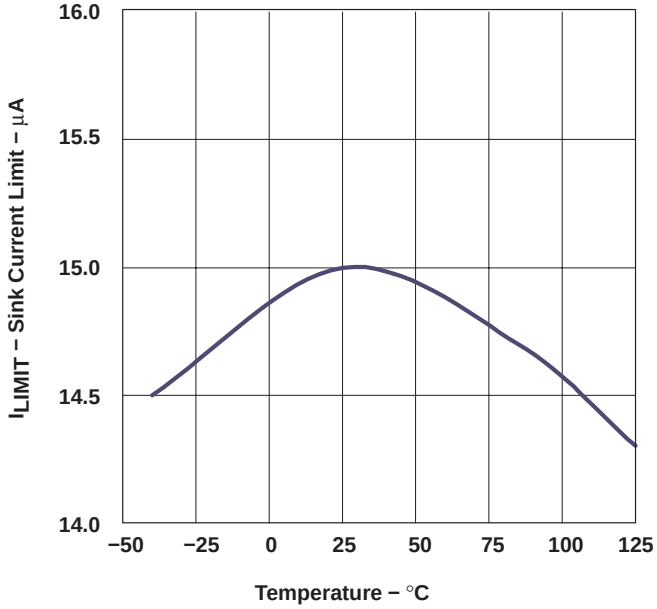


Figure 15

OVERCURRENT

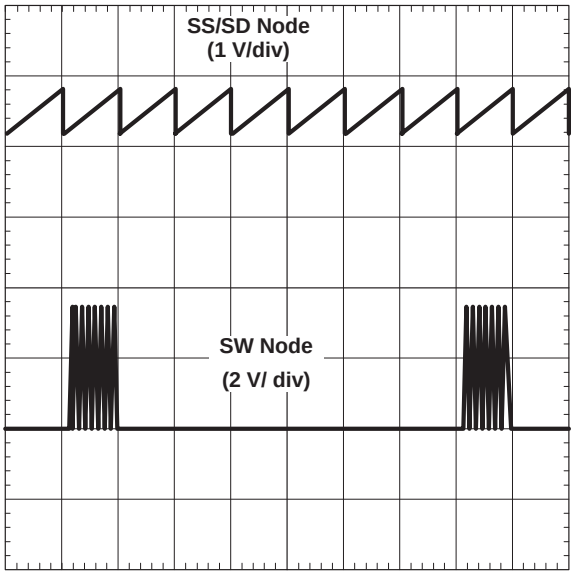


Figure 16

TYPICAL PREDICTIVE DELAY SWITCHING

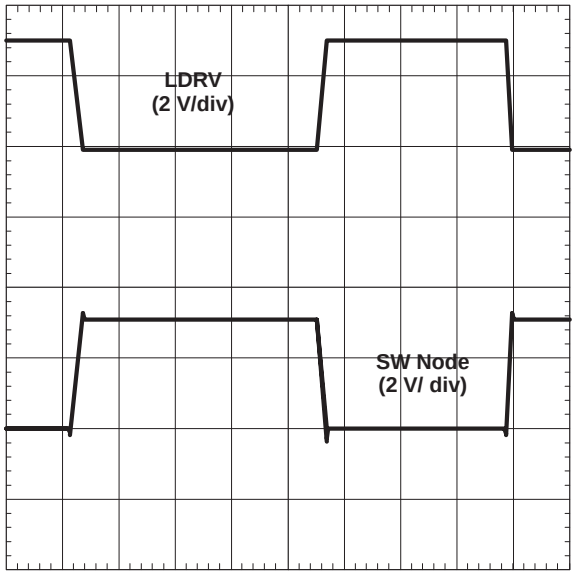


Figure 17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40000DGQ	ACTIVE	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40000	Samples
TPS40000DGQG4	ACTIVE	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40000	Samples
TPS40000DGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40000	Samples
TPS40001DGQ	NRND	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	40001	
TPS40001DGQR	NRND	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40001	
TPS40001DGQRG4	NRND	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40001	
TPS40002DGQ	NRND	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	40002	
TPS40002DGQR	NRND	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	40002	
TPS40003DGQ	NRND	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	40003	
TPS40003DGQG4	NRND	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	40003	
TPS40003DGQR	NRND	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40003	
TPS40005DGQR	NRND	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	40005	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

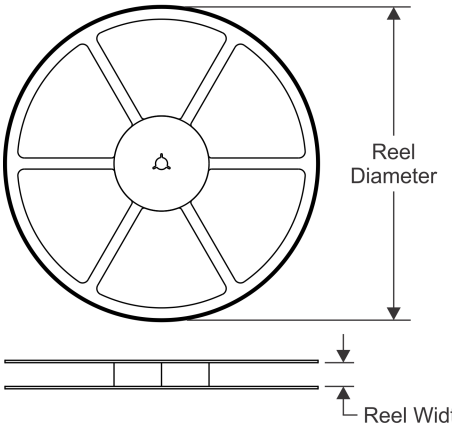
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

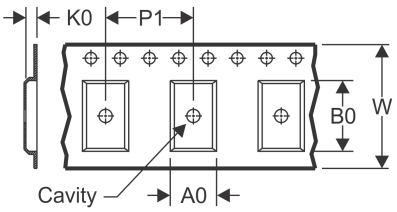
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

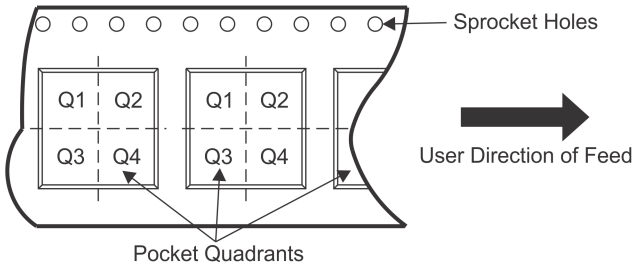


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

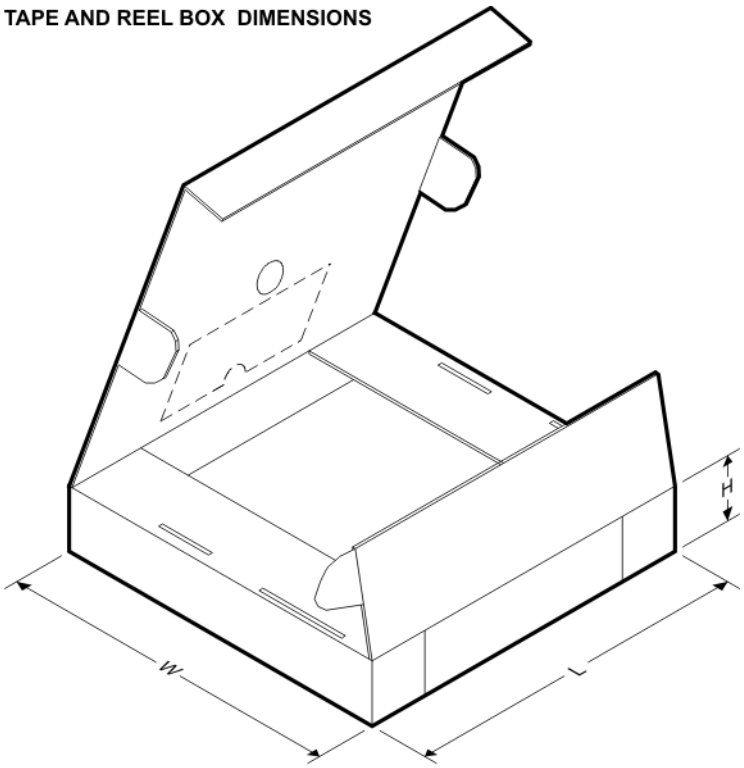
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40000DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS40001DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS40002DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS40003DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS40005DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40000DGQR	HVSSOP	DGQ	10	2500	346.0	346.0	35.0
TPS40001DGQR	HVSSOP	DGQ	10	2500	367.0	367.0	38.0
TPS40002DGQR	HVSSOP	DGQ	10	2500	346.0	346.0	35.0
TPS40003DGQR	HVSSOP	DGQ	10	2500	367.0	367.0	38.0
TPS40005DGQR	HVSSOP	DGQ	10	2500	346.0	346.0	35.0

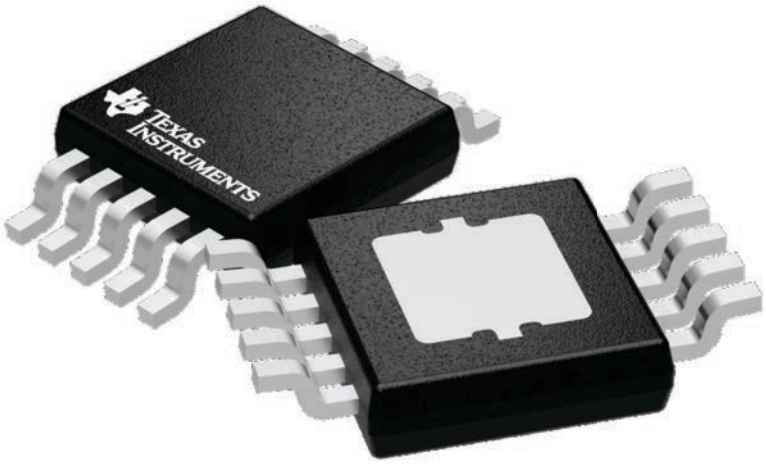
GENERIC PACKAGE VIEW

DGQ 10

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

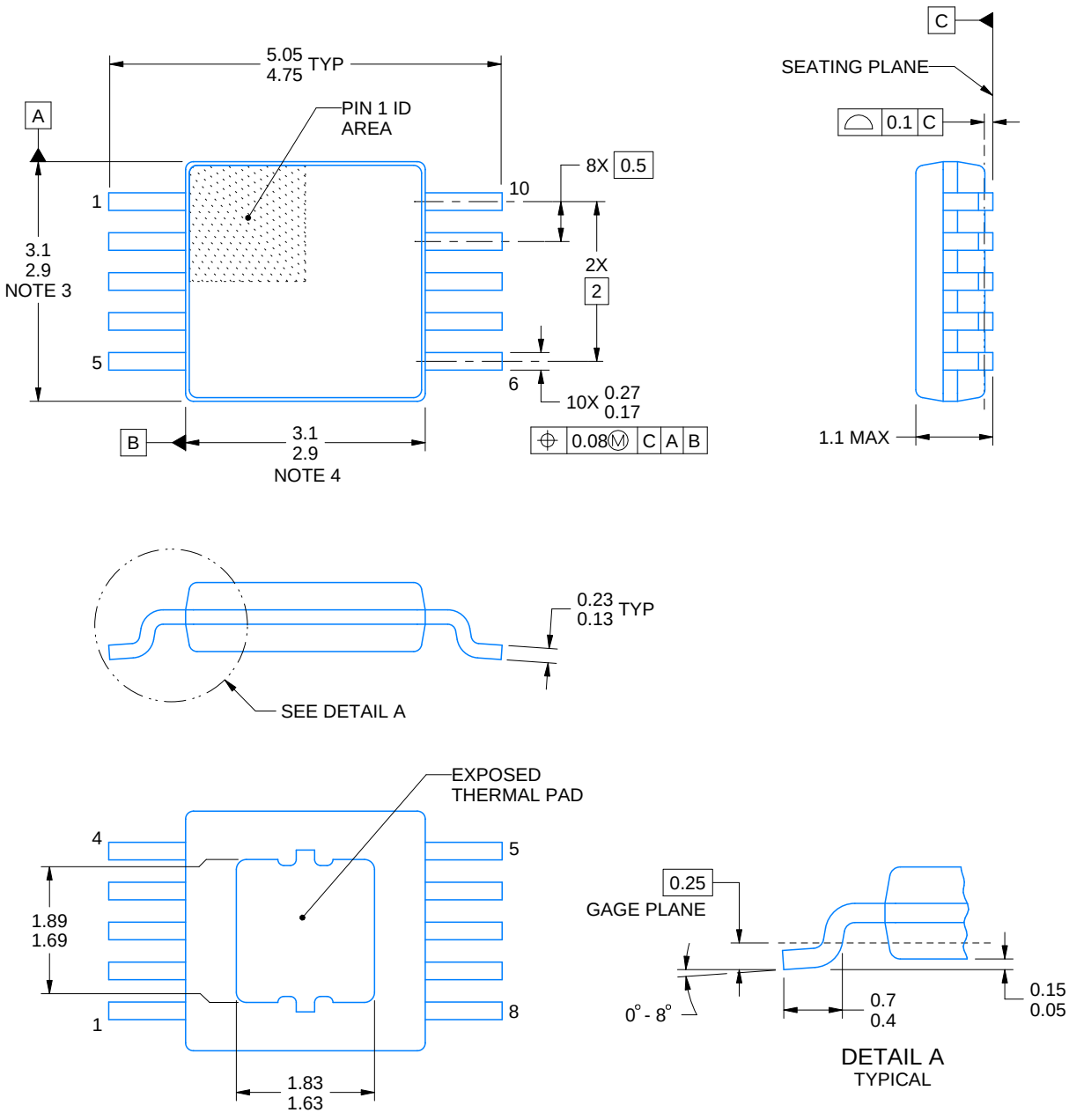
4224775/A

PACKAGE OUTLINE

DGQ0010D

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE

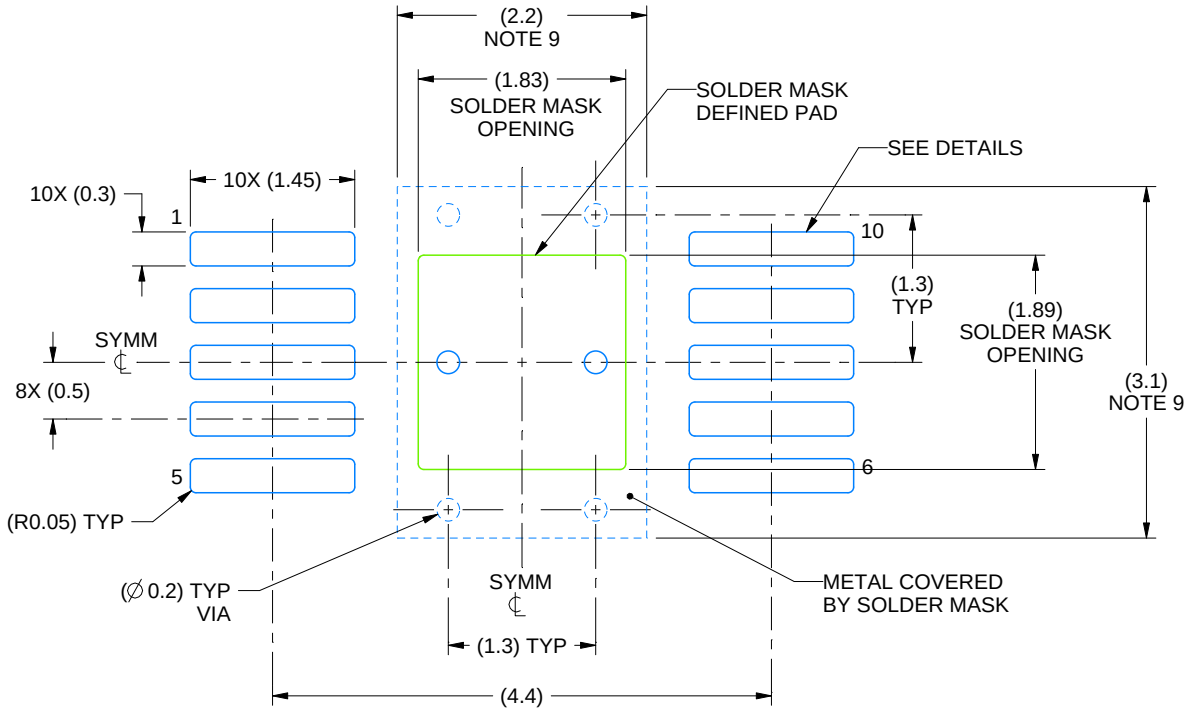


4218842/A 01/2019

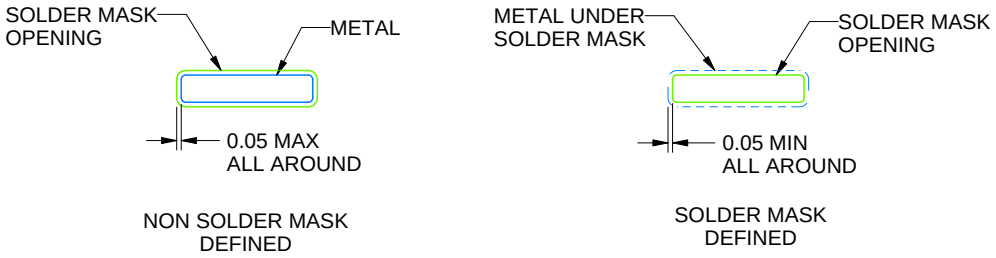
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
SCALE:15X

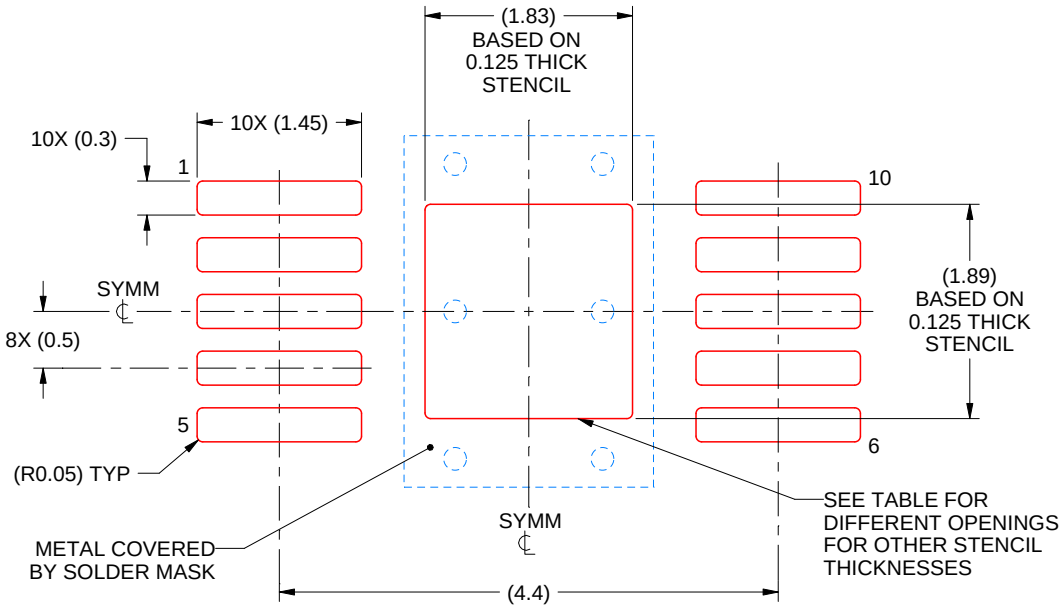


SOLDER MASK DETAILS

4218842/A 01/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.11
0.125	1.83 X 1.89 (SHOWN)
0.150	1.67 X 1.73
0.175	1.55 X 1.60

4218842/A 01/2019

NOTES: (continued)

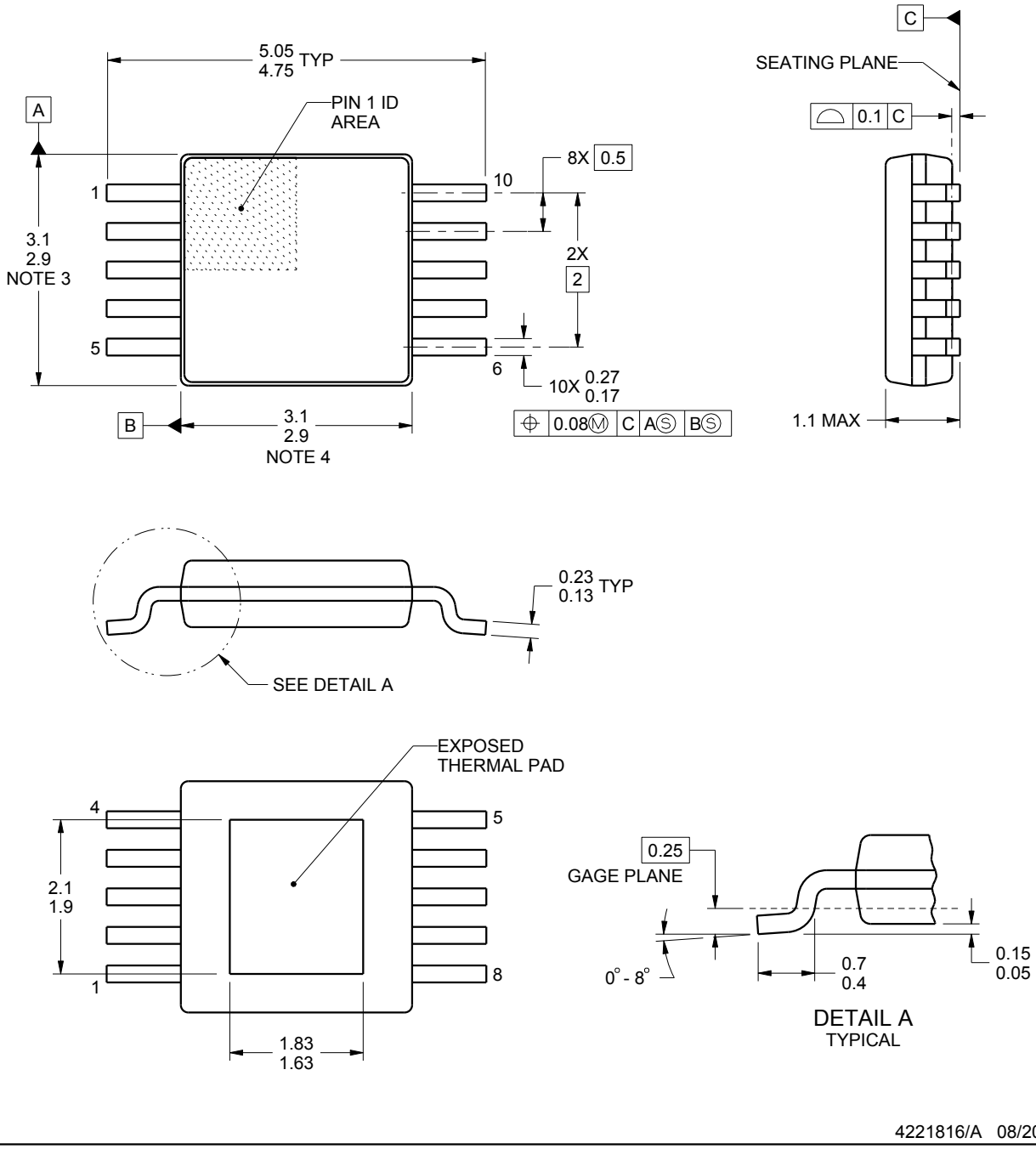
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGQ0010E

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE

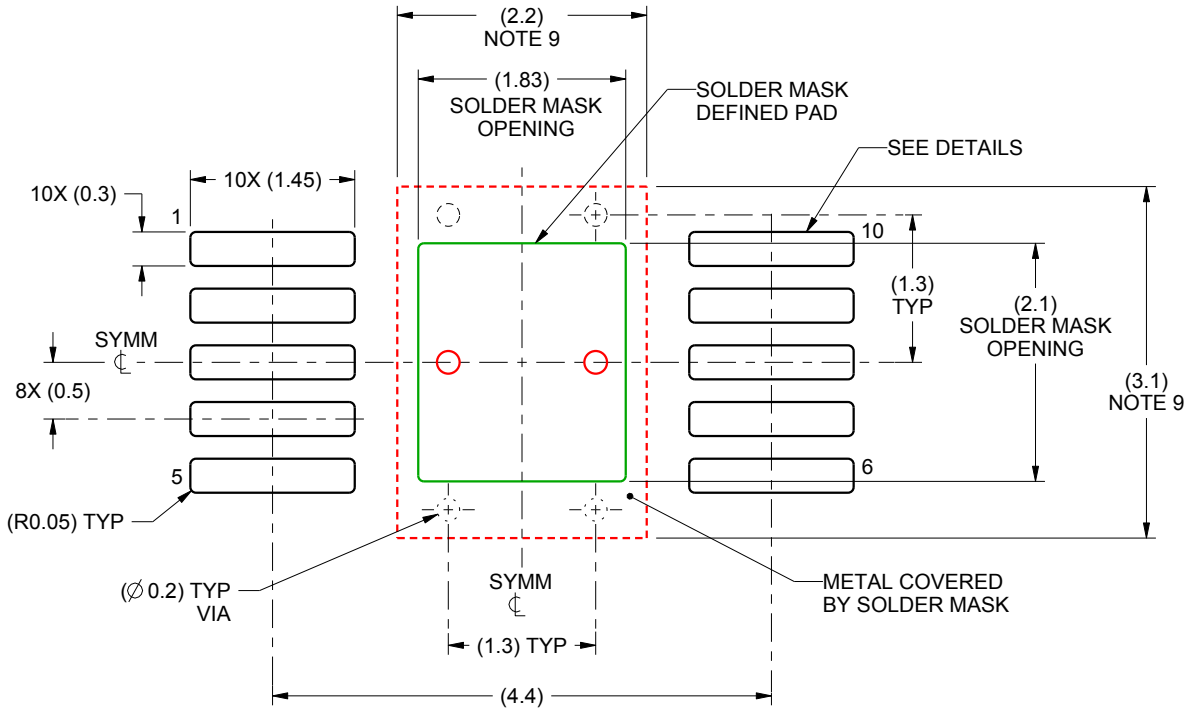


4221816/A 08/2015

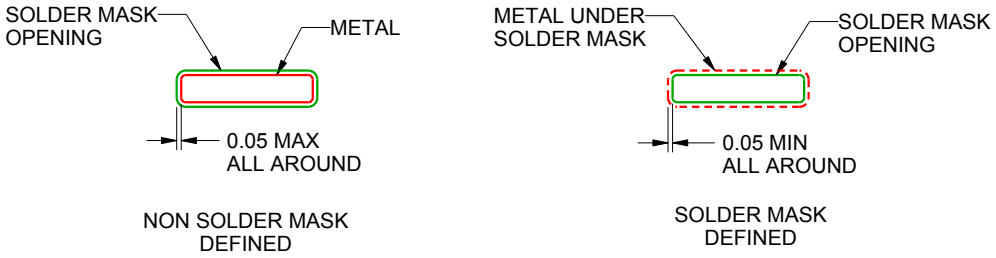
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
SCALE:15X

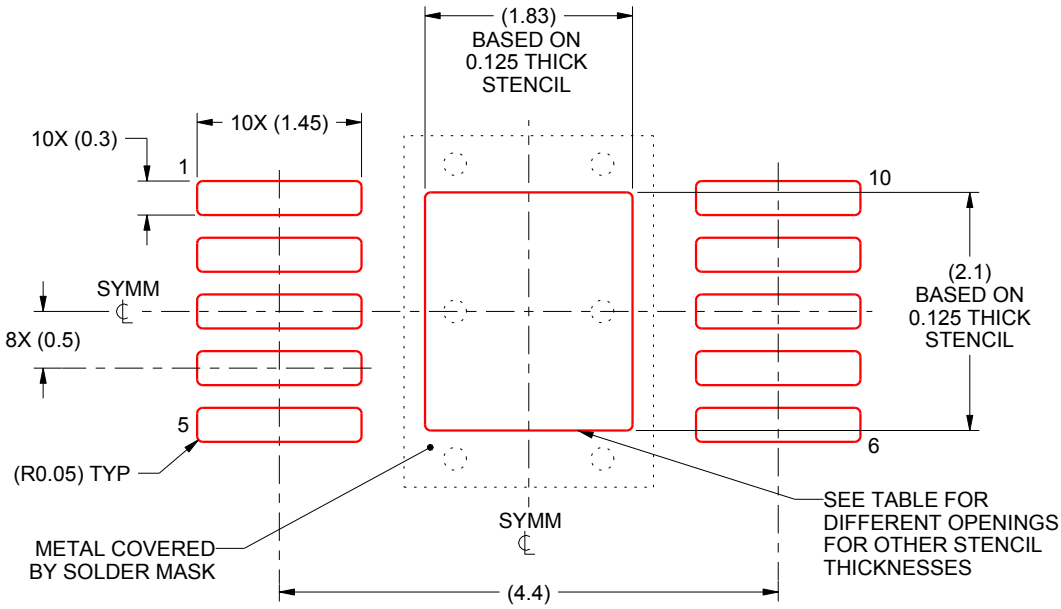


SOLDER MASK DETAILS

4221816/A 08/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.35
0.125	1.83 X 2.1 (SHOWN)
0.150	1.67 X 1.92
0.175	1.55 X 1.77

4221816/A 08/2015

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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