

具有集成开关的 6A 降压稳压器

查询样品: [TPS53314](#)

特性

- 转换输入电压范围: **3 V 至 15 V**
- **VDD** 输入电压范围: **4.5 V 至 25 V**
- 输出电压范围: **0.6 V 至 5.5 V**
- **5V LDO** 输出
- 具有 **6A** 连续输出电流的集成功率 **MOSFET**
- **<10 μ A** 停机电流
- 用于提高轻负载效率的 **Auto-Skip Eco-mode™**
- 具有快速瞬态响应的 **D-CAP™** 模式
- 可利用一个外部电阻器在 **250 kHz 至 1 MHz** 的范围内选择开关频率
- 内置 **1%、0.6V** 基准
- **0.7-ms、1.4-ms、2.8-ms** 和 **5.6-ms** 可选内部电压伺服软启动
- 预充电启动能力
- 集成型升压开关
- 可通过外部电阻器来调节过流限值
- 过压/欠压、**UVLO** 和过热保护
- 支持全陶瓷输出电容器
- 漏极开路电源状态良好指示
- 采用 **PowerPAD™** 的 **40 引脚 QFN** 封装

应用

- 服务器和台式计算机
- 笔记本电脑
- 电信设备

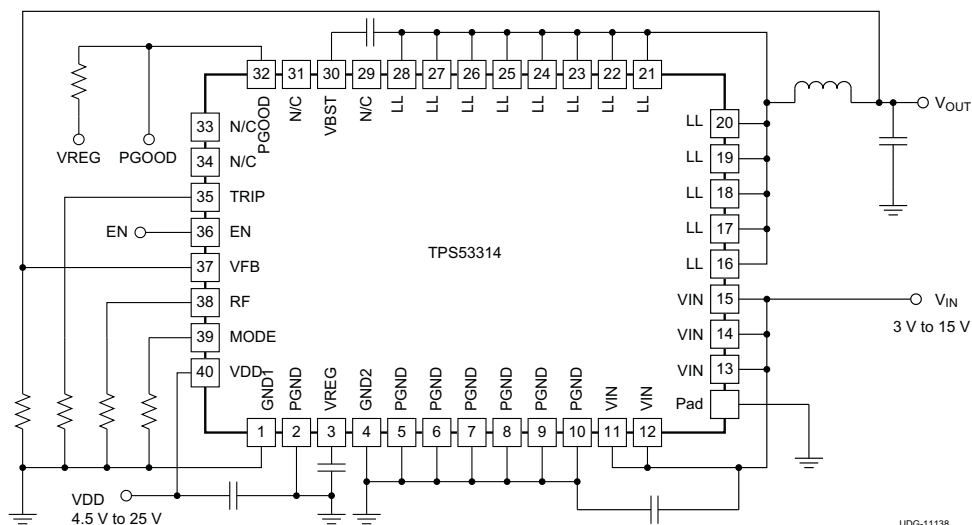
说明

TPS53314 是一款具有集成型 MOSFET 的 D-CAP™ 模式、6A 同步开关。该器件专为实现易用性、低外部组件数和小封装电源系统而设计。

该器件具有单轨输入支持能力、一个 20-m Ω 和一个 7.5-m Ω 集成型 MOSFET、1% 准确度、0.6 V 基准以及集成型升压开关。部分具有竞争力的特性包括: > 96% 的最大效率、3 V 至 15 V 的宽输入电压范围、超低的外部组件数、用于实现超快瞬态响应的 D-CAP™ 模式控制、可选的自动跳跃和 PWM 操作方式、内部软启动控制、可调频率且无需补偿。

转换输入电压范围为 3 V 至 15 V，电源电压范围为 4.5 V 至 25 V，而输出电压范围则为 0.6 V 至 5.5 V。

TPS53314 采用 5 mm $\times$ 7 mm 40 引脚 QFN 封装，并具有 -40°C 至 85°C 的规定温度范围。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Eco-mode, D-CAP, PowerPAD are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

版权 © 2011, Texas Instruments Incorporated
English Data Sheet: [SLUSAK3](#)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE	ORDERING NUMBER	PINS	TRANSPORT MEDIA	MINIMUM QUANTITY	ECO PLAN
–40°C to 85°C	Plastic QFN (RGF)	TPS53314RGFR	40	Tape and reel	3000	Green (RoHS and no Pb/Br)
		TPS53314RGFT	40	Mini reel	250	

- (1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

			VALUE	UNIT
Input voltage range	VIN (main supply)		–0.3 to 17	V
	VDD		–0.3 to 28	
	VBST		–0.3 to 24	
	VBST(with respect to LL)		–0.3 to 7	
	EN, TRIP, VFB, RF, MODE		–0.3 to 7	
Output voltage range	LL	DC	–1 to 23	V
		Pulse < 20 ns, E = 5 μJ	–7	
	PGOOD, VREG		–0.3 to 7	
	PGND		–0.3 to 0.3	
Source/Sink Current	VBST		50	mA
Operating free-air temperature, T _A			–40 to 85	°C
Storage temperature range, T _{stg}			–55 to 150	°C
Junction temperature range, T _J			–40 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			300	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TPS53314	UNITS
		RGF(40 PINS)	
θ _{JA}	Junction-to-ambient thermal resistance	35.8	°C/W
θ _{JCTop}	Junction-to-case (top) thermal resistance	23.8	
θ _{JB}	Junction-to-board thermal resistance	10.1	
ψ _{JT}	Junction-to-top characterization parameter	0.4	
ψ _{JB}	Junction-to-board characterization parameter	10.0	
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	2.8	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com).

RECOMMENDED OPERATING CONDITIONS

		VALUE	UNIT
Input voltage range	VIN (main supply)	3 to 15	V
	VDD	4.5 to 25	
	VBST	4.5 to 21	
	VBST(with respect to LL)	4.5 to 6.5	
	EN, TRIP, VFB, RF, MODE	–0.1 to 6.5	
Output voltage range	LL	–0.8 to 15	V
	PGOOD, VREG	–0.1 to 6.5	
Source/Sink Current	VBST	50	mA
Junction temperature range, T _J		–40 to 125	°C

ELECTRICAL CHARACTERISTICS

Over recommended free-air temperature range, VDD = 12 V (Unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND SUPPLY CURRENT						
V _{VIN}	VIN pin power conversion input voltage		3		15	V
V _{DD}	Supply input voltage		4.5		25	V
I _{VIN(leak)}	VIN pin leakage current	V _{EN} = 0 V			1	μA
I _{VDD}	VDD supply current	VDD current, T _A = 25°C, No Load, V _{EN} = 5 V, V _{VFB} = 0.630 V		420	590	μA
I _{VDDSDN}	VDD shutdown current	VDD current, T _A = 25°C, No Load, V _{EN} = 0 V			10	μA
INTERNAL REFERENCE VOLTAGE						
V _{VFB}	VFB regulation voltage	VFB voltage, CCM condition ⁽¹⁾		0.6000		V
		T _A = 25°C	0.597	0.600	0.603	V
		T _A = 0°C to 85°C	0.5952	0.600	0.6048	
		T _A = -40°C to 85°C	0.594	0.600	0.606	
I _{VFB}	VFB input current	V _{VFB} = 0.630 V, T _A = 25°C		0.002	0.2	μA
LDO OUTPUT						
V _{VREG}	LDO output voltage	0 mA ≤ I _{VREG} ≤ 30 mA	4.77	5.0	5.35	V
I _{VREG}	LDO output current ⁽¹⁾	Maximum current allowed from LDO			30	mA
V _{DO}	LDO drop out voltage	V _{DD} = 4.5 V, I _{VREG} = 30 mA			295	mV
BOOT STRAP SWITCH						
V _{FBST}	Forward voltage	V _{VREG-VBST} , I _F = 10 mA, T _A = 25°C		0.1	0.2	V
I _{VBSTLK}	VBST leakage current	V _{VBST} = 23 V, V _{LL} = 17 V, T _A = 25°C		0.01	1.5	μA
DUTY AND FREQUENCY CONTROL						
t _{OFF(min)}	Minimum off time	T _A = 25°C	150	260	400	ns
t _{ON(min)}	Minimum on time	V _{VIN} = 17 V, V _{OUT} = 0.6 V, R _{RF} = 0 Ω to V _{REG} , T _A = 25°C ⁽¹⁾		35		
SOFTSTART						
t _{SS}	Internal SS time from V _{OUT} = 0 to V _{OUT} = 95%	R _{MODE} = 39 kΩ		0.7		ms
		R _{MODE} = 100 kΩ		1.4		
		R _{MODE} = 200 kΩ		2.8		
		R _{MODE} = 470 kΩ		5.6		
POWERGOOD						
V _{THPG}	PG threshold	PG in from lower	92.5%	96%	98.5%	
		PG in from higher	107.5%	110%	112.5%	
		PG hysteresis	2.5%	5%	7.8%	
R _{PG}	PG transistor on-resistance		15	30	55	Ω
t _{PGDEL}	PG Delay after soft-start		0.8	1	1.2	ms

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS

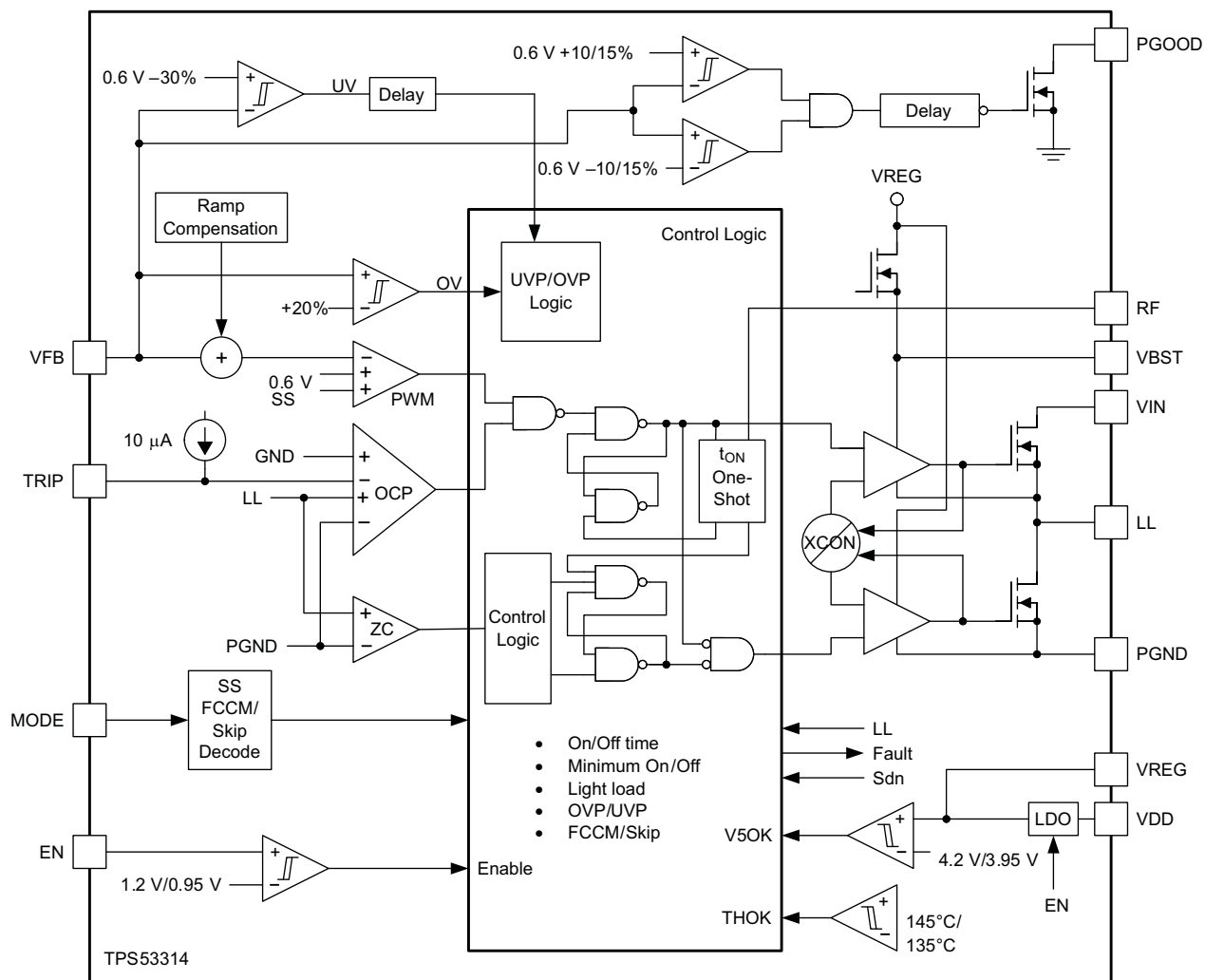
Over recommended free-air temperature range, VDD = 12 V (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
LOGIC THRESHOLD AND SETTING CONDITIONS							
V _{EN}	EN voltage threshold	Enable	1.8			V	
		Disable	0.6				
I _{EN}	EN input current	V _{EN} = 5 V	1.0			μA	
f _{SW}	Switching frequency	R _{RF} = 0 Ω to GND, T _A = 25°C ⁽¹⁾	200	250	300	kHz	
		R _{RF} = 187 kΩ to GND, T _A = 25°C ⁽¹⁾	250	300	350		
		R _{RF} = 619 kΩ to GND, T _A = 25°C ⁽¹⁾	350	400	450		
		R _{RF} = Open, T _A = 25°C ⁽¹⁾	450	500	550		
		R _{RF} = 866 kΩ to VREG, T _A = 25°C ⁽¹⁾	580	650	720		
		R _{RF} = 309 kΩ to VREG, T _A = 25°C ⁽¹⁾	670	750	820		
		R _{RF} = 124 kΩ to VREG, T _A = 25°C ⁽¹⁾	770	850	930		
		R _{RF} = 0 Ω to VREG, T _A = 25°C ⁽¹⁾	880	970	1070		
PROTECTION: CURRENT SENSE							
I _{TRIP}	TRIP source current	V _{TRIP} = 1 V, T _A = 25°C	9.4	10.0	10.6	μA	
TC _{ITRIP}	TRIP current temperature coefficient	On the basis of 25°C ⁽²⁾	4700			ppm/°C	
V _{TRIP}	Current limit threshold setting range	V _{TRIP-GND} voltage	0.2	0.6		V	
V _{OCL}	Current limit threshold	V _{TRIP} = 0.6 V	67	75	83	mV	
		V _{TRIP} = 0.2	19	26	33		
V _{OCLN}	Negative current limit threshold	V _{TRIP} = 0.6 V	−83	−75	−67		mV
		V _{TRIP} = 0.2 V	−33	−26	−19		
V _{AZCADJ}	Auto zero cross adjustable range	Positive	3	15	mV		
		Negative	−15 −3				
PROTECTION: UVP and OVP							
V _{OVP}	OVP trip threshold	OVP detect	115%	120%	125%		
t _{OVPDEL}	OVP propagation delay time	VFB delay with 50-mV overdrive	1			μs	
V _{UVP}	Output UVP trip threshold time	UVP detect	65%	70%	75%		
t _{UVPDEL}	Output UVP propagation delay time		0.8	1	1.2	ms	
t _{UVPEN}	Output UVP enable delay time	from EN to UVP workable, R _{MODE} = 39 kΩ	2.0	2.6	3.2	ms	
UVLO							
V _{UVVREG}	VREG UVLO threshold	Wake up	4.00	4.20	4.32	V	
		Hysteresis	0.25				
THERMAL SHUTDOWN							
T _{SDN}	Thermal shutdown threshold	Shutdown temperature ⁽²⁾	145			°C	
		Hysteresis ⁽²⁾	10				

(1) Not production tested. Test condition is VIN = 12 V, VOUT = 1.1 V, IOUT = 5 A using application circuit shown in 图 33.

(2) Ensured by design. Not production tested.

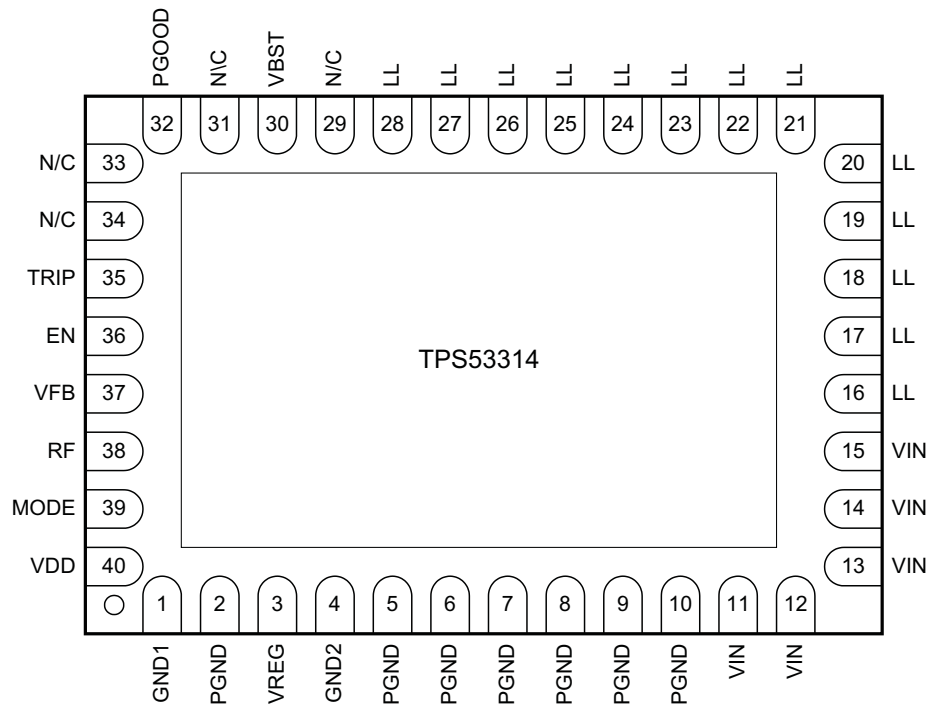
FUNCTIONAL BLOCK DIAGRAM



UDG-11139

PIN CONFIGURATION

**TPS53314
RGF-40
(TOP VIEW)**



PIN DESCRIPTIONS

PIN		I/O/P ⁽¹⁾	DESCRIPTION
NAME	NO.		
EN	36	I	Enable pin.
GND1	1	G	GND for controller
GND2	4	G	GND for half-bridge
LL	16	B	Output of converted power. Connect this pin to the output Inductor.
	17		
	18		
	19		
	20		
	21		
	22		
	23		
	24		
	25		
	26		
	27		
	28		
MODE	39	I	Soft-start and skip/CCM selection. Connect a resistor to select soft-start time using 表 1 . The soft-start time is detected and stored into internal register during start-up.

(1) I=Input, O=Output, B=Bidirectional, P=Supply, G=Ground

PIN DESCRIPTIONS (接下页)

PIN		I/O/P ⁽¹⁾	DESCRIPTION
NAME	NO.		
N/C	29		No connection
	31		
	33		
	34		
PGOOD	32	O	Open drain power good flag. Provides a 1-ms start up delay after the VFB pin voltage falls within specified limits. When the VFB pin voltage goes outside the specified limits, the PGOOD pin goes low after a 2-μs delay.
PGND	2	G	Power GND
	5		
	6		
	7		
	8		
	9		
	10		
RF	38	I	Switching frequency selection. Connect a resistance to GND or VREG to select switching frequency using 表 2 . The switching frequency is detected and stored during the startup.
TRIP	35	I	OCL detection threshold setting pin. 10 μA at room temperature, 4700 ppm/°C current is sourced and set the OCL trip voltage as follows. $V_{OCL} = V_{TRIP}/8 \quad (V_{TRIP} \leq 0.6 \text{ V}, V_{OCL} \leq 75 \text{ mV})$
VBST	30	P	Supply input for high-side FET gate driver (boost terminal). Connect capacitor from this pin to LL-node. Internally connected to the VREG pin via bootstrap MOSFET switch.
VDD	40	P	Controller power supply input.
VFB	37	I	Output feedback input. Connect this pin to V _{OUT} through a resistor divider.
VIN	11	P	Conversion power input.
	12		
	13		
	14		
	15		
VREG	3	P	5-V LDO output.
Pad	–	–	Package thermal pad. Use proper number of vias to connect to GND plane for heat dissipation.

TYPICAL CHARACTERISTICS

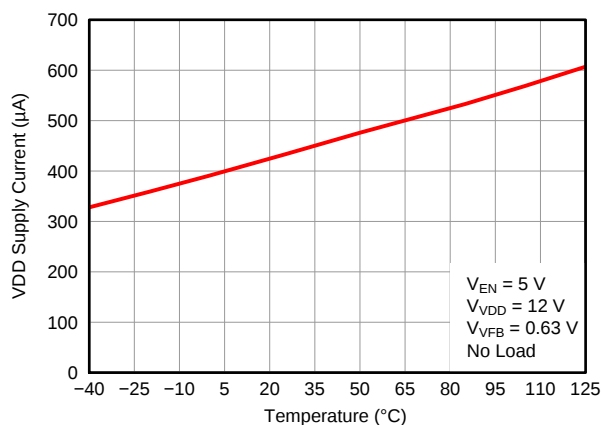


图 1. VDD Supply Current vs. Temperature

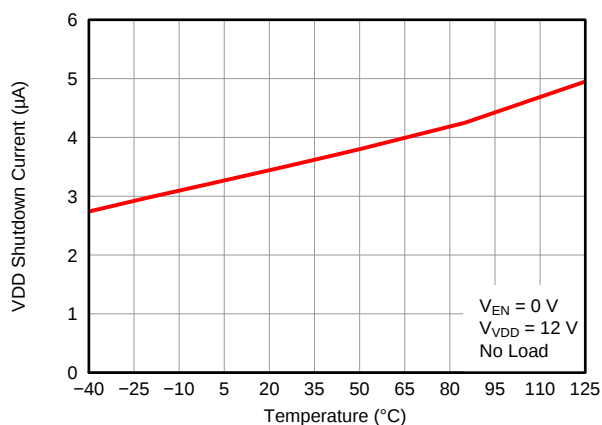


图 2. VDD Shutdown Current vs. Temperature

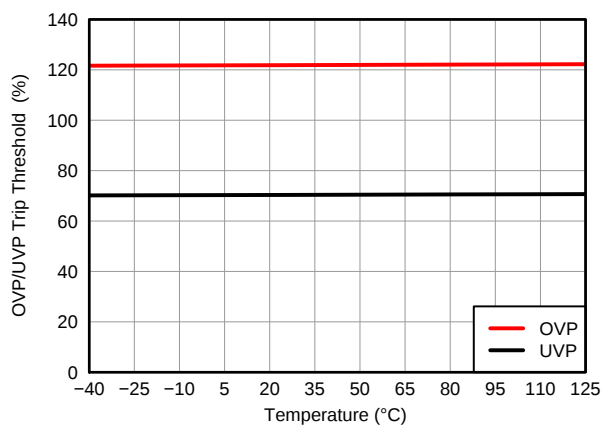


图 3. OVP/UVP Trip Threshold vs. Temperature

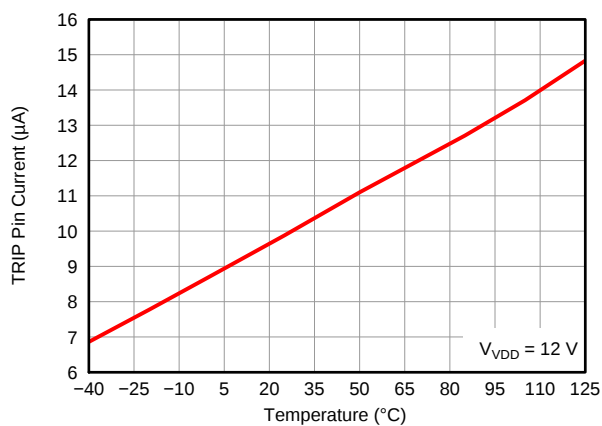


图 4. Trip Pin Current vs. Temperature

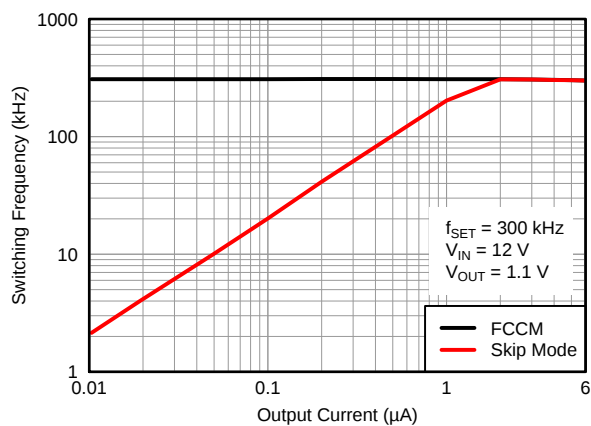


图 5. Frequency vs. Temperature ($f_{SET} = 300\text{ kHz}$)

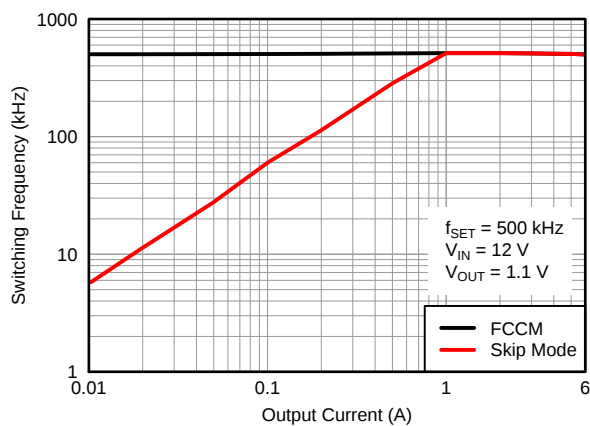


图 6. Frequency vs. Temperature ($f_{SET} = 500\text{ kHz}$)

TYPICAL CHARACTERISTICS

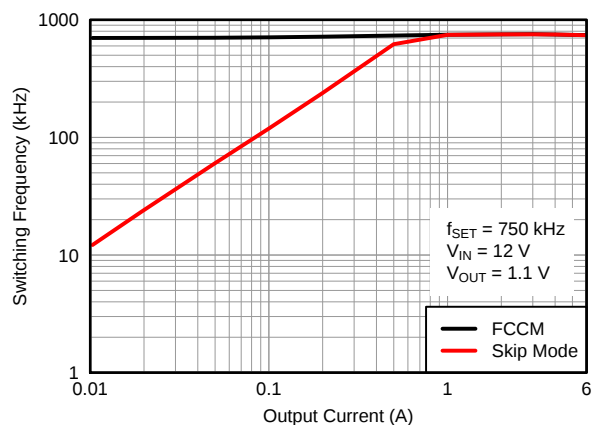
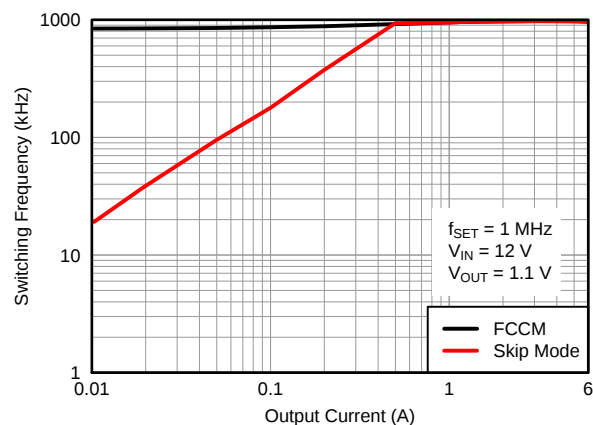
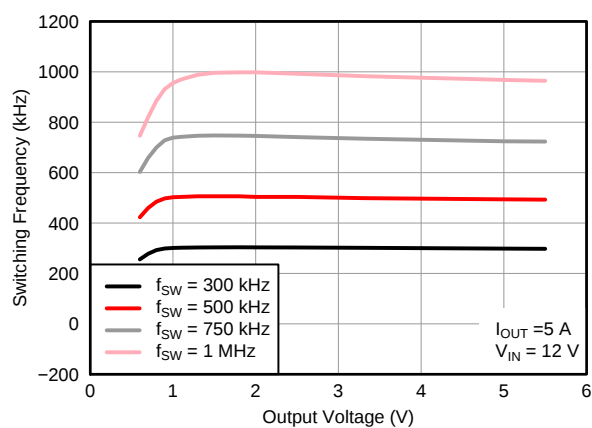
图 7. Frequency vs. Temperature ($f_{SET} = 750 \text{ kHz}$)图 8. Frequency vs. Temperature ($f_{SET} = 1 \text{ MHz}$)

图 9. Switching Frequency vs. Output Voltage

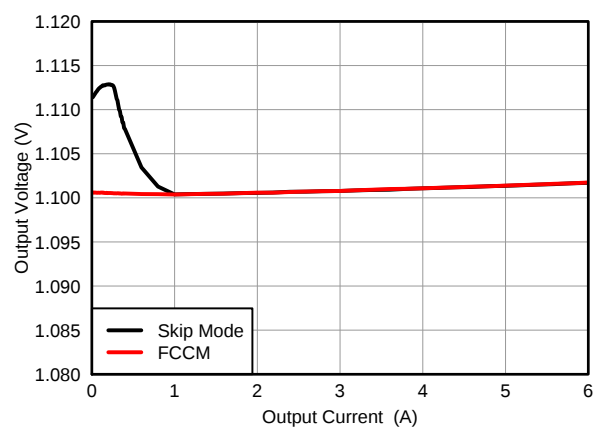


图 10. Output Voltage vs. Output Current

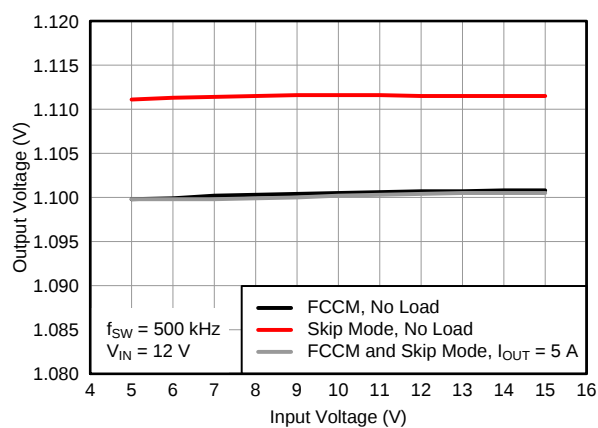


图 11. Output Voltage vs. Input Voltage

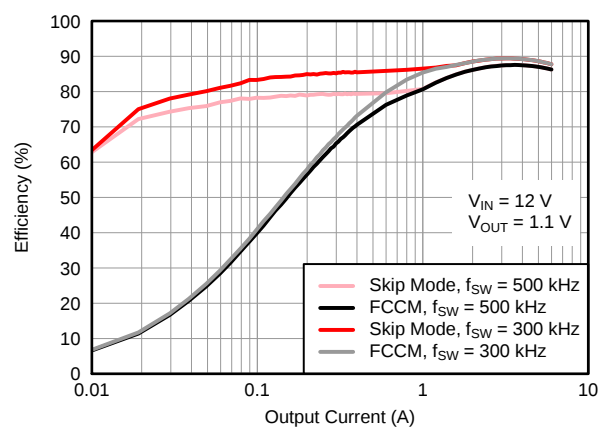


图 12. Efficiency vs. Output Current

TYPICAL CHARACTERISTICS

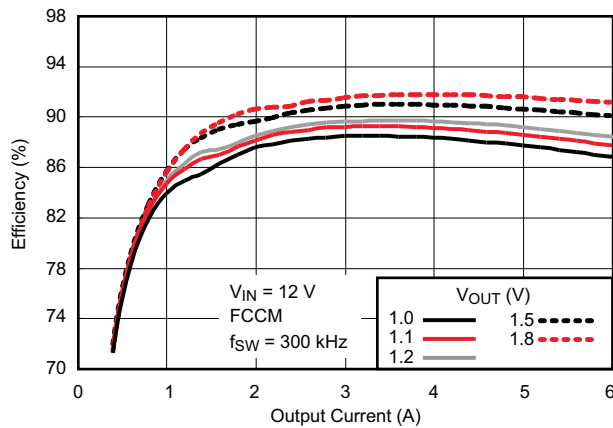


图 13. Efficiency vs Output Current,
Inductors: PCMC065T-1R0

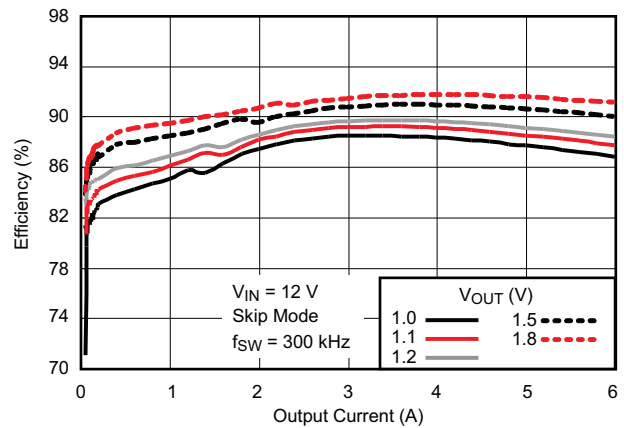


图 14. Efficiency vs Output Current,
Inductors: PCMC065T-1R0

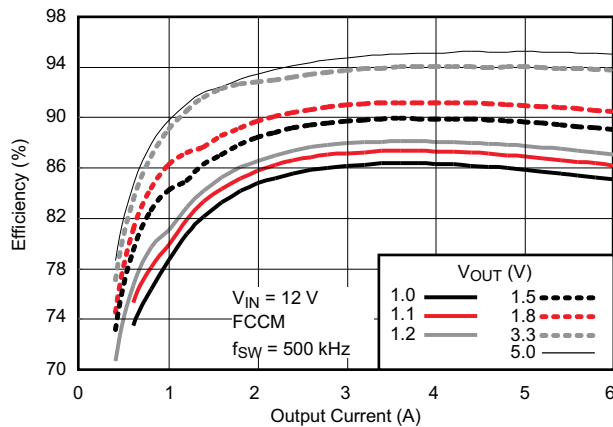


图 15. Efficiency vs Output Current,
Inductors: $V_{OUT} \leq 3.3$ V: PCMC065T-1R0, $V_{OUT} = 5$ V:
PG0642.222

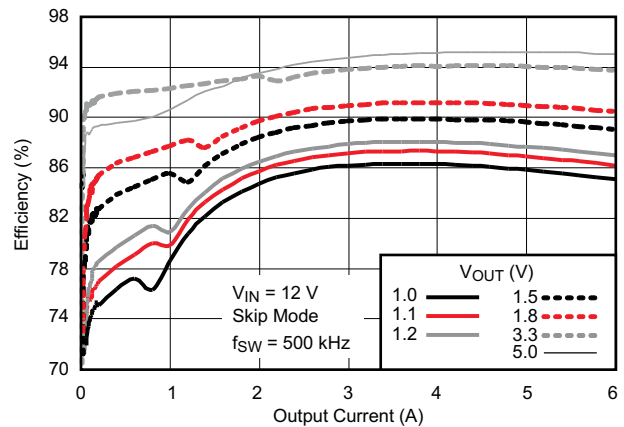


图 16. Efficiency vs Output Current,
Inductors: $V_{OUT} \leq 3.3$ V: PCMC065T-1R0, $V_{OUT} = 5$ V:
PG0642.222

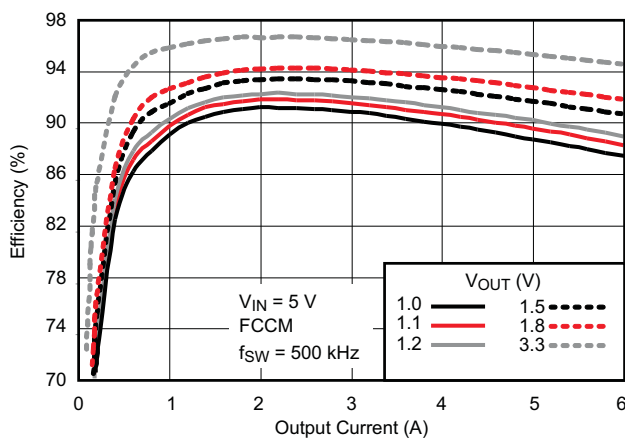


图 17. Efficiency vs Output Current,
Inductor: PCMC065T-1R0

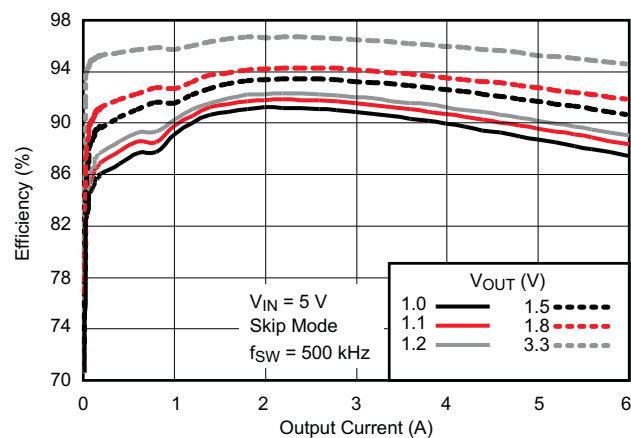


图 18. Efficiency vs Output Current,
Inductor: PCMC065T-1R0

TYPICAL CHARACTERISTICS

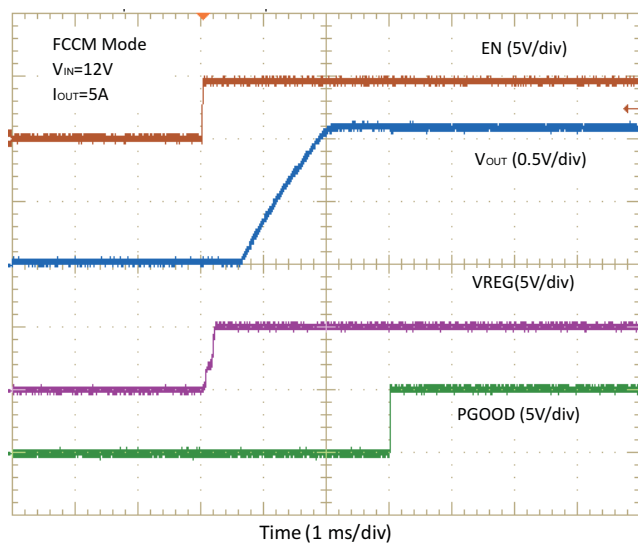


图 19. Start-Up

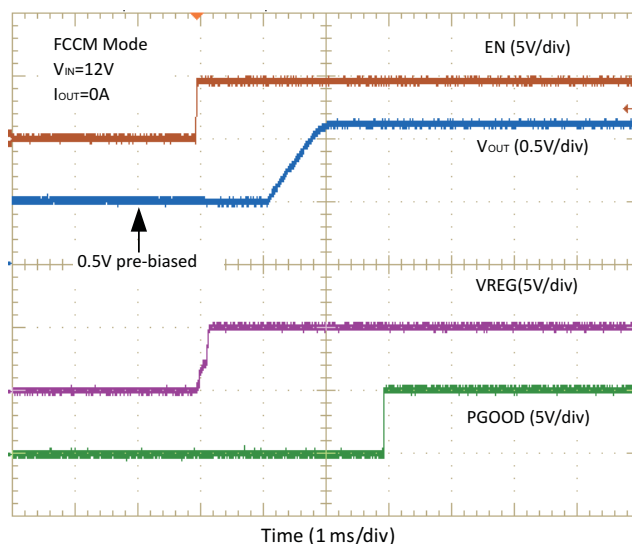


图 20. Pre-Bias Start-Up

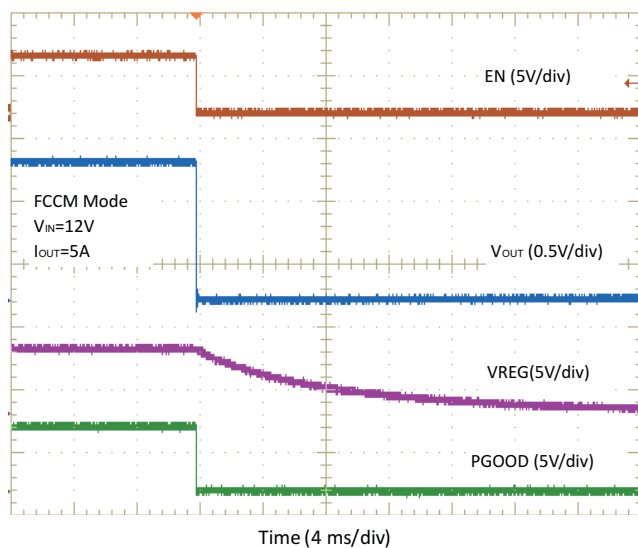


图 21. Turn-Off

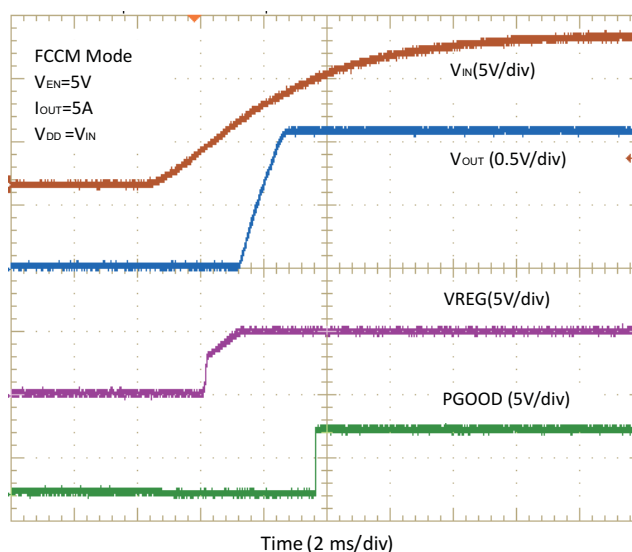


图 22. UVLO Start-Up

TYPICAL CHARACTERISTICS

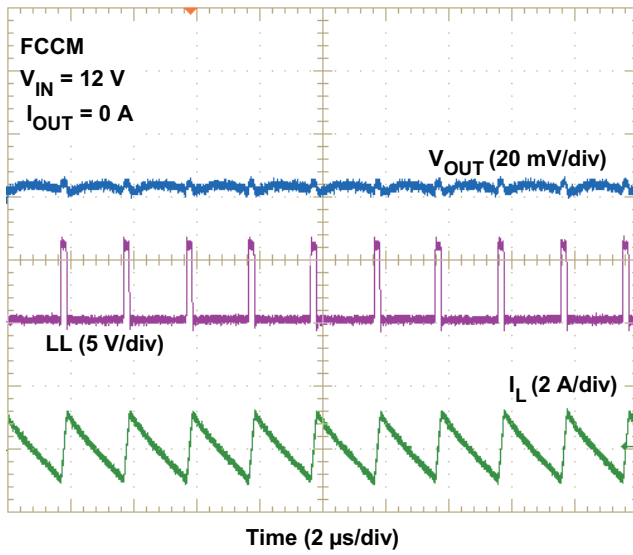


图 23. 1.1-V Output FCCM Steady-State Operation

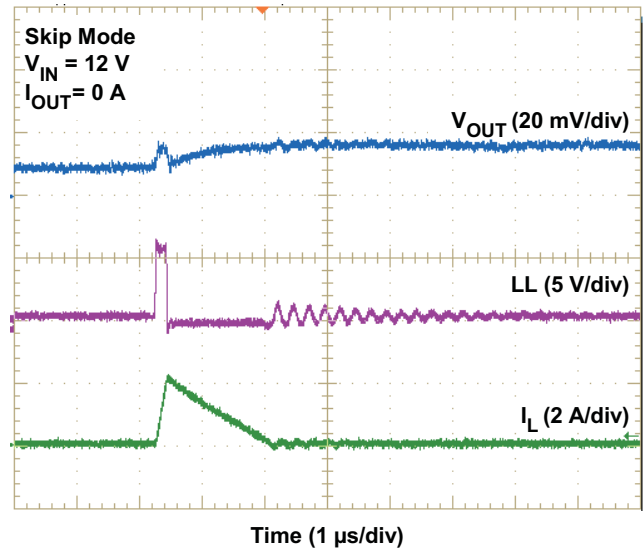


图 24. 1.1-V Output Skip Mode Steady-State Operation

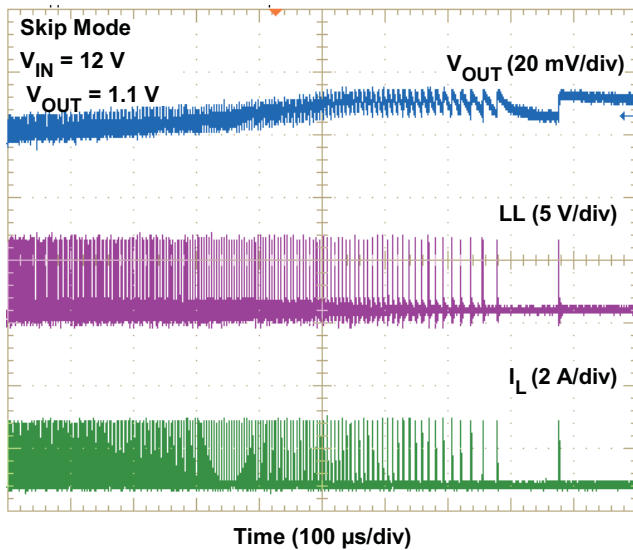


图 25. CCM to DCM Transition

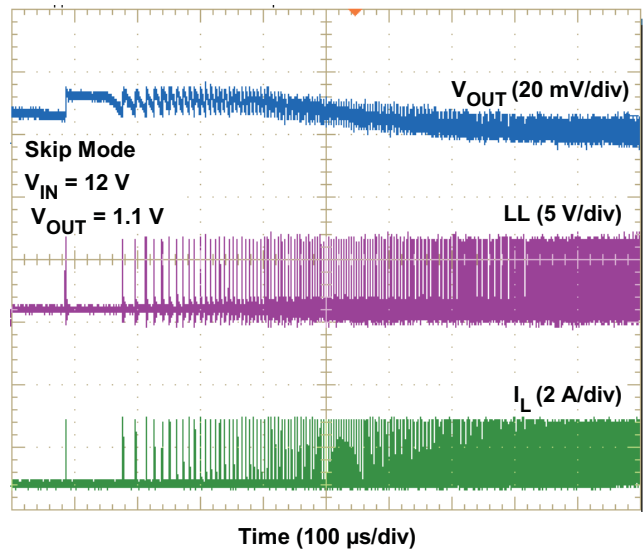


图 26. DCM to CCM Transition

TYPICAL CHARACTERISTICS

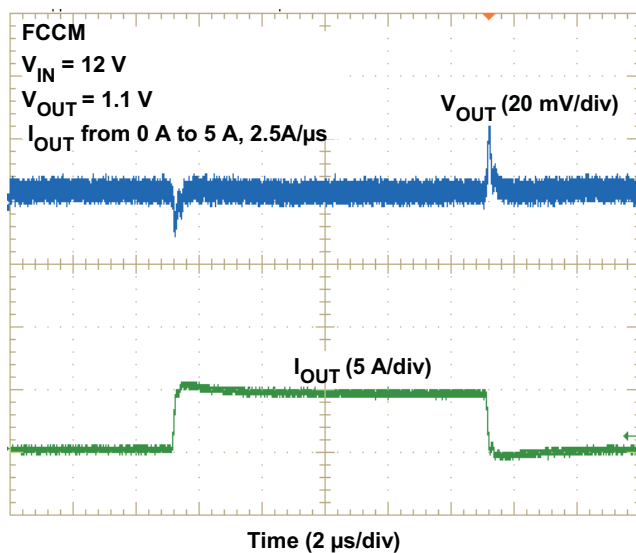


图 27. FCCM Load Transient

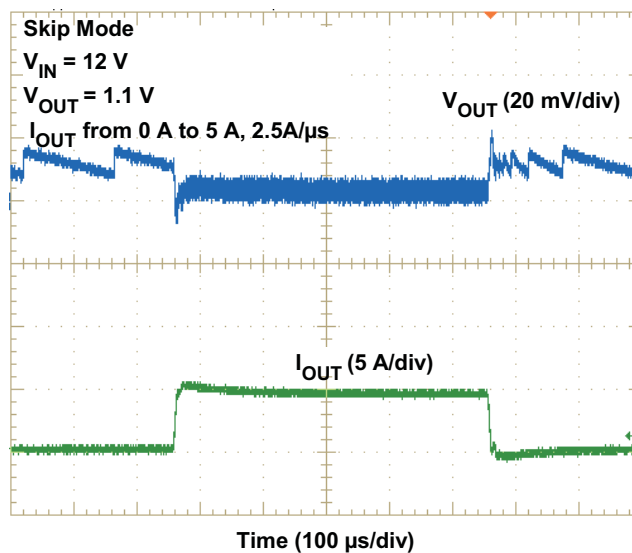


图 28. Skip Mode Load Transient

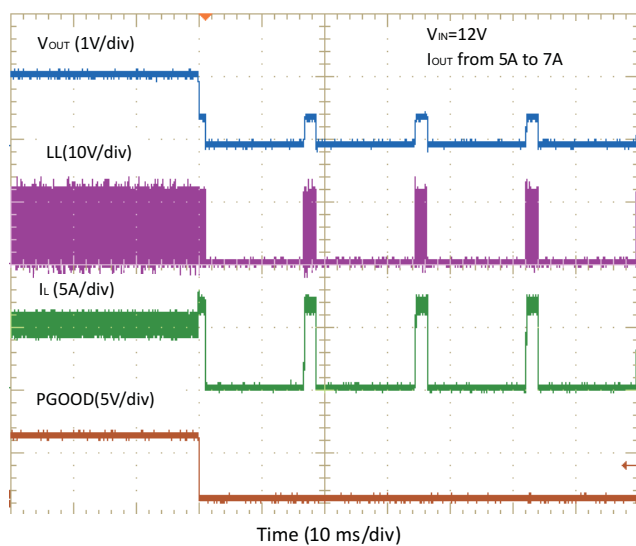


图 29. Overcurrent Protection

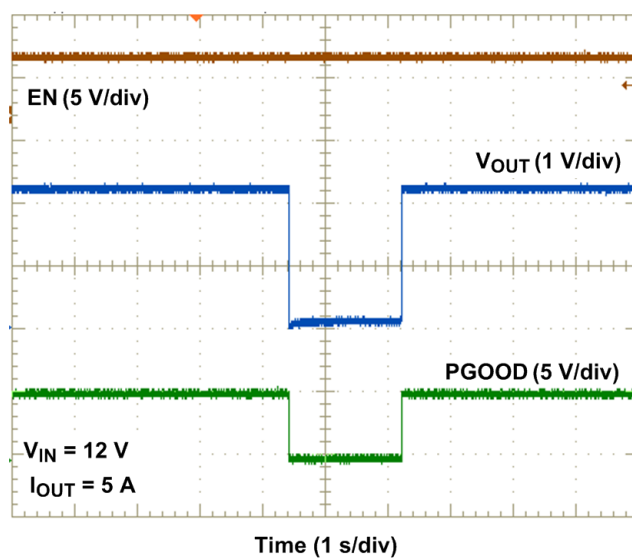


图 30. Over-temperature Protection

TYPICAL CHARACTERISTICS

图 31, shows the thermal signature of the TPS53314 EVM, $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.1\text{ V}$, $I_{OUT} = 6\text{ A}$, $f_{SW} = 500\text{ kHz}$ at room temperature with no airflow.

图 32 shows the thermal signature of the TPS53314 EVM, $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 6\text{ A}$, $f_{SW} = 650\text{ kHz}$ at room temperature with no airflow.

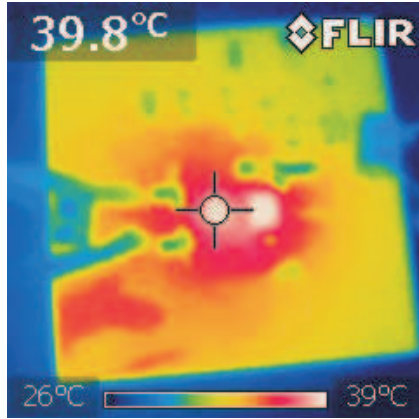


图 31. Thermal Signature of TPS53314 EVM,
 $f_{SW} = 500\text{ kHz}$

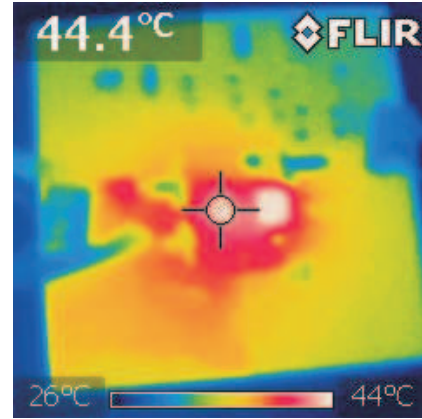


图 32. Thermal Signature of TPS53314 EVM,
 $f_{SW} = 650\text{ kHz}$

APPLICATION INFORMATION

APPLICATION CIRCUIT DIAGRAM

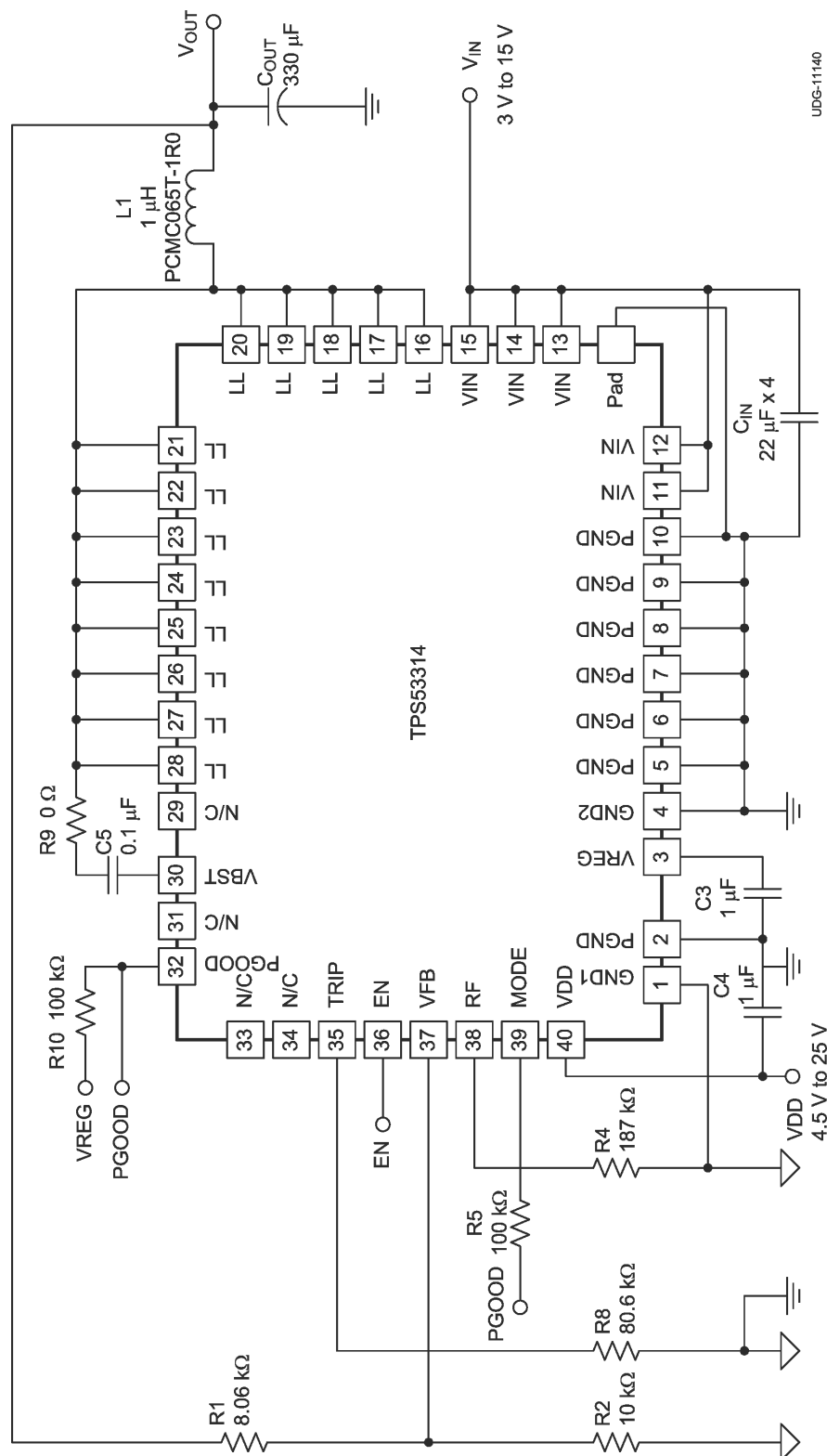
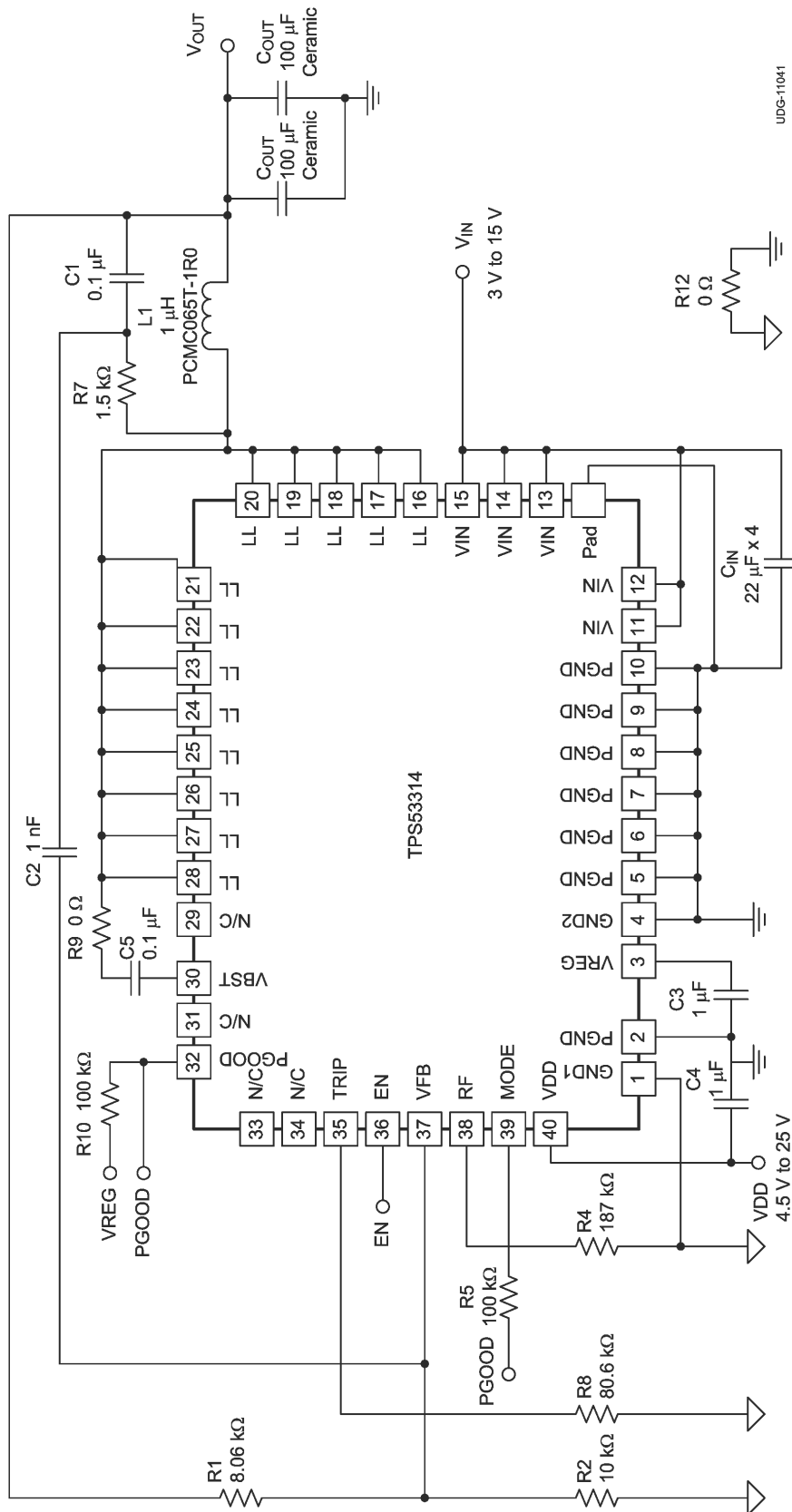


图 33. Typical Application Circuit Diagram



UDG-11041

图 34. Typical Application Circuit Diagram with Ceramic Output Capacitors

General Description

The TPS53314 is a high-efficiency, single channel, synchronous buck converter suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP™ mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 3 V up to 15 V. The D-CAP™ mode uses the ESR of the output capacitor(s) to sense the device current. One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or the VREG pin. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

The TPS53314 has a MODE pin to select between auto-skip mode and forced continuous conduction mode (FCCM) for light load conditions. The MODE pin also sets the selectable soft-start time ranging from 0.7 ms to 5.6 ms.

Enable and Soft Start

When the EN pin voltage rises above the enable threshold voltage (typically 1.2 V), the controller enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 5 V at the VREG pin. The controller then uses the first 250 μ s to calibrate the switching frequency setting resistance attached to the RF pin and stores the switching frequency code in internal registers. However, switching is inhibited during this phase. In the second phase, an internal DAC starts ramping up the reference voltage from 0 V to 0.6 V. Depending on the MODE pin setting, the ramping up time varies from 0.7 ms to 5.6 ms. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

表 1. Soft-Start and MODE

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R _{MODE} (k Ω)
Auto Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM ⁽¹⁾	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

(1) The device transitions into FCCM after the PGOOD pin goes high.

Adaptive On-Time D-CAP™ Control

The TPS53314 does not have a dedicated oscillator to determine switching frequency. However, the device operates with pseudo-constant frequency by feed-forwarding the input and output voltages into the on-time one-shot timer. The adaptive on-time control adjusts the on-time to be inversely proportional to the input voltage

and proportional to the output voltage $\left(t_{ON} \propto \frac{V_{OUT}}{V_{IN}} \right)$.

This makes the switching frequency fairly constant in steady state conditions over a wide input voltage range. The switching frequency is selectable from eight preset values by a resistor connected between the RF pin and GND or between the RF pin and the VREG pin as shown in 表 2. (Leaving the resistance open sets the switching frequency to 500 kHz.)

表 2. Resistor and Switching Frequency

RESISTOR (R _{RF}) CONNECTIONS	SWITCHING FREQUENCY (kHz)
0 Ω to GND	250
187 kΩ to GND	300
619 kΩ to GND	400
Open	500
866 kΩ to VREG	600
309 kΩ to VREG	750
124 kΩ to VREG	850
0 Ω to VREG	970

The off-time is modulated by a PWM comparator. The VFB node voltage (the mid-point of resistor divider) is compared to the internal 0.6-V reference voltage added with a ramp signal. When the signal values match, the PWM comparator asserts a set signal to terminate the off-time (turn off the low-side MOSFET and turn on high-side MOSFET). The set signal is valid if the inductor current level is below the OCP threshold, otherwise the off-time is extended until the current level falls below the threshold.

图 35 和 图 36 show two on-time control schemes.

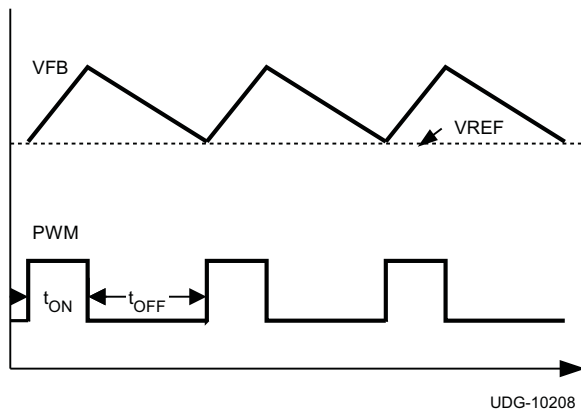


图 35. On-Time Control Without Ramp Compensation

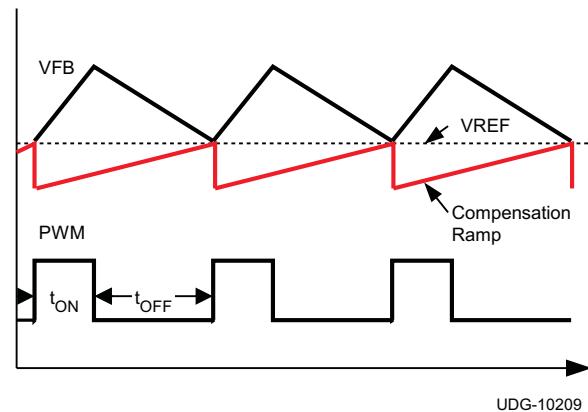


图 36. On-Time Control With Ramp Compensation

Small Signal Model

From small-signal loop analysis, a buck converter using D-CAP™ mode can be simplified as shown in 图 37.

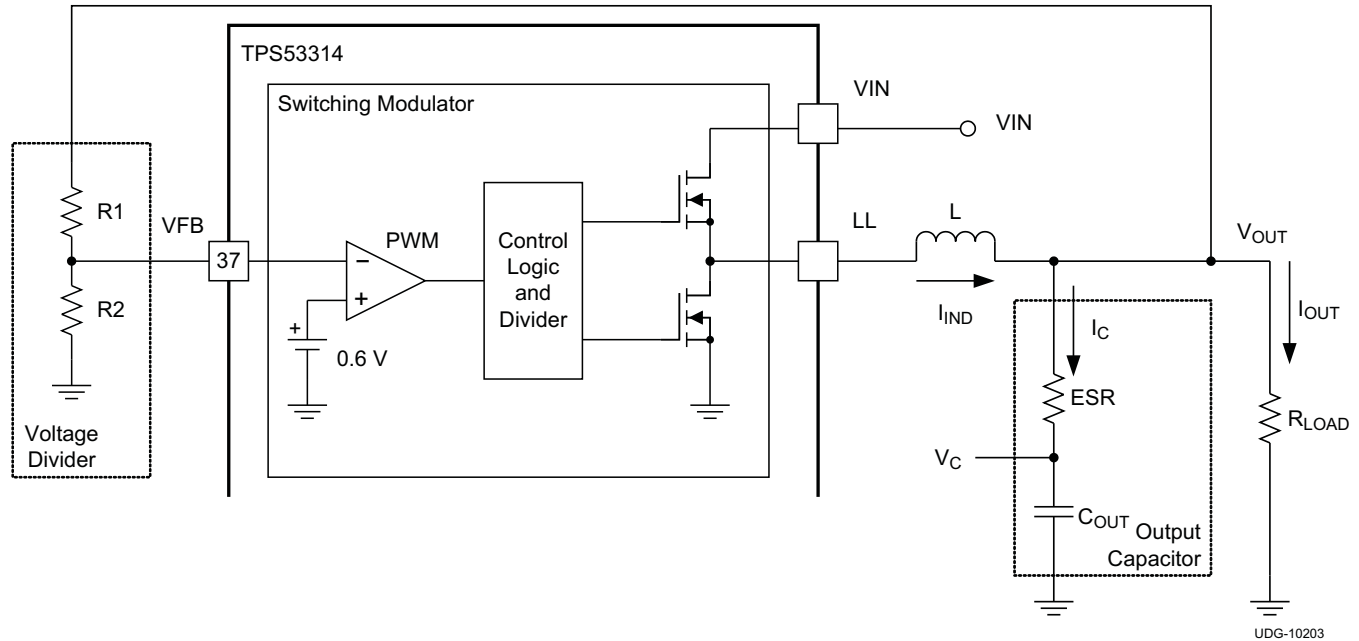


图 37. Simplified Modulator Model

The output voltage is compared with the internal reference voltage (ramp signal is ignored here for simplicity). The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator can be assumed high enough to keep the voltage at the beginning of each on-cycle substantially constant.

$$H(s) = \frac{1}{s \times \text{ESR} \times C_{\text{OUT}}} \quad (1)$$

For the loop stability, the 0 dB frequency, f_0 , defined in 公式 2 must be lower than $\frac{1}{4}$ of the switching frequency.

$$f_0 = \frac{1}{2\pi \times \text{ESR} \times C_{\text{OUT}}} \leq \frac{f_{\text{SW}}}{4} \quad (2)$$

According to 公式 2, the loop stability of D-CAP™ mode modulator is mainly determined by the capacitor chemistry. For example, specialty polymer capacitors (SP-CAP) have C_{OUT} on the order of several 100 μF and ESR in range of 10 m Ω . These makes f_0 on the order of 100 kHz or less and the loop is stable. However, ceramic capacitors have an f_0 at more than 700 kHz, and need special care when used with this modulator. An application circuit using ceramic capacitors is described in [External Parts Selection](#) section under *All Ceramic Output Capacitors*.

Ramp Signal

The TPS53314 adds a ramp signal to the 0.6-V reference in order to improve jitter performance. The feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the signal-to-noise ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jittery and more stable. The ramp signal is controlled to start with -7 mV at the beginning of an on-cycle and becomes 0 mV at the end of an off-cycle in steady state.

Auto-Skip Eco-mode™ Light Load Operation

While the MODE pin is pulled low via R_{MODE} , the TPS53314 automatically reduces the switching frequency at light-load conditions to maintain high efficiency. Detailed operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The synchronous MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode (DCM). The on-time is maintained as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light-load operation $I_{OUT(LL)}$ (i.e., the threshold between continuous and discontinuous conduction mode) can be calculated as shown in 公式 3.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where

- f_{SW} is the PWM switching frequency (3)

Switching frequency versus output current in the light load condition is a function of L , V_{IN} and V_{OUT} , but it decreases almost proportionally to the output current from the $I_{OUT(LL)}$ given in 公式 3. For example, it is 60 kHz at $I_{OUT(LL)}/5$ if the frequency setting is 300 kHz.

Adaptive Zero Crossing

The TPS53314 has an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. It prevents SW-node swing-up caused by postponed detection and minimizes diode conduction period caused by premature detection. As a result, better light-load efficiency is delivered.

Forced Continuous Conduction Mode

When the MODE pin is tied to PGOOD through a resistor, the controller keeps continuous conduction mode (CCM) during light-load conditions. In this mode, the switching frequency is maintained over the entire load range which is suitable for applications needing tight control of the switching frequency at a cost of lower efficiency.

Power Good

The TPS53314 has powergood output that indicates high when switcher output is within the target. The powergood function is activated after soft-start has finished. If the output voltage becomes within +10% or –5% of the target value, internal comparators detect the powergood state and the powergood signal becomes high after a 1-ms internal delay. If the output voltage goes outside of +15% or –10% of the target value, the power-good signal becomes low after two microsecond (2-μs) internal delay. The powergood output is an open drain output and must be pulled up externally.

In order for the PGOOD logic to be valid, the VDD input must be higher than 1 V. To avoid invalid PGOOD logic before the TPS53314 is powered up, it is recommended the PGOOD be pull to VREG (either directly or through a resistor divider) because VREG remains low when the device is off.

Current Sense and Overcurrent Protection

TPS53314 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the *OFF* state and the controller maintains the *OFF* state during the period in that the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, TPS53314 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, R_{TRIP} . The TRIP pin sources I_{TRIP} current, which is 10 μA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as shown in 公式 4.

$$V_{TRIP} (mV) = R_{TRIP} (k\Omega) \times I_{TRIP} (\mu A) \quad (4)$$

The inductor current is monitored by the voltage between the GND pin and the LL pin. The GND pin is used as positive current sensing node and the LL pin is used as negative current sensing node. The TRIP pin current, I_{TRIP} , has a 4700ppm/ $^{\circ}C$ temperature slope to compensate the temperature dependency of the $R_{DS(on)}$.

As the comparison is done during the *OFF* state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{OCP} , can be calculated as shown in 公式 5.

$$I_{OCP} = \frac{V_{TRIP}}{(8 \times R_{DS(on)})} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{(8 \times R_{DS(on)})} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (5)$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor, therefore the output voltage tends to decrease. Eventually, it crosses the undervoltage protection threshold and shuts down. After a hiccup delay (16 ms with 0.7-ms sort-start), the controller restarts. If the overcurrent condition remains, the procedure is repeated and the device enters hiccup mode.

During CCM, the negative current limit (NCL) protects the internal FET from carrying too much current. The NCL detect threshold is set as the same absolute value as positive OCL but negative polarity. Note that the threshold continues to represent the valley value of the inductor current.

Overvoltage and Undervoltage Protection

The TPS53314 monitors a resistor divided feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, TPS53314 latches OFF both high-side and low-side MOSFETs drivers. The controller restarts after a hiccup delay (16 ms with 0.7-ms soft-start). This function is enabled 1.5 ms after the soft-start is completed.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and latches ON the low-side MOSFET driver. The output voltage decreases. If the output voltage reaches the UV threshold, then both high-side MOSFET and low-side MOSFET driver is OFF and the device restarts after a hiccup delay. If the OV condition remains, both high-side MOSFET and low-side MOSFET driver remains OFF until the OV condition is removed.

UVLO Protection

The TPS53314 uses VREG undervoltage lockout protection (UVLO). When the VREG voltage is lower than the UVLO threshold voltage, the switch mode power supply shuts off. This is a non-latch protection.

Thermal Shutdown

TPS53314 includes a temperature monitoring feature. If the temperature exceeds the threshold value (typically 145 $^{\circ}C$), TPS53314 shuts off. When the temperature falls approximately 10 $^{\circ}C$ below the threshold value, the device turns on again. This is a non-latch protection.

External Parts Selection

The external components selection is a simple process using D-CAP™ Mode.

1. CHOOSE THE INDUCTOR

The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage and improves signal-to-noise ratio and helps stable operation.

$$L = \frac{1}{I_{\text{IND(ripple)}} \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} = \frac{3}{I_{\text{OUT(max)}} \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} \quad (6)$$

The inductor requires a low DCR to achieve good efficiency. It also requires enough room above peak inductor current before saturation. The peak inductor current can be estimated in 公式 7.

$$I_{\text{IND(peak)}} = \frac{V_{\text{TRIP}}}{8 \times R_{\text{DS(on)}}} + \frac{1}{L \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} \quad (7)$$

2. CHOOSE THE OUTPUT CAPACITOR(S)

When organic semiconductor capacitor(s) or specialty polymer capacitor(s) are used, for loop stability, capacitance and ESR should satisfy 公式 2. For jitter performance, 公式 8 is a good starting point to determine ESR.

$$\text{ESR} = \frac{V_{\text{OUT}} \times 10(\text{mV}) \times (1-D)}{0.6(\text{V}) \times I_{\text{IND(ripple)}}} = \frac{10(\text{mV}) \times L \times f_{\text{SW}}}{0.6(\text{V})} = \frac{L \times f_{\text{SW}}}{60} (\Omega)$$

where

- D is the duty factor
- t_{SW} is the switching period
- the required output ripple slope is approximately 10 mV per t_{SW} in terms of V_{VFB}

3. DETERMINE THE VALUE OF R1 AND R2

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in 图 37. R1 is connected between VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended R2 value is from 10kΩ to 20kΩ. Determine R1 using 公式 9.

$$R1 = \frac{V_{\text{OUT}} - \frac{I_{\text{IND(ripple)}} \times \text{ESR}}{2} - 0.6}{0.6} \times R2 \quad (9)$$

4. CHOOSE THE OVERCURRENT SETTING RESISTOR

The overcurrent setting resistor, R_{TRIP} , can be determined using 公式 10.

$$R_{\text{TRIP}}(\text{k}\Omega) = \frac{\left(I_{\text{OCP}} - \left(\frac{1}{2 \times L \times f_{\text{SW}}} \right) \times \frac{(V_{\text{IN}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN}}} \right) \times 8 \times R_{\text{DS(on)}}(\text{m}\Omega)}{I_{\text{TRIP}}(\mu\text{A})}$$

where

- I_{TRIP} is the TRIP pin sourcing current (10 μA)
- $R_{\text{DS(on)}}$ is the on-resistance value of the low-side MOSFET (7.5 mΩ)

External Component Selection with All Ceramic Output Capacitors

When ceramic output capacitors are used, the stability criteria in 公式 2 cannot be satisfied. The ripple injection approach as shown in 图 34 is implemented to increase the ripple on the VFB pin and make the system stable. C2 can be fixed at 1 nF. The value of C1 can be selected between 10 nF to 200 nF.

The increased ripple on the VFB pin causes the increase of the VFB DC value. The AC ripple coupled to the VFB pin has two components, one coupled from SW node and the other coupled from V_{OUT} and they can be calculated using 公式 11 and 公式 12.

$$V_{\text{INJ_SW}} = \frac{V_{\text{IN}} - V_{\text{OUT}}}{R7 \times C1} \times \frac{D}{f_{\text{SW}}} \quad (11)$$

$$V_{\text{INJ_OUT}} = \text{ESR} \times I_{\text{IND(ripple)}} + \frac{I_{\text{IND(ripple)}}}{8 \times C_{\text{OUT}} \times f_{\text{SW}}} \quad (12)$$

The DC value of VFB can be calculated by 公式 13:

$$V_{\text{VFB}} = 0.6 + \frac{V_{\text{INJ_SW}} + V_{\text{INJ_OUT}}}{2} \quad (13)$$

And the resistor divider value can be determined by 公式 14:

$$R1 = \frac{V_{\text{OUT}} - V_{\text{FB}}}{V_{\text{FB}}} \times R2 \quad (14)$$

LAYOUT CONSIDERATIONS

Certain points must be considered before starting a layout work using the TPS53314.

- The power components (including input/output capacitors, inductor and TPS53314) should be placed on one side of the PCB (solder side). Other small signal components should be placed on another side (component side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE and RF should be placed away from high-voltage switching nodes such as LL, VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- Place the VIN decoupling capacitors as close to the VIN and PGND pins as possible to minimize the input AC current loop.
- Since the TPS53314 controls output voltage referring to voltage across the V_{OUT} capacitor, the top-side resistor of the voltage divider should be connected to the positive node of VOUT capacitor. In a same manner both bottom side resistor and GND pad of the device should be connected to the negative node of V_{OUT} capacitor. The trace from these resistors to the VFB pin should be short and thin. Place on the component side and avoid via(s) between these resistors and the device.
- Connect the overcurrent setting resistors from TRIP pin to ground and make the connections as close as possible to the device. The trace from TRIP pin to resistor and from resistor to ground should avoid coupling to a high-voltage switching node.
- Connect the frequency setting resistor from RF pin to ground, or to the VREG pin, and make the connections as close as possible to the device. The trace from the RF pin to the resistor and from the resistor to ground should avoid coupling to a high-voltage switching node.
- Connect the MODE setting resistor from MODE pin to ground, or to the PGOOD pin, and make the connections as close as possible to the device. The trace from the MODE pin to the resistor and from the resistor to ground should avoid coupling to a high-voltage switching node.
- The PCB trace defined as switch node, which connects the LL pins and high-voltage side of the inductor, should be as short and wide as possible.
- Connect the ripple injection V_{OUT} signal (V_{OUT} side of the C1 capacitor in 图 34) from the terminal of ceramic output capacitor. The AC coupling capacitor (C2 in 图 34) should be placed near the device and R7 and C1 can be placed near the power stage.

重要声明

德州仪器(TI) 及其下属子公司有权在不事先通知的情况下, 随时对所提供的产品和服务进行更正、修改、增强、改进或其它更改, 并有权随时中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的硬件产品的性能符合TI 标准保修的适用规范。仅在TI 保证的范围内, 且TI 认为有必要时才会使用测试或其它质量控制技术。除非政府做出了硬性规定, 否则没有必要对每种产品的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险, 客户应提供充分的设计与操作安全措施。

TI 不对任何TI 专利权、版权、屏蔽作品权或其它与使用了TI 产品或服务的组合设备、机器、流程相关的TI 知识产权中授予的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息, 不能构成从TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可, 或是TI 的专利权或其它知识产权方面的许可。

对于TI 的产品手册或数据表, 仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。在复制信息的过程中对内容的篡改属于非法的、欺诈性商业行为。TI 对此类篡改过的文件不承担任何责任。

在转售TI 产品或服务时, 如果存在对产品或服务参数的虚假陈述, 则会失去相关TI 产品或服务的明示或暗示授权, 且这是非法的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

TI 产品未获得用于关键的安全应用中的授权, 例如生命支持应用(在该类应用中一旦TI 产品故障将预计造成重大的人员伤亡), 除非各方官员已经达成了专门管控此类使用的协议。购买者的购买行为即表示, 他们具备有关其应用安全以及规章衍生所需的所有专业技术和知识, 并且认可和同意, 尽管任何应用相关信息或支持仍可能由TI 提供, 但他们将独力负责满足在关键安全应用中使用其产品及TI 产品所需的所有法律、法规和安全相关要求。此外, 购买者必须全额赔偿因在此类关键安全应用中使用TI 产品而对TI 及其代表造成的损失。

TI 产品并非设计或专门用于军事/航空应用, 以及环境方面的产品, 除非TI 特别注明该产品属于“军用”或“增强型塑料”产品。只有TI 指定的军用产品才满足军用规格。购买者认可并同意, 对TI 未指定军用的产品进行军事方面的应用, 风险由购买者单独承担, 并且独力负责在此类相关使用中满足所有法律和法规要求。

TI 产品并非设计或专门用于汽车应用以及环境方面的产品, 除非TI 特别注明该产品符合ISO/TS 16949 要求。购买者认可并同意, 如果他们在汽车应用中使用任何未被指定的产品, TI 对未能满足应用所需要求不承担任何责任。

可访问以下URL 地址以获取有关其它TI 产品和应用解决方案的信息:

产品	应用		
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	http://www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	http://www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	http://www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	http://www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	http://www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	http://www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	http://www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	http://www.ti.com.cn/microcontrollers	无线通信	www.ti.com.cn/wireless
RFID 系统	http://www.ti.com.cn/rfidsys		
RF/IF 和 ZigBee® 解决方案	www.ti.com.cn/radiofre		
TI E2E 工程师社区	http://e2e.ti.com/cn/		

邮寄地址: 上海市浦东新区世纪大道 1568 号, 中建大厦 32 楼 邮政编码: 200122
Copyright © 2011 德州仪器 半导体技术(上海)有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53314RGFR	ACTIVE	VQFN	RGF	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 53314	Samples
TPS53314RGFT	ACTIVE	VQFN	RGF	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 53314	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

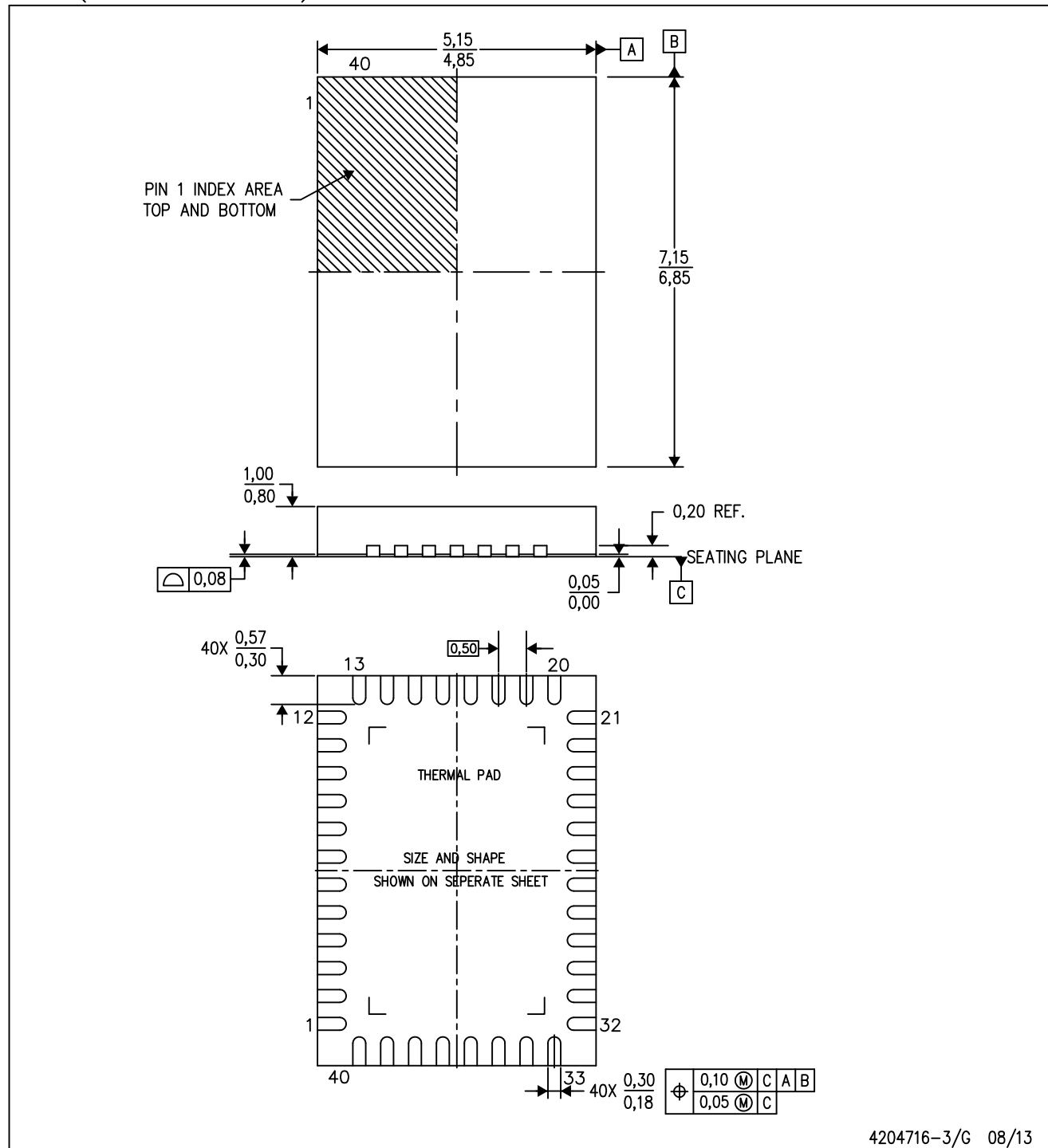
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGF (R-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4204716-3/G 08/13

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding lands and the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGF (R-PVQFN-N40)

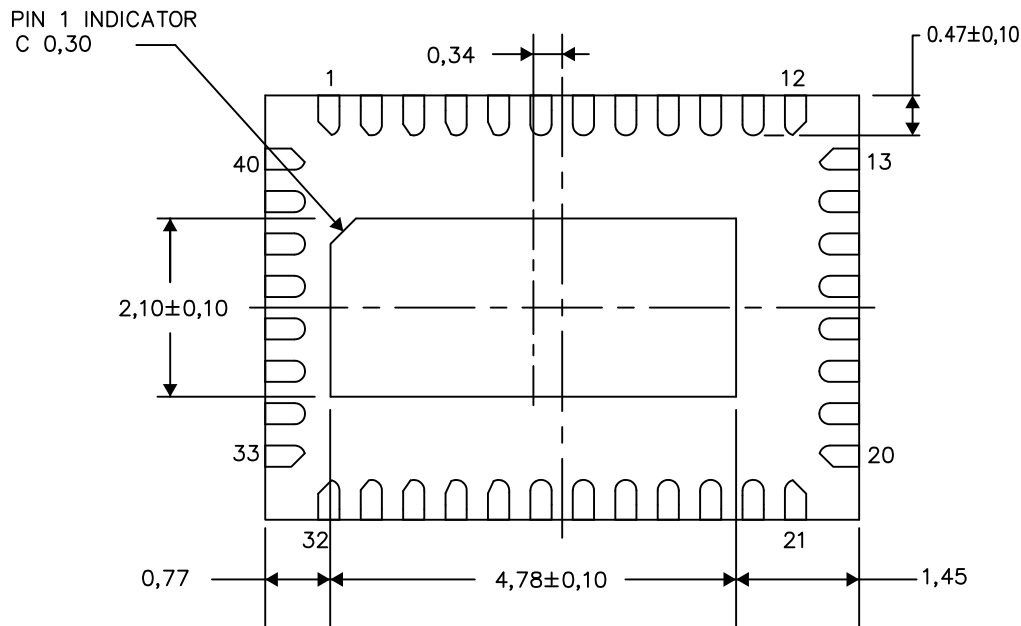
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



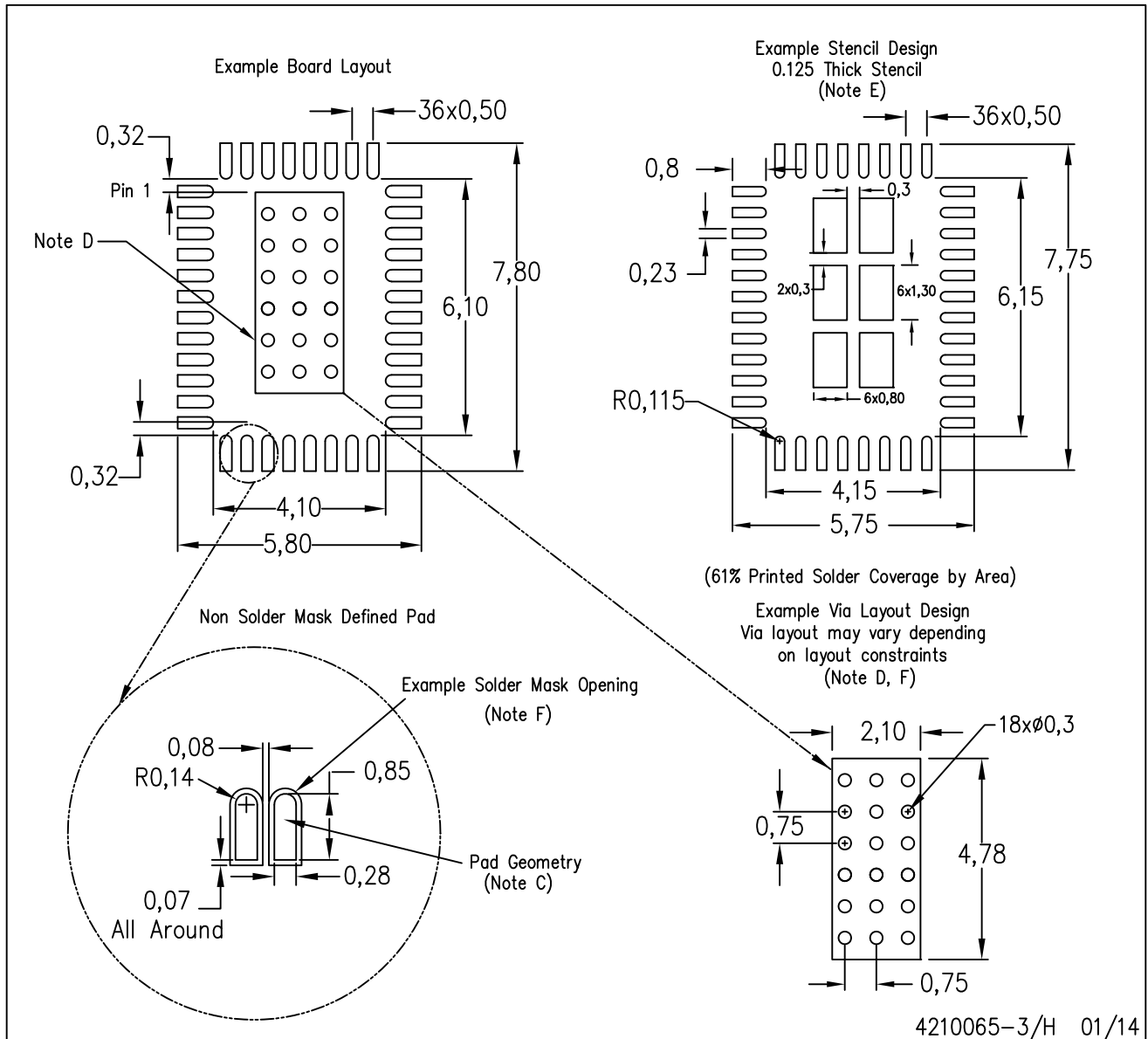
Bottom View
Exposed Thermal Pad Dimensions

4206345-7/N 01/14

NOTE: A. All linear dimensions are in millimeters

RGF (R-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2020 德州仪器半导体技术（上海）有限公司