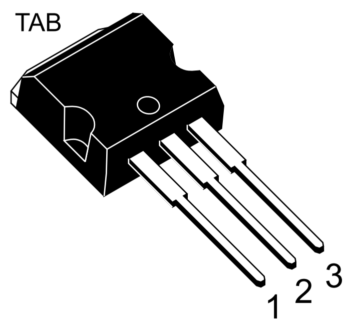
STB130NS04ZB-1

Automotive-grade N-channel clamped, 7 mΩ typ., 80 A fully protected Mesh overlay™ Power MOSFET in a I^2PAK package

Datasheet - production data



Features

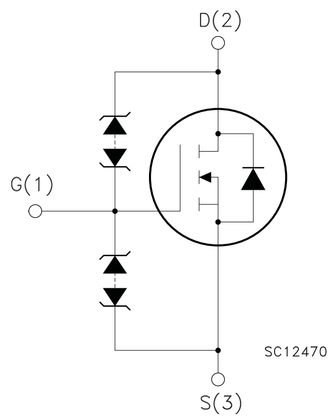
Type	V_{DS}	$R_{DS(on)}$ max.	I_D
STB130NS04ZB-1	Clamped	9 mΩ	80 A

- Designed for automotive applications and AEC-Q101 qualified
- 100% avalanche tested
- Low capacitance and gate charge
- 175°C maximum junction temperature

Applications

- High switching current
- Linear applications

Figure 1. Internal schematic diagram



Description

This fully clamped MOSFET is produced using ST's latest advanced Mesh overlay process, which is based on an innovative strip layout. The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions, such as those encountered in the automotive environment. The device is also well-suited for other applications where extra ruggedness is required.

Table 1. Device summary

Order code	Marking	Package	Packaging
STB130NS04ZB-1	B130NS04ZB	I^2PAK	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	Clamped	V
V_{GS}	Gate-source voltage	Clamped	V
I_D	Drain current (continuous) at T_C = 25°C	80	A
I_D	Drain current (continuous) at T_C = 100°C	60	A
I_{DG}	Drain gate current (continuous)	± 50	mA
I_{GS}	Gate source current (continuous)	± 50	mA
I_{DM}(1)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25°C	300	W
	Derating factor	2.0	W/°C
ESD	Gate-source human body model C=100 pF, R=1.5 kΩ	4	kV
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Pulse width limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	0.50	°C/W
R_{thj-a}	Thermal resistance junction-ambient Max	62.5	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	80	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=30V)	500	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 -40 < Tj < 175 °C	33			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 16 V V_{DS} = 16 V,T_j = 125 °C			10 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±10 V			10	nA
V_{GSS}	Gate-source breakdown voltage	I_{GS}= ± 100µA	18			V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} = I_D = 1 mA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V ,I_D = 40 A		7	9	mΩ

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15V, I_D = 40A	-	50		S
C_{iss}	Input capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0	-	2700		pF
C_{oss}	Output capacitance		-	1275		pF
C_{rss}	Reverse transfer capacitance		-	285		pF
Q_g	Total gate charge	V_{DD}=20V, I_D = 80A V_{GS} =10V (see Figure 15)	-	80	105	nC
Q_{gs}	Gate-source charge		-	20		nC
Q_{gd}	Gate-drain charge		-	27		nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 17.5 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14)	-	40	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	220	-	ns
t_f	Fall time		-	100	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		80	A
I_{SDM}(1)	Source-drain current (pulsed)		-		320	A
V_{SD}(2)	Forward on voltage	I_{SD}=80A, V_{GS}=0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD}=80A, di/dt = 100A/µs, V_{DD}=25V, Tj=150°C (see Figure 16)	-	90		ns
Q_{rr}	Reverse recovery charge		-	0.18		µC
I_{RRM}	Reverse recovery current		-	4		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

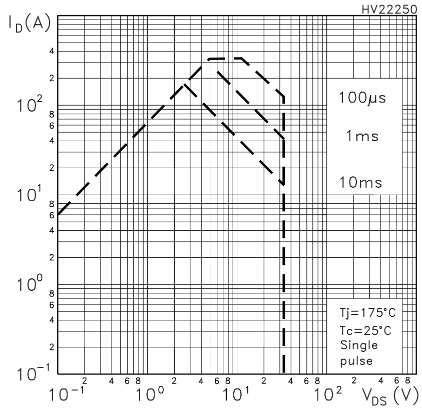


Figure 3. Thermal impedance

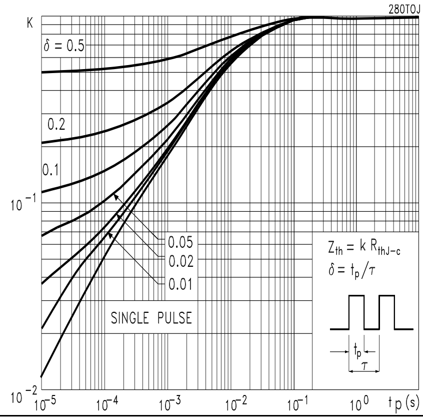


Figure 4. Output characteristics

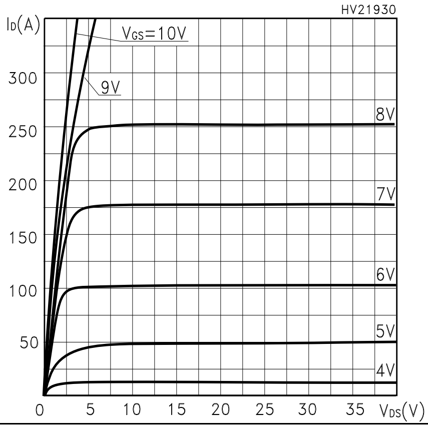


Figure 5. Transfer characteristics

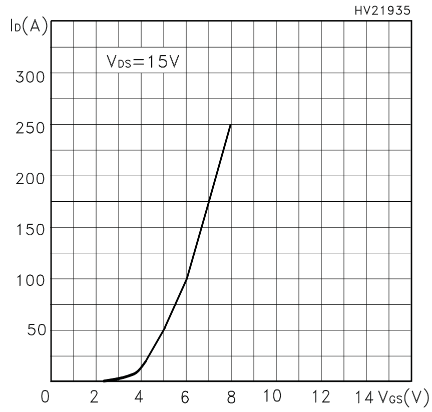


Figure 6. Transconductance

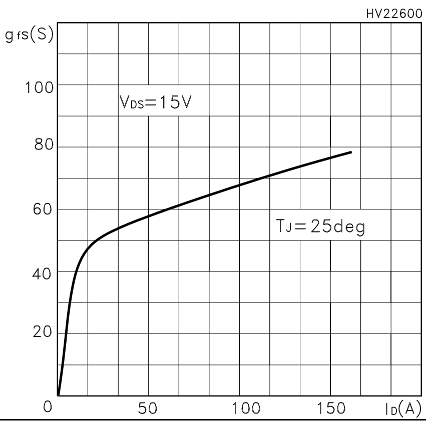


Figure 7. Static drain-source on resistance

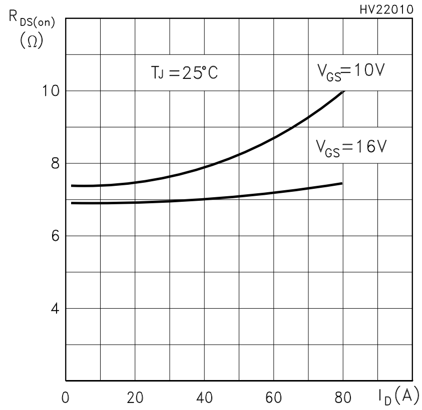


Figure 8. Gate charge vs gate-source voltage

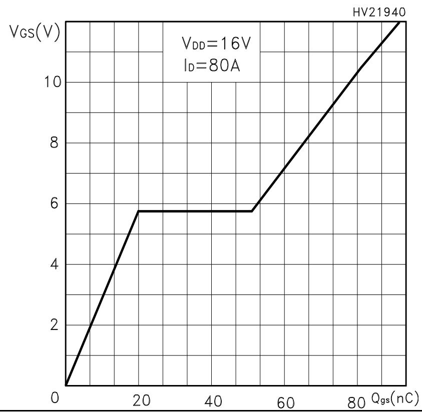


Figure 9. Normalized on resistance vs temperature

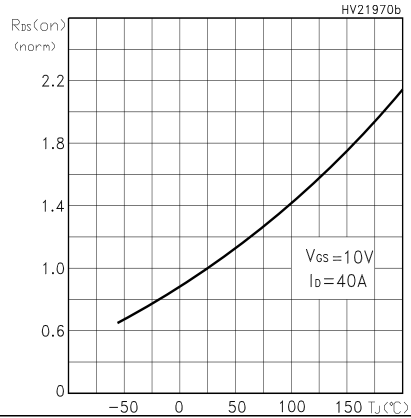


Figure 10. Normalized gate threshold voltage vs temperature

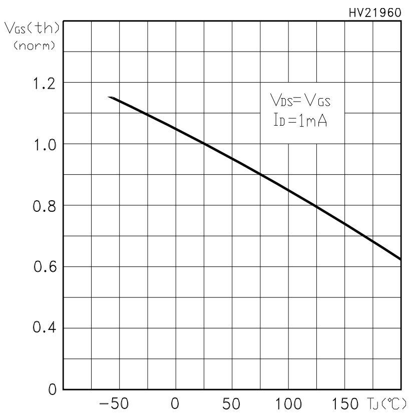


Figure 11. Source-drain diode forward characteristics

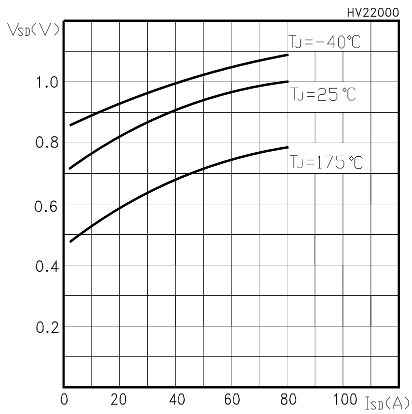


Figure 12. Capacitance variations

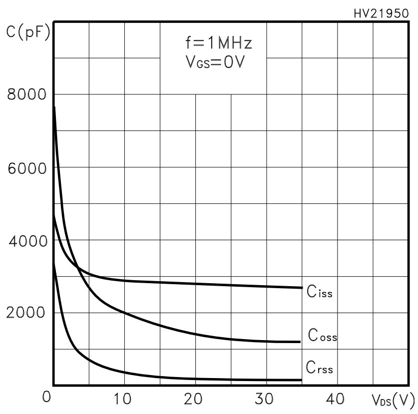
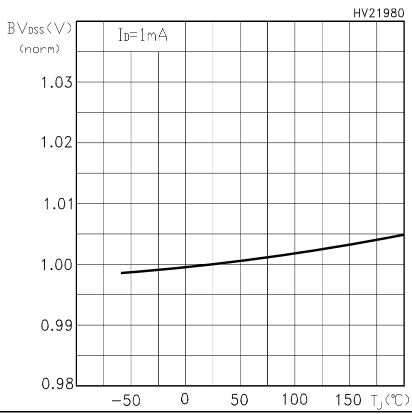


Figure 13. Normalized B_{VDSS} vs temperature



3 Test circuit

Figure 14. Switching times test circuit for resistive load

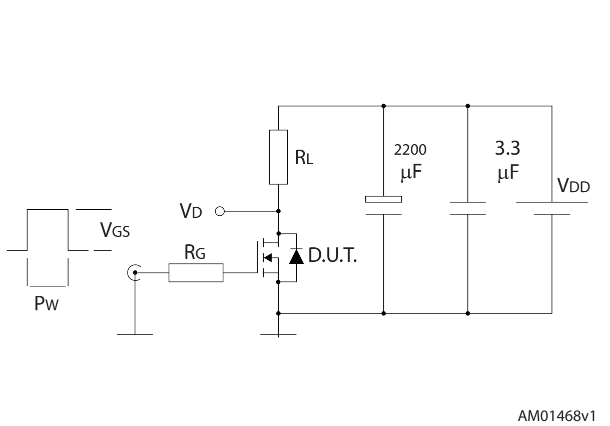


Figure 15. Gate charge test circuit

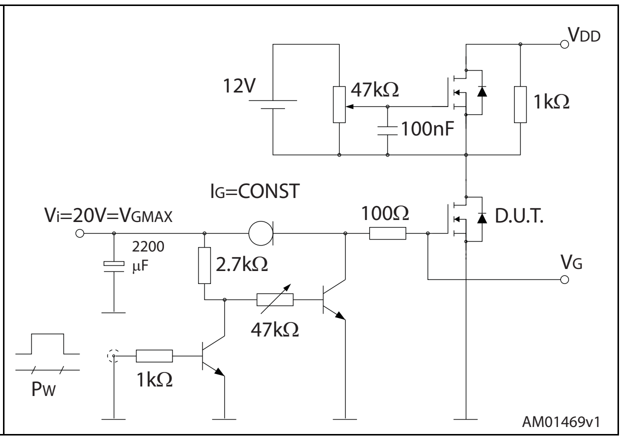


Figure 16. Test circuit for inductive load switching and diode recovery times

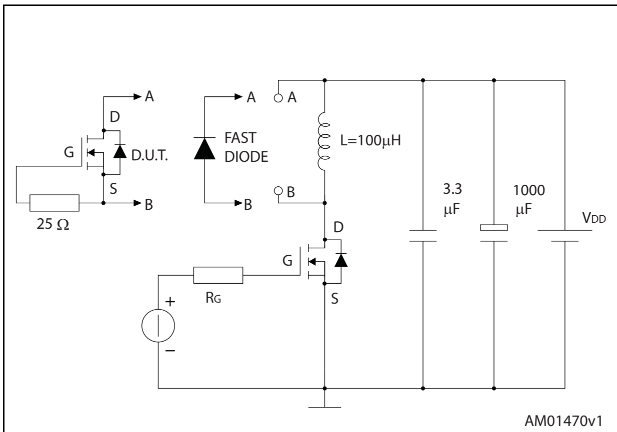


Figure 17. Unclamped Inductive load test circuit

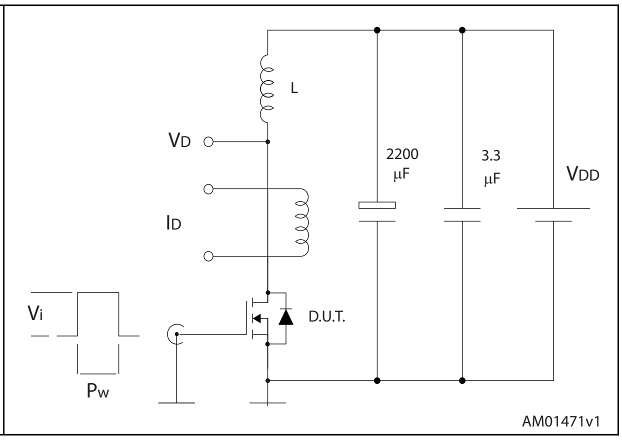


Figure 18. Unclamped inductive waveform

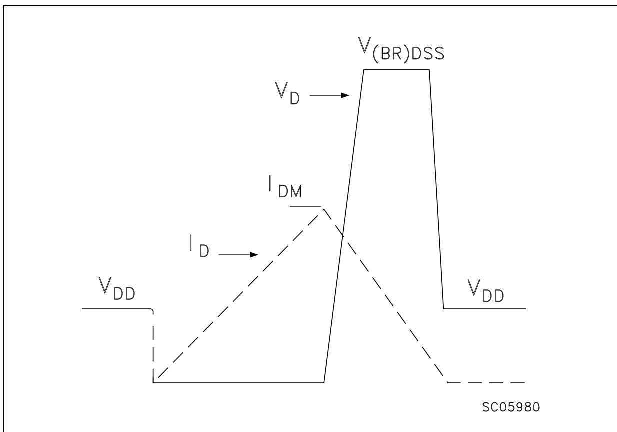
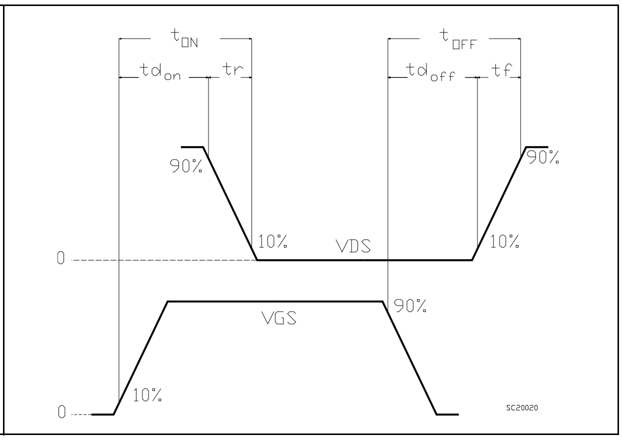


Figure 19. Switching time waveform



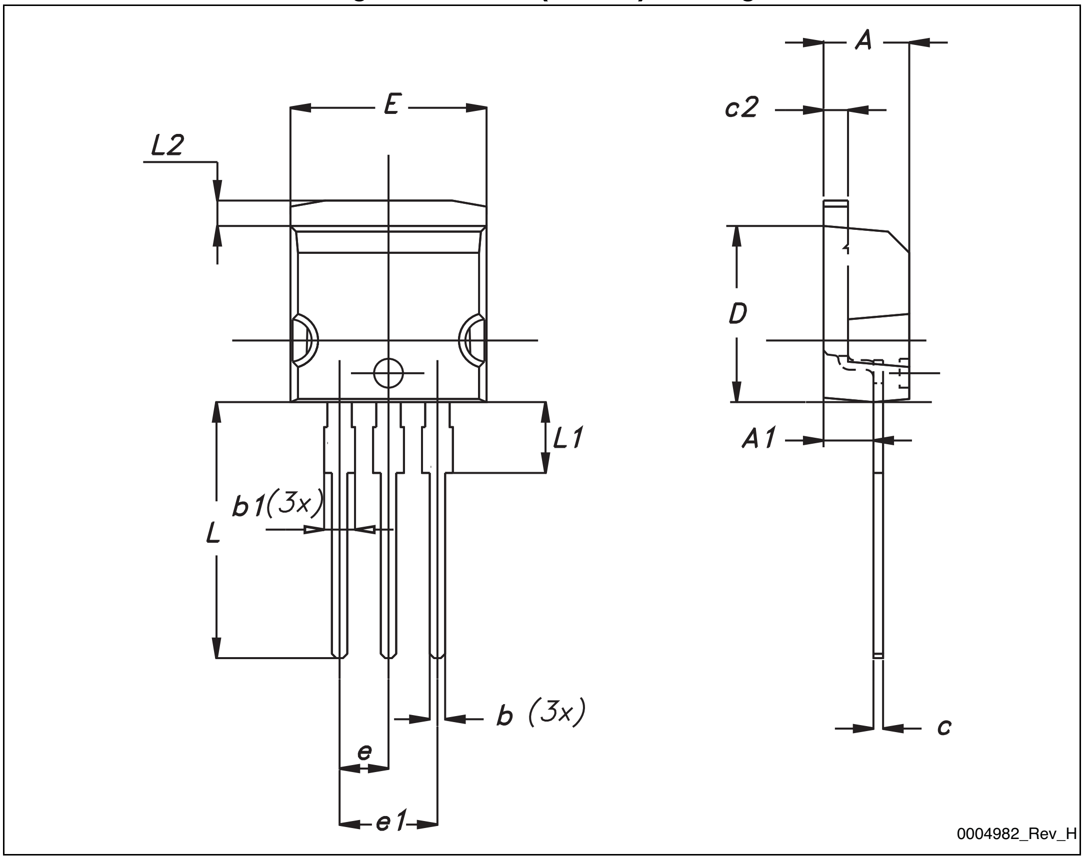
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 20. I²PAK (TO-262) drawing



5 Revision history

Table 10. Revision history

Date	Revision	Changes
16-Sep-2014	1	First release.