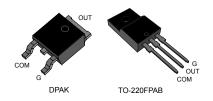
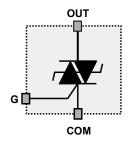


2 A - 800 V overvoltage protected AC switch





FeaturesTriac wi

- Triac with overvoltage crowbar technology
- High noise immunity: static dV/dt > 500 V/µs
- · TO-220FPAB insulated package:
 - complies with UL standards (File ref : E81734)
 - insulation voltage: 2000 V_{RMS}
- · Benefits:
 - Enables equipment to meet IEC 61000-4-5
 - High off-state reliability with planar technology
 - Needs no external overvoltage protection
 - Reduces the power passive component count
 - Interfaces directly with the micro-controller
 - High immunity against fast transients described in IEC 61000-4-4 standards

Applications

- · AC mains static switching in appliance and industrial control systems
- Driving low power highly inductive loads like solenoid, pump, fan, and micromotor

Description

The ACST2 series belongs to the ACS / ACST power switch family. This high performance device is suited to home appliances or industrial systems and drives loads up to 2 $\rm A$.

This ACST2 switch embeds a Triac structure with a high voltage clamping device to absorb the inductive turn-off energy and withstand line transients such as those described in the IEC 61000-4-5 standards. The component needs a low gate current to be activated ($I_{\rm GT}$ < 10 mA) and still shows a high electrical noise immunity complying with IEC standards such as IEC 61000-4-4 (fast transient burst test).

Product status link
ACST2

Product summary		
I _{T(RMS)}	2 A	
V _{DRM} /V _{RRM}	800 V	
I _{GT}	10 mA	



1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter			Value	Unit
	On state was surrout (full sine ways)	TO-220FPAB	T _c = 105 °C		
I _{T(RMS)}	On-state rms current (full sine wave)	DPAK	T _c = 110 °C	2	Α
l	Non repetitive surge peak on-state current	f = 50 Hz	t _p = 20 ms	8.0	
ITSM	T _j initial = 25 °C, (full cycle sine wave)	f = 60 Hz	t _p = 16.7 ms	8.4	A
I ² t	I ² t for fuse selection	·	t _p = 10 ms	0.5	A ² s
dI/dt	Critical rate of rise on-state current $I_G = 2 \times I_{GT}$, tr $\leq 100 \text{ ns}$ $f = 120 \text{ Hz}$ $T_j =$		T _j = 125 °C	50	A/µs
V _{PP} ⁽¹⁾	Non repetitive line peak pulse voltage ⁽¹⁾	2	kV		
P _{G(AV)}	Average gate power dissipation	0.1	W		
P _{GM}	Peak gate power dissipation (t _p = 20 μs)	10	W		
I _{GM}	Peak gate current (t _p = 20 μs)	1.6	Α		
T _{stg}	Storage temperature range	-40 to +150	°C		
T _j	Operating junction temperature range	-40 to +125	°C		
T _L	Lead temperature for soldering during 10 s (at 3 mm from plas	260	°C		
V _{ins}	Insulation rms voltage (60 seconds)	2000	V		

^{1.} according to test described by standard IEC 61000-4-5, see Figure 16 for conditions

Table 2. Electrical characteristics (T_j = 25 °C, unless otherwise specified)

Symbol	Test conditions Quadra			Value	Unit
I _{GT} ⁽¹⁾	$V_{OLIT} = 12 \text{ V, R}_{I} = 33 \Omega$	1 - 11 - 111	Max.	10	mA
V _{GT}	V001 - 12 V, N 33 M	1-11-111	Max.	1.1	V
$V_{\sf GD}$	$V_{OUT} = V_{DRM}$, $R_L = 3.3 \text{ k}\Omega$, $T_j = 125 ^{\circ}\text{C}$	1 - 11 - 111	Min.	0.2	V
IH ⁽²⁾	I _{OUT} = 100 mA	Max.	10	mA	
IL	a = 1.2 x lgr	1 - 111	Max.	25	mA
'L	1G - 1.2 × 1G	II		35	
dV/dt ⁽²⁾	V_{OUT} = 67% V_{DRM} , gate open, T_j = 125 °C	Min.	500	V/µs	
(dl/dt)c ⁽²⁾	$(dV/dt)c = 15 V/\mu s, T_j = 125 °C$	Min.	0.5	A/ms	
V _{CL}	I _{CL} = 0.1 mA, t _p = 1 ms		Min.	850	V

^{1.} Minimum I_{GT} is guaranteed at 5% of I_{GT} max

DS5161 - Rev 6 page 2/15

^{2.} For both polarities of OUT pin referenced to COM pin



Table 3. Static characteristics

Symbol	Test condition	Test conditions			Unit
V _{TM} ⁽¹⁾	I _{OUT} = 2.8 A, t _p = 500 μs	T _j = 25 °C	Max.	2	V
V _{T0} ⁽¹⁾	Threshold voltage	T _j = 125 °C	Max.	0.9	V
R _D ⁽¹⁾	Dynamic resistance	T _j = 125 °C	Max.	250	mΩ
I _{DRM}	V _{OUT} = V _{DRM} / V _{RRM}	T _j = 25 °C	Max.	10	μΑ
I _{RRM}	VOUI - VDRM/ VRRM	T _j = 125 °C	ividx.	0.5	mA

^{1.} For both polarities of OUT pin referenced to COM pin

Table 4. Thermal characteristics

Symbol	Parameter		Value	Unit
D.,	Junction to case for full cycle sine wave conduction	DPAK	4.5	
R _{th(j-c)}	Juniculon to case for full cycle sine wave conduction	TO-220FPAB	7	90.004
В	Junction to ambient	TO-220FPAB	60	°C/W
R _{th(j-a)}	Junction to ambient, S _{CU} ⁽¹⁾ = 0.5 cm ²	DPAK	70	

^{1.} S_{CU} = copper surface under tab

DS5161 - Rev 6 page 3/15



1.1 Characteristics (curves)

Figure 1. Maximum power dissipation versus on-state RMS current (full cycle)

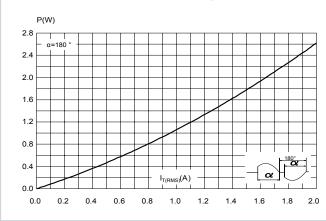


Figure 2. On-state RMS current versus case temperature

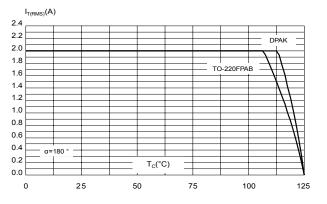


Figure 3. On-state RMS current versus ambient temperature

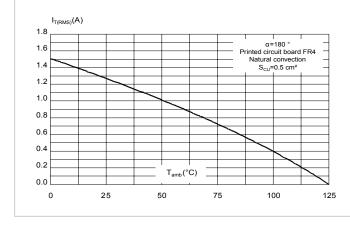


Figure 4. Relative variation of thermal impedance junction to case versus pulse duration (TO-220FPAB)

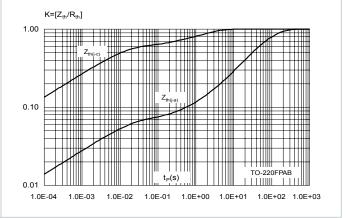


Figure 5. Relative variation of thermal impedance junction to case versus pulse duration (DPAK)

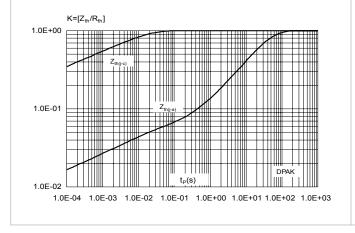
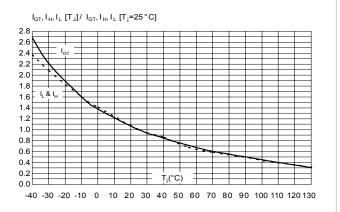


Figure 6. Relative variation of gate trigger, holding and latching current versus junction temperature (typical value)



DS5161 - Rev 6 page 4/15



Figure 7. Relative variation of static dV/dt versus junction temperature

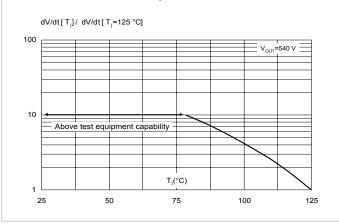


Figure 8. Relative variation of critical rate of decrease of main current versus reapplied dV/dt (typical values)

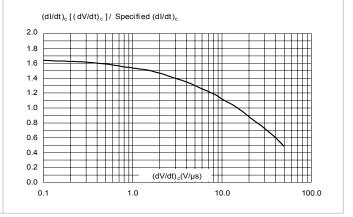


Figure 9. Relative variation of critical rate of decrease of main current versus junction temperature

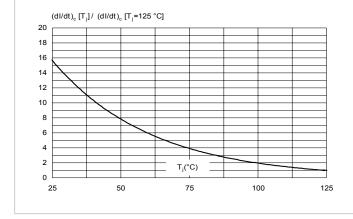


Figure 10. Surge peak on-state current versus number of cycles

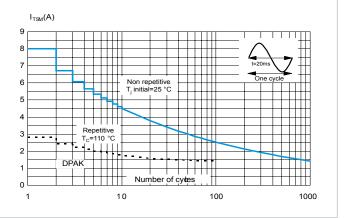


Figure 11. Non repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10 ms and corresponding value

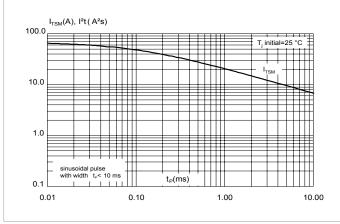
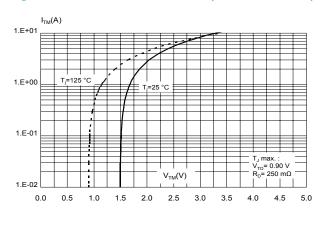


Figure 12. On-state characteristics (maximum values)



DS5161 - Rev 6 page 5/15



Figure 13. Thermal resistance junction to ambient versus copper surface under tab (typical values)

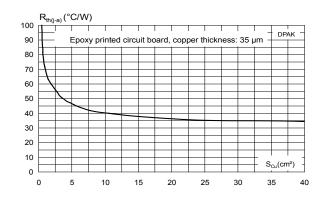
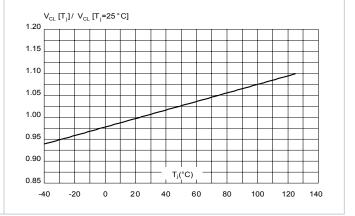


Figure 14. Relative variation of clamping voltage V_{CL} versus junction temperature



DS5161 - Rev 6 page 6/15

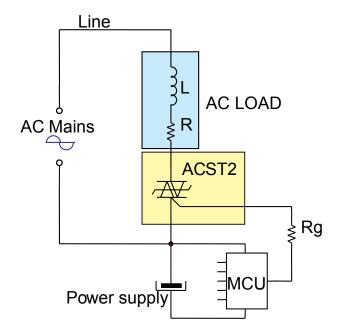


2 Application information

2.1 Typical application descriptions

The ACST2 device has been designed to switch on and off highly inductive or resistive loads such as pump, valve, fan, or bulb lamp. Thanks to its high sensitivity (I_{GT} max = 10 mA), the ACST2 can be driven directly by logic level circuits through a resistor as shown on the typical application diagram. Thanks to its thermal and turn-off commutation performances, the ACST2 switch can drive, without any additional snubber, an inductive load up to 2 A.

Figure 15. AC induction motor control – typical diagram



DS5161 - Rev 6 page 7/15



2.2 AC line transient voltage ruggedness

In comparison with standard Triacs, which are not robust against surge voltage, the ACST2 is self-protected against over-voltage, specified by the new parameter V_{CL} . In addition, the ACST2 is a sensitive device (I_{GT} = 10 mA), but provides a high noise immunity level against fast transients. The ACST2 switch can safely withstand AC line transient voltages either by clamping the low energy spikes, such as inductive spikes at switch off, or by switching to the on state (for less than 10 ms) to dissipate higher energy shocks through the load. This safety feature works even with high turn-on current ramp up.

The test circuit of Figure 16 represents the ACST2 application, and is used to stress the ACST switch according to the IEC 61000-4-5 standard conditions. With the additional effect of the load which is limiting the current, the ACST switch withstands the voltage spikes up to 2 kV on top of the peak line voltage. The protection is based on an overvoltage crowbar technology. The ACST2 folds back safely to the on state as shown in Figure 17. The ACST2 recovers its blocking voltage capability after the surge and the next zero current crossing. Such a non repetitive test can be done at least 10 times on each AC line voltage polarity.

Figure 16. Overvoltage ruggedness test circuit for resistive and inductive loads for IEC 61000-4-5 standards

Surge generator

2kV surge

Rgene

ACST210-8x

Rg

Rg

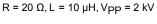
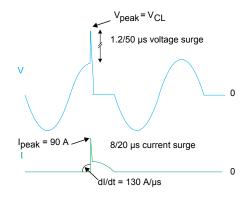


Figure 17. Typical voltage and current waveforms across the ACST4 during IEC 61000-4-5 standard test



DS5161 - Rev 6 page 8/15



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 TO-220FPAB package information

- Epoxy meets UL94, V0
- Recommended torque: 0.4 to 0.6 N·m

Dia L6 L2 *L7* L3 F1 L4 F2 -G1-

Figure 18. TO-220FPAB package outline

DS5161 - Rev 6 page 9/15



Table 5. TO-220FPAB package mechanical data

	Dimensions					
Ref.	Millimeters		Incl	hes		
	Min.	Max.	Min.	Max.		
Α	4.40	4.60	0.1739	0.1818		
В	2.5	2.7	0.0988	0.1067		
D	2.50	2.75	0.0988	0.1087		
E	0.45	0.70	0.0178	0.0277		
F	0.75	1.0	0.0296	0.0395		
F1	1.15	1.70	0.0455	0.0672		
F2	1.15	1.70	0.0455	0.0672		
G	4.95	5.20	0.1957	0.2055		
G1	2.40	2.70	0.0949	0.1067		
Н	10.00	10.40	0.3953	0.4111		
L2	16.00	0 typ.	0.632	4 typ.		
L3	28.60	30.60	1.1304	1.2095		
L4	9.80	10.6	0.3874	0.4190		
L5	2.90	3.60	0.1146	0.1423		
L6	15.90	16.40	0.6285	0.6482		
L7	9.00	9.30	0.3557	0.3676		
Dia	3.0	3.20	0.1186	0.1265		

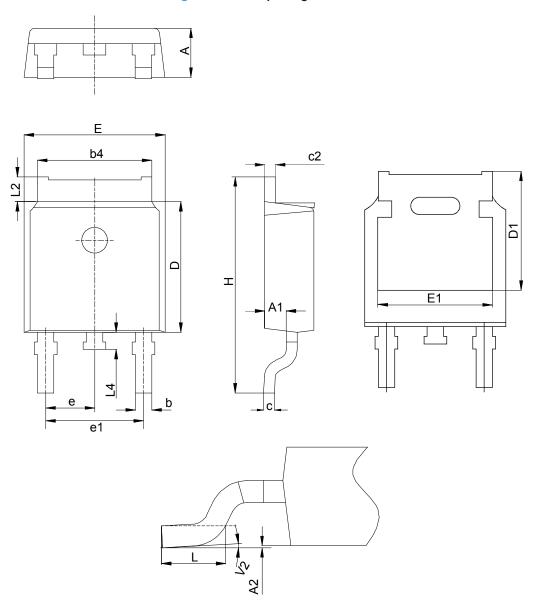
DS5161 - Rev 6 page 10/15



3.2 DPAK package information

- Molding compouned resin is halogen free and meets UL94 flammability standard, level V0
- · Lead-free package leads plating

Figure 19. DPAK package outline



DS5161 - Rev 6 page 11/15



	Dimensions					
Ref.		Millimeters		Inches ⁽¹⁾		
	Min.	Тур.	Max.	Min.	Тур.	Max.
А	2.18		2.40	0.0858		0.0945
A1	0.90		1.10	0.0354		0.0433
A2	0.03		0.23	0.0012		0.0091
b	0.64		0.90	0.0252		0.354
b4	4.95		5.46	0.1949		0.2150
С	0.46		0.61	0.0181		0.0240
c2	0.46		0.60	0.0181		0.0236
D	5.97		6.22	0.2350		0.2449
D1	4.95		5.60	0.1949		0.2205
E	6.35		6.73	0.2500		0.2650
E1	4.32		5.50	0.1701		0.2165
е		2.286			0.0900	
e1	4.40		4.70	0.1732		0.1850
Н	9.35		10.40	0.3681		0.4094
L	1.00		1.78	0.0394		0.0701
L2			1.27			0.0500
L4	0.60		1.02	0.0236		0.0402
V2 ⁽²⁾	-8°		+8°	-8°		+8°

Table 6. DPAK package mechanical data

Note:

This package drawing may slightly differ from the physical package. However, all the specified dimensions are guaranteed.

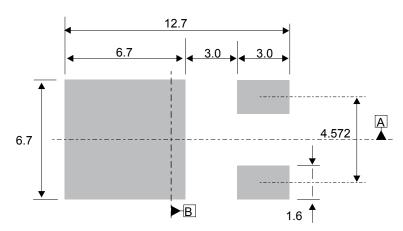


Figure 20. DPAK recommended footprint (dimensions are in mm)

The device must be positioned within $\bigcirc 0.05 \text{ AB}$

DS5161 - Rev 6 page 12/15

^{1.} Dimensions in inches are given for reference only

^{2.} Degree



4 Ordering information

Figure 21. Ordering information scheme

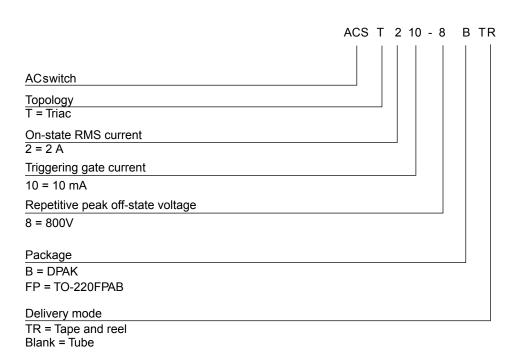


Table 7. Ordering information

Order code	Marking	Package	Weight	Base qty.	Packing mode
ACST210-8B		DPAK	0.2 a	50	Tube
ACST210-8BTR	ACST2108	DPAK	0.3 g	2500	Tape and reel
ACST210-8FP		TO-220FPAB	2.4 g	50	Tube

DS5161 - Rev 6 page 13/15



Revision history

Table 8. Document revision history

Date	Version	Changes
01-Mar-2007	1	Initial release.
13-Apr-2010	2	Updated ECOPACK statement. Reformatted for consistency with other datasheets in this product class.
01-Jul-2010	3	Updated Figure 22.
24-May-2014	4	Updated DPAK package information and reformatted to current standard.
14-Jun-2017	5	Updated features in cover page and Table 2. Updated Figure 8, Figure 9, Figure 10, Figure 14 and Section 3. Minor text changes.
19-Dec-2019	6	Update DPAK package information.

DS5161 - Rev 6 page 14/15



IMPORTANT NOTICE - PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics - All rights reserved

DS5161 - Rev 6 page 15/15