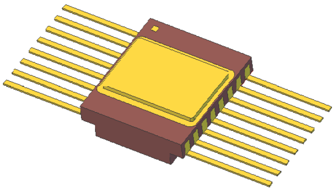
RHFLVDS325

Rad-hard quad LVDS receiver

Datasheet - production data



Ceramic Flat-16

The upper metallic lid is electrically connected to ground

Features

- LVDS input
- CMOS output
- ANSI TIA/EIA-644 compliant
- 400 Mbps (200 MHz)
- Cold spare on all pins
- Fail-safe function
- 3.3 V operating power supply
- 4.8 V absolute rating
- Power consumption: 43 mW at 3.3 V
- Hermetic package
- Large input common mode: -1 V to +4 V
- Guaranteed up to 300 krad TID
- SEL immune up to 135 MeV.cm²/mg
- SET/SEU immune up to 32 MeV.cm²/mg

Description

The RHFLVDS325 is a quad, low-voltage differential signaling (LVDS) receiver specifically designed, packaged and qualified for use in aerospace environments in a low-power and fast data transmission standard.

The circuit features an internal fail-safe function to ensure a known state in case of an input short circuit or a floating input.

All pins have cold spare buffers to ensure they are in high impedance when V_{CC} is tied to GND.

Designed using ST's proprietary CMOS process with specific mitigation techniques, the RHFLVDS325 achieves “best in the class” for hardness to total ionisation dose and heavy ions.

The RHFLVDS325 can operate over a large temperature range of -55 °C to +125 °C and is housed in a hermetic Ceramic Flat-16 package.

Table 1. Device summary

Reference	SMD pin	Quality level	Package	Lead finish	Mass	EPPL(1)	Temp. range
RHFLVDS325K1	-	Engineering model	Ceramic Flat-16	Gold	0.65 g	-	-55 °C to 125 °C
RHFLVDS325K01V	5962F98652	QML-V Flight				Target	

1. EPPL = ESA preferred part list

Contents

1 Functional description

Figure 1. Logic diagram and logic symbol

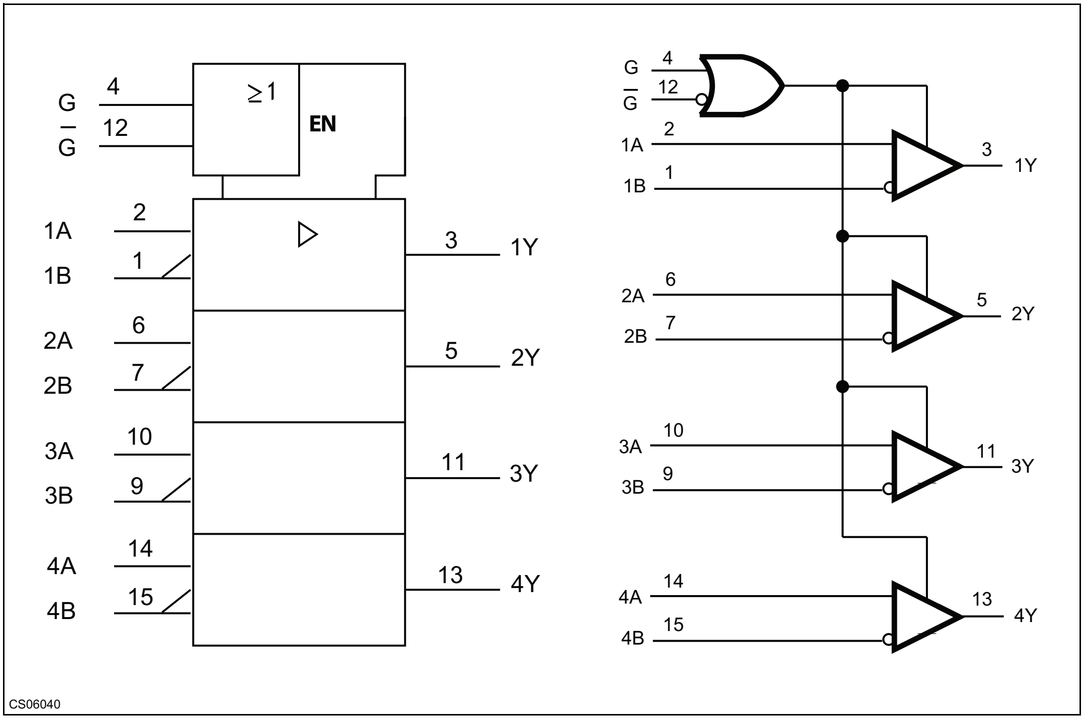


Table 2. Truth table

Differential inputs	Enables		Output
A, B	G	$\overline{G}$	Y
$V_{ID} \geq 100$ mV	H	X	H
	X	L	H
-100 mV < V_{ID} < 100 mV	H	X	?
	X	L	?
$V_{ID} \leq -100$ mV	H	X	L
	X	L	L
X	L	H	Z
Open/Short or terminated	H	X	H
	X	L	H

Note: 1 *The G input features an internal pull-up network. The $\overline{G}$ input features an internal pull-down network. If they are floating the circuit is enabled.*

2 *Vid = V_{IA}-V_{IB}*

3 *L = low level, H = high Level, X = irrelevant, Z = high impedance (off). ? = intermediate*

2 Pin configuration

Figure 2. Pin connections (top view)

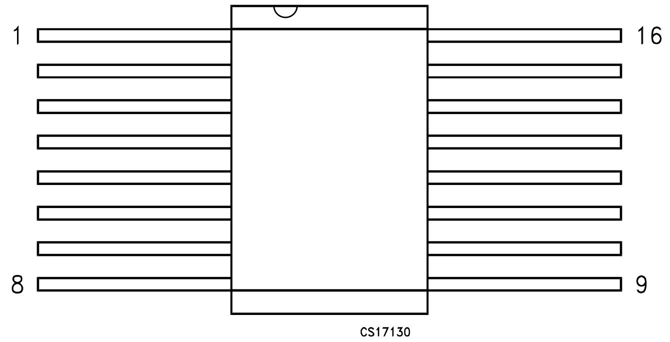


Table 3. Pin description

Pin number	Symbol	Name and function
2, 6, 10, 14	1A to 4A	Receiver inputs
1, 7, 9, 15	1B to 4B	Negated receiver inputs
3, 5, 11, 13	1Y to 4Y	Receiver outputs
4	G	Enable
12	$\overline{G}$	
8	GND	Ground
16	V_{CC}	Supply voltage

3 Maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	4.8	V
V_i	TTL inputs (operating or cold-spare)	-0.3 to 4.8	
V_{OUT}	TTL outputs (operating or cold-spare)	-0.3 to 4.8	
V_{CM}	LVDS common mode (operating or cold-spare)	-2 to +5	
T_{stg}	Storage temperature range	-65 to +150	°C
T_j	Maximum junction temperature	+150	
R_{thjc}	Thermal resistance junction to case(2)	22	°C/W
ESD	HBM: Human body model – All pins excepted LVDS inputs – LVDS inputs vs. GND	2 8	kV
	CDM: Machine model	500	V

1. All voltages, except differential I/O bus voltage, are with respect to the network ground terminal.
2. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.

Table 5. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{CM}	Static common mode on the receiver	- 1		+ 4	
T_A	Ambient temperature range	-55		+125	°C

4 Radiation

Total dose (MIL-STD-883 TM 1019)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHFLVDS325 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, between 50 and 300 rad/s only (full CMOS technology).

All parameters provided in *Table 7: Electrical characteristics* apply to both pre- and post-irradiation, as follows:

- All test are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

Heavy ions

The behavior of the product when submitted to heavy ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 6. Radiations

Type	Characteristics	Value	Unit
TID	High-dose rate (50 - 300 rad/sec) up to:	300	krad
Heavy ions	SEL immune up to: (with a particle angle of 60 ° at 125 °C)	135	MeV.cm²/mg
	SEL immune up to: (with a particle angle of 0 ° at 125 °C)	67	
	SET/SEU immune up to: (at 25 °C)	32	

5 Electrical characteristics

In *Table 7* below, V_{CC} = 3 V to 3.6 V, capa-load (CL) = 10 pF, typical values are at T_{amb} = +25 °C, min. and max values are at T_{amb} = - 55 °C and + 125 °C unless otherwise specified

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Total enabled supply current, receivers enabled, not switching	V_{ID} = 400 mV		13	15	mA
I_{CCZ}	Total disabled supply current, receivers disabled	V_{ID} = 400 mV G = GND and $\overline{G}$ = V_{CC}			4	
I_{OFF}	LVDS input power-off leakage current(1)	V_{CC} = 0 V, V_{IN} = -1 V to 4 V	-60		60	µA
	TTL I/O power-off leakage current(1)	V_{CC} = 0 V, V_{IN}, G and $\overline{G}$ = 3.6 V, V_{OUT} = 3.6 V	-10		10	
V_{IH}	Enable threshold high level	G and $\overline{G}$ inputs	2		V_{CC}	V
V_{IL}	Enable threshold low level		GND		0.8	
I_{IH}	High level input current	G and $\overline{G}$ inputs V_{CC} = 3.6 V, V_{IN} = V_{CC}	-10		10	µA
I_{IL}	Low level input current	G and $\overline{G}$ inputs V_{CC} = 3.6 V, V_{IN} = 0	-10		10	
V_{TL}	Differential input low threshold	V_{CM} = 1.2 V			-100	mV
V_{TH}	Differential input high threshold	V_{CM} = 1.2 V	100			
V_{CL}	TTL input clamp voltage	I_{CL} = 18 mA	-1.5			V
V_{CMR}	Common mode voltage range	V_{ID} = 200 mVp-p	- 1		4	V
V_{CMREJ}	Common mode rejection(2)	F = 10 MHz		300		mVp-p
I_{ID}	Differential input current	V_{ID} = 400 mVp-p	-10		10	µA
I_{ICM}	Common mode input current	V_{IC} = - 1V to + 4V	-70		70	
V_{OH}	Output voltage high	I_{OH} = -0.4 mA, V_{CC} = 3 V	2.7			V
V_{OL}	Output voltage low	I_{OL} = 2 mA, V_{CC} = 3 V			0.25	
I_{OS}	Output short-circuit current	V_{OUT} = 0 V	-90		-30	mA
I_{OZ}	Output tri-state current	Disabled, V_{OUT} = 0 V or V_{CC}	-10		10	µA
C_{IN}	Input capacitance	On each LVDS input vs. GND		3		pF
R_{out}	Output resistance			45		Ω
t_{PHLD}	Propagation delay time, high to low output	V_{ID} = 200 mVp-p, input pulse from 1.1 V to 1.3 V, V_{CM} = 1.2 V Load: refer to *Figure 3*	1		3.5	ns
t_{PLHD}	Propagation delay time, low to high output		1		3.5	

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{SK1}	Channel to channel skew[3]	V_{ID} = 200 mVp-p Load: refer to *Figure 3*			0.6	ns
t_{SK2}	Chip to chip skew[4][5]				3	
t_{SKD}	Differential skew[6] (t_{PHLD}-t_{PLHD})				0.6	
t_{PLZ}	Propagation delay time, low level to high impedance output	Load: refer to *Figure 4*			12	
t_{PHZ}	Propagation delay time, high level to high impedance output				12	
t_{PZH}	Propagation delay time, high impedance to high level output				12	
t_{PZL}	Propagation delay time, high impedance to low level output				12	
t_{D1}	Fail-safe to active time			1		µs
t_{D2}	Active to fail-safe time			1		

1. All pins except pin under test and V_{CC} are floating.
2. Guaranteed by characterization on the bench.
3. t_{SK1} is the maximum delay time difference between all outputs of the same device (measured with all inputs connected together).
4. t_{SK2} is the maximum delay time difference between outputs of all devices when they operate with the same supply voltage, at the same temperature.
5. Guaranteed by design. t_{SKD} is the maximum delay time difference between t_{PHLD}-t_{PLHD}
6. t_{SKD} is the maximum delay time difference between t_{PHLD} and t_{PLHD}, see *Figure 3*.

Cold sparing

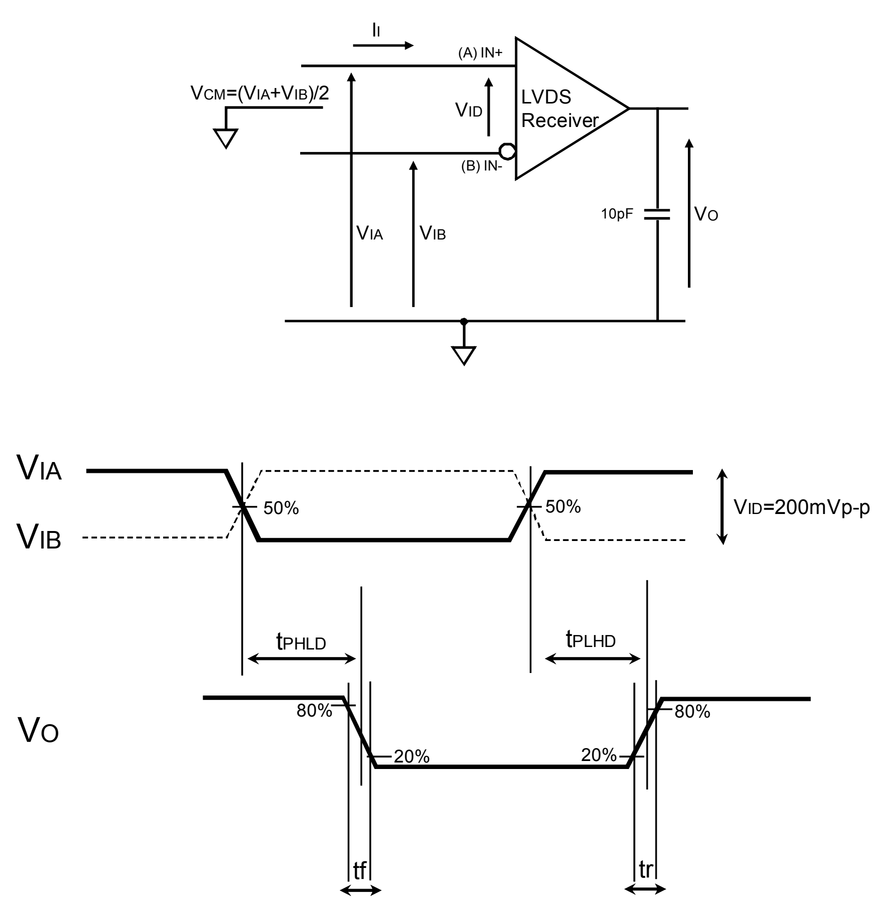
The RHFLVDS325 features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V (V_{CC} = GND) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices to be kept powered off so that they can be switched on only when required. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between the I/Os and V_{CC}. The ESD protection is ensured through a non-conventional dedicated structure.

Fail-safe

In many applications, inputs need a fail-safe function to avoid an uncertain output state when the inputs are not connected properly. In case of an LVDS input short circuit or floating inputs, the TTL outputs remain in stable logic-high state.

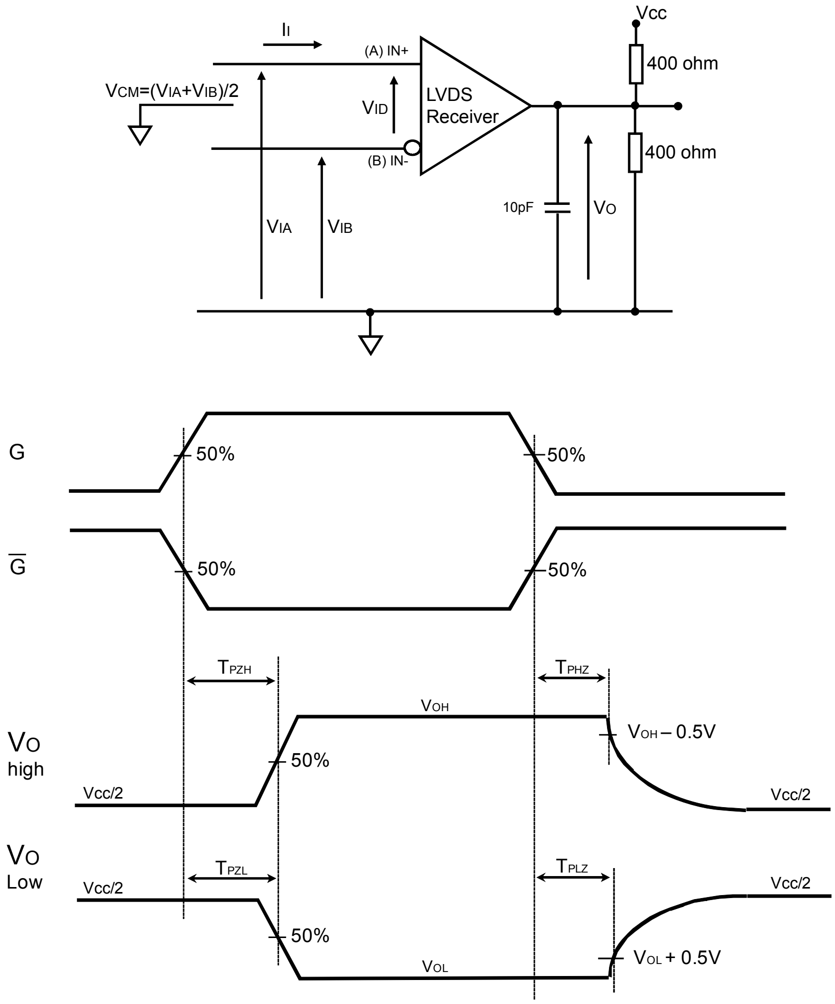
6 Test circuit

Figure 3. Timing test circuit and waveform



1. All input pulses are supplied by a generator with the following characteristics: t_r or t_f ≤ 1 ns, f = 1 MHz, Z_O = 50 Ω, and duty cycle = 50%.
2. The product is guaranteed in test with CL = 10 pF

Figure 4. Enable and disable time test circuit and waveform



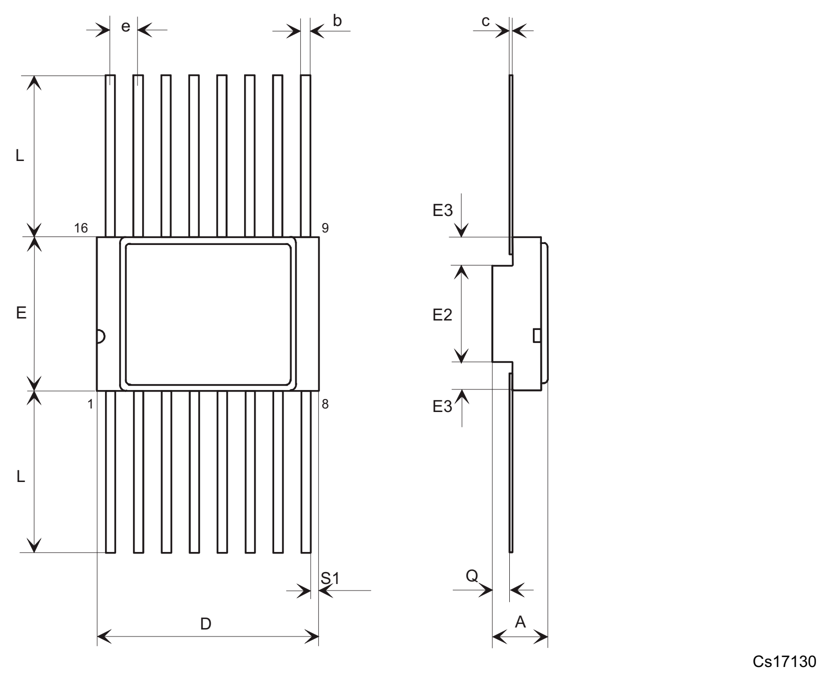
1. All input pulses (including G and $\overline{G}$) are supplied by a generator with the following characteristics: t_r or t_f ≤ 1 ns, f_G or $f_{\overline{G}}$ = 500 kHz, and pulse width G or $\overline{G}$ = 500 ns.
2. *The product is guaranteed in test with CL = 10 pF*

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 Ceramic Flat-16 package information

Figure 5. Ceramic Flat-16 package mechanical drawing



1. The upper metallic lid is electrically connected to ground.

Table 8. Ceramic Flat-16 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.31		2.72	0.091		0.107
b	0.38		0.48	0.015		0.019
c	0.10		0.18	0.004		0.007
D	9.75		10.13	0.384		0.399
E	6.75		7.06	0.266		0.278
E2		4.32			0.170	
E3	0.76			0.030		
e		1.27			0.050	
L	6.35		7.36	0.250		0.290
Q	0.66		1.14	0.026		0.045
S1	0.13			0.005		

8 Ordering information

Table 9. Order codes

Order code	Description	Temp. range	Package	Marking[1]	Packing
RHFLVDS325K1	Engineering model	-55 °C to 125 °C	Ceramic Flat-16	RHFLVDS325K1	Strip pack
RHFLVDS325K01V	QML-V flight			TBD	

1. Specific marking only. Complete marking includes the following:
- SMD pin (on QML-V flight only)
- ST logo
- Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)
- QML logo (Q or V)
- Country of origin (FR = France).

Note: *Contact your ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.*

9 Shipping information

Date code

The date code is structured as follows:

- Engineering model: EM xyywwz
- QML flight model: FM yywwz

Where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

10 Revision history

Table 10. Document revision history

Date	Revision	Changes
21-Oct-2015	1	Initial release
28-Apr-2017	2	*Table 1: Device summary*: added mass value