STD5N65M6

N-channel 650 V, 1.15 Ω typ., 4 A MDmesh™ M6 Power MOSFET in a DPAK package

Datasheet - production data

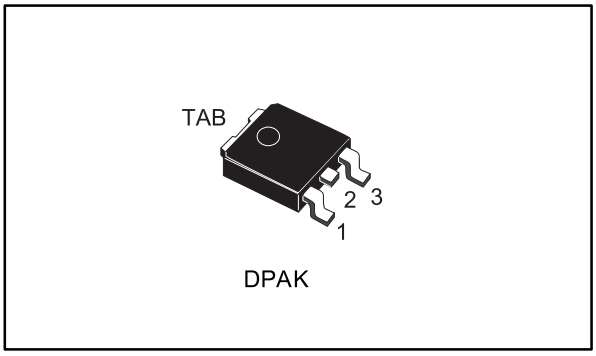
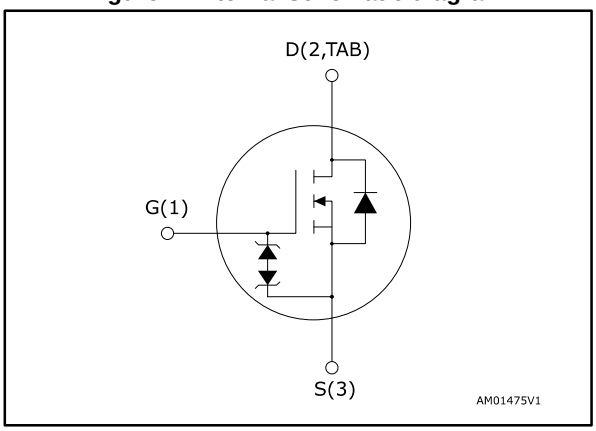


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD5N65M6	650 V	1.3 Ω	4 A

- Reduced switching losses
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ * area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STD5N65M6	5N65M6	DPAK	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	4	A
I_D	Drain current (continuous) at T_C = 100 °C	2.5	A
I_{DM}(1)	Drain current (pulsed)	16	A
P_{TOT}	Total dissipation at T_C = 25 °C	45	W
dv/dt(2)	Peak diode recovery voltage slope	5	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

(1)Pulse width limited by safe operating area

(2)$I_{SD} \leq 4$ A, di/dt = 400 A/µs; $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD} = 400 V

(3)$V_{DS} \leq 520$ V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.78	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	50	

Notes:

(1)When mounted on FR-4 board of inch², 2oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1	A
E_{as}	Single pulse avalanche energy (starting T_j=25°C, I_D= I_{AR}, V_{DD}=50 V)	90	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V; T_C = 125 °C (1)			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.25	3	3.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2 A		1.15	1.3	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	170	-	pF
C_{oss}	Output capacitance		-	20	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	35	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0 A	-	5	-	Ω
Q_g	Total gate charge	V_{DD} = 350 V, I_D = 1 A, V_{GS}= 10 V, (see *Figure 15: "Test circuit for gate charge behavior"*)	-	5.1	-	nC
Q_{gs}	Gate-source charge		-	0.8	-	nC
Q_{gd}	Gate-drain charge		-	2	-	nC

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 325 V, I_D = 2 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Test circuit for resistive load switching times"* and *Figure 19: "Switching time waveform"*)	-	6.5	-	ns
t_r	Rise time		-	5.9	-	ns
$t_{d(off)}$	Turn-off delay time		-	17.4	-	ns
t_f	Fall time		-	15.2	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4	A
I_{SDM}(1)	Source-drain current (pulsed)		-		16	A
V_{SD}(2)	Forward on voltage	I_{SD} = 4 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 4 A, di/dt = 100 A/µs, V_{DD} = 60 V, (see *Figure 19: "Switching time waveform"*)	-	222		ns
Q_{rr}	Reverse recovery charge		-	1.24		µC
I_{RRM}	Reverse recovery current		-	11.2		A
t_{rr}	Reverse recovery time	I_{SD} = 4 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 19: "Switching time waveform"*)	-	264		ns
Q_{rr}	Reverse recovery charge		-	1.39		µC
I_{RRM}	Reverse recovery current		-	10.5		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

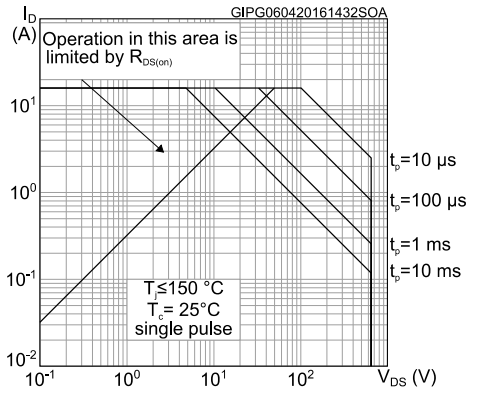


Figure 3: Thermal impedance

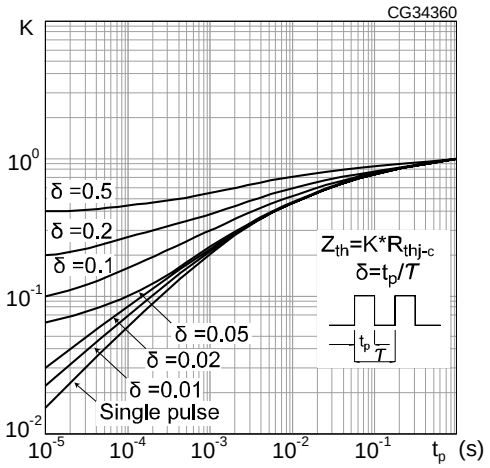


Figure 4: Output characteristics

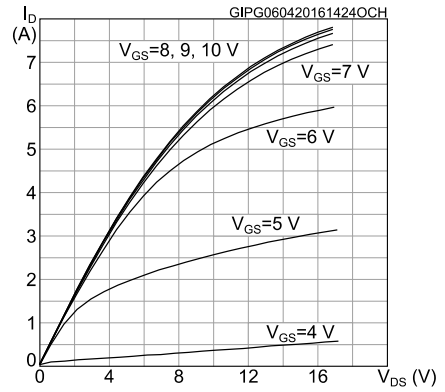


Figure 5: Transfer characteristics

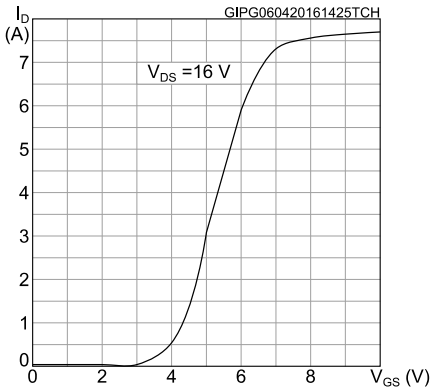


Figure 6: Gate charge vs gate-source voltage

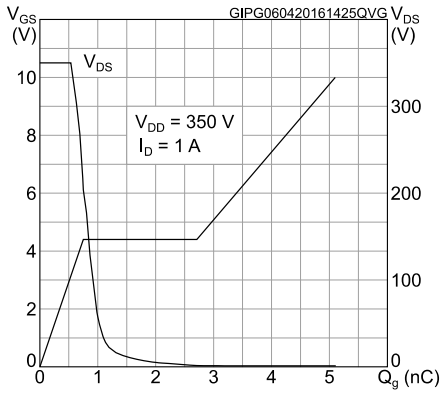


Figure 7: Static drain-source on-resistance

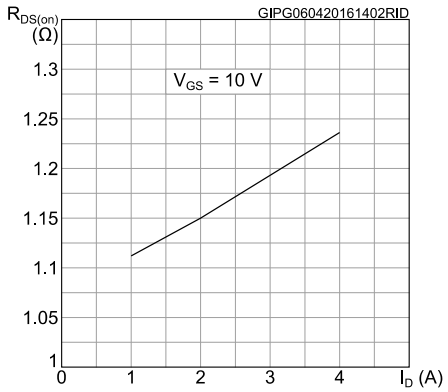


Figure 8: Capacitance variations

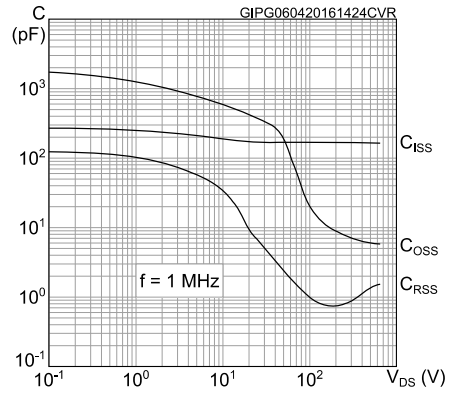


Figure 9: Normalized gate threshold voltage vs temperature

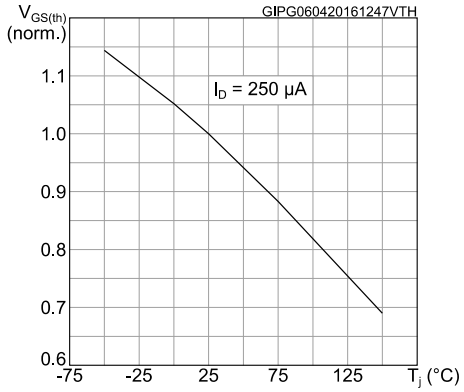


Figure 10: Normalized on-resistance vs temperature

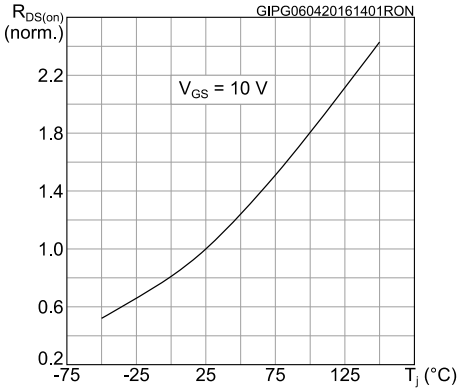


Figure 11: Normalized V(BR)DSS vs temperature

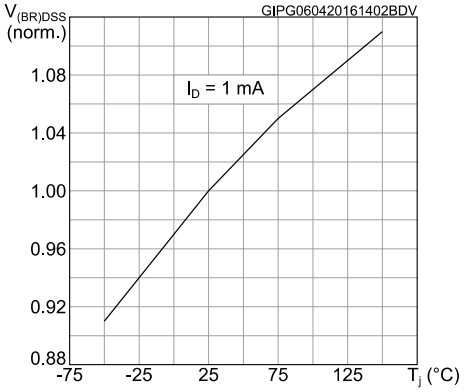


Figure 12: Output capacitance stored energy

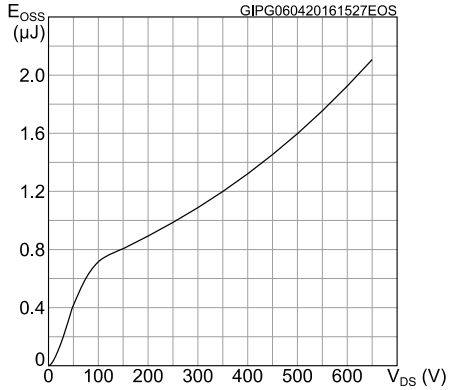
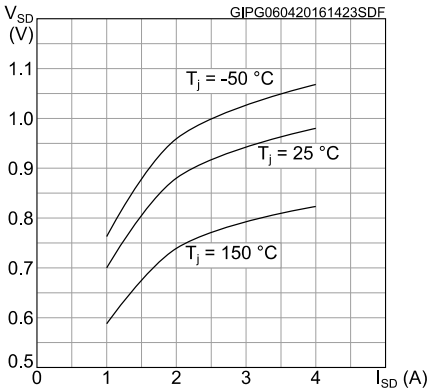


Figure 13: Source-drain diode forward characteristics



3 Test circuits

Figure 14: Test circuit for resistive load switching times

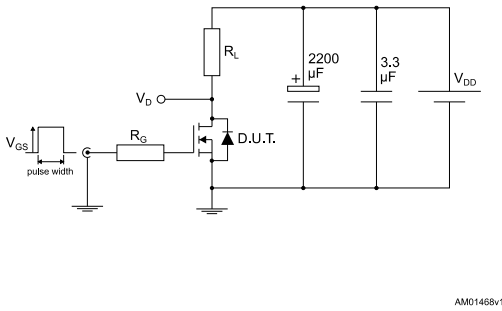


Figure 15: Test circuit for gate charge behavior

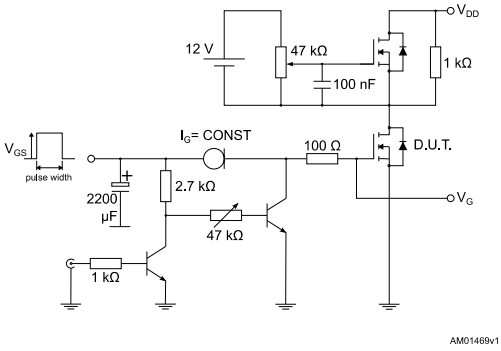


Figure 16: Test circuit for inductive load switching and diode recovery times

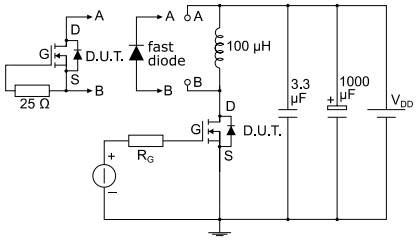


Figure 17: Unclamped inductive load test circuit

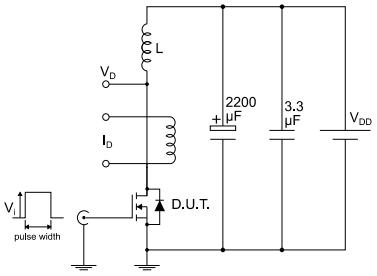


Figure 18: Unclamped inductive waveform

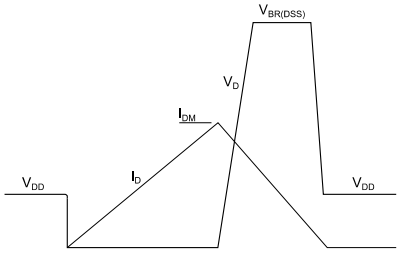
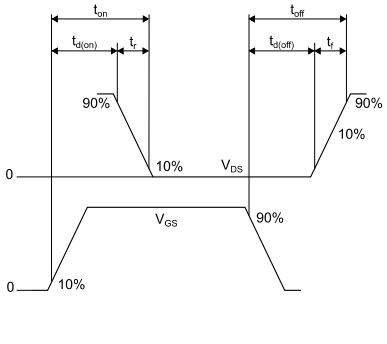


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) package information

Figure 20: DPAK (TO-252) type A package outline

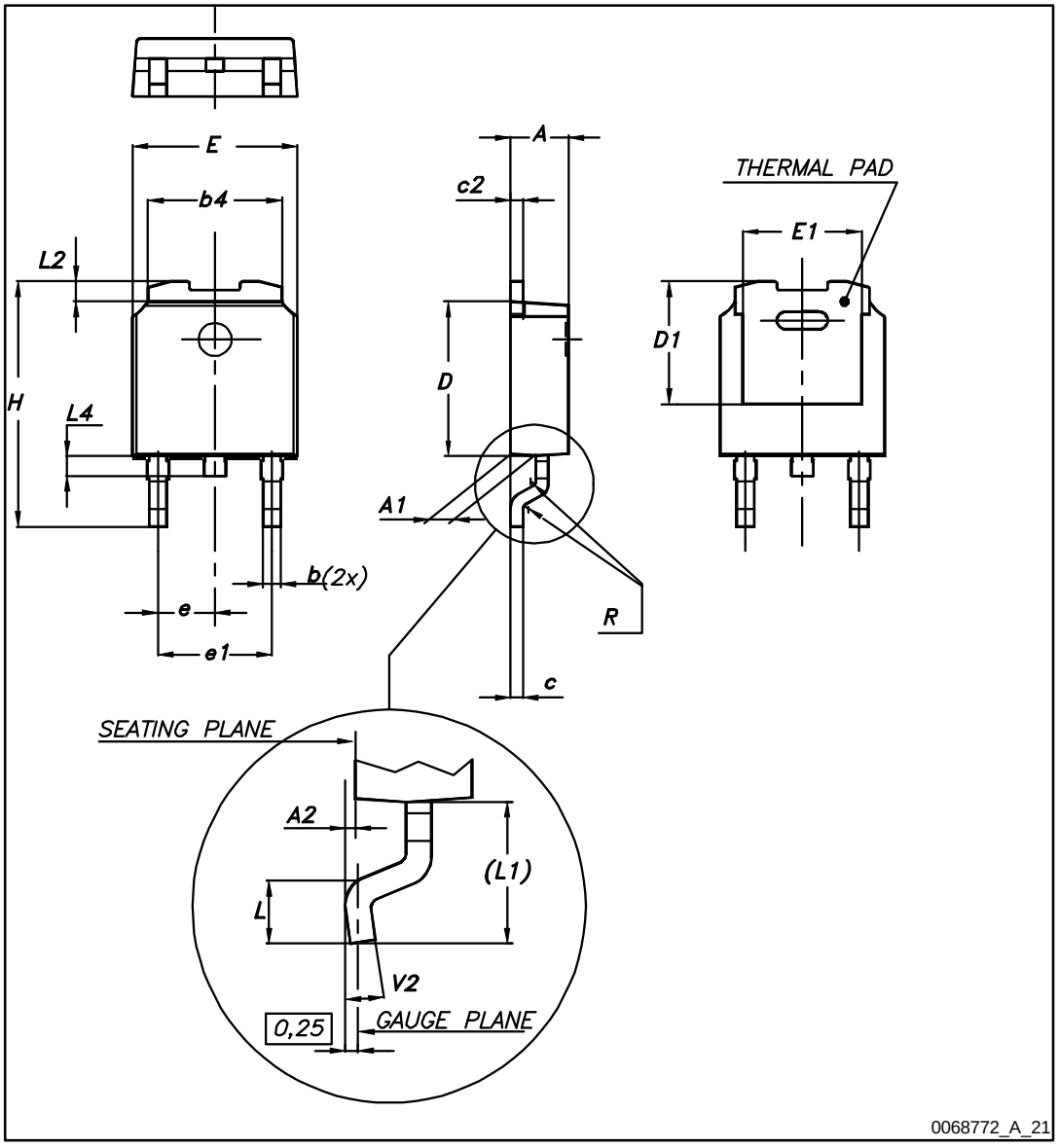
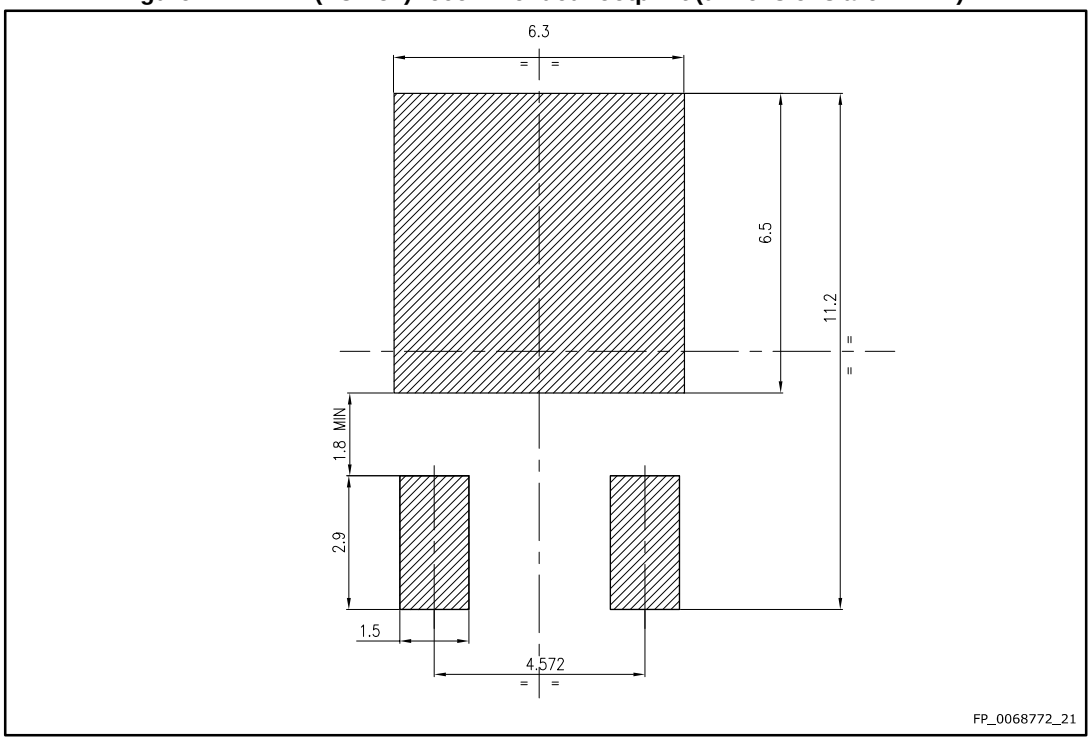


Table 9: DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) packing information

Figure 22: DPAK (TO-252) tape outline

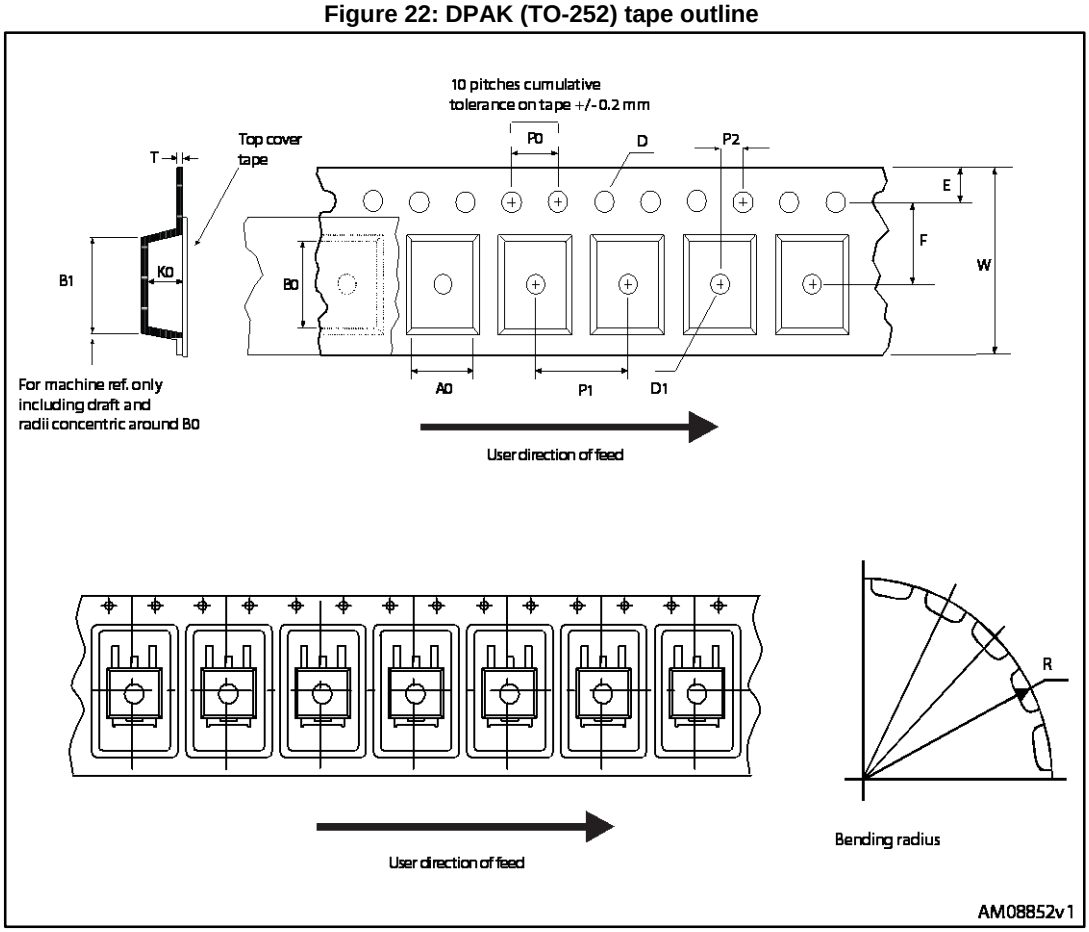


Figure 23: DPAK (TO-252) reel outline

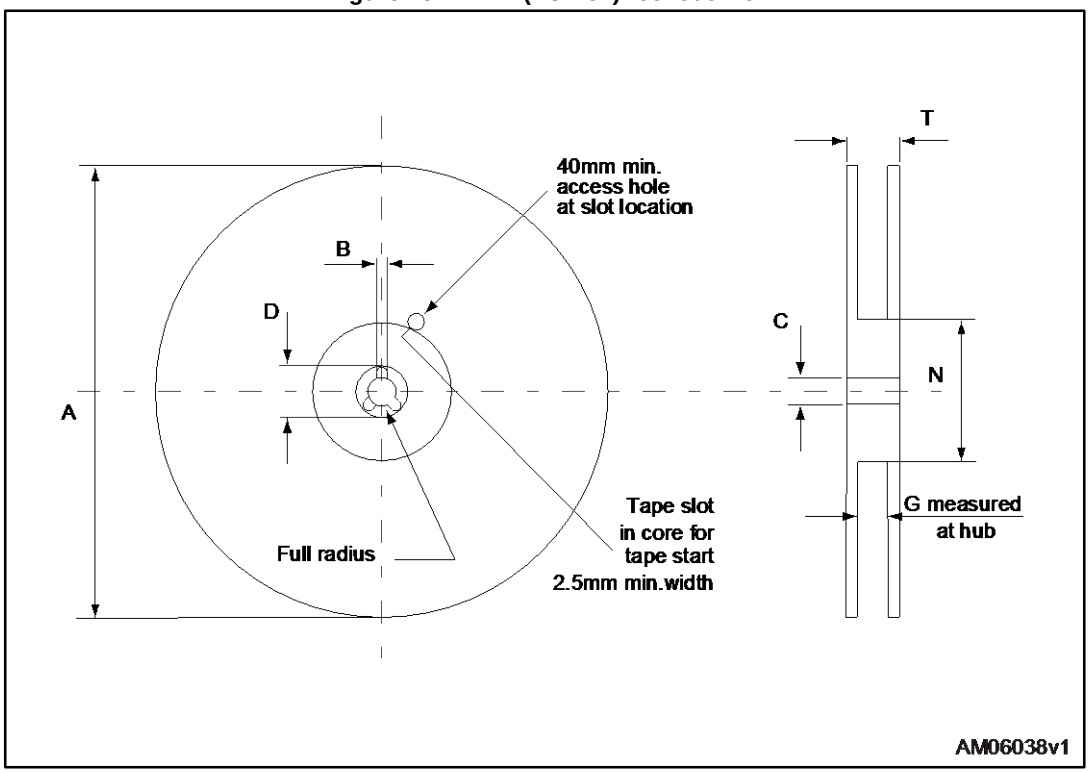


Table 10: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
05-May-2016	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.