STF45N10F7



N-channel 100 V, 0.0145 Ω typ., 30 A, STripFET™ VII DeepGATE™ Power MOSFET in a TO-220FP package

Datasheet - production data

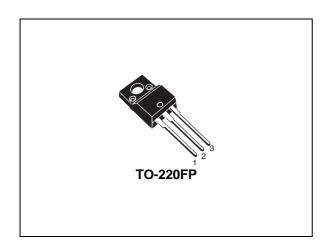
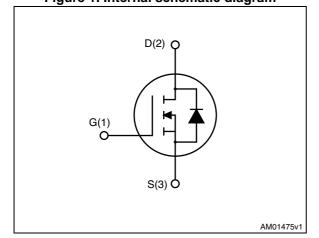


Figure 1. Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max. ⁽¹⁾	I _D	P _{TOT}
STF45N10F7	100 V	$0.018~\Omega$	30 A	25 W

- 1. @ VGS = 10 V
- Ultra low on-resistance
- 100% avalanche tested

Applications

· Switching applications

Description

This device utilizes the 7th generation of design rules of ST's proprietary STripFETTM technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STF45N10F7	45N10F7	TO-220FP	Tube

Contents STF45N10F7

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STF45N10F7 Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	100	V
V _{GS}	Gate-source voltage	20	V
I _D	Drain current (continuous) at T _C = 25 °C	30	Α
I _D	Drain current (continuous) at T _C = 100 °C	21.4	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	120	Α
P _{TOT}	Total dissipation at T _c = 25 °C	25	W
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;TC=25 °C)		V
TJ	Operating junction temperature	-55 to 175	°C
T _{stg}	Storage temperature	-55 10 175	°C

^{1.} Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case		°C/W
R _{thj-amb}	thj-amb Thermal resistance junction-ambient		°C/W

Electrical characteristics STF45N10F7

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage (V _{GS} = 0)	I _D = 1 mA	100		-	٧
1	Zero gate voltage drain	V _{DS} = 100 V			10	μΑ
I _{DSS} current (current (V _{GS} = 0)	V _{DS} = 100 V; T _C =125 °C			100	μΑ
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.5		4.5	٧
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 15 A		0.0145	0.018	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	1640	-	pF
C _{oss}	Output capacitance	$V_{DS} = 50 \text{ V, f} = 1 \text{ MHz,}$ $V_{GS} = 0$	-	360	i	pF
C _{rss}	Reverse transfer capacitance		-	25	-	pF
Qg	Total gate charge	V _{DD} = 50 V, I _D = 30 A V _{GS} = 10 V	-	25	-	nC
Q _{gs}	Gate-source charge		-	5.1	-	nC
Q _{gd}	Gate-drain charge	Figure 14	-	12.2	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 50 \text{ V}, I_{D} = 15 \text{ A},$ $R_{G} = 4.7 \Omega, V_{GS} = 10 \text{ V}$ Figure 13	-	15	-	ns
t _r	Rise time		-	17	-	ns
t _{d(off)}	Turn-off delay time		-	24	-	ns
t _f	Fall time		-	8	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		30	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		120	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 30 A, V _{GS} = 0	-		1.1	٧
t _{rr}	Reverse recovery time	I _{SD} = 30 A,	-	53		ns
Q _{rr}	Reverse recovery charge	$di/dt = 100 A/\mu s$,	-	67		nC
I _{RRM}	Reverse recovery current	$V_{DD} = 80 \text{ V}, T_j = 150 ^{\circ}\text{C}$	-	2.5		Α

^{1.} Pulse width limited by safe operating area.

^{2.} Pulsed: pulse duration=300 μ s, duty cycle 1.5%.

Electrical characteristics STF45N10F7

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance

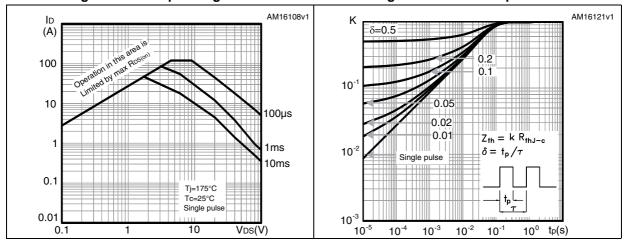


Figure 4. Output characteristics

Figure 5. Transfer characteristics

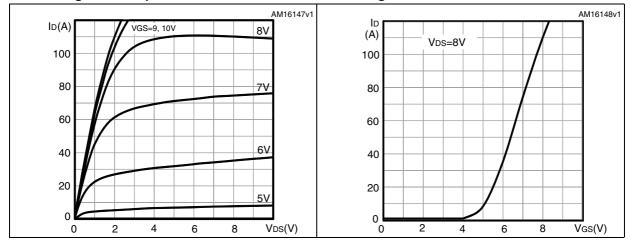


Figure 6. Gate charge vs gate-source voltage

Figure 7. Static drain-source on-resistance

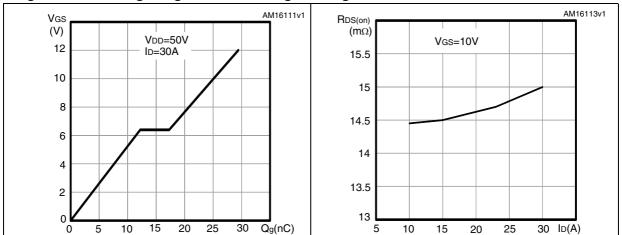
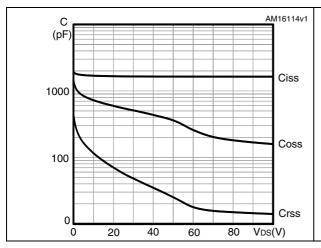


Figure 8. Capacitance variations

Figure 9. Normalized gate threshold voltage vs temperature



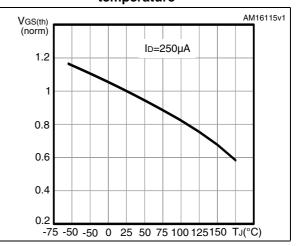
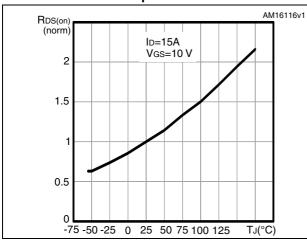


Figure 10. Normalized on-resistance vs temperature

Figure 11. Normalized $V_{(BR)DS}$ vs temperature



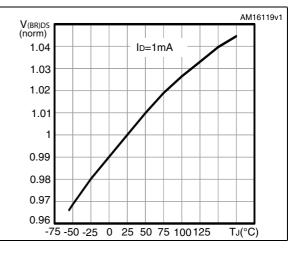
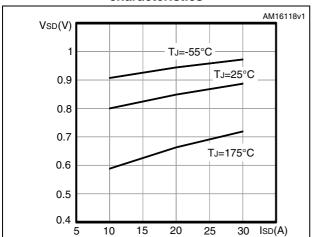


Figure 12. Source-drain diode forward characteristics





Test circuits STF45N10F7

3 Test circuits

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

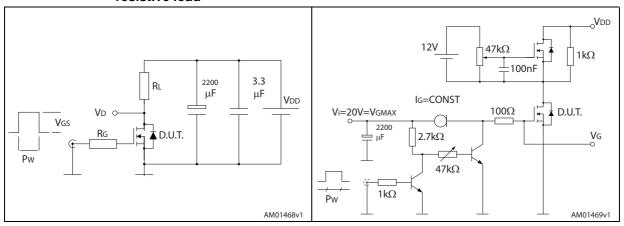


Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped inductive load test circuit

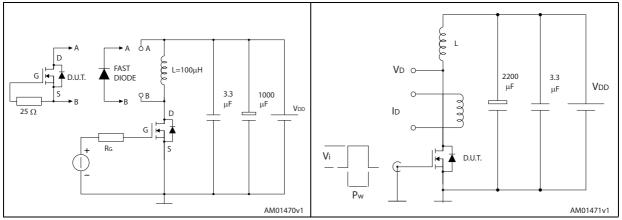
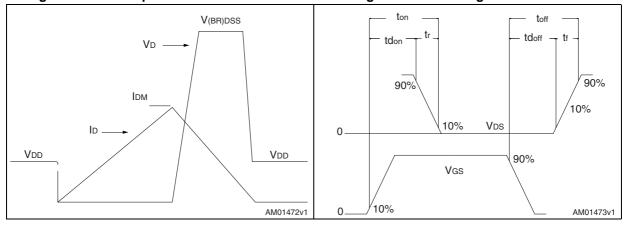


Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform



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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.



Table 8. TO-220FP mechanical data

Dim		mm	
Dim.	Min.	Тур.	Max.
Α	4.4		4.6
В	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
Н	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

-*B*-Dia L6 L2 *L7* L3 F1 **L4** F2 Ε -G1-7012510_Rev_K_B

Figure 19. TO-220FP drawing

Revision history STF45N10F7

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Dec-2012	1	First release.
06-Dec-2012	2	Minor text changes The part number STH110N10F7-2 has been moved to a separate datasheet The part number STP110N10F7 has been moved to a separate datasheet
11-Nov-2013	3	Document status promoted from preliminary to production data.

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