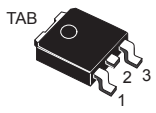
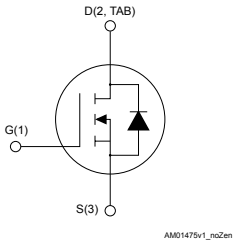
STD20NF06T4

Datasheet

N-channel 60 V, 32 mΩ typ., 24 A, STripFET II Power MOSFET in a DPAK package



DPAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD20NF06T4	60 V	40 mΩ	24 A	60 W

- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Product status link
STD20NF06T4

Product summary	
Order code	STD20NF06T4
Marking	D20NF06
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	60	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	24	A
	Drain current (continuous) at T_C = 100 °C	17	
I_{DM}(1)	Drain current (pulsed)	96	A
P_{TOT}	Total power dissipation at T_C = 25 °C	60	W
dv/dt(2)	Peak diode recovery voltage slope	10	V/ns
E_{AS}(3)	Single pulse avalanche energy	300	mJ
T_{stg}	Storage temperature range	-55 to 175	°C
T_j	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 24 A, di/dt ≤ 100 A/ns, V_{DD} = 80% $V_{(BR)DSS}$*
3. *Starting T_j = 25 °C, I_D = 10 A, V_{DD} = 45 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	2.5	°C/W
R_{thJB}(1)	Thermal resistance, junction-to-board	50	

1. *When mounted on a 1-inch² FR-4, 2 Oz copper board.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 60 V			1	µA
		V_{GS} = 0 V, V_{DS} = 60 V, T_C = 125 °C(1)			10	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 12 A		32	40	mΩ

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	V_{DS} = 25 V, I_D = 12 A	-	15	-	S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	690	-	pF
C_{oss}	Output capacitance		-	170	-	pF
C_{rss}	Reverse transfer capacitance		-	68	-	pF
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 10 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times)	-	10	-	ns
t_r	Rise time		-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	30	-	ns
t_f	Fall time		-	8	-	ns
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 20 A, V_{GS} = 10 V, R_G = 4.7 Ω (see Figure 14. Test circuit for gate charge behavior)	-	23	-	nC
Q_{gs}	Gate-source charge		-	5	-	
Q_{gd}	Gate-drain charge		-	7.5	-	

Table 5. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		24	A
I_{SDM}(1)	Source-drain current (pulsed)		-		96	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 24 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs,	-	65		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 30 V, T_J = 150 °C	-	150		nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	4.6		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

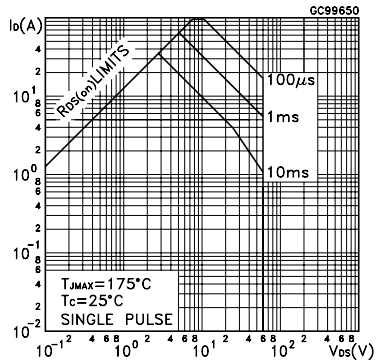


Figure 2. Thermal impedance

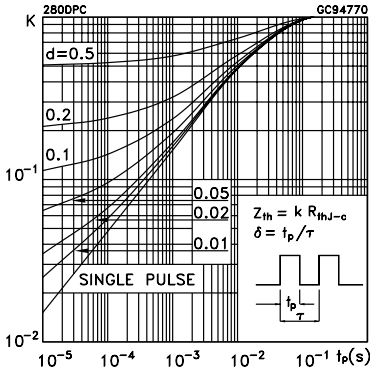


Figure 3. Output characteristics

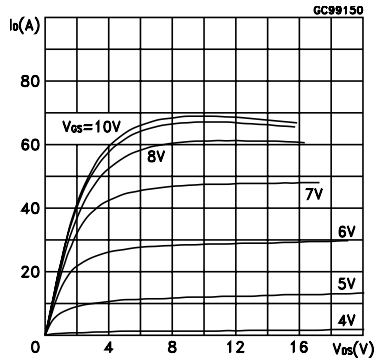


Figure 4. Transfer characteristics

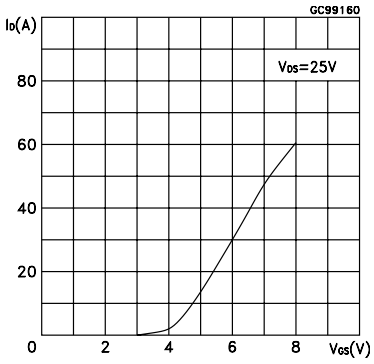


Figure 5. Transconductance

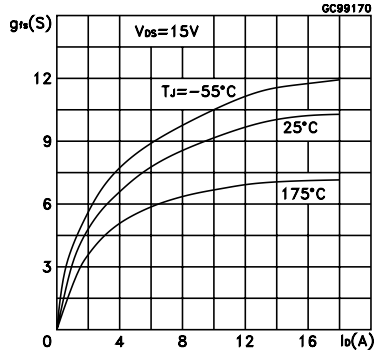


Figure 6. Static drain-source on-resistance

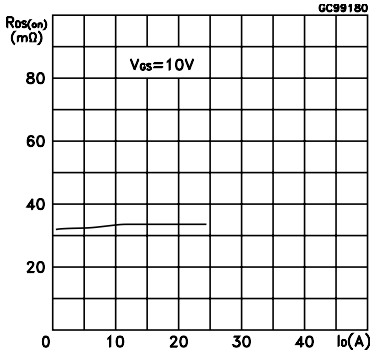


Figure 7. Gate charge vs gate-source voltage

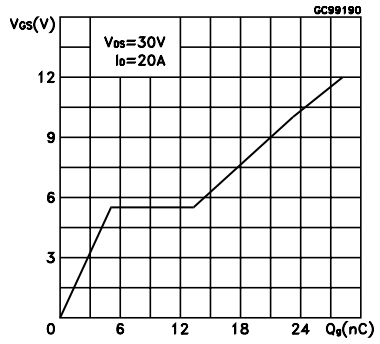


Figure 8. Capacitance variations

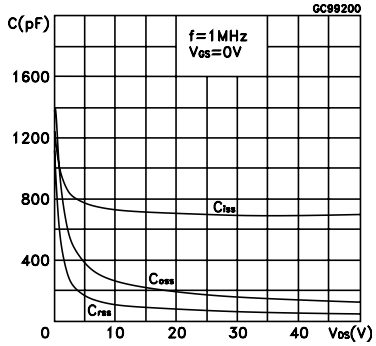


Figure 9. Normalized gate threshold voltage vs temperature

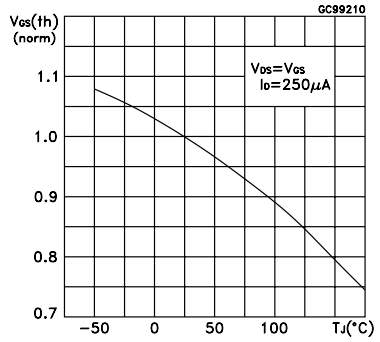


Figure 10. Normalized on-resistance vs temperature

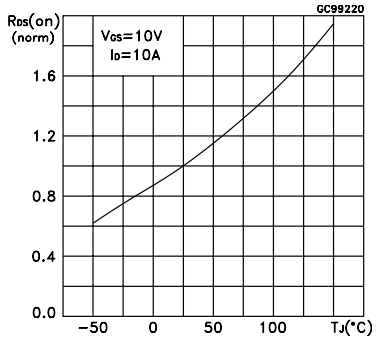


Figure 11. Source-drain diode forward characteristics

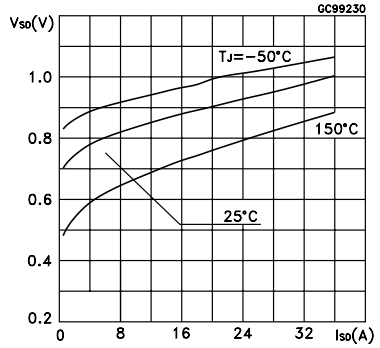
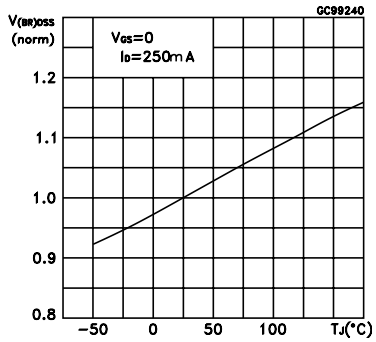


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 13. Test circuit for resistive load switching times

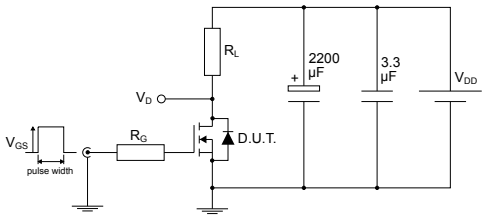


Figure 14. Test circuit for gate charge behavior

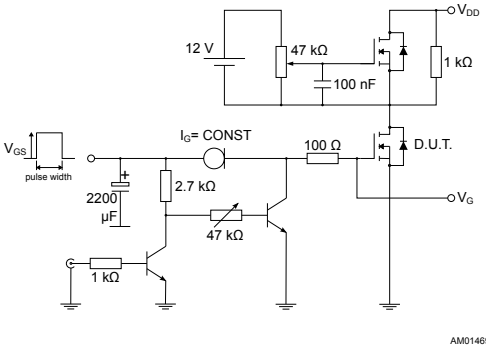


Figure 15. Test circuit for inductive load switching and diode recovery times

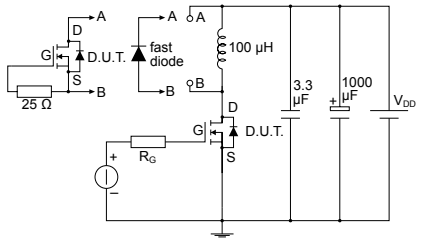


Figure 16. Unclamped inductive load test circuit

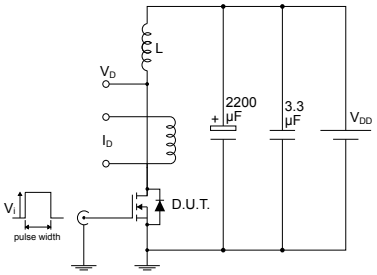


Figure 17. Unclamped inductive waveform

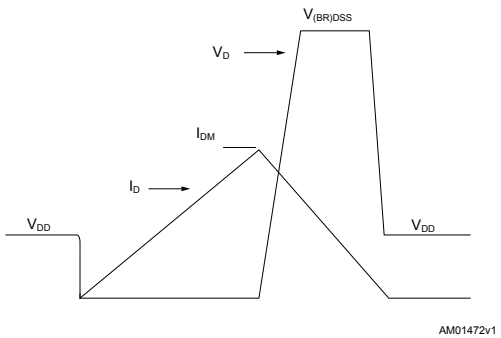
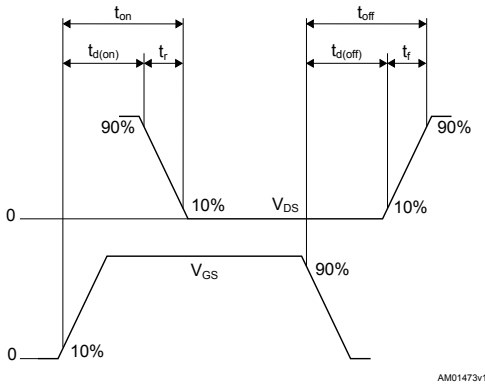


Figure 18. Switching time waveform

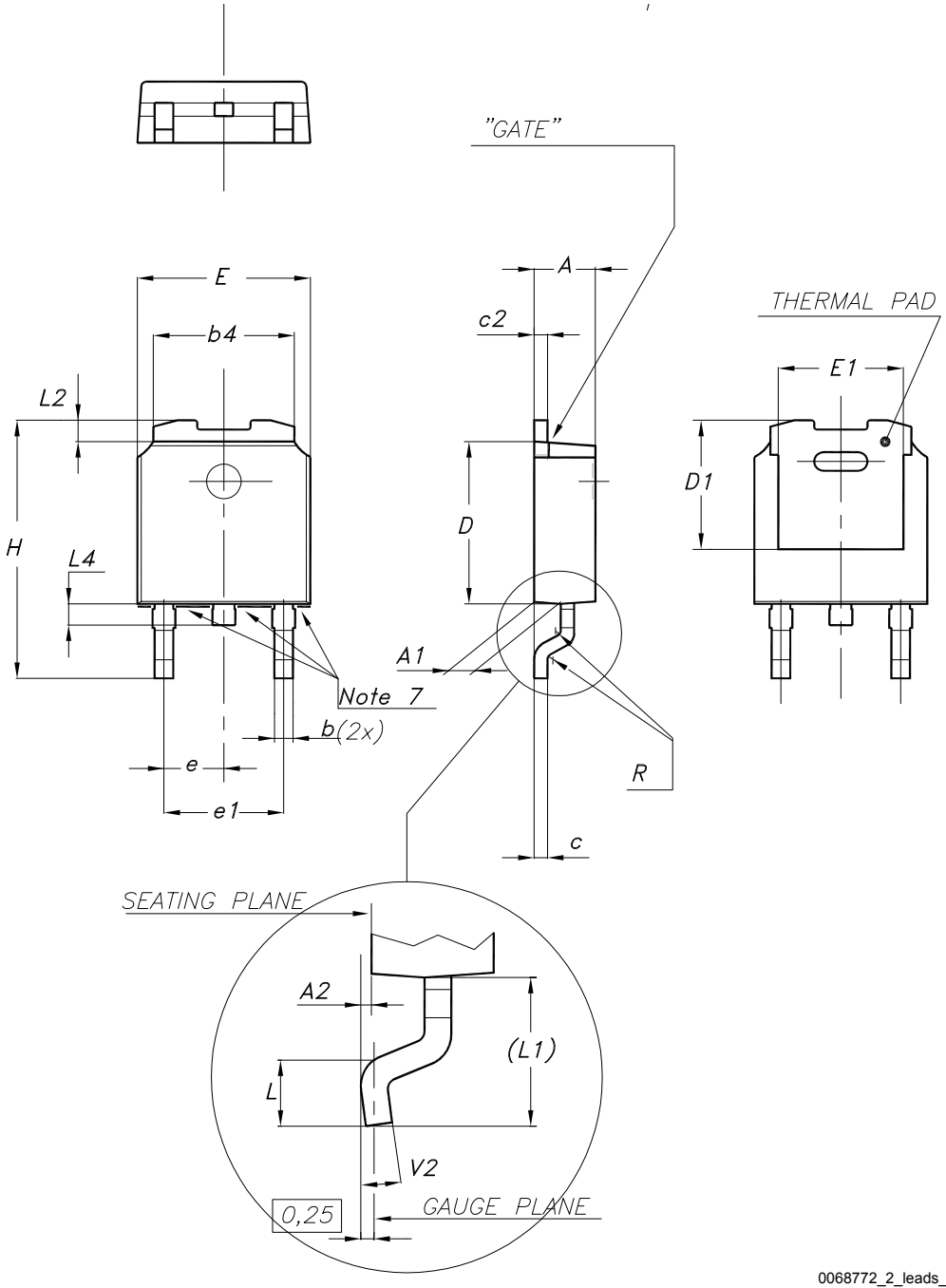


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) 2 leads SMD package information

Figure 19. DPAK (TO-252) type A die pad package outline



0068772_2_leads_SMD_Rev_30

Table 6. **DPAK (TO-252) type A die pad mechanical data**

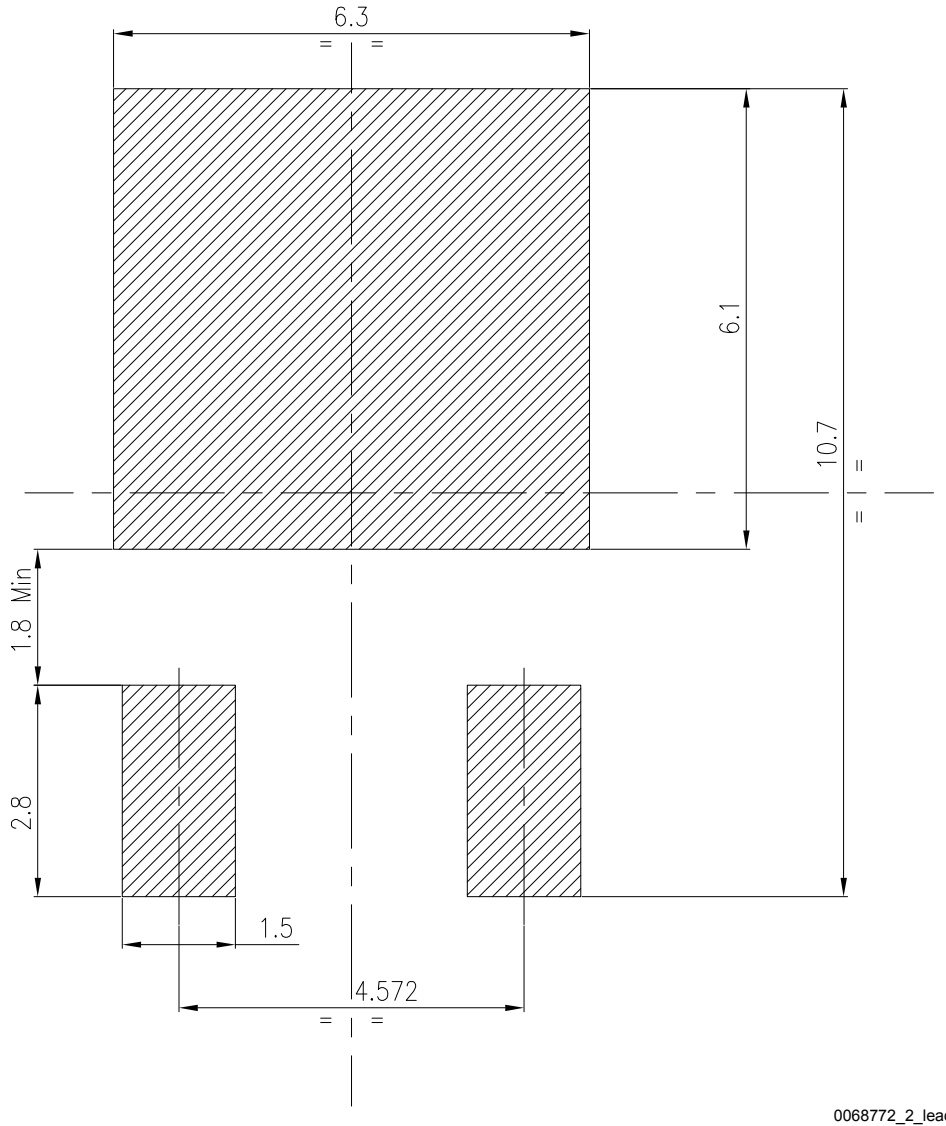
Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) 2 leads SMD max die pad package information

Table 7. **DPAK (TO-252) type A max die pad mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20. DPAK (TO-252) type A recommended footprint (dimensions are in mm)



Revision history

Table 8. **Document revision history**

Date	Version	Changes
03-May-2021	1	First release.

Contents