

## 1ch Gate Driver Providing Galvanic Isolation **2500Vrms Isolation Voltage** BM60055FV-C

#### **General Description**

The BM60055FV-C is a gate driver with an isolation voltage of 2500Vrms, I/O delay time of 250ns, minimum input pulse width of 170ns. It incorporates the fault signal output function (FLT\_UVLO, FLT\_SC, FLT\_OT), under voltage lockout (UVLO) function, short circuit protection (SCP) function, over temperature protection (OT) function, over current protection (OC) function, Soft turn off function, 2 level turn off function, active miller clamping function, switching controller function and output state feedback function (OSFB).

#### Features

- Fault Signal Output Function
- Under Voltage Lockout Function
- Short Circuit Protection Function
- Over Current Protection Function
- Over Temperature Protection
- Temperature Compensation of OC
- Soft Turn Off Function of SCP
- 2 Level Turn Off Function
- Active Miller Clamping
- Switching Controller
- Output State Feedback Function
- UL1577 Recognized:File No. E356010

■ AEC-Q100 Qualified (Note 1)

(Note 1:Grade1)

#### Applications

- Automotive isolated IGBT/MOSFET inverter gate drive.
- Automotive DC-DC converter.
- Industrial inverters system.
- UPS system.

#### **Typical Application Circuit**

#### **Key Specifications**

- Isolation Voltage:Maximum Gate Drive Voltage:
- ■I/O Delay Time:
- ■Minimum Input Pulse Width:

2500 [Vrms] (Max) 24 [V] (Max) 250 [ns] (Max) 170 [ns] (Max)

## Package

SSOP-B28W

**W(Typ) x D(Typ) x H(Max)** 9.2mm x 10.4mm x 2.4mm



Figure 1. Typical Application Circuit

OProduct structure : Silicon integrated circuit OThis product has no designed protection against radioactive rays

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### **Recommended Range Of External Constants**

| Pin Name | Symbol            | Recon | Unit |     |      |
|----------|-------------------|-------|------|-----|------|
|          | Symbol            | Min   | Тур  | Max | Unit |
| TC       | Rtc               | 1.25  | -    | 50  | kΩ   |
| RTOFF    | RRTOFF            | 4.6   | 10   | 30  | kΩ   |
| V_BATT   | CVBATT            | 3     | -    | -   | μF   |
| VCC2     | C <sub>VCC2</sub> | 0.4   | -    | -   | μF   |
| VREG     | $C_{VREG}$        | 0.1   | 1    | 10  | μF   |

#### **Pin Configuration**



Figure 2. Pin configuration

## **Pin Descriptions**

| Pin No. | Pin Name | Function  |
|---------|----------|---|
| 1       | GND2     | Output-side ground pin  |
| 2       | UVLOIN   | Output-side UVLO setting pin                                      |
| 3       | OCIN     | Over current detection pin  |
| 4       | SCPIN    | Short circuit detection pin                                       |
| 5       | LVOFF    | 2-level turn off level setting pin                                |
| 6       | RTOFF    | 2-level turn off time setting pin                                 |
| 7       | TCOMP    | Temperature compensation pin of OC                                |
| 8       | ТО       | Constant current output pin / Over temperature detection pin      |
| 9       | TC       | Constant current setting resistor connection pin                  |
| 10      | PROOUT   | Soft turn-off pin   |
| 11      | VCC2     | Output-side power supply pin                                      |
| 12      | OUT1     | Output pin  |
| 13      | OUT2     | Input and output pin for miller clamp / Gate voltage input pin    |
| 14      | GND2     | Output-side ground pin  |
| 15      | GND1     | Input-side ground pin   |
| 16      | FLT_UVLO | Fault (UVLO) output pin   |
| 17      | INB      | Control input pin B   |
| 18      | INA      | Control input pin A   |
| 19      | OSFB     | Output state feedback output pin                                  |
| 20      | FLT_OT   | Fault (OT) output pin   |
| 21      | FLT_SC   | Fault (SCP) output pin  |
| 22      | FB       | Error amplifier inverting input pin for switching controller      |
| 23      | COMP     | Error amplifier output pin for switching controller               |
| 24      | V_BATT   | Main power supply pin   |
| 25      | VREG     | Power supply pin for driving MOSFET for switching controller      |
| 26      | FET_G    | MOSFET control pin for switching controller                       |
| 27      | SENSE    | Current feedback resistor connection pin for switching controller |
| 28      | GND1     | Input-side ground pin   |

## **Absolute Maximum Ratings**

| Parameter   | Symbol              | Rating  | Unit |
|---|---------------------|---|------|
| Main Power Supply Voltage                                     | VBATTMAX            | -0.3 to +40.0 <sup>(Note 2)</sup>                 | V    |
| Output-Side Supply Voltage                                    | V <sub>CC2MAX</sub> | -0.3 to +30.0 <sup>(Note 3)</sup>                 | V    |
| INA, INB Pin Input Voltage                                    | VINMAX              | -0.3 to +7.0 <sup>(Note 2)</sup>                  | V    |
| FLT_UVLO Pin, FLT_SC Pin, FLT_OT Pin, OSFB Pin Input Voltage  | Veltmax             | -0.3 to +7.0 <sup>(Note 2)</sup>                  | V    |
| FLT_UVLO Pin, FLT_SC Pin, FLT_OT Pin, OSFB Pin Output Current | IFLT                | 10  | mA   |
| FB Pin Input Voltage  | V <sub>FBMAX</sub>  | -0.3 to +7.0 <sup>(Note 2)</sup>                  | V    |
| COMP Pin Input Voltage  | Vсомрмах            | -0.3 to +7.0 <sup>(Note 2)</sup>                  | V    |
| SENSE Pin Input Voltage                                       | VSENSEMAX           | -0.3 to +7.0 <sup>(Note 2)</sup>                  | V    |
| FET_G Pin Output Current (Peak5µs)                            | IFET_GPEAK          | 1000  | mA   |
| SCPIN Pin, OCIN Pin Input Voltage                             | Vscpinmax, Vocinmax | -0.3 to +6.0 <sup>(Note 3)</sup>                  | V    |
| UVLOIN Pin Input Voltage                                      | VUVLOINMAX          | -0.3 to V <sub>CC2</sub> +0.3 <sup>(Note 3)</sup> | V    |
| LVOFF Pin Input Voltage                                       | VLVOFFINMAX         | -0.3 to V <sub>CC2</sub> +0.3 <sup>(Note 3)</sup> | V    |
| TCOMP Pin Input Voltage                                       | VTCOMPINMAX         | -0.3 to V <sub>CC2</sub> +0.3 <sup>(Note 3)</sup> | V    |
| TO Pin Input Voltage  | V <sub>TOMAX</sub>  | -0.3 to V <sub>CC2</sub> +0.3 <sup>(Note 3)</sup> | V    |
| TO Pin Output Current   | I <sub>TOMAX</sub>  | 8   | mA   |
| OUT1 Pin Output Current (Peak5µs)                             | IOUT1PEAK           | 5000 <sup>(Note 4)</sup>                          | mA   |
| OUT2 Pin Output Current (Peak5µs)                             | IOUT2PEAK           | 5000 <sup>(Note 4)</sup>                          | mA   |
| PROOUT Pin Output Current (Peak30µs)                          | IPROOUTPEAK10       | 2000 <sup>(Note 4)</sup>                          | mA   |
| Operating Temperature Range                                   | Topr                | -40 to +125                                       | °C   |
| Storage Temperature Range                                     | Tstg                | -55 to +150                                       | °C   |
| Junction Temperature  | Tjmax               | +150  | °C   |

(Note 2) Relative to GND1 (Note 3) Relative to GND2

(Note 3) NealWe to GND2 (Note 4) Should not exceed Tj=150°C **Caution**: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

## Thermal Resistance<sup>(Note5)</sup>

| Parameter  |             | Thermal Res            | Unit                     |      |
|--|-------------|------------------------|--------------------------|------|
| Parameter  | Symbol      | 1s <sup>(Note 7)</sup> | 2s2p <sup>(Note 8)</sup> | Unit |
| Junction to Ambient  | θја         | 112.9                  | 64.4                     | °C/W |
| Junction to Top Characterization Parameter <sup>(Note 6)</sup> | $\Psi_{JT}$ | 34                     | 23                       | °C/W |

(Note 5)Based on JESD51-2A(Still-Air) (Note 6)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package. (Note 7)Using a PCB board based on JESD51-3. (Note 8)Using a PCB board based on JESD51-7.

| Layer Number of<br>Measurement Board | Material  | Board Size                 |
|--------------------------------------|-----------|----------------------------|
| Single                               | FR-4      | 114.3mm x 76.2mm x 1.57mmt |
| Тор                                  |           |                            |
| Copper Pattern                       | Thickness |                            |
| Footprints and Traces                | 70µm      |                            |
|                                      |           |                            |
| Layer Number of<br>Measurement Board | Material  | Board Size                 |

| 4 Layers              | FR-4      | 114.3mm x 76.2mm x       | x 1.6mmt |                   |           |        |  |
|-----------------------|-----------|--------------------------|----------|-------------------|-----------|--------|--|
| Тор                   |           | 2 Internal Layers        |          | 2 Internal Layers |           | Bottom |  |
| Copper Pattern        | Thickness | Copper Pattern Thickness |          | Copper Pattern    | Thickness |        |  |
| Footprints and Traces | 70µm      | 74.2mm x 74.2mm          | 35µm     | 74.2mm x 74.2mm   | 70µm      |        |  |

## Recommended Operating Conditions (Ta= -40°C to +125°C)

| Parameter                  | Symbol                     | Min | Max  | Units |
|----------------------------|----------------------------|-----|------|-------|
| Main Power Supply Voltage  | VBATT <sup>(Note 9)</sup>  | 4.5 | 30.0 | V     |
| Output-side Supply Voltage | Vcc2 <sup>(Note 10)</sup>  | 9   | 24   | V     |
| Output side UVLO voltage   | Vuv2th <sup>(Note10)</sup> | 6   | -    | V     |

(Note 9) GND1 reference (Note 10) GND2 reference

#### **Insulation Related Characteristics**

| Parameter                                     | Symbol | Characteristic   | Unit |
|---|--------|------------------|------|
| Insulation Resistance (V <sub>IO</sub> =500V) | Rs     | >10 <sup>9</sup> | Ω    |
| Insulation Withstand Voltage / 1min           | Viso   | 2500             | Vrms |
| Insulation Test Voltage / 1sec                | Viso   | 3000             | Vrms |

## **Electrical Characteristics**

(Unless otherwise specified Ta=-40°C to +125°C, V<sub>BATT</sub>=4.5V to 30V, V<sub>CC2</sub>=9V to 24V)

| Unless otherwise specified Ta<br>Parameter | Symbol             | <u>5 C, VBATT=</u><br>Min | 4.5 V 10 30 V<br>Typ | , v <sub>CC2</sub> =9∨τ<br>Max | U 24 V)<br>Unit | Conditions                                    |
|--|--------------------|---------------------------|----------------------|--------------------------------|-----------------|---|
| General                                    | Cymbol             |                           | 1)P                  | max                            | Onic            | Conditions                                    |
| Main Power Supply                          |                    | 0.5                       | 4.0                  | 0.0                            |                 | FET_G Pin                                     |
| Circuit Current 1                          | IBATT1             | 0.5                       | 1.3                  | 2.2                            | mA              | switching operation                           |
| Main Power Supply                          |                    |                           |                      |                                | _               | FET_G Pin                                     |
| Circuit Current 2                          | I <sub>BATT2</sub> | 0.4                       | 1.2                  | 2.1                            | mA              | No Switching                                  |
| Output Side Circuit Current                | Icc2               | 1.8                       | 3.2                  | 4.8                            | mA              | RTC=10kΩ                                      |
| Switching Power Supply Cont                |                    |                           |                      |                                |                 |   |
| FET_G Output Voltage H1                    | VFETGH1            | 4.5                       | 5.0                  | 5.5                            | V               | I <sub>FET_G</sub> =0A(open)                  |
| FET_G Output Voltage H2                    | Vfetgh2            | 4.0                       | 4.5                  | -                              | V               | V_BATT=4.5V<br>I <sub>FET_G</sub> =0A(open)   |
| FET_G Output Voltage L                     | VFETGL             | 0                         | -                    | 0.3                            | V               | I <sub>FET_G</sub> =0A(open)                  |
| FET_G ON-Resistance                        |                    |                           |                      |                                |                 |   |
| (Source-side)                              | Rongh              | 3                         | 6                    | 12                             | Ω               | IFET_G=10mA                                   |
| FET_G ON-Resistance                        | _                  |                           |                      |                                | _               |   |
| (Sink-side)                                | Rongl              | 0.3                       | 0.6                  | 1.3                            | Ω               | IFET_G=10mA                                   |
| Oscillation Frequency                      | fosc_sw            | 80                        | 100                  | 120                            | kHz             |   |
| Soft-start Time                            | tss                | -                         | -                    | 50                             | ms              |   |
| FB Pin Threshold Voltage                   | Vfb                | 1.47                      | 1.50                 | 1.53                           | V               |   |
| FB Pin Input Current                       | IFB                | -0.8                      | 0                    | +0.8                           | μA              |   |
| COMP Pin Sink Current                      | ICOMPSINK          | -160                      | -80                  | -40                            | μA              |   |
| COMP Pin Source Current                    | ICOMPSOURCE        | 40                        | 80                   | 160                            | μA              |   |
| Over Voltage Detection<br>Threshold        | V <sub>OVTH</sub>  | 1.60                      | 1.65                 | 1.70                           | V               |   |
| Under Voltage Detection<br>Threshold       | Vuvth              | 1.23                      | 1.30                 | 1.37                           | V               |   |
| Over-Current Detection<br>Threshold        | Vостн              | 0.17                      | 0.20                 | 0.23                           | V               |   |
| V_BATT UVLO OFF Voltage                    | Vuvlobatth         | 4.05                      | 4.25                 | 4.45                           | V               |   |
| V_BATT UVLO ON Voltage                     | VUVLOBATTL         | 3.95                      | 4.15                 | 4.35                           | V               |   |
| Maximum ON DUTY                            | Donmax             | 75                        | 85                   | 95                             | %               |   |
| Protection Holding Time                    | t DCDCRLS          | 20                        | 40                   | 60                             | ms              |   |
| Logic Block                                |                    |                           |                      |                                |                 |   |
| Logic High Level Input Voltage             | VINH               | 3.5                       | -                    | -                              | V               | INA, INB                                      |
| Logic Low Level Input Voltage              | VINL               | -                         | -                    | 1.5                            | V               | INA, INB                                      |
| Logic Pull-Down Resistance                 | RIND               | 25                        | 50                   | 100                            | kΩ              | INA, INB                                      |
| Logic Input Filtering Time                 | tinfil             | 70                        | 120                  | 170                            | ns              | INA, INB                                      |
| Output                                     |                    |                           |                      | 1                              |                 | · ·   |
| OUT1 ON-Resistance<br>(Source-side)        | R <sub>ONH</sub>   | 0.25                      | 0.60                 | 1.35                           | Ω               | I <sub>OUT1</sub> =40mA                       |
| OUT1 ON-Resistance<br>(Sink-side)          | Ronl               | 0.05                      | 0.40                 | 1.15                           | Ω               | Iout1=40mA                                    |
| OUT1 Maximum Current                       | Ioutmax            | 5.0                       | -                    | -                              | Α               | V <sub>CC2</sub> =15V<br>Guaranteed by design |
| PROOUT ON-Resistance                       | Ronpro             | 0.35                      | 0.70                 | 1.45                           | Ω               | IPROOUT=40mA                                  |
| Turn ON time                               | <b>t</b> PON       | 130                       | 190                  | 250                            | ns              |   |
| Turn OFF time                              | <b>t</b> POFF      | 130                       | 190                  | 250                            | ns              |   |
| Propagation Distortion                     | <b>t</b> PDIST     | -60                       | 0                    | +60                            | ns              | tpoff - tpon                                  |

## **Electrical Characteristics - continued**

(Unless otherwise specified Ta=-40°C to +125°C, V<sub>BATT</sub>=4.5V to 30V, V<sub>CC2</sub>=9V to 24V)

| Parameter                      | Symbol                | Min   | Тур   | Max   | Unit  | Conditions              |
|--------------------------------|-----------------------|-------|-------|-------|-------|-------------------------|
| Rise Time                      | trise                 | -     | 30    | 50    | ns    | Load=1nF                |
| Fall Time                      | tFALL                 | -     | 30    | 50    | ns    | Load=1nF                |
| OUT2 ON-Resistance             | R <sub>ON2</sub>      | 0.1   | 0.45  | 1.2   | Ω     | I <sub>OUT2</sub> =40mA |
| OUT2 ON Threshold Voltage      | V <sub>OUT2ON</sub>   | 2.7   | 3.0   | 3.3   | V     |                         |
| Common Mode Transient Immunity | CM                    | 100   | -     | -     | kV/µs | Design assurance        |
| Protection Functions           |                       |       | 1     | 1     | 1     | 1                       |
| Output-side UVLO OFF           | Vuvlo2h               | 0.95  | 1.00  | 1.05  | V     |                         |
| Threshold Voltage              | • 0 • 20211           | 0.00  |       | 1.00  |       |                         |
| Output-side UVLO ON            | Vuvlo2l               | 0.85  | 0.90  | 0.95  | V     |                         |
| Threshold Voltage              | VOVLOZE               | 0.00  | 0.00  | 0.00  | v     |                         |
| Output-side UVLO               | t <sub>UVLO2FIL</sub> | 1.5   | 2.0   | 2.5   | μs    |                         |
| Filtering Time                 | UVLO2FIL              | 1.5   | 2.0   | 2.5   | μο    |                         |
| Output-side UVLO Delay Time    |                       | 4.5   |       | 2.0   |       |                         |
| (OUT)                          | tduvlo20ut            | 1.5   | 2.2   | 2.9   | μs    |                         |
| Output-side UVLO Delay Time    |                       | 4.5   |       | 05    |       |                         |
| (FLT_UVLO)                     | <b>t</b> duvlo2flt    | 1.5   | -     | 65    | μs    |                         |
| Over Current Detection         |                       |       |       |       |       |                         |
| Voltage1                       | V <sub>OCDET</sub>    | 0.658 | 0.700 | 0.742 | V     | TCOMP=VCC2              |
| Over Current Detection         |                       |       |       |       |       | TO=4V                   |
| Voltage2                       | Vocdet                | 0.394 | 0.420 | 0.441 | V     | TCOMP=GND2              |
| Over Current Detection         |                       |       |       |       |       | TO=3V                   |
| Voltage3                       | VOCDET                | 0.658 | 0.700 | 0.742 | V     | TCOMP=GND2              |
|                                |                       |       |       |       |       | TO=2.2V                 |
| Over Current Detection         | Vocdet                | 0.874 | 0.930 | 0.986 | V     |                         |
| Voltage4                       |                       |       |       |       |       | TCOMP=GND2              |
| Over Current Detection         | <b>t</b> DOCFIL       | 0.70  | 1.00  | 1.30  | μs    |                         |
| Filtering Time                 |                       |       |       |       |       |                         |
| Over Current Detection         | Vdocout               | 0.73  | 1.03  | 1.33  | μs    | OUT1=30kΩ Pull down     |
| Delay Time (OUT)               |                       |       |       |       | -     |                         |
| Over Current Detection         | Vdocprout             | 0.73  | 1.03  | 1.33  | μs    | PROOUT=30kΩ Pull up     |
| Delay Time (PROUT)             |                       |       |       |       | · ·   | '                       |
| Over Current Detection         | VDOCFLT_SC            | 0.75  | 1.05  | 1.35  | μs    |                         |
| Delay Time (FLT_SC)            | 1000121_00            |       |       |       | P     |                         |
| Short Circuit Detection        | VSCPDET               | 0.95  | 1.00  | 1.05  | V     |                         |
| Voltage                        | VGCFDET               | 0.00  | 1.00  | 1.00  | •     |                         |
| Short Circuit Detection        | toopru                | 0.10  | 0.20  | 0.30  | 116   |                         |
| Filtering Time                 | <b>t</b> SCPFIL       | 0.10  | 0.20  | 0.30  | μs    |                         |
| Short Circuit Detection        |                       | 0.47  | 0.00  | 0.00  |       |                         |
| Delay Time (OUT)               | <b>t</b> DSCPOUT      | 0.17  | 0.23  | 0.38  | μs    | OUT1=30kΩ Pull down     |
| Short Circuit Detection        |                       | 0.40  | 0.05  | 0.40  |       |                         |
| Delay Time (PROOUT)            | <b>t</b> dscpproout   | 0.19  | 0.25  | 0.40  | μs    | PROOUT=30kΩ Pull up     |
| Short Circuit Detection        |                       |       |       | _     |       |                         |
| Delay Time (FLT_SC)            | tdscpflt_sc           | 0.23  | 0.29  | 0.44  | μs    |                         |
| TC Pin Voltage                 | V <sub>TC</sub>       | 0.975 | 1.000 | 1.025 | V     |                         |
| TO Pin Output Current          | ITO                   | 0.97  | 1.00  | 1.03  | mA    | R <sub>TC</sub> =10kΩ   |
| TO Pin Disconnect Detection    | 10                    | 0.01  | 1.00  | 1.00  |       |                         |
|                                | Vтон                  | 7     | 8     | 9     | V     |                         |
| Voltage                        |                       |       |       |       |       |                         |

## **Electrical Characteristics - continued**

(Unless otherwise specified Ta=-40°C to +125°C, V\_{BATT}=4.5V to 30V, V\_{CC2}=9V to 24V)

| Parameter   | Symbol          | Min  | Тур  | Max  | Unit | Conditions                       |
|---|-----------------|------|------|------|------|----------------------------------|
| Over Temperature Detection<br>Voltage(ON)         | Votdeton        | 1.96 | 2.0  | 2.04 | V    |                                  |
| Over Temperature Detection<br>Voltage(OFF)        | Votdetoff       | 2.15 | 2.2  | 2.25 | V    |                                  |
| Over Temperature Detection<br>Delay time (OUT)    | tdotout         | 2    | 10   | 30   | μs   | OUT1=30kΩ Pull down              |
| Over Temperature Detection<br>Delay Time (FLT_OT) | <b>t</b> dotflt | 1    | -    | 35   | μs   |                                  |
| FLT_UVLO, FLT_SC, FLT_OT<br>ON-Resistance         | Ronflt          | -    | 30   | 80   | Ω    | IFLT=5mA                         |
| Fault (UVLO) Output<br>Holding Time               | tuvlo_fltrls    | 20   | 40   | 60   | ms   |                                  |
| Fault (SCP) Output<br>Holding Time                | tscp_fltrls     | 20   | 40   | 60   | ms   |                                  |
| 2-Level Turn Off Voltage<br>Offset 1              | VLVOFF1         | -300 | -150 | 0    | mV   | V <sub>CC2</sub> =15V, LVOFF=12V |
| 2-Level Turn Off Voltage<br>Offset 2              | VLVOFF2         | -350 | -200 | -50  | mV   | V <sub>CC2</sub> =15V, LVOFF=8V  |
| 2-Level Turn Off Enable<br>Threshold Voltage      | Vlvoffth        | 0.7  | 1.0  | 1.3  | V    |                                  |
| 2-Level Turn Off Time                             | <b>t</b> rtoff  | 1.93 | 2.3  | 2.67 | μs   | R <sub>RTOFF</sub> =16kΩ         |
| Gate State H Detection<br>Threshold Voltage       | Vosfbh          | 4.5  | 5.0  | 5.5  | V    |                                  |
| Gate State L Detection<br>Threshold Voltage       | Vosfbl          | 4.0  | 4.5  | 5.0  | V    |                                  |
| OSFB Output ON-Resistance                         | Rosfb           | -    | 30   | 80   | Ω    | Iosfb=5mA                        |

## UL1577 Ratings Table

Following values are described in UL Report.

| Parameter                               | Value | Unit | Conditions                    |
|---|-------|------|-------------------------------|
| Side 1 (Input Side) Circuit Current     | 1.3   | mA   | VBATT=14V,OUT1=L              |
| Side 2 (Output Side) Circuit Current    | 3.2   | mA   | Vcc2=15V, OUT1=L              |
| Side 1 (Input Side) Consumption Power   | 18.2  | mW   | V <sub>BATT</sub> =14V,OUT1=L |
| Side 2 (Output Side) Consumption Power  | 48    | mW   | Vcc2=15V, OUT1=L              |
| Isolation Voltage                       | 2500  | Vrms |                               |
| Maximum Operating (Ambient) Temperature | 125   | °C   |                               |
| Maximum Junction Temperature            | 150   | °C   |                               |
| Maximum Storage Temperature             | 150   | °C   |                               |
| Maximum Data Transmission Rate          | 2.9   | MHz  |                               |

## **Typical Performance Curves**



## Typical Performance Curves – continued



Figure 7. Soft-start Time

Figure 8. FB Pin Threshold Voltage



Figure 9. COMP Pin Sink Current

Figure 10. COMP Pin Source Current

## Typical Performance Curves - continued



Figure 11. Over-Current Detection Threshold









## Typical Performance Curves - continued









Figure 19. Over Current Detection Voltage

Figure 20. Short Circuit Detection Voltage



Figure 21. Over Temperature Detection Voltage

## Description of Pins and Cautions on Layout of Board

- 1. V\_BATT (Main power supply pin) This is the main power supply pin. Connect a bypass capacitor between V\_BATT and GND1 in order to suppress voltage variations. Make sure that power is supplied even when the switching power supply is not used, since the internal reference voltage of the input side of chip is generated from this power supply.
- 2. GND1 (Input-side ground pin) The GND1 pin is a ground pin for the input side.
- 3. GND2 (Output-side ground pin) The GND2 pin is a ground pin for the output side. Connect GND2 pin to the emitter / source of the output device.
- 4. INA, INB (Control input pin A, Control input pin B) They are pins for determining the output logic.

| INB | INA | OUT1 |  |  |  |  |  |  |  |  |
|-----|-----|------|--|--|--|--|--|--|--|--|
| Н   | L   | L    |  |  |  |  |  |  |  |  |
| Н   | Н   | L    |  |  |  |  |  |  |  |  |
| L   | L   | L    |  |  |  |  |  |  |  |  |
| L   | Н   | Н    |  |  |  |  |  |  |  |  |

5. FLT\_UVLO, FLT\_SC, FLT\_OT (Fault output pins)

These pins have open drains that output fault signals when faults occur (i.e., when the under voltage lockout function (UVLO) or short circuit protection function (SCP) or over current protection function (OC) or over temperature protection (OT) is activated).

| State                                   | FLT_UVLO | FLT_SC | FLT_OT |
|---|----------|--------|--------|
| While in normal operation               | Hi-Z     | Hi-Z   | Hi-Z   |
| V_BATT UVLO or VCC2 UVLO or TO pin open | L        | Hi-Z   | Hi-Z   |
| SCP or OC                               | Hi-Z     | L      | Hi-Z   |
| ОТ                                      | Hi-Z     | Hi-Z   | L      |

#### 6. OSFB (Output pin for monitoring gate condition)

This is an open drain pin which outputs the state of gate logic of the output element monitored with OUT2 pin.

| OUT2(input) | OSFB |
|-------------|------|
| Н           | Hi-Z |
| L           | L    |

7. FB (Error amplifier inverting input pin for switching controller)

This is a voltage feedback pin of the switching controller. This pin combine with voltage monitoring at over voltage protection function for switching controller. When over voltage or under voltage protection is activated, switching controller will be at OFF state (FET\_G pin outputs Low). When the protection holding time (t<sub>DCDCRLS</sub>) is completed, the protection function will be released. Under voltage function is not activated during soft-start time.

- COMP (Error amplifier output pin for switching controller) This is the gain control pin of the switching controller. Connect a phase compensation capacitor and resistor. When the switching controller is not used, connect it to GND1.
- 9. VREG (Power supply pin for the driving MOSFET of the switching controller) This is the power supply pin for the driving MOSFET of the switching controller transformer drive. Be sure to connect a capacitor between VREG and GND1 even when the switching controller is not used, in order to prevent oscillation and to suppress voltage variation due to FET\_G output current.

## Description of Pins and Cautions on Layout of Board - continued

- FET\_G (MOSFET control pin for switching controller)
   This is a MOSFET control pin for the switching controller transformer drive. Leave it open when the switching controller is
   not used.
- 11. SENSE (Connection to the current feedback resistor of the switching controller)

This is a pin connected to the resistor of the switching controller current feedback. FET\_G pin output duty is controlled by the voltage value of this pin. This pin combines with current monitoring at over current protection function for switching controller. When over current protection is activated, switching controller will be at minimum duty state (FET\_G pin outputs pulse of minimum duty).

- 12. OUT1(Output pin) The OUT1 pin is a gate driving pin.
- 13. OUT2 (Miller clamp pin) The OUT2 pin is for preventing the increase in gate voltage due to the Miller current of the power device connected to the OUT pin. It also functions as a pin for monitoring gate voltage for miller clamp function and for output state feedback function. If both functions are not used, short-circuit the OUT2 pin to the GND2 pin.
- 14. PROOUT (Soft turn-OFF pin) This pin is for soft turn-OFF of output pin when short-circuit protection or over current protection is in action.
- 15. SCPIN (Short circuit current detection pin)

This pin is used to detect current for short circuit protection. When the SCPIN voltage exceeds the voltage set with the V<sub>SCPDET</sub> parameter, the SCP function will be activated, this will make the IC function in an open state. To avoid such trouble, connect a resistor between the SCPIN and the GND2 or short the SCPIN pin to GND2 when the SCP function is not used.

16. OCIN (Over current detection pin)

This pin is used to detect current for over current protection. When the OCIN voltage exceeds the voltage set with the  $V_{OCDET}$  parameter, the OC function will be activated, this will make the IC function in an open state. To avoid such trouble, connect a resistor between the OCIN and the GND2 or short the OCIN pin to GND2 when the OC function is not used.

- TCOMP (Temperature compensation pin)
   This pin is for temperature compensation of over current detection. If the function is used, connect TCOMP to GND2. If the function is not used, connect TCOMP to VCC2.
- LVOFF (2-level turn off level setting pin) The LVOFF pin is a pin used to make setting of 2-level turn off voltage. The voltage of LVOFF pin is 2-level turn off level. When the VLVOFF > VLVOFFTH, 2-level turn off function is activated.
- RTOFF (2-level turn off time setting pin) The RTOFF pin is a pin used to make the setting of 2-level turn off time. Connect a resistor R<sub>RTOFF</sub> between the RTOFF pin and the GND2 pin.
- 20. TC (Resistor connection pin for setting constant current source output) The TC pin is a resistor connection pin for setting the constant current output. If an arbitrary resistance value is connected between TC and GND2, it is possible to set the constant current value output from TO.
- 21. TO (Constant current output / sensor voltage input pin) The TO pin is constant current output / voltage input pin. It can be used as a temperature protection input by connecting an element with arbitrary impedance between TO pin and GND2. Furthermore, the TO pin disconnect detection function is built-in.
- 22. UVLOIN (Output-side UVLO setting input pin) The UVLOIN pin is a pin for deciding UVLO setting value of VCC2. The threshold value of UVLO can be set by dividing the resistance voltage of VCC2 and inputting such value.

1. Fault Status Output

This function is used to output a fault signal from the FLT\_UVLO pin when the under voltage lockout function (UVLO) is activated, the FLT\_SC pin when the short circuit protection function (SCP) or over current protection (OC) is activated, and the FLT\_OT pin when the over temperature protection (OT) is activated.

The functions of UVLO and SCP/OC is to hold the fault signal until fault output holding time ( $t_{UVLO\_FLTRLS}$ ,  $t_{SCP\_FLTRLS}$ ) is completed.

| Status  | FLT_UVLO pin |
|---------|--------------|
| Normal  | Hi-Z         |
| UVLO    | L            |
|         |              |
| Status  | FLT_SC pin   |
| Normal  | Hi-Z         |
| SCP, OC | L            |



Figure 22. Fault Status Output Timing Chart (SCP/OC,UVLO)

The OT function holds the fault signal until TO pin voltage goes high above VTODETOFF.

| Status | FLT_OT pin |
|--------|------------|
| Normal | Hi-Z       |
| ОТ     | L          |



When UVLO function is activated during SCP or OC, the Fault output holding time occurs after UVLO cancellation.



Figure 24. Fault Status Output Timing Chart (SCP/OC and UVLO)

2. Under Voltage Lockout (UVLO) Function

BM60055FV-C incorporates the under voltage lockout (UVLO) function on V\_BATT and VCC2. When the power supply voltage drops to the UVLO ON voltage, OUT1 turns off and the FLT\_UVLO pin will both output the "L" signal. When the power supply voltage rises to the UVLO OFF voltage, these pins will be reset. However, during the fault output holding time set in "Fault status output" section, the OUT1 pin and the FLT\_UVLO pin will hold the "L" signal. In addition, to prevent mis-triggering due to noise, mask time is set on both low and high voltage sides.



When  $V_{LVOFF} < V_{LVOFFTH}$ , normal turn off is activated.



Figure 27. UVLO Operation Timing Chart (Normal Turn off)

When  $V_{LVOFF} > V_{LVOFFTH}$ , 2-level turn off is activated.



Figure 28. UVLO Operation Timing Chart (2 level turn off)

3. Short Circuit Protection (SCP) Function

When the SCPIN pin voltage exceeds a voltage set with the V<sub>SCPDET</sub> parameter, the SCP function will be activated. When the SCP function is activated, soft turn off is activated.

When the SCP function is activated, OUT1 pin voltage will be set to the "Hi-Z" level and the PROOUT pin voltage will be set to "L" level first. Next, OUT2 pin voltage < V<sub>OUT2ON</sub>, internal MOS of OUT2 pin is turned ON (miller clamping) and OUT1 will become L.





4. Over Current Protection (OC) Function

When the OCIN pin voltage exceeds a voltage set with the V<sub>OCDET</sub> parameter, the OC function will be activated. When the OC function is activated, soft turn off is activated.

When the OC function is activated, OUT1 pin voltage will be set to the "Hi-Z" level and the PROOUT pin voltage will be set to "L" level first. Next, OUT2 pin voltage < V<sub>OUT2ON</sub>, internal MOS of OUT2 pin is turned ON (miller clamping) and OUT1 will become L.



Figure 30. OC Operation Timing Chart

5. 2-Level Turn Off

When  $V_{LVOFF} > V_{LVOFFTH}$ , 2-level turn off is activated.

2-level turn off time t<sub>RTOFF</sub> and voltage level V<sub>LVOFF</sub> is adjustable by external elements of RTOFF pin and LVOFF pin. The values of the 2-level turn off level V<sub>LVOFF</sub> is determined by the values of the voltage of LVOFF pin. The values of the 2-level turn off time t<sub>RTOFF</sub> is determined by the values of the resistor R<sub>RTOFF</sub> according to the following formula (typical values):

 $t_{RTOFF} = 0.145 \times R_{RT} [k\Omega] + 0.05$  [us]

The propagation delay time (ON) of the OUT1 is delayed for the same time as the 2-level turn off time  $t_{RTOFF}$ . When  $V_{LVOFF} < V_{LVOFFTH}$ , turn on time does not include 2-level turn off time and normal turn off is activated.



Figure 31. 2 level turn off function block diagram



Figure 32. Timing Chart of Turn Off

6. Temperature Compensation of OC

When TCOMP = GND2, temperature compensation of OC is activated. If the function is not used, connect TCOMP to VCC2.

#### TCOMP=GND2

The temperature of OC detection voltage can be compensated in accordance with TO voltage.

 $V_{oc} = -0.283 \times V_{To} + 1.552$  [V]

#### TCOMP=VCC2

 $V_{0C} = 0.7$  [V]

#### 7. Miller Clamping

When OUT1=L and OUT2 pin voltage <  $V_{OUT2ON}$ , internal MOS of OUT2 pin is turned ON, and Miller clamp function operates.

| IN | OUT2 pin<br>input voltage | OUT2 |
|----|---------------------------|------|
| L  | Not more than<br>Vout20N  | L    |
| Н  | Х                         | Hi-Z |



Figure 33. Block Diagram of Miller Clamp Function





#### 8. Over Temperature Protection Function

Constant current is supplied from TO pin from the built-in constant current circuit. This current value can be adjusted in accordance with the resistance value connected between TC and GND2. Furthermore, TO pin has voltage input function, and when the TO pin voltage < VOTDETON OUT1 turns off and FLT\_OT becomes L. When the TO pin voltage goes high above VOTDETOFF, the OT function will be released.



Figure 35. Block Diagram of Temperature Monitor Function





Figure 36. OT Operation Timing Chart (Normal turn off)

When VLVOFF > VLVOFFTH, 2-level turn off is activated.



Figure 37. OT Operation Timing Chart (2 level turn off)

- 9. Switching Controller
  - (1) Basic action

This IC has a built-in switching power supply controller which repeats ON/OFF synchronizing with internal clock. When V\_BATT voltage is supplied (V<sub>BATT</sub> > V<sub>UVLOBATTH</sub>), FET\_G pin starts switching by soft-start. Output voltage is determined by the following equation by external resistance and winding ratio "n" of flyback transformer (n= V<sub>OUT2</sub> side winding number)

 $V_{OUT2} = V_{FB} \times \{ (R_1 + R_2) / R_2 \} \times n[V]$ 

(2) MAX DUTY

When, for example, output load is large, and voltage level of SENSE pin does not reach current detection level, output is forcibly turned OFF by Maximum On Duty (D<sub>ONMAX</sub>).

| (3) | Pin conditions when the switching power supply controller is not used   |
|-----|---|
|     | - Local process with a second state of a second balance of the second state in a second state of the se |

| Implement pin connection as shown below when switching power supply is not used. |          |                      |  |  |  |  |  |  |  |  |
|--|----------|----------------------|--|--|--|--|--|--|--|--|
| Pin Number   | Pin Name | Treatment Method     |  |  |  |  |  |  |  |  |
| 22   | FB       | Connect to VREG      |  |  |  |  |  |  |  |  |
| 23   | COMP     | Connect to GND1      |  |  |  |  |  |  |  |  |
| 24   | V_BATT   | Connect power supply |  |  |  |  |  |  |  |  |
| 25   | VREG     | Connect capacitor    |  |  |  |  |  |  |  |  |
| 26   | FET_G    | No connection        |  |  |  |  |  |  |  |  |
| 27   | SENSE    | Connect to GND1      |  |  |  |  |  |  |  |  |

10. Output State Feedback Function

When the gate logic of output device monitored with OUT2 pin is H, a logic H is the output from OSFB pin. When OUT2 pin is L, a logic L is the output from OSFB pin.

# **Description of Functions and Examples of Constant Setting - continued** 11. I/O Condition Table

| 11. | I/O Condition Tab | Input Output |       |    |      |      |       |     |     |      |      |      |        |   |        |        |      |
|-----|-------------------|--------------|-------|----|------|------|-------|-----|-----|------|------|------|--------|---|--------|--------|------|
| No. | Status            | V_BATT       | SCPIN | TO | VCC2 | OCIN | LVOFF | INB | INA | OUT2 | OUT1 | OUT2 | PROOUT |   | FLT_SC | FLT_OT | OSFB |
| 1   |                   | UVLO         | Н     | Х  | Х    | Х    | Х     | L   | Н   | Н    | Z    | Z    | L      | L | L*     | Z      | L    |
| 2   | V_BATT UVLO       | UVLO         | Н     | Х  | Х    | Х    | Х     | L   | Н   | L    | L    | L    | Ζ      | L | Z      | Z      | L    |
| 3   | SCP               | UVLO         | Н     | Х  | Х    | Х    | Х     | Х   | L   | Н    | L    | Ζ    | Ζ      | L | Z      | Z      | L    |
| 4   |                   | UVLO         | Н     | Х  | Х    | Х    | Х     | Х   | L   | L    | L    | L    | Ζ      | L | Ζ      | Ζ      | L    |
| 5   |                   | UVLO         | L     | L  | Х    | L    | Н     | Х   | Х   | Н    | Т    | Ζ    | Ζ      | L | Ζ      | L      | L    |
| 6   | V_BATT UVLO       | UVLO         | L     | L  | Х    | L    | Н     | Х   | Х   | L    | Т    | L    | Ζ      | L | Ζ      | L      | L    |
| 7   | ОТ                | UVLO         | L     | L  | Х    | L    | L     | Х   | Х   | Н    | L    | Ζ    | Ζ      | L | Ζ      | L      | L    |
| 8   |                   | UVLO         | L     | L  | Х    | L    | L     | Х   | Х   | L    | L    | L    | Z      | L | Ζ      | L      | L    |
| 9   |                   | UVLO         | L     | Н  | L    | Х    | Н     | Х   | Х   | Н    | Т    | Ζ    | Z      | L | Ζ      | Z      | L    |
| 10  | V_BATT UVLO       | UVLO         | L     | Н  | L    | Х    | Н     | Х   | Х   | L    | Т    | L    | Ζ      | L | Z      | Z      | L    |
| 11  | VCC2 UVLO         | UVLO         | L     | Н  | Х    | L    | L     | Х   | Х   | Н    | L    | Ζ    | Ζ      | L | Ζ      | Z      | L    |
| 12  |                   | UVLO         | L     | Н  | Х    | L    | L     | Х   | Х   | L    | L    | L    | Z      | L | Ζ      | Z      | L    |
| 13  |                   | UVLO         | L     | Н  | Н    | Н    | Х     | L   | Н   | Н    | Ζ    | Z    | L      | L | L*     | Z      | L    |
| 14  | V_BATT UVLO       | UVLO         | L     | Н  | Н    | Н    | Х     | L   | Н   | L    | L    | L    | Z      | L | Z      | Z      | L    |
| 15  | OC                | UVLO         | L     | Н  | Н    | Н    | Х     | Х   | L   | Н    | L    | Z    | Z      | L | Ζ      | Z      | L    |
| 16  |                   | UVLO         | L     | Н  | Н    | Н    | Х     | Х   | L   | L    | L    | L    | Z      | L | Ζ      | Z      | L    |
| 17  |                   | UVLO         | L     | Н  | Н    | L    | Н     | Х   | Х   | Н    | Т    | Z    | Z      | L | Z      | Z      | L    |
| 18  | V_BATT UVLO       | UVLO         | L     | Н  | Н    | L    | Н     | Х   | Х   | L    | Т    | L    | Z      | L | Z      | Z      | L    |
| 19  | V_D/(110V20       | UVLO         | L     | Н  | Н    | L    | L     | Х   | Х   | Н    | L    | Z    | Z      | L | Z      | Z      | L    |
| 20  |                   | UVLO         | L     | Н  | Н    | L    | L     | Х   | Х   | L    | L    | L    | Z      | L | Ζ      | Z      | L    |
| 21  |                   | 0            | Н     | L  | L    | Х    | Х     | L   | Н   | Н    | Ζ    | Ζ    | L      | L | L*     | Ζ      | L    |
| 22  | SCP<br>OT         | 0            | Н     | L  | L    | Х    | Х     | L   | Н   | L    | L    | L    | Z      | L | Ζ      | Z      | L    |
| 23  | VCC2 UVLO         | 0            | Н     | L  | L    | Х    | Х     | Х   | L   | Н    | L    | Ζ    | Ζ      | L | Ζ      | Z      | L    |
| 24  |                   | 0            | Н     | L  | L    | Х    | Х     | Х   | L   | L    | L    | L    | Ζ      | L | Ζ      | Z      | L    |
| 25  |                   | 0            | Н     | L  | Н    | Х    | Х     | L   | Н   | Н    | Ζ    | Ζ    | L      | Ζ | L*     | L      | Ζ    |
| 26  | SCP               | 0            | н     | L  | н    | х    | х     | L   | Н   | L    | L    | L    | Z      | Z | Z      | L      | L    |
| 27  | ОТ                | 0            | Н     | L  | Н    | Х    | Х     | Х   | L   | Н    | L    | Ζ    | Ζ      | Ζ | Ζ      | L      | Ζ    |
| 28  |                   | 0            | Н     | L  | н    | Х    | Х     | Х   | L   | L    | L    | L    | Z      | Z | Z      | L      | L    |
| 29  |                   | 0            | Н     | н  | L    | Х    | Х     | L   | Н   | Н    | Ζ    | Ζ    | L      | L | L*     | Ζ      | L    |
| 30  | SCP               | 0            | Н     | Н  | L    | Х    | Х     | L   | Н   | L    | L    | L    | Ζ      | L | Ζ      | Ζ      | L    |
| 31  | VCC2 UVLO         | 0            | Н     | Н  | L    | Х    | Х     | Х   | L   | Н    | L    | Ζ    | Ζ      | L | Ζ      | Ζ      | L    |
| 32  |                   | 0            | Н     | Н  | L    | Х    | Х     | Х   | L   | L    | L    | L    | Ζ      | L | Ζ      | Ζ      | L    |

: V\_BATT > UVLO, X: Don't care, Z: Hi-Z, T: 2-level turn off,

L\*: 40ms low pulse, SCP or OC is prior to the others.

| No.         Status         Image: Status |     |           | Input  |       |    |      |      |       |     | uou | Output |      |      |        |          |        |        |      |
|--|-----|-----------|--------|-------|----|------|------|-------|-----|-----|--------|------|------|--------|----------|--------|--------|------|
| OT         OC         L  | No. | Status    | V_BATT | SCPIN | ТО | VCC2 | OCIN | LVOFF | INB | INA | OUT2   | OUT1 | OUT2 | PROOUT | FLT_UVLO | FLT_SC | FLT_OT | OSFB |
| NCC2 UVL0         O         L <thl< th=""> <thl< th=""> <thl< t=""></thl<></thl<></thl<>   | 33  |           | 0      | L     | L  | L    | L    | Н     | Х   | Х   | Н      | Т    | Ζ    | Ζ      | L        | Z      | Z      | L    |
| 100         10   | 34  | ОТ        | 0      | L     | L  | L    | L    | Н     | Х   | Х   | L      | Т    | L    | Ζ      | L        | Ζ      | Ζ      | L    |
| 37         38         39         39         39         39         39         30<   | 35  | VCC2 UVLO | 0      | L     | L  | L    | L    | L     | Х   | Х   | Н      | L    | Ζ    | Ζ      | L        | Ζ      | Ζ      | L    |
| 38         39         SCP         0         H         H         H         X         X         L         H         L         L         L         Z <thz< th="">         Z         <thz< th="">         Z</thz<></thz<>  | 36  |           | 0      | L     | L  | L    | L    | L     | Х   | Х   | L      | L    | L    | Ζ      | L        | Ζ      | Ζ      | L    |
| SCP         O         H         H         H         X         X         L         H         Z  | 37  |           | 0      | Н     | Н  | Н    | Х    | Х     | L   | Н   | Н      | Ζ    | Ζ    | L      | Ζ        | L*     | Ζ      | Z    |
| 39         0         H         H         X         X         X         L         H         Z   | 38  | SCD       | 0      | Н     | Н  | Н    | Х    | Х     | L   | Н   | L      | L    | L    | Ζ      | Ζ        | Ζ      | Ζ      | L    |
| 11         0         1 <   | 39  | 306       | 0      | Н     | Н  | Н    | Х    | Х     | Х   | L   | Н      | Ζ    | Ζ    | Ζ      | Ζ        | Ζ      | Ζ      | Z    |
| 100         1  | 40  |           | 0      | Н     | Н  | Н    | Х    | Х     | Х   | L   | L      | L    | L    | Ζ      | Ζ        | Ζ      | Ζ      | L    |
| 43         OT         O         L         L         H         L         X         X         H         L         Z         Z         L         L         L           44         O         L         H         L         H         L         X         X         L         L         Z         Z         L         L         L         L           45         O         L         H         L         L         H         X         X         L         T         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z <td>41</td> <td></td> <td>0</td> <td>L</td> <td>L</td> <td>Н</td> <td>L</td> <td>Н</td> <td>Х</td> <td>Х</td> <td>Н</td> <td>Т</td> <td>Ζ</td> <td>Z</td> <td>Z</td> <td>Ζ</td> <td>L</td> <td>Z</td>  | 41  |           | 0      | L     | L  | Н    | L    | Н     | Х   | Х   | Н      | Т    | Ζ    | Z      | Z        | Ζ      | L      | Z    |
| 43     0     1 </td <td>42</td> <td>ОТ</td> <td>0</td> <td>L</td> <td>L</td> <td>Н</td> <td>L</td> <td>Н</td> <td>Х</td> <td>Х</td> <td>L</td> <td>Т</td> <td>L</td> <td>Ζ</td> <td>Ζ</td> <td>Ζ</td> <td>L</td> <td>L</td>  | 42  | ОТ        | 0      | L     | L  | Н    | L    | Н     | Х   | Х   | L      | Т    | L    | Ζ      | Ζ        | Ζ      | L      | L    |
| 45     0     1 </td <td>43</td> <td>01</td> <td>0</td> <td>L</td> <td>L</td> <td>Н</td> <td>L</td> <td>L</td> <td>Х</td> <td>Х</td> <td>Н</td> <td>L</td> <td>Z</td> <td>Ζ</td> <td>Ζ</td> <td>L</td> <td>L</td> <td>Z</td>  | 43  | 01        | 0      | L     | L  | Н    | L    | L     | Х   | Х   | Н      | L    | Z    | Ζ      | Ζ        | L      | L      | Z    |
| 46         0         L         H         L         L         H         X         X         L         T         L         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         Z         L         Z         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         Z         Z         L         Z         Z         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L         L <thl< th="">         L         L         L</thl<>   | 44  |           | 0      | L     | L  | Н    | L    | L     | Х   | Х   | L      | L    | L    | Ζ      | Ζ        | L      | L      | L    |
| VCC2 UVLO         O         L         H         L         L         L         X         X         H         Z         Z         Z         L         Z  | 45  |           | 0      | L     | Н  | L    | L    | Н     | Х   | Х   | Н      | Т    | Ζ    | Ζ      | L        | Ζ      | Ζ      | L    |
| 47     0     L     H     L     L     X     X     H     Z     Z     L     Z </td <td>46</td> <td></td> <td>0</td> <td>L</td> <td>Н</td> <td>L</td> <td>L</td> <td>Н</td> <td>Х</td> <td>Х</td> <td>L</td> <td>Т</td> <td>L</td> <td>Z</td> <td>L</td> <td>Ζ</td> <td>Ζ</td> <td>L</td>  | 46  |           | 0      | L     | Н  | L    | L    | Н     | Х   | Х   | L      | Т    | L    | Z      | L        | Ζ      | Ζ      | L    |
| 49     0     L     H     H     X     L     H     H     Z     Z     L     Z     L     Z </td <td>47</td> <td>1002 0120</td> <td>0</td> <td>L</td> <td>Н</td> <td>L</td> <td>L</td> <td>L</td> <td>Х</td> <td>Х</td> <td>Н</td> <td>Ζ</td> <td>Ζ</td> <td>Ζ</td> <td>L</td> <td>Ζ</td> <td>Ζ</td> <td>L</td>   | 47  | 1002 0120 | 0      | L     | Н  | L    | L    | L     | Х   | Х   | Н      | Ζ    | Ζ    | Ζ      | L        | Ζ      | Ζ      | L    |
| 50         OC         L         H         H         H         X         L         H         L         L         L         Z  | 48  |           | 0      | L     | Н  | L    | L    | L     | Х   | Х   | L      | L    | L    | Z      | L        | Ζ      | Ζ      | L    |
| OC         O         L         H         H         X         X         L         H         L         L         Z   | 49  |           | 0      | L     | Н  | Н    | Н    | Х     | L   | Н   | Н      | Ζ    | Ζ    | L      | Ζ        | L*     | Ζ      | Z    |
| 51       0       L       H       H       X       X       L       H       L       Z   | 50  | 00        |        | L     | Н  | Н    | Н    | Х     | L   | Н   | L      | L    | L    |        |          |        |        |      |
| 53       0       L       H       H       L       H       H       X       H       T       Z   |     |           |        | L     |    |      |      |       |     | L   | Н      | L    | L    |        |          |        |        | Z    |
| 54         55         56         57         58         59         60         61         62         63  | 52  |           | 0      | L     | Н  | Н    | Н    | Х     | Х   | L   | L      | L    | L    | Z      | Z        | Z      | Z      | L    |
| 55       56         56         57         58         59         60         61         62         63  | 53  |           | 0      | L     | Н  | Н    | L    | Н     | Н   | Х   | Н      | Т    | Ζ    | Z      | Z        | Z      | Ζ      | Z    |
| 56         57         58         59         60         61         62         63  | 54  |           | 0      | L     | Н  | Н    | L    | Н     | Н   | Х   | L      | Т    | L    | Z      | Z        | Ζ      | Ζ      | L    |
| 57         58         59         60         61         62         63   | 55  |           | 0      | L     | Н  | Н    | L    | L     | Н   | Х   | Н      | L    | Ζ    | Ζ      | Ζ        | Ζ      | Ζ      | Z    |
| 58       Normal       O       L       H       H       L       H       L       H       Z </td <td>56</td> <td></td> <td>0</td> <td>L</td> <td>Н</td> <td>Н</td> <td>L</td> <td>L</td> <td>Н</td> <td>Х</td> <td>L</td> <td>L</td> <td>L</td> <td>Ζ</td> <td>Ζ</td> <td>Ζ</td> <td>Ζ</td> <td>L</td>   | 56  |           | 0      | L     | Н  | Н    | L    | L     | Н   | Х   | L      | L    | L    | Ζ      | Ζ        | Ζ      | Ζ      | L    |
| Normal       O       L       H       H       L       L       H       H       Z <td>57</td> <td></td> <td>0</td> <td>L</td> <td>Н</td> <td>Н</td> <td>L</td> <td>Н</td> <td>L</td> <td>Н</td> <td>Н</td> <td>Н</td> <td>Z</td> <td>Z</td> <td>Z</td> <td>Z</td> <td>Z</td> <td>Ζ</td>   | 57  |           | 0      | L     | Н  | Н    | L    | Н     | L   | Н   | Н      | Н    | Z    | Z      | Z        | Z      | Z      | Ζ    |
| 59       O       L       H       H       L       L       H       H       H       Z   | 58  | - Normal  | 0      | L     | Н  | Н    | L    | Н     | L   | Н   | L      | Н    | Ζ    | Ζ      | Ζ        | Ζ      | Z      | L    |
| 61         62         63   | 59  |           | 0      | L     | н  | н    | L    | L     | L   | Н   | Н      | Н    | Ζ    | Ζ      | Ζ        | Ζ      | Z      | Z    |
| 62       O       L       H       H       L       H       L       Z   | 60  |           | 0      | L     | н  | н    | L    | L     | L   | Н   | L      | Н    | Ζ    | Z      | Z        | Z      | Z      | L    |
| 63 O L H H L L L H L Z Z Z Z Z Z   | 61  |           | 0      | L     | Н  | н    | L    | Н     | L   | L   | Н      | Т    | Ζ    | Ζ      | Ζ        | Ζ      | Z      | Z    |
|  | 62  |           | 0      | L     | н  | н    | L    | Н     | L   | L   | L      | Т    | L    | Z      | Z        | Z      | Z      | L    |
| 64 O L H H L L L L L L Z Z Z L   | 63  |           | 0      | L     | н  | н    | L    | L     | L   | L   | Н      | L    | Ζ    | Z      | Z        | Z      | Z      | Z    |
|  | 64  |           | 0      | L     | н  | н    | L    | L     | L   | L   | L      | L    | L    | Z      | Z        | Z      | Z      | L    |

: V\_BATT > UVLO, X: Don't care, Z: Hi-Z, T: 2-level turn off,

L\*: 40ms low pulse, SCP or OC is prior to the others.

12. Power Supply Startup / Shutdown Sequence



- ------ : Since the VCC2 to GND2 pin voltage is low and the output MOS does not turn ON, the output pins become Hi-Z conditions. ----- :Since the V\_BATT pin voltage is low and the FLT\_UVLO output MOS does not turn
  - ON, the output pins become Hi-Z conditions.

Figure 38. Power Supply Startup / Shutdown Sequence

## Selection of Components Externally Connected



Figure 39. For using switching power supply controller



## I/O Equivalent Circuit

| Pin No. | Pin Name                           | - Input Output Equivalent Circuit Diagram |  |  |  |  |  |  |
|---------|------------------------------------|---|--|--|--|--|--|--|
| 140.    | Pin Function                       |   |  |  |  |  |  |  |
| 2       | UVLOIN                             |   |  |  |  |  |  |  |
|         | Output-side UVLO setting pin       |   |  |  |  |  |  |  |
| 3       | OCIN                               |   |  |  |  |  |  |  |
|         | Over current detection pin         |   |  |  |  |  |  |  |
| 4       | SCPIN                              |   |  |  |  |  |  |  |
|         | Short circuit detection pin        | GND2                                      |  |  |  |  |  |  |
|         | LVOFF                              | VCC2                                      |  |  |  |  |  |  |
| 5       | 2-level turn off level setting pin |   |  |  |  |  |  |  |
|         | RTOFF                              | VCC2                                      |  |  |  |  |  |  |
| 6       | 2-level turn off time setting pin  |   |  |  |  |  |  |  |
|         | TCOMP                              | VCC2                                      |  |  |  |  |  |  |
| 7       | Temperature compensation pin of OC |   |  |  |  |  |  |  |

## I/O Equivalent Circuit - continued

|         | Pin Name  |   |  |  |
|---------|---|---|--|--|
| Pin No. | Pin Function  | Input Output Equivalent Circuit Diagram |  |  |
| 8       | то  | VCC2                                    |  |  |
|         | Constant current output pin /<br>Over temperature detection pin   |   |  |  |
|         | TC  |   |  |  |
| 9       | Constant current setting resistor connection pin                  |   |  |  |
|         | PROOUT  |   |  |  |
| 10      | Soft turn-off pin   | GND2                                    |  |  |
|         | OUT1  |   |  |  |
| 12      | Output pin  | GND2                                    |  |  |
| 13      | OUT2  | VCC2                                    |  |  |
|         | Input and output pin for miller clamp /<br>Gate voltage input pin |   |  |  |

#### I/O Equivalent Circuit - continued Pin Name Pin No. Input Output Equivalent Circuit Diagram Pin Function FLT\_UVLO 16 Fault (UVLO) output pin FLT\_UVLO OSFB OSFB 19 Output state feedback output pin W FLT SC FLT\_OT FLT\_OT 20 Fault (OT) output pin FLT\_SC GND1 21 Fault (SCP) output pin Inter nal power V\_BATT( INB supply 17 Control input pin B INA INB INA 18 GND1( Control input pin A Internal Power V\_BATT( Supply FB 22 FΒ Error amplifier inverting input pin for switching controller GND1 (

## I/O Equivalent Circuit - continued

| Pin | Pin Name   | Input Output Equivalent Circuit Diagram       |  |  |
|-----|--|---|--|--|
| No. | Pin Function   |   |  |  |
| 23  | COMP   | V_BATT O Internal power<br>supply<br>COMP O M |  |  |
| 23  | Error amplifier output pin for switching controller                  |   |  |  |
| 25  | VREG   | Internal power<br>supply                      |  |  |
|     | Power supply pin for driving MOS FET<br>for switching controller     |   |  |  |
| 26  | FET_G  |   |  |  |
|     | MOS FET control pin for switching<br>controller                      |   |  |  |
|     | SENSE  |   |  |  |
| 27  | Current feedback resistor connection pin<br>for switching controller |   |  |  |

## **Operational Notes**

#### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

#### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

#### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

#### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

#### 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

#### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

#### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

#### 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

#### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

#### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

## **Operational Notes – continued**

#### 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

#### 12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode. When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Figure 41. Example of monolithic IC structure

#### 13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.



Product class C : for Automotive applications Packaging and forming specification E2 : Embossed tape and reel (SSOP-B28W)

## **Marking Diagrams**



## **Physical Dimension, Tape and Reel Information** Package Name SSOP-B28W 9. $2\pm 0.1$ (Max 9.55 (include.BURR)) $4^{\circ} + 6^{\circ}_{-4^{\circ}}$ 281 5 3 $10.4\pm0.$ 0 + 0. 15 $\sim$ $\infty$ $2\pm 0.$ $5\pm 0.$ . 0 14 1PIN MARK 0.375 0. $17 \stackrel{+0.05}{_{-0.03}}$ S 0 2. 4MAX $2\pm 0.$ сi 05 □0.08S $1\pm0.$ 0. $22^{+0.05}_{-0.04}$ $\bigcirc 0.08 \bigcirc$ 0.65 o. PKG:SSOP-B28W Drawing No. ; EX072-5001 $(UN \ I \ T : mm)$ < Tape and Reel Information > Таре Embossed carrier tape Quantity 1500pcs Direction of feed E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



## **Revision History**

| Date   | Revision | Changes                          |  |
|--|----------|----------------------------------|--|
| 15.Feb.2016  | 001      | New Release                      |  |
| 06.Jun.2016 002 Modify typo (p.1-9,11-12,14-24,27)<br>Clarified the description and context (p.25-26, 29-32) |          |                                  |  |
| 03.Apr.2018  | 003      | p. 9 Adding UL1577 Ratings Table |  |

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| JAPAN   | USA | EU         | CHINA   |
|---------|-----|------------|---------|
| CLASSII |     | CLASS II b | CLASSII |
|         |     | CLASSⅢ     | CLASSII |

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  - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
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