Datasheet

Gate Driver Providing Galvanic Isolation Series

Isolation Voltage 2500 Vrms 1ch Gate Driver Providing Galvanic Isolation

BM61M22BFJ-C

General Description

The BM61M22BFJ-C is a gate driver providing galvanic isolation with an isolation voltage of 2500 Vrms, maximum I/O delay time of 60 ns, and minimum input pulse width of 60 ns. It incorporates the Under-voltage Lockout (UVLO) function.

Features

- AEC-Q100 Qualified *(Note 1)*
- Providing Galvanic Isolation
- Under-voltage Lockout Function
- UL1577 (pending)

(Note 1) Grade1

Applications

- IGBT Gate Driver
- MOSFET Gate Driver

Key Specifications

■ Isolation Voltage:	2500 Vrms
■ Maximum Gate Drive Voltage:	24 V
■ Maximum I/O Delay Time:	60 ns
■ Minimum Input Pulse Width:	60 ns

Package	**W (Typ) x D (Typ) x H (Max)**
SOP-JW8	4.9 mm x 6.0 mm x 1.65 mm

Typical Application Circuits

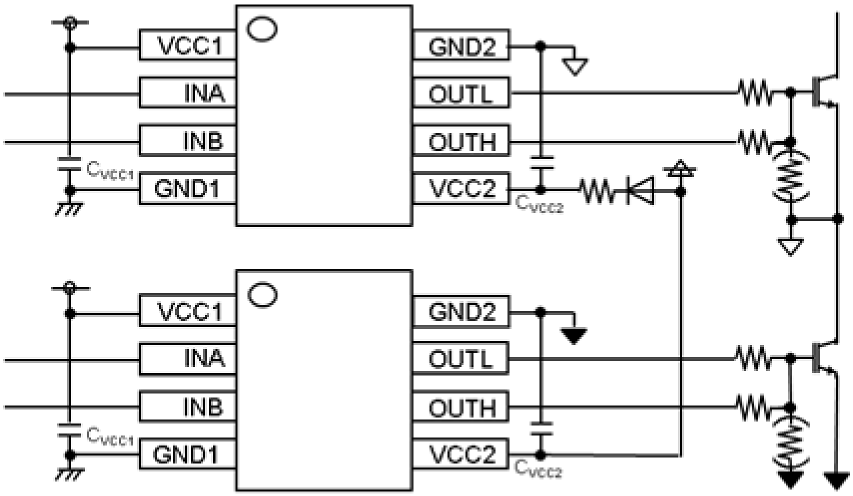

Figure 1. Typical Application Circuits (in case of 2ch)

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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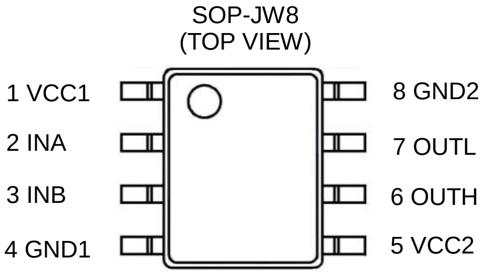
Recommended Range of External Constants

Pin Name	Symbol	Recommended Value			Unit
		Min	Typ	Max	
VCC1	C_{VCC1}	0.1	1.0	-	µF
VCC2	C_{VCC2}	0.33	-	-	µF

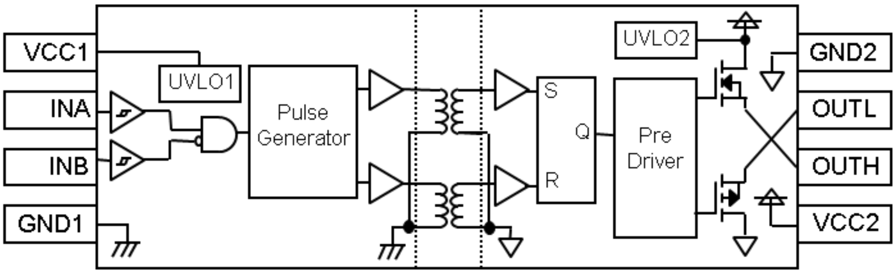
C_{VCC2}: For supplying gate charge current of MOS FET/IGBT.

Pin Configurations



Pin No.	Pin Name	Function
1	VCC1	Input side power supply pin
2	INA	Control input pin A
3	INB	Control input pin B
4	GND1	Input side ground pin
5	VCC2	Output side power supply pin
6	OUTH	Source side output pin for gate driving
7	OUTL	Sink side output pin for gate driving
8	GND2	Output side ground pin

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Input Side Supply Voltage	V_{CC1}	-0.3 to +7.0 *(Note 2)*	V
Output Side Supply Voltage	V_{CC2}	-0.3 to +30.0 *(Note 3)*	V
INA Pin Input Voltage	V_{INA}	-0.3 to +VCC1+0.3 or +7.0 *(Note 2)*	V
INB Pin Input Voltage	V_{INB}	-0.3 to +VCC1+0.3 or +7.0 *(Note 2)*	V
Gate Drive Output Current (10 µs)	$I_{OUTPEAK}$	self limited	A
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

(Note 2) Relative to GND1.
(Note 3) Relative to GND2.

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 4)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 6)*	2s2p*(Note 7)*	
SOP-JW8				
Input Side Junction to Ambient	θ_{JA1}	202.0	111.6	°C/W
Output Side Junction to Ambient	θ_{JA2}	202.5	111.6	°C/W
Input Side Junction to Top Characterization Parameter*(Note 5)*	Ψ_{JT1}	68	48	°C/W
Output Side Junction to Top Characterization Parameter*(Note 5)*	Ψ_{JT2}	72	42	°C/W

(Note 4) Based on JESD51-2A (Still-Air).
(Note 5) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 6) Using a PCB board based on JESD51-3.
(Note 7) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Input Side Supply Voltage	V_{CC1}*(Note 8)*	4.5	5.5	V
Output Side Supply Voltage	V_{CC2}*(Note 9)*	9	24	V
Operating Temperature	Topr	-40	+125	°C

(Note 8) Relative to GND1.
(Note 9) Relative to GND2.

Insulation Related Characteristics

Parameter	Symbol	Characteristic	Unit
Insulation Resistance (V_{IO} = 500 V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage (1 min)	V_{ISO}	2500	Vrms
Insulation Test Voltage (1 s)	V_{ISO}	3000	Vrms

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Electrical Characteristics

(Unless otherwise specified Ta = -40 °C to +125 °C, V_{CC1} = 4.5 V to 5.5 V, V_{CC2} = 9 V to 24 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Input Side Circuit Current 1	I_{CC11}	0.25	0.50	1.00	mA	INA = L, INB = H
Input Side Circuit Current 2	I_{CC12}	1.50	3.00	6.00	mA	INA = H, INB = L
Output Side Circuit Current 1	I_{CC21}	0.30	0.60	1.20	mA	OUT (OUTL and OUTH are shorted) = L
Output Side Circuit Current 2	I_{CC22}	0.22	0.45	0.90	mA	OUT = H
Logic Block						
Logic High Level Input Voltage	V_{INH}	2.0	-	V_{CC1}	V	INA, INB
Logic Low Level Input Voltage	V_{INL}	0	-	0.8	V	INA, INB
Logic Pull Down Resistance	R_{IND}	25	50	100	kΩ	INA
Logic Pull Up Resistance	R_{INU}	25	50	100	kΩ	INB
Minimum Input Pulse Width	t_{INMIN}	60	-	-	ns	INA, INB
Output						
OUT ON Resistance (Source)	R_{ONH}	0.60	1.35	3.00	Ω	I_{OUT} = -40 mA
OUT ON Resistance (Sink)	R_{ONL}	0.25	0.80	1.70	Ω	I_{OUT} = +40 mA
OUT Maximum Current (Source)	$I_{OUTMAXH}$	2.0	3.0	-	A	V_{CC2} = 15 V, Guaranteed by design
OUT Maximum Current (Sink)	$I_{OUTMAXL}$	2.0	3.0	-	A	V_{CC2} = 15 V, Guaranteed by design
Turn ON Time	t_{PONA}	40	50	60	ns	INA = PWM, INB = L
	t_{PONB}	40	50	60	ns	INA = H, INB = PWM
Turn OFF Time	t_{POFFA}	40	50	60	ns	INA = PWM, INB = L
	t_{POFFB}	40	50	60	ns	INA = H, INB = PWM
Propagation Distortion	t_{PDISTA}	-10	0	+10	ns	t_{POFFA} - t_{PONA}
	t_{PDISTB}	-10	0	+10	ns	t_{POFFB} - t_{PONB}
Part-to-part Skew	t_{SK-PP}	-	-	12	ns	Same temperature Guaranteed by design
Rise Time	t_{RISE}	-	15	-	ns	OUT - GND2 = 2 nF
Fall Time	t_{FALL}	-	15	-	ns	OUT - GND2 = 2 nF
Common Mode Transient Immunity	CM	100	-	-	kV/µs	Guaranteed by design
Protection Functions						
VCC1 UVLO OFF Voltage	V_{UVLO1H}	3.35	3.50	3.65	V	
VCC1 UVLO ON Voltage	V_{UVLO1L}	3.25	3.40	3.55	V	
VCC1 UVLO Mask Time	$t_{UVLO1MSK}$	0.6	1.7	3.4	µs	
VCC2 UVLO OFF Voltage	V_{UVLO2H}	7.2	7.8	8.4	V	
VCC2 UVLO ON Voltage	V_{UVLO2L}	6.8	7.4	8.0	V	
VCC2 UVLO Mask Time	$t_{UVLO2MSK}$	1.0	2.9	5.0	µs	

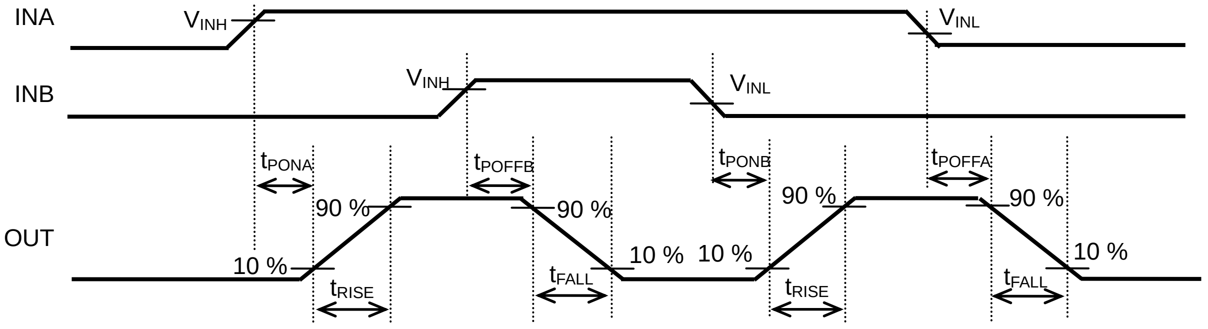

Figure 2. IN-OUT Timing Chart

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Typical Performance Curves

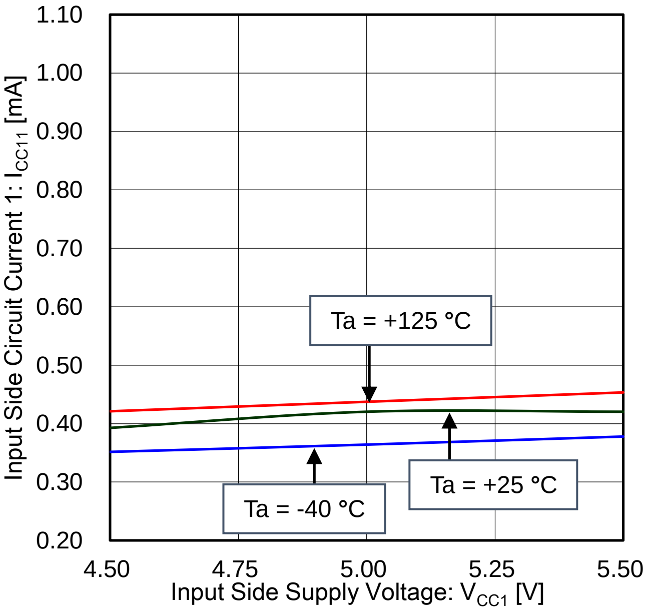

Figure 3. Input Side Circuit Current 1
vs Input Side Supply Voltage

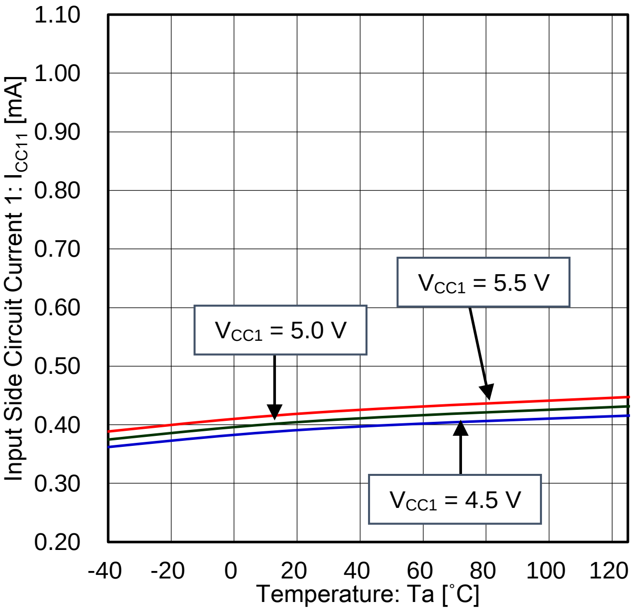

Figure 4. Input Side Circuit Current 1 vs Temperature

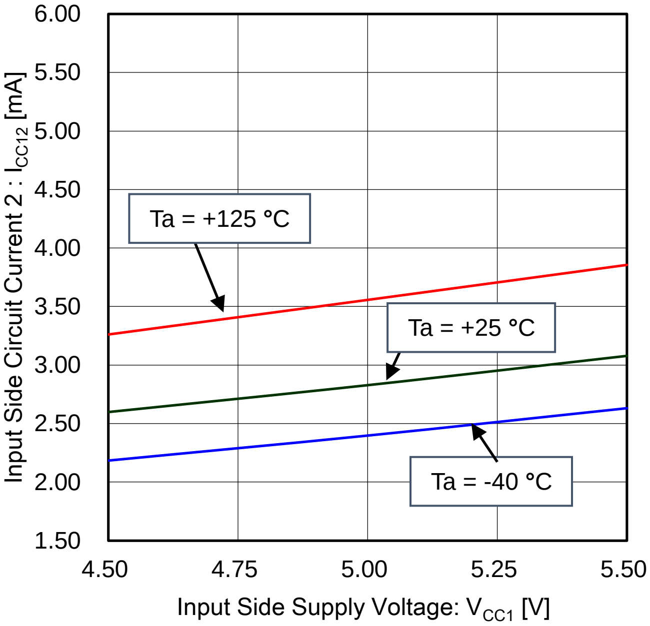

Figure 5. Input Side Circuit Current 2
vs Input Side Supply Voltage

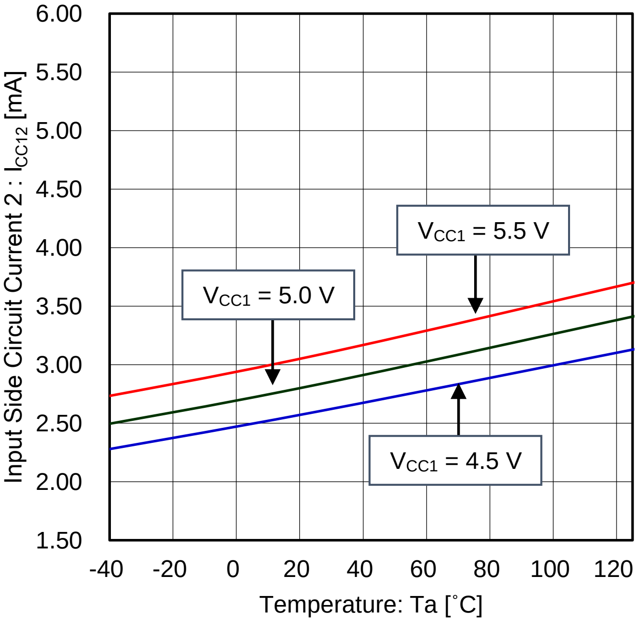

Figure 6. Input Side Circuit Current 2 vs Temperature

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Typical Performance Curves - continued

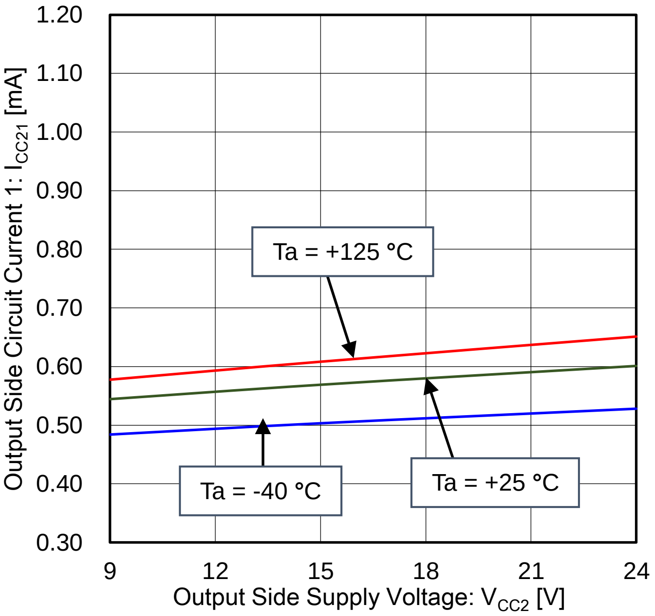

Figure 7. Output Side Circuit Current 1
vs Output Side Supply Voltage (OUT = L)

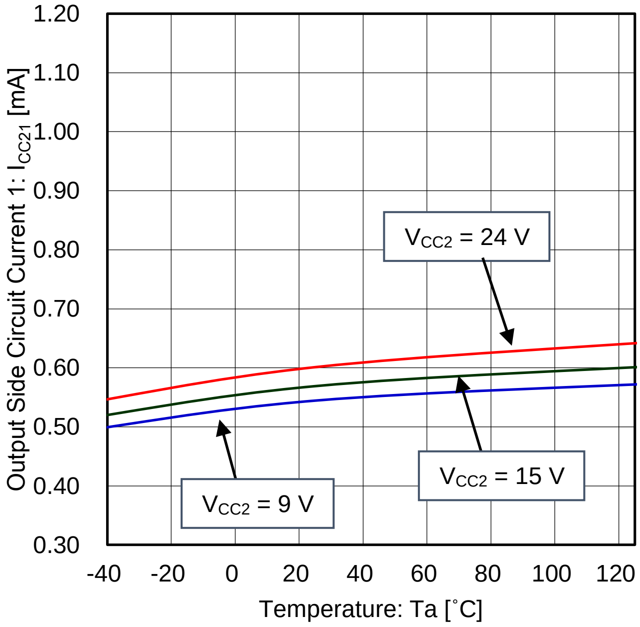

Figure 8. Output Side Circuit Current 1
vs Temperature (OUT = L)

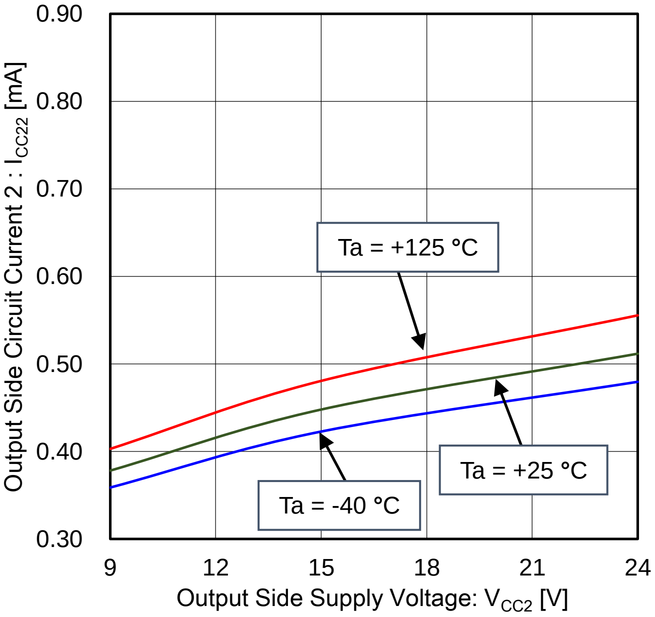

Figure 9. Output Side Circuit Current 2
vs Output Side Supply Voltage (OUT = H)

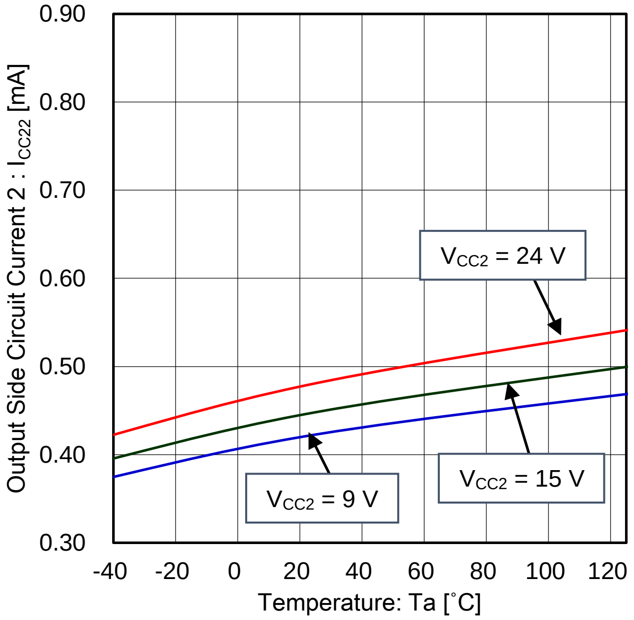

Figure 10. Output Side Circuit Current 2
vs Temperature (OUT = H)

Typical Performance Curves - continued

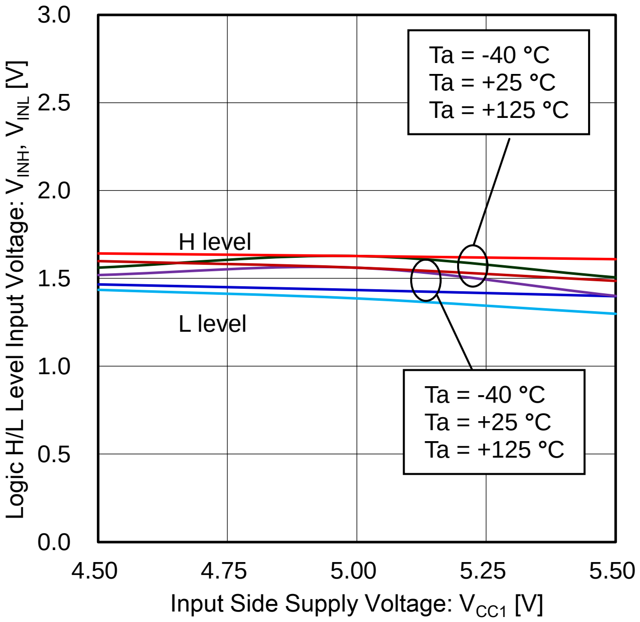

Figure 11. Logic H/L Level Input Voltage vs Input Side Supply Voltage

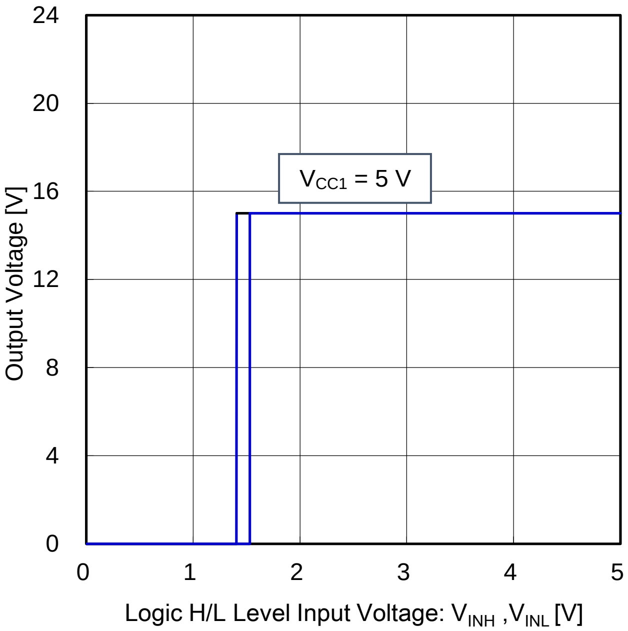

Figure 12. Output Voltage vs Logic H/L Level Input Voltage (V_{CC1} = 5 V, V_{CC2} = 15 V, Ta = 25 °C)

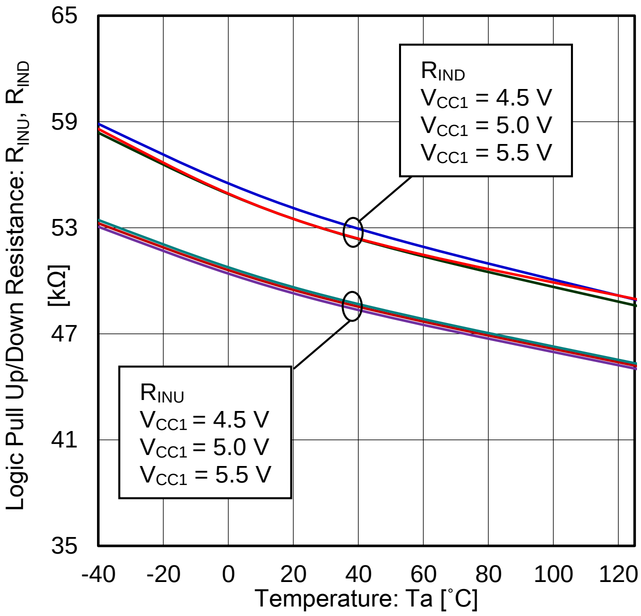

Figure 13. Logic Pull Up/Down Resistance vs Temperature

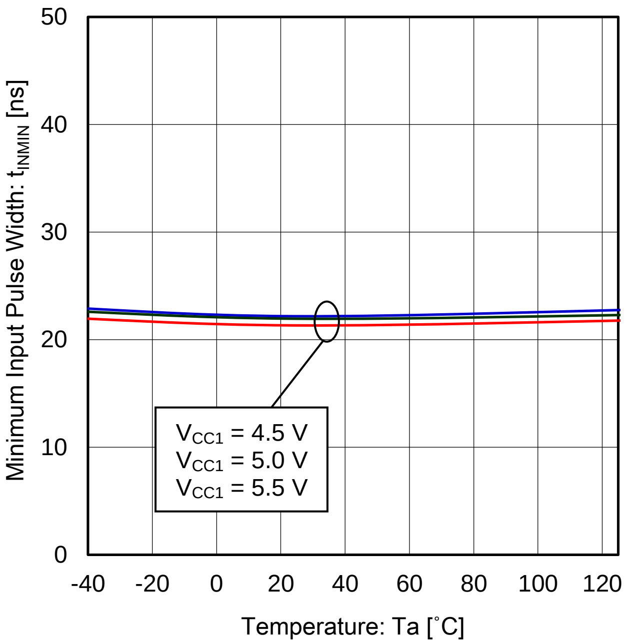

Figure 14. Minimum Input Pulse Width vs Temperature

Typical Performance Curves – continued

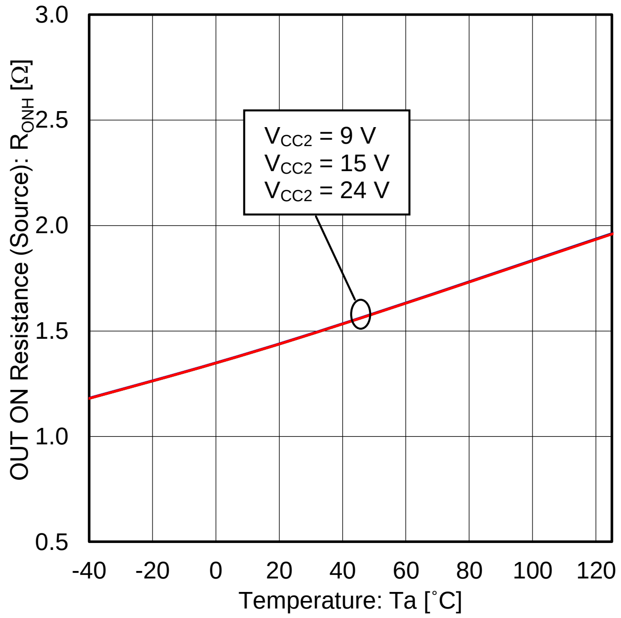

Figure 15. OUT ON Resistance (Source) vs Temperature

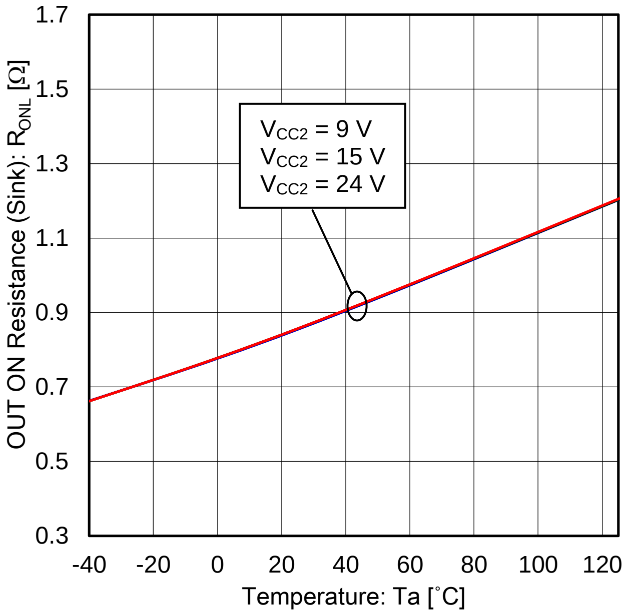

Figure 16. OUT ON Resistance (Sink) vs Temperature

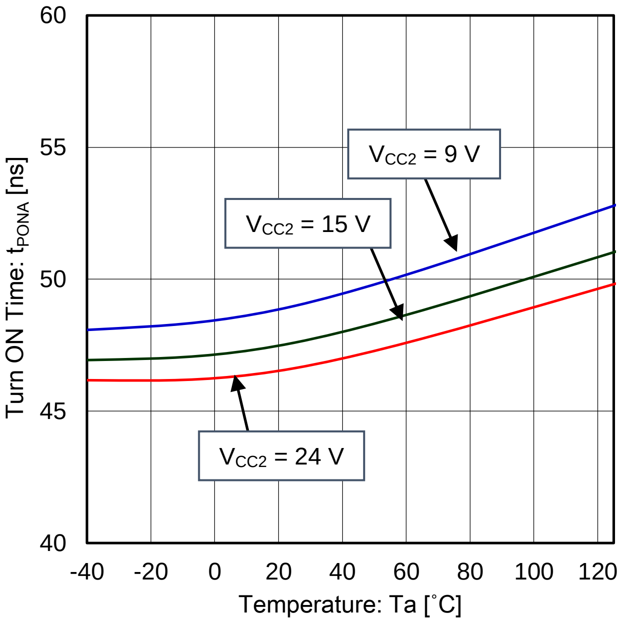

Figure 17. Turn ON Time vs Temperature
(INA = PWM, INB = L)

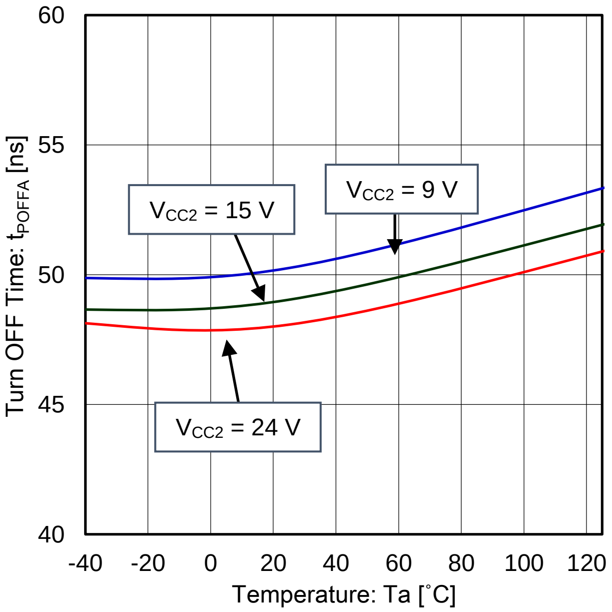

Figure 18. Turn OFF Time vs Temperature
(INA = PWM, INB = L)

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Typical Performance Curves – continued

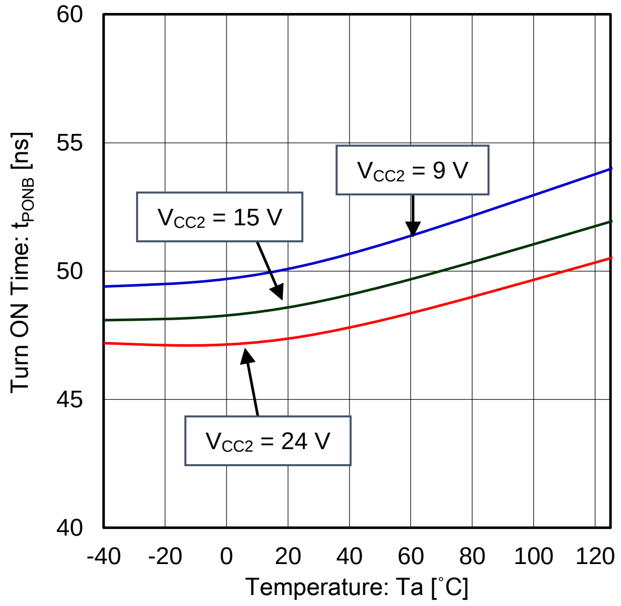

Figure 19. Turn ON Time vs Temperature
(INA = H, INB = PWM)

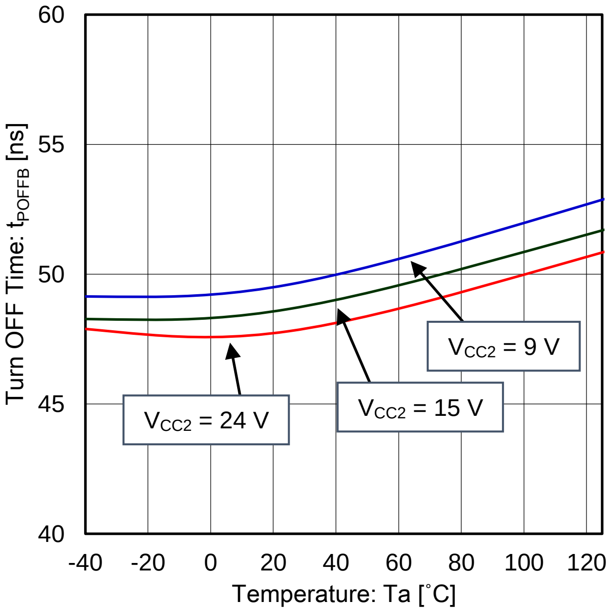

Figure 20. Turn OFF Time vs Temperature
(INA = H, INB = PWM)

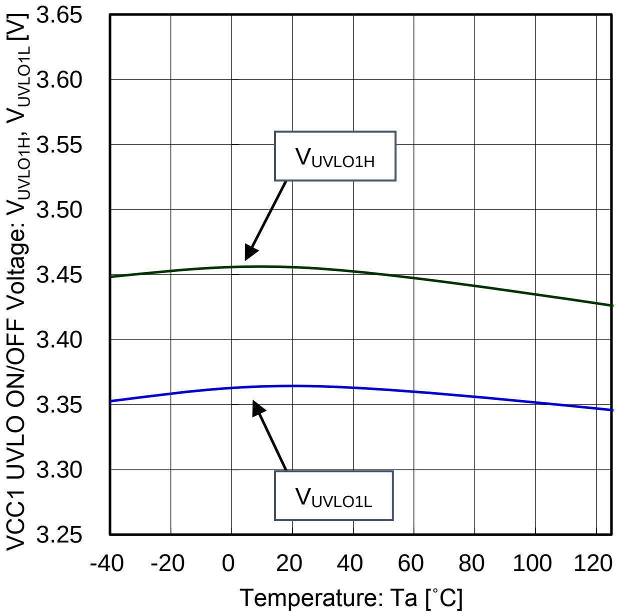

Figure 21. VCC1 UVLO ON/OFF Voltage vs Temperature

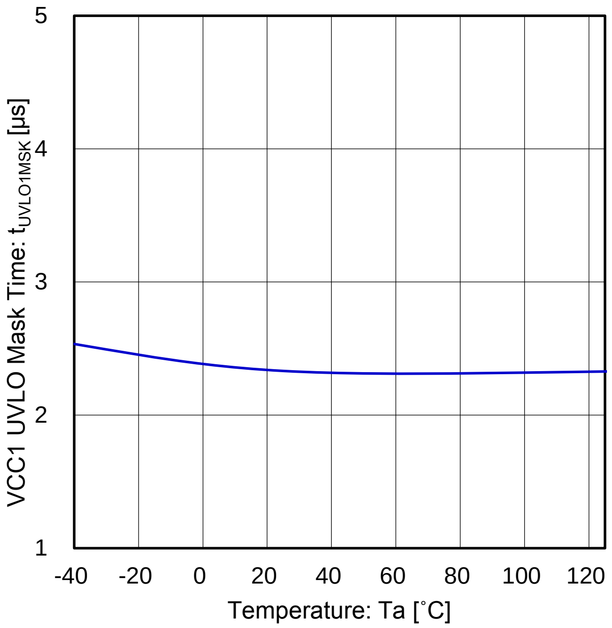

Figure 22. VCC1 UVLO Mask Time vs Temperature

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Typical Performance Curves – continued

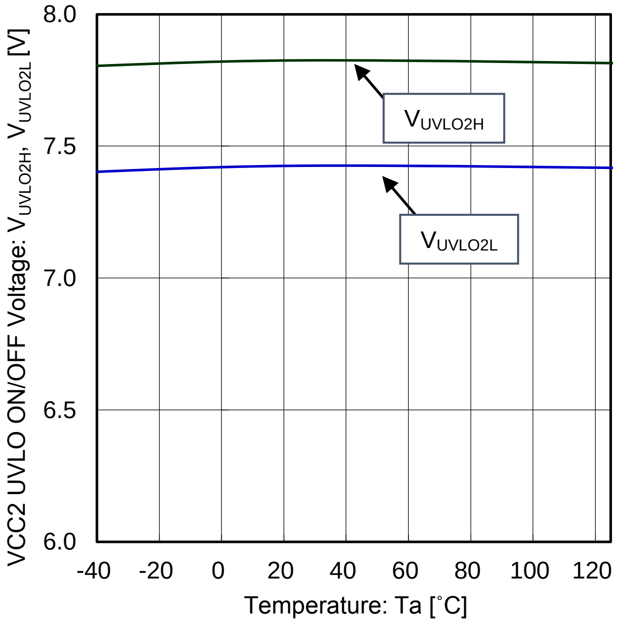

Figure 23. VCC2 UVLO ON/OFF Voltage vs Temperature

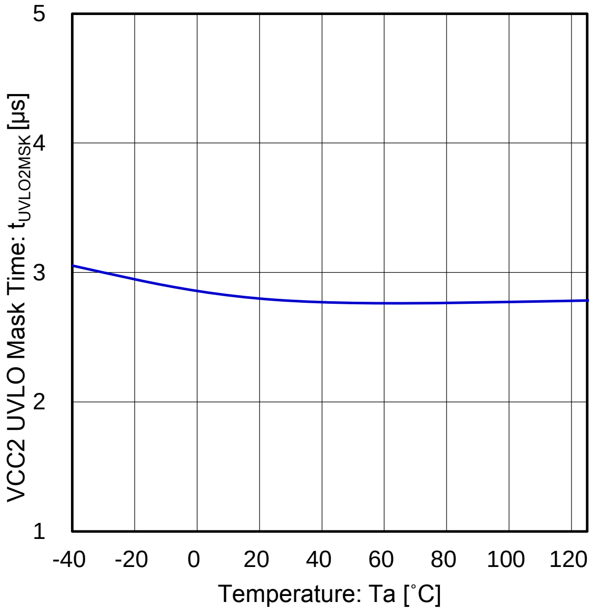

Figure 24. VCC2 UVLO Mask Time vs Temperature

Pin Descriptions

1. VCC1 (Input side power supply pin)
   The VCC1 pin is a power supply pin on the input side. To suppress voltage fluctuations due to the current to drive internal transformers, connect a bypass capacitor between the VCC1 and the GND1 pins.

2. GND1 (Input side ground pin)
   The GND1 pin is a ground pin on the input side.

3. VCC2 (Output side power supply pin)
   The VCC2 pin is a power supply pin on the output side. To reduce voltage fluctuations due to the OUTH and OUTL pins output current, connect a bypass capacitor between the VCC2 pin and the GND2 pin.

4. GND2 (Output side ground pin)
   The GND2 pin is a ground pin on the output side.

5. INA, INB (Control input pin)
   The INA, INB are pins used to determine output logic.

INB	INA	OUTH	OUTL
L	L	Hi-Z	L
L	H	H	Hi-Z
H	L	Hi-Z	L
H	H	Hi-Z	L

6. OUTH, OUTL (Output pin for gate driving)
   The OUT pin is used to drive the gate of a power device. OUTH is the source output. OUTL is the sink output.

Description of Functions and Examples of Constant Setting

1. Under-voltage Lockout (UVLO) Function

The BM61M22BFJ-C incorporates the Under-voltage Lockout (UVLO) Function both on the input and the output sides. When the power supply voltage drops to the UVLO ON voltage (low voltage side typ 3.4 V, high voltage side typ 7.4 V), the OUT (OUTL and OUTH are shorted) pin will output the “L” signal. When the power supply voltage rises to the UVLO OFF voltage, these pins are reset. In addition, to prevent malfunctions due to noises, a mask time of $t_{UVLO1MSK}$ (typ 1.7 μs) and $t_{UVLO2MSK}$ (typ 2.9 μs) are set on both the low and the high voltage sides. After the input side UVLO is released, the OUT pin will output the “H” signal from the time after the input signal switches.

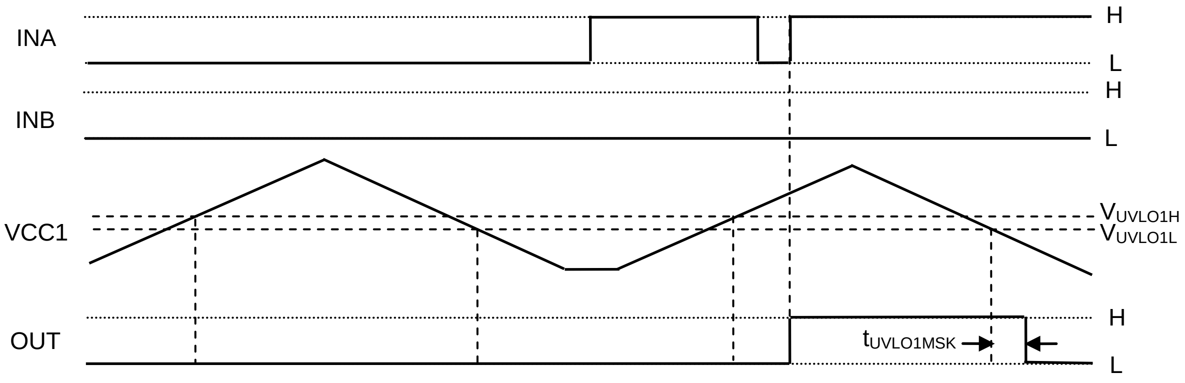

Figure 25. Input Side UVLO Function Operation Timing Chart

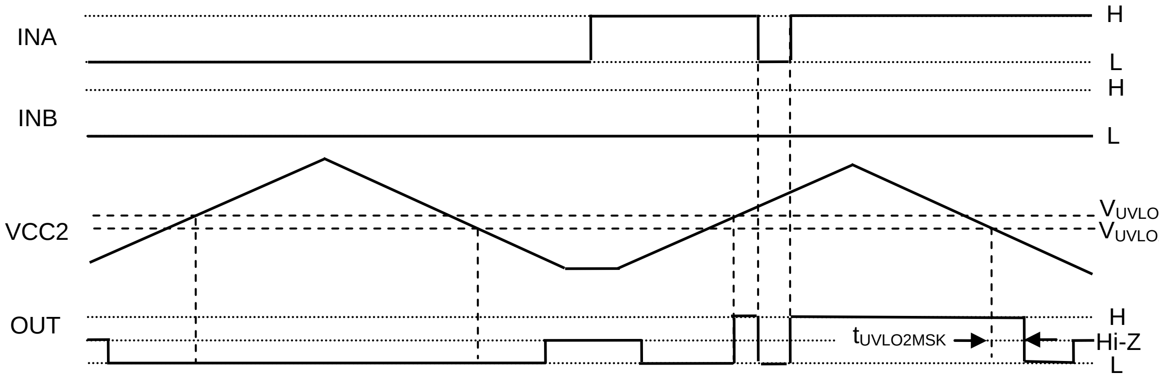

Figure 26. Output Side UVLO Function Operation Timing Chart

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Description of Functions and Examples of Constant Setting – continued

2. I/O Condition Table

No.	Status	Input				Output	
		VCC1	VCC2	INB	INA	OUTH	OUTL
1	VCC1UVLO	UVLO	X	X	X	Hi-Z	L
2	VCC2UVLO	X	UVLO	X	X	Hi-Z	L
3	INB Active	○	○	H	X	Hi-Z	L
4	Normal operation L input	○	○	L	L	Hi-Z	L
5	Normal operation H input	○	○	L	H	H	Hi-Z

○: VCC1 or VCC2 > UVLO, X: Don't care

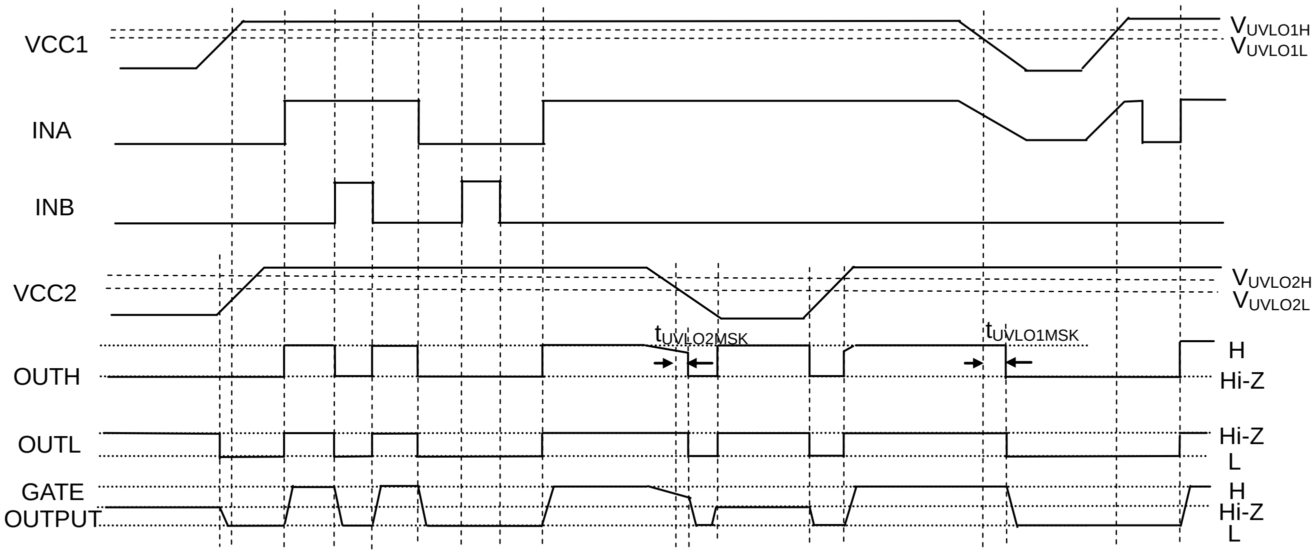

Figure 27. IN-OUT Timing Chart

Selection of Components Externally Connected

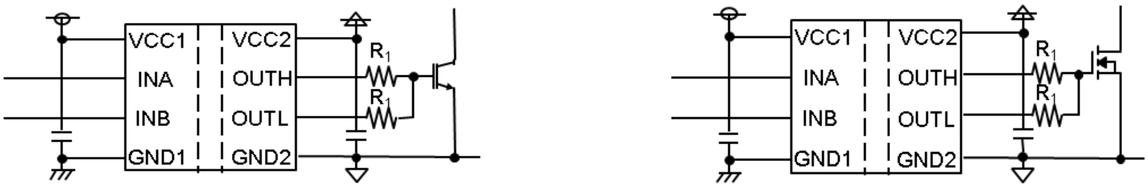

Figure 28. For Driving IGBT or MOSFET

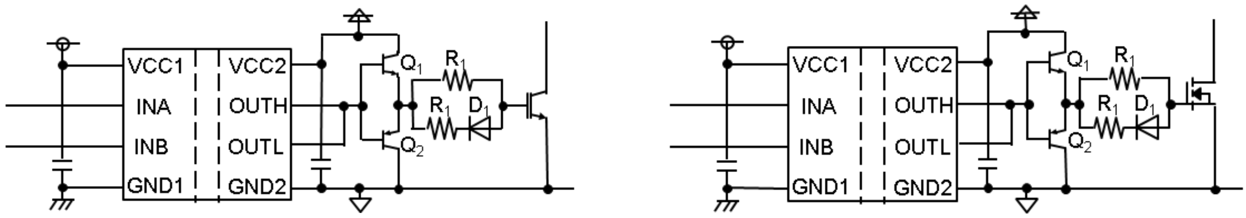

Figure 29. For Driving IGBT or MOSFET with Buffer Circuits

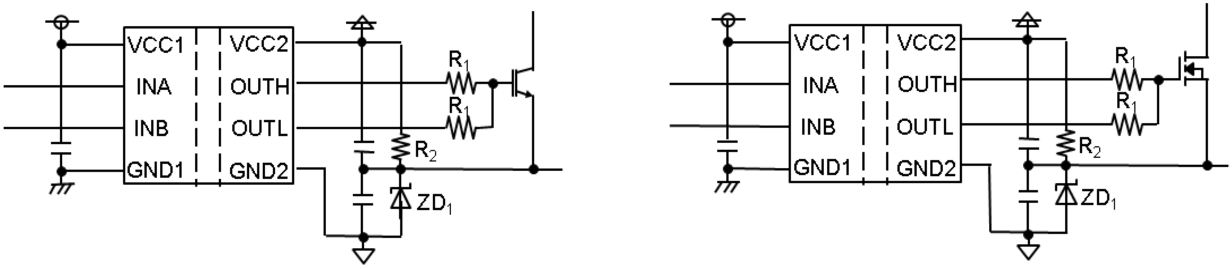

Figure 30. For Driving IGBT or MOSFET with Negative Power Supply

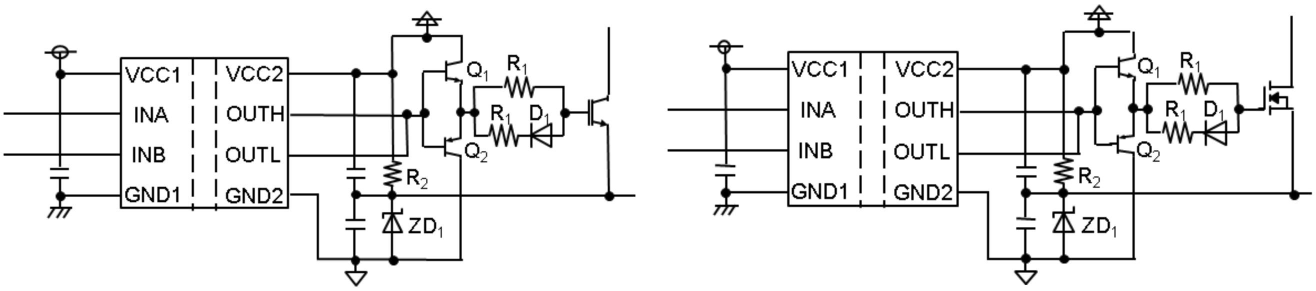

Figure 31. For Driving IGBT or MOSFET with Buffer Circuits & Negative Power Supply

Symbol	Manufacturer	Element	Recommended Components
R_1	ROHM	Resistor	LTR Series
R_2	ROHM	Resistor	LTR Series MCR Series
Q_1	ROHM	NPN Transistor	2SCR542PFRA
Q_2	ROHM	PNP Transistor	2SAR542PFRA
D_1	ROHM	Diode	RBR3MM30A RBR5LAM30A
ZD_1	ROHM	Zener Diode	YFZV Series

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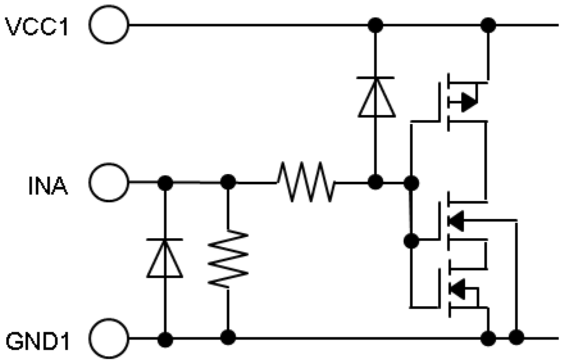
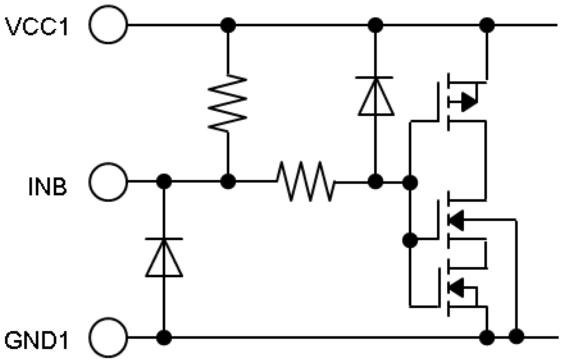
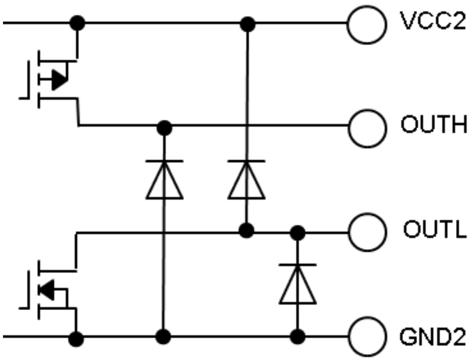
I/O Equivalence Circuits

<table>
<tr><th>Pin No</th><th>Name (Function)</th><th>I/O equivalence circuits</th></tr>
<tr><td>2</td><td>INA (Control input pin A)</td><td>
</td></tr>
<tr><td>3</td><td>INB (Control input pin B)</td><td>
</td></tr>
<tr><td>6</td><td>OUTH (Source side output pin)</td><td rowspan="2">
</td></tr>
<tr><td>7</td><td>OUTL (Sink side output pin)</td></tr>
</table>

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Regarding the Input Pin of the IC**
    This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

    When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
    When GND > Pin B, the P-N junction operates as a parasitic transistor.

    Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

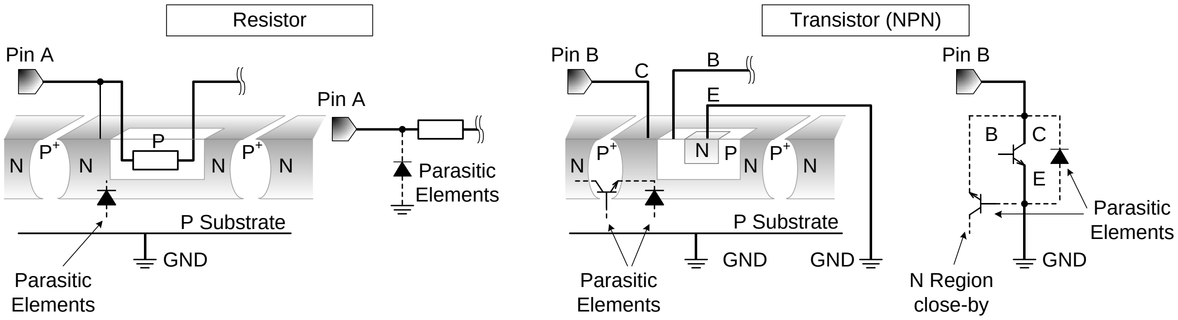
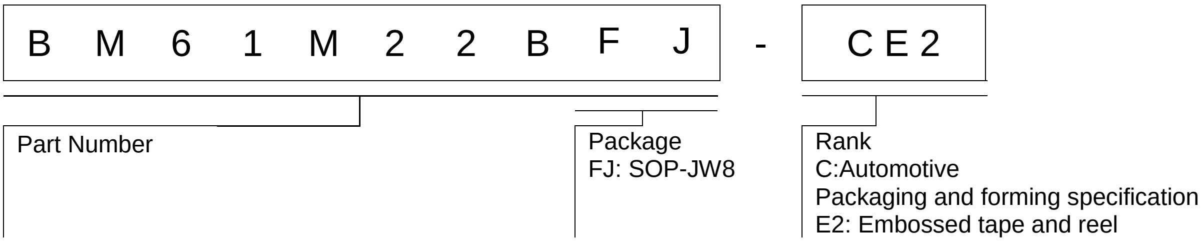


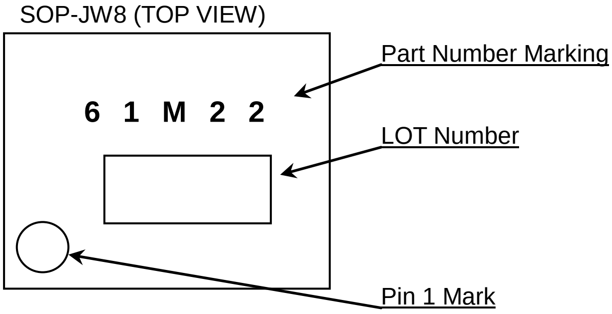
Figure 32. Example of IC Structure

11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

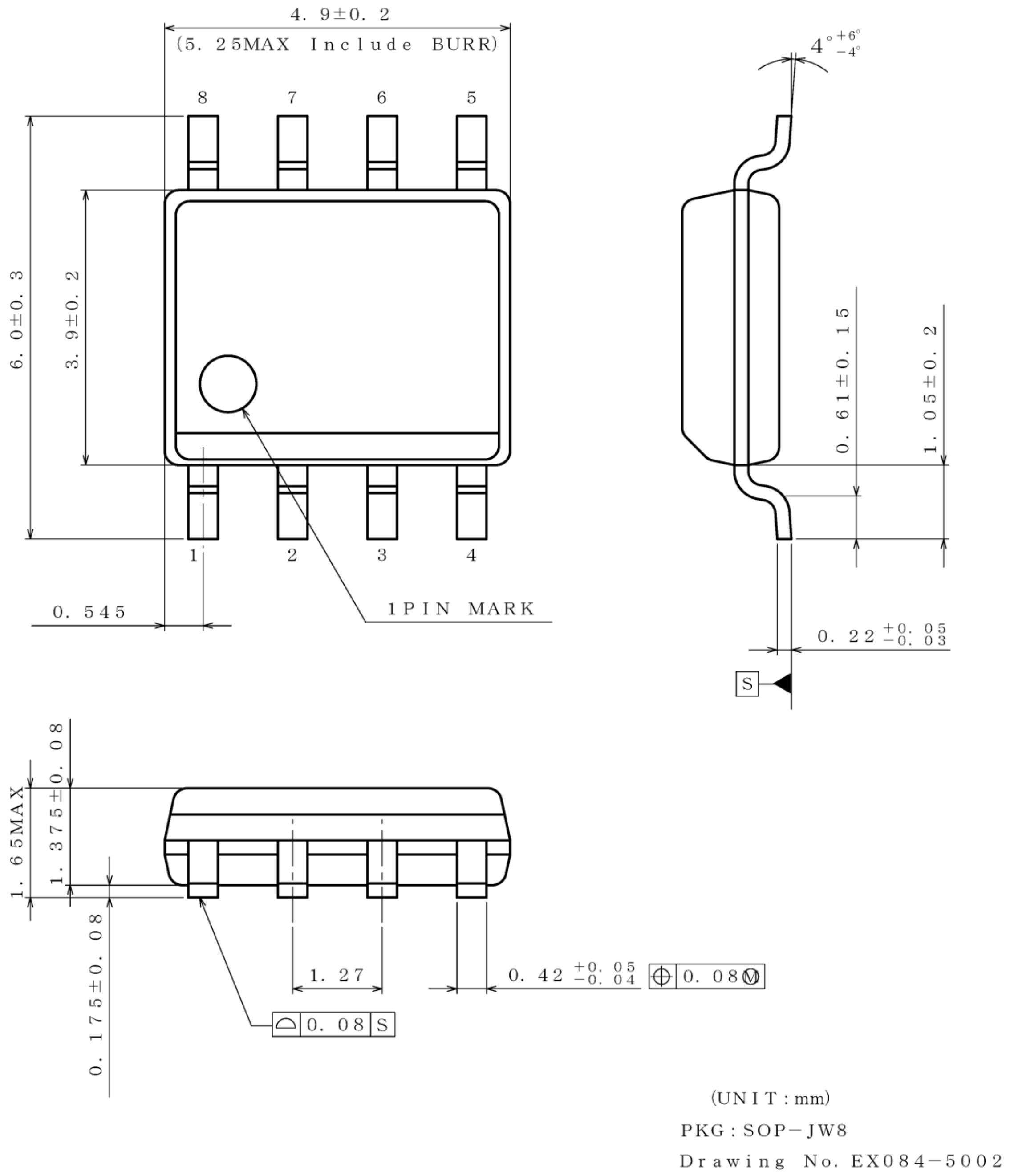


Marking Diagram



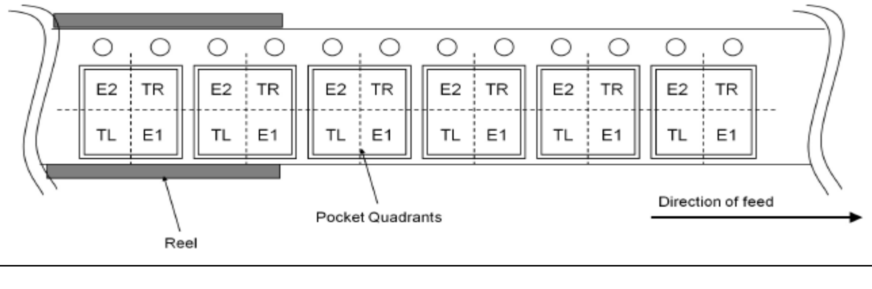
Physical Dimension and Packing Information

Package Name	SOP-JW8



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
24.Apr.2020	001	New Release

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Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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