bq77904、bq77905 3 节至 20 节超低功耗电压、电流、温度和断线可堆叠锂离子电池保护器

1 特性

- 正常模式：6µA（bq77904 和 bq77905）
- 整套电压、电流和温度保护
- 可将电池节数从 3 节扩展到 20 节或更多
- 电压保护（精度为 ±10mV）
  - 过压：3V 至 4.575V
  - 欠压：1.2V 至 3V
- 开路电池和断线检测 (OW)
- 电流保护
  - 过流放电 1：–10mV 至 –85mV
  - 过流放电 2：–20mV 至 +170mV
  - 放电短路：–40mV 至 +340mV
  - 在整个温度范围内，电压 ≤ 20mV 时的精度为 ±20%，电压 > 20mV 时的精度为 ±30%
- 温度保护
  - 过热充电：45°C 或 50°C
  - 过热放电：65°C 或 70°C
  - 欠温充电：-5°C 或 0°C
  - 欠温放电：-20°C 或 -10°C
- 其他 特性
  - 独立充电 (CHG) 和放电 (DSG) FET 驱动器
  - 每节电芯输入的绝对最大额定电压为 36V
  - 内置自检功能，具有高可靠性
- 关断模式：0.5µA（最大值）

2 应用范围

- 电动工具、园艺工具
- 启停电池组
- 铅酸 (PbA) 备用电池
- 轻型电动车辆
- 储能系统、不间断电源 (UPS)
- 10.8V 至 72V 电池组

3 说明

bq77904 和 bq77905 器件是低功耗的电池组保护器，它实现了一整套的电压、电流和温度保护，而无需微控制器 (MCU) 控制。该器件的可堆叠接口可进行简单扩展，以支持 3S 到 20S 或更多电池节数的 可从 3 节扩展至 20 节或更多。保护阈值和延迟均为出厂编程设定，有多种配置可供选用。为提升灵活性，还提供了单独的过热和欠温放电阈值（OTD 和 UTD）以及过热和欠温充电阈值（OTC 和 UTC）。

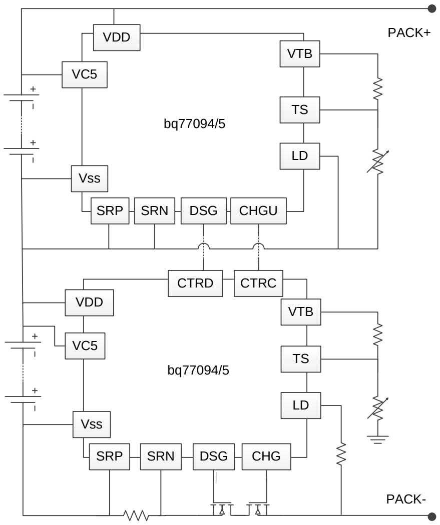
此器件可通过集成的独立 CHG 和 DSG 低侧 NMOS FET 驱动器实现电池组保护，这些驱动器可通过两个控制引脚禁用。这些控制引脚还能够以简单经济的方式为更多节串联电池（6 节以上）提供电池保护解决方案。为此，只需将上级器件的 CHG 和 DSG 输出级联到下级器件控制引脚。为减少组件数量，所有保护故障均使用内部延迟计时器。

器件信息[(1)]

器件编号	封装	封装尺寸（标称值）
bq77904	TSSOP (20)	6.50mm × 4.40mm
bq77905		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图



English Data Sheet: SLUSCM3

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision G (September 2017) to Revision H	Page
• 已更改 为了使表达更加简单明了，通篇更改了产品说明书中的一些措辞	1
• Added the bq7790518 device to the bq77905 *Device Comparison* table.	3

Changes from Revision F (May 2017) to Revision G	Page
• Added bq7790511 and bq7790512 to the *Device Comparison* table.	3

Changes from Revision E (March 2017) to Revision F	Page
• Changed the bq7790400 setting: OV delay from 1 s to 2 s. UV from 2800 mV to 2200 mV, UV delay from 1 s to 2 s, UV Hyst from 200 to 400 mV, UV load recovery from N to Y. OCD2 from 80 mV to 60 mV, OCD2 delay from 700 to 350 ms. SCD from 160 mV to 100 mV.	3
• Added bq7790508 and bq7790509 to the *Device Comparison* table.	3

Changes from Revision D (March 2017) to Revision E	Page
• Added bq7790505 to the *Device Comparison* table.	3
• Changed UTC(REC) at 5°C typ from 68.8 to 69.73 %VTB. Changed UTC(REC) at 10°C typ from 64.23 to 65.52 %VTB.	8

Changes from Revision C (February 2017) to Revision D	Page
• Changed VOTD, VOTD(REC), VOTC, VOTC(REC), VUTD, VUTD(REC), VUTC, VUTC(REC) MIN and MAX specification values.	7

Changes from Revision B (November 2016) to Revision C — Page

- Added values in the *Thermal Information* table to align with JEDEC standards. 7

Changes from Revision A (June 2016) to Revision B — Page

- 已更改 *特性中所列项目的顺序* 1
- Table 1 and Table 2, Changed OTC To: UTC in last column under Temperature. Changed bq7790400 and bq7790503 to Production Data. Updated the bq7790503 configuration 3
- Changed pin number from 16-pin to 20-pin 5
- Corrected max value on the UTD at –20°C spec 8
- 已更改 comparator flowcharts with new flowcharts 15
- Corrected CTRC and CTRD delay time entries 19

Changes from Original (June 2016) to Revision A — Page

- 将器件状态从“产品预览”更改成了“生产” 1

5 Device Comparison

DEVICE	NUMBER OF CELLS	PROTECTIONS	TYPICAL NORMAL MODE CURRENT (μA)	PACKAGE
bq77904	3, 4	OV, UV, OW, OTD, OTC, UTD, UTC, OCD1, OCD2, SCD, CTRC, CTRD	6	20-TSSOP
bq77905	3, 4, 5			

Unless otherwise specified, the devices in Table 1 and Table 2 come, by default, with the state comparator enabled with a 2-mV threshold. Filtered fault detection is used by default. Contact Texas Instruments for new configuration options or devices in preview.

Table 1. bq77904 Device Comparison

	OV			UV				OW	OCD1		OCD2		SCD	Current Fault Recovery		Temperature (°C)[1]			
Part Number	Threshold(mV)	Delay(s)	Hyst(mV)	Thresh (mV)	Delay(s)	Hyst(mV)	Load Removal Recovery(Y/N)	Current(nA)	Threshold (mV)	Delay (ms)	Threshold (mV)	Delay (ms)	Threshold (mV)	Delay (s)	Method	OTD	OTC	UTD	UTC
bq7790400	4225	2	100	2200	2	400	Y	0 (disable)	40	1420	60	350	100	0	Load Removal	70	50	–20	–5

(1) These thresholds are target based on temperature, but they are dependent on external components that could vary based on customer selection. The circuit is based on the 103AT NTC thermistor connected to TS and VSS, and a 10-kΩ resistor connected to VTB and TS. Actual thresholds must be determined in mV. Refers to the overtemperature and undertemperature mV threshold in the Electrical Characteristics table.

Table 2. bq77905 Device Comparison

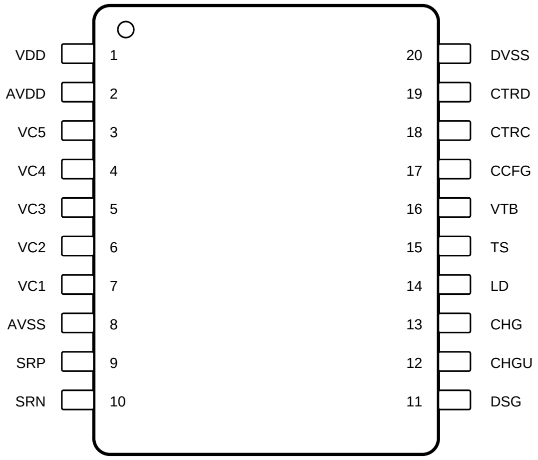
	OV			UV				OW	OCD1		OCD2		SCD	Current Fault Recovery		Temperature (°C)[1]			
Part Number	**Threshold(mV)**	**Delay(s)**	**Hyst(mV)**	**Thresh (mV)**	**Delay(s)**	**Hyst(mV)**	**Load Removal Recovery(Y/N)**	**Current(nA)**	**Threshold (mV)**	**Delay (ms)**	**Threshold (mV)**	**Delay (ms)**	**Threshold (mV)**	**Delay (s)**	**Method**	**OTD**	**OTC**	**UTD**	**UTC**
bq7790500	4200	0.5	100	2600	1	400	Y	100	30	1420	50	700	120	1	Load Removal + Delay	70	50	–20	0
bq7790502	4250	1	200	2700	1	200	Y	100	85	700	120	350	240	—	Load Removal	70	50	–20	–5
bq7790503	4200	1	100	2700	2	400	Y	100	80	1420	160	350	320	—	Load Removal	70	50	–20	–5
bq7790505	4250	1	200	2700	1	200	N	0	60	10	80	5	100	9	Load Removal + Delay	65	45	–20	0
bq7790508	3900	1	200	2000	1	400	Y	100	50	700	100	90	200	1	Load Removal + Delay	70	50	–20	–5
bq7790509	4250	1	100	2500	1	400	Y	100	50	700	100	90	200	1	Load Removal + Delay	70	50	–20	–5
bq7790511	4250	1	200	2700	1	200	Y	100	50	350	120	90	280	—	Load Removal	65	45	–20	0
bq7790512	4175	1	100	2800	1	400	Y	100	75	1420	150	350	300	1	Load Removal + Delay	65	45	–20	0
bq7790518[2]	4250	1	100	2750	1	200	Y	100	70	180	140	20	300	1	Load Removal	70	50	–20	0

(1) These thresholds are target based on temperature, but they are dependent on external components that could vary based on customer selection. Circuit is based on 103AT NTC thermistor connected to TS and VSS, and a 10-kΩ resistor connected to VTB and TS. Actual thresholds must be determined in mV. Refers to the overtemperature and undertemperature mV threshold in the Electrical Characteristics table.

(2) Contact TI for more information.

6 Pin Configuration and Functions

PW Package
20-Pin TSSOP
Top View



Not to scale

Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	**NO.**		
AVDD	2	O	Analog supply (only connect to a capacitor)
AVSS	8	P	Analog ground
CCFG	17	I	Cell in series-configuration input
CHG	13	O	CHG FET driver. Use on a single device or on the bottom device of a stack configuration.
CHGU	12	O	CHG FET signal.Use for the upper device of a stack configuration to feed the CHG signal to the CTRC pin of the lower device.
CTRC	18	I	CHG and DSG override inputs
CTRD	19	I	
DSG	11	O	DSG FET driver
DVSS	20	P	Digital ground
LD	14	I	PACK– load removal detection
SRN	10	I	Current sense input connecting to the PACK– side of sense resistor
SRP	9	I	Current sense input connecting to the battery side of sense resistor
TS	15	I	Thermistor measurement input. Connect a 10-kΩ resistor to AVSS pin if the function is not used.
VC1	7	I	Cell voltage sense inputs
VC2	6	I	
VC3	5	I	
VC4	4	I	
VC5	3	I	Cell voltage sense inputs (Pin 3 must be connected to Pin 4 on the bq77904 device.)
VDD	1	P	Supply voltage
VTB	16	O	Thermistor bias output

(1) I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). All values are referenced to VSS unless otherwise noted.(1)

			MIN	MAX	UNIT
V_I	Input voltage	VDD, VC5, VC4, VC3, VC2, VC1, CCFG, CTRD, CTRC	–0.3	36	V
		LD	–30	20	V
		SRN, SRP, TS, AVDD, CCFG	–0.3	3.6	V
V_O	Output voltage range	DSG, CHGU	–0.3	20	V
		CHG	–30	20	V
		VTB	–0.3	3.6	V
I_I	Input current	LD, CHG		500	µA
I_I	Input current	CHGU, DSG		1	mA
I_O	Output current	CHG		1	mA
I_O	Output current	CHGU, DSG		1	mA
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{BAT}	Supply voltage	VDD	3	25	V
V_I	Input voltage	VC5-VC4, VC4-VC3, VC3-VC2, VC2-VC1, VC1-VSS	0	5	V
		CTRD, CTRC	0	(VDD + 5)	
		CCFG	0	AVDD	
		SRN, SRP	–0.2	0.8	
		LD	0	16	
		TS	0	VTB	
V_O	Output voltage	CHG, CHGU, DSG	0	16	V
		VTB, AVDD	0	3	
T_A	Operating free-range temperature		–40	85	°C

7.4 Thermal Information

THERMAL METRIC[1]		bq77904 bq77905 PW (TSSOP) 20 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Typical values stated at T_A = 25ºC and VDD = 16 V (bq77904) or 20 V (bq77905). MIN and MAX values stated with T_A = –40ºC to +85ºC and VDD = 3 to 20 V (bq77904) or VDD = 3 to 25 V (bq77905) unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(POR)}$	POR threshold	VDD rising, 0 to 6 V			4	V
$V_{(SHUT)}$	Shutdown threshold	VDD falling, 6 to 0 V	2		3.25	V
$V_{(AVDD)}$	AVDD voltage	$C_{(VDD)}$ = 1 µF	2.1	2.5	3.25	V
SUPPLY AND LEAKAGE CURRENT						
I_{CC}	NORMAL mode current (bq77904/bq77905)	Cell1 through Cell5 = 4 V, VDD = 20 V (bq77905)		6	9	µA
$I_{(CFAULT)}$	Fault condition current	State comparator on		8	12	µA
I_{OFF}	SHUTDOWN mode current	VDD < V_{SHUT}			0.5	µA
$I_{LKG(OW\_DIS)}$	Input leakage current at VCx pins	All cell voltages = 4 V, Open-wire disable configuration	–100	0	100	nA
$I_{LKG(100nA)}$	Open-wire sink current at VCx pins	All cell voltages = 4 V, 100-nA configuration	30	110	175	nA
$I_{LKG(200nA)}$	Open-wire sink current at VCx pins	All cell voltages = 4 V, 200-nA configuration	95	210	315	nA
$I_{LKG(400nA)}$	Open-wire sink current at VCx pins	All cell voltages = 4 V, 400-nA configuration	220	425	640	nA
PROTECTION ACCURACIES						
V_{OV}	Overvoltage programmable threshold range		3000		4575	mV
V_{UV}	Undervoltage programmable threshold range		1200		3000	mV
$V_{(VA)}$	OV, UV, detection accuracy	T_A = 25ºC, OV detection accuracy	–10		10	mV
		T_A = 25ºC, UV detection accuracy	–18		18	mV
		T_A = 0 to 60ºC	–28		26	mV
		T_A = –40 to 85ºC	–40		40	mV
$V_{HYS(OV)}$	OV hysteresis programmable threshold range		0		400	mV
$V_{HYS(UV)}$	UV hysteresis programmable threshold range		200		800	mV
V_{OTD}	Overtemperature in discharge programmable threshold (ratio of V_{TB})	Threshold for 65°C[1]	19.71%	20.56%	21.86%	V
		Threshold for 70°C [1]	17.36%	18.22%	19.51%	VTB

(1) Based on a 10-KΩ pull-up and 103AT thermistor

Electrical Characteristics (continued)

Typical values stated at T_A = 25ºC and VDD = 16 V (bq77904) or 20 V (bq77905). MIN and MAX values stated with T_A = –40ºC to +85ºC and VDD = 3 to 20 V (bq77904) or VDD = 3 to 25 V (bq77905) unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OTD(REC)}$	Overtemperature in discharge recovery (ratio of V_{TB})	Recovery threshold at 55°C for when V_{OTD} is at 65°C(1)	25.24%	26.12%	27.44%	VTB
		Recovery threshold at 60°C for when V_{OTD} is at 70°C(1)	22.12%	23.2%	24.24%	VTB
V_{OTC}	Overtemperature in charge programmable threshold (ratio of V_{TB})	Threshold for 45°C(1)	32.14%	32.94%	34.54%	VTB
		Threshold for 50°C(1)	29.15%	29.38%	31.45%	VTB
$V_{OTC(REC)}$	Overtemperature in charge recovery (ratio of V_{TB})	Recovery threshold at 35°C when V_{OTD} is at 45°C(1)	38.63%	40.97%	40.99%	VTB
		Recovery threshold at 40°C when V_{OTD} is at 50°C(1)	36.18%	36.82%	38.47%	VTB
V_{UTD}	Undertemperature in discharge programmable threshold (ratio of V_{TB})	Threshold for –20°C(1)	86.41%	87.14%	89.72%	VTB
		Threshold for –10°C(1)	80.04%	80.94%	83.10%	VTB
$V_{UTD(REC)}$	Undertemperature in discharge recovery (ratio of V_{TB})	Recovery threshold at –10°C when V_{UTD} is at –20°C(1)	80.04%	80.94%	83.10%	VTB
		Recovery threshold at 0°C when V_{UTD} is at –10°C(1)	71.70%	73.18%	74.86%	VTB
V_{UTC}	Undertemperature in charge programmable threshold (ratio of V_{TB})	Threshold for –5°C(1)	75.06%	77.22%	78.32%	VTB
		Threshold for 0°C(1)	71.70%	73.18%	74.86%	VTB
$V_{UTC(REC)}$	Undertemperature in Charge Recovery (ratio of V_{TB})	Recovery threshold at 5°C when V_{UTC} is at –5°C(1)	68.80%	69.73%	71.71%	VTB
		Recovery threshold at 10°C when V_{UTC} is at 0°C(1)	64.67%	65.52%	67.46%	VTB
V_{OCD1}	Overcurrent discharge 1 programmable threshold range, (V_{SRP} – V_{SRN})		–85		–10	mV
V_{OCD2}	Overcurrent discharge 2 programmable threshold range, (V_{SRP} – V_{SRN})		–20		–170	mV
V_{SCD}	Short circuit discharge programmable threshold range, (V_{SRP} – V_{SRN})		–40		–340	mV
V_{CCAL}	OCD1 detection accuracy at lower thresholds	V_{OCD1} > –20 mV	–30%		30%	
V_{CCAH}	OCD1, OCD2, SCD detection accuracy	V_{OCD1} ≤ –20 mV; all OCD2 and SCD threshold ranges	–20%		20%	
V_{OW}	Open-wire fault voltage threshold at VCx per cell with respect to VC_{x-1}	Voltage falling on VCx, 3.6 V to 0 V	450	500	550	mV
$V_{OW(HYS)}$	Hysteresis for open wire fault	Voltage rising on VCx, 0 V to 3.6 V		100		mV
CHARGE AND DISCHARGE FET DRIVERS						
$V_{(FETON)}$	CHG/CHGU/DSG on	VDD ≥ 12 V, CL = 10 nF	11	12	14	V
		VDD < 12 V, CL = 10 nF	VDD – 1		VDD	V
$V_{(FETOFF)}$	CHG/CHGU/DSG off	No load when CHG/CHGU/DSG is off.			0.5	V
$R_{(CHGOFF)}$	CHG off resistance	CHG off for > t_{CHGPDN} and pin held at 2 V		0.5		kΩ
$R_{(DSGOFF)}$	CHGU/DSG off resistance	CHGU/DSG off and pin held at 2 V		10	16	Ω
$I_{CHG(CLAMP)}$	CHG clamp current	CHG off and pin held at 18 V			450	µA

Electrical Characteristics (continued)

Typical values stated at T_A = 25ºC and VDD = 16 V (bq77904) or 20 V (bq77905). MIN and MAX values stated with T_A = –40ºC to +85ºC and VDD = 3 to 20 V (bq77904) or VDD = 3 to 25 V (bq77905) unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CHG(CLAMP)}$	CHG clamp voltage	$I_{CHG(CLAMP)}$ = 300 µA	16	18	20.5	V
t_{CHGON}	CHG on rise time	CL = 10 nF, 10% to 90%		50	150	µs
t_{DSGON}	CHGU/DSG on rise time	CL = 10 nF, 10% to 90%		2	75	µs
t_{CHGOFF}	CHG off fall time	CL = 10 nF, 90% to 10%		15	30	µs
t_{DSGOFF}	CHGU/DSG off fall time	CL = 10 nF, 90% to 10%		5	15	µs
CTRC AND CTRD CONTROL						
V_{CTR1}	Enable FET driver (VSS)	With respect to VSS. Enabled < MAX			0.6	V
V_{CTR2}	Enable FET driver (Stacked)	Enabled > MIN	VDD + 2.2			V
$V_{CTR(DIS)}$	Disable FET driver	Disabled between MIN and MAX	2.04		VDD + 0.7	V
$V_{CTR(MAXV)}$	CTRC and CTRD clamp voltage	I_{CTR} = 600 nA	VDD + 2.8	VDD + 4	VDD + 5	V
t_{CTRDEG_ON}(2)	CTRC and CTRD deglitch for ON signal			7		ms
t_{CTRDEG_OFF}(2)	CTRC and CTRD deglitch for OFF signal			7		ms
CURRENT STATE COMPARATOR						
$V_{(STATE\_D1)}$	Discharge qualification threshold1	Measured at SRP-SRN	–3	–2	–1	mV
$V_{(STATE\_C1)}$	Charge qualification threshold1	Measured at SRP-SRN	1	2	3	mV
t_{STATE}(2)	State detection qualification time				1.2	ms
LOAD REMOVAL DETECTION						
$V_{LD(CLAMP)}$	LD clamp voltage	$I_{(LDCLAMP)}$ = 300 µA	16	18	20.5	V
$I_{LD(CLAMP)}$	LD clamp current	$V_{(LDCLAMP)}$ = 18 V			450	µA
V_{LDT}	LD threshold	Load removed < when V_{LDT}	1.25	1.3	1.35	V
$R_{LD(INT)}$	LD input resistance when enabled	Measured to VSS	160	250	375	kΩ
t_{LD_DEG}	LD detection deglitch		1	1.5	2.3	ms
CCFG PIN						
$V_{(CCFGL)}$	CCFG threshold low (ratio of V_{AVDD})	3-cell configuration			10%	V
$V_{(CCFGH)}$	CCFG threshold high (ratio of V_{AVDD})	4-cell configuration	65%		100%	V
$V_{(CCFGHZ)}$	CFG threshold high-Z (ratio of V_{AVDD})	5-cell configuration, CCFG floating, internally biased	25%	33%	45%	V
t_{CCFG_DEG}(2)	CCFG deglitch			6		ms
CUSTOMER TEST MODE (CTM)						
$V_{(CTM)}$	Customer test mode entry voltage at VDD	VDD > VC5 + $V_{(CTM)}$, T_A = 25°C	8.5		10	V
t_{CTM_ENTRY}(3)	Delay time to enter and exit Customer Test Mode	VDD > VC5 + $V_{(CTM)}$, T_A = 25°C	50			ms
t_{CTM_DELAY}(3)	Delay time of faults while in Customer Test Mode	T_A = 25°C			200	ms
$t_{CTM\_OC\_REC}$(3)	Fault recovery time of OCD1, OCD2, and SCD faults while in Customer Test Mode	1 s and 8 s options, T_A = 25°C			100	ms

(2) Not production tested parameters. Specified by design
(3) The device is in a no fault state prior to entering Customer Test Mode.

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
PROTECTION DELAYS[1]						
t_{OVn_DELAY}	Overvoltage detection delay time	0.5-s delay option	0.4	0.5	0.8	s
		1-s delay option	0.8	1	1.4	
		2-s delay option	1.8	2	2.7	
		4.5-s delay option	4	4.5	5.2	
t_{UVn_DELAY}	Undervoltage detection delay time	1-s delay option	0.8	1	1.5	s
		2-s delay option	1.8	2	2.7	
		4.5-s delay option	4	4.5	5.5	
		9-s delay option	8	9	10.2	
t_{OWn_DELAY}	Open-wire detection delay time		3.6	4.5	5.3	s
t_{OTC_DELAY}	Overtemperature charge detection delay time		3.6	4.5	5.3	s
t_{UTC_DELAY}	Undertemperature charge detection delay time		3.6	4.5	5.3	s
t_{OTD_DELAY}	Overtemperature discharge detection delay time		3.6	4.5	5.3	s
t_{UTD_DELAY}	Undertemperature discharge detection delay time		3.6	4.5	5.3	s
t_{OCD1_DELAY}	Overcurrent 1 detection delay time	10-ms delay option	8	10	15	ms
		20-ms delay option	17	20	26	
		45-ms delay option	36	45	52	
		90-ms delay option	78	90	105	
		180-ms delay option	155	180	205	
		350-ms delay option	320	350	405	
		700-ms delay option	640	700	825	
		1420-ms delay option	1290	1420	1620	
t_{OCD2_DELAY}	Overcurrent 2 detection delay time	5-ms delay option	4	5	8	ms
		10-ms delay option	8	10	15	
		20-ms delay option	17	20	26	
		45-ms delay option	36	45	52	
		90-ms delay option	78	90	105	
		180-ms delay option	155	180	205	
		350-ms delay option	320	350	405	
		700-ms delay option	640	700	825	
t_{SCD_RELAY}	Short-circuit detection delay time	360-µs delay option	220	400	610	µs
t_{CD_REC}	Overcurrent 1, Overcurrent 2, and Short-circuit recovery delay time	1-s option	0.8	1	1.4	s
		9-s option	8	9	10.2	

(1) Not production tested parameters. Specified by design

7.7 Typical Characteristics

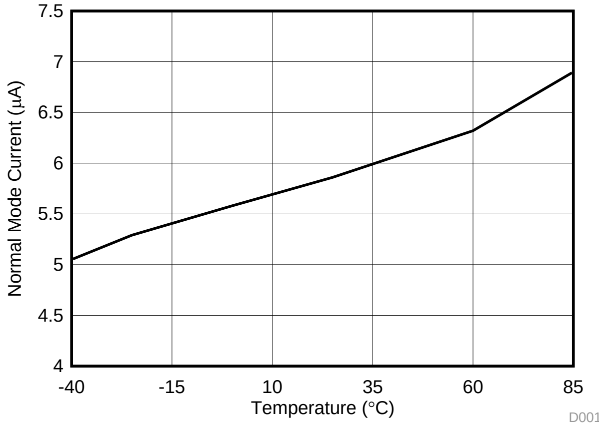


图 1. NORMAL Mode Current

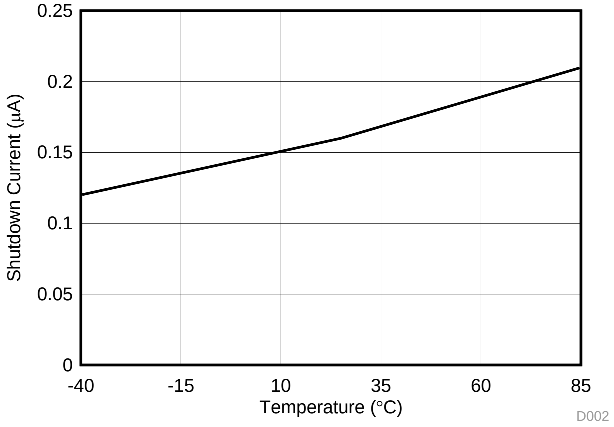


图 2. Shutdown Current

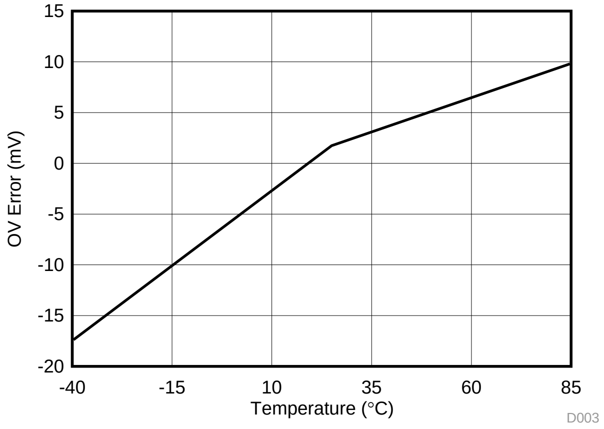


图 3. OV Error at 4.25-V Threshold

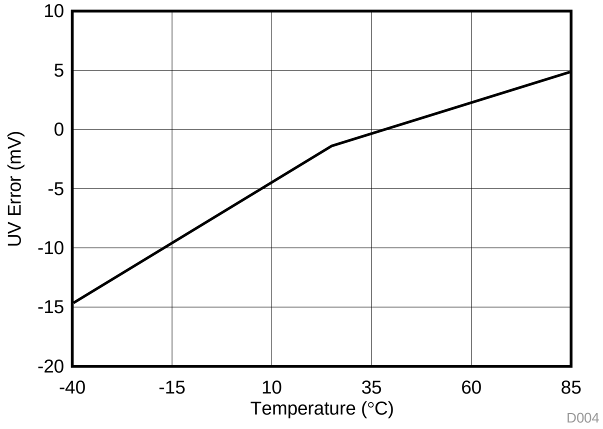


图 4. UV Error at 2.8-V Threshold

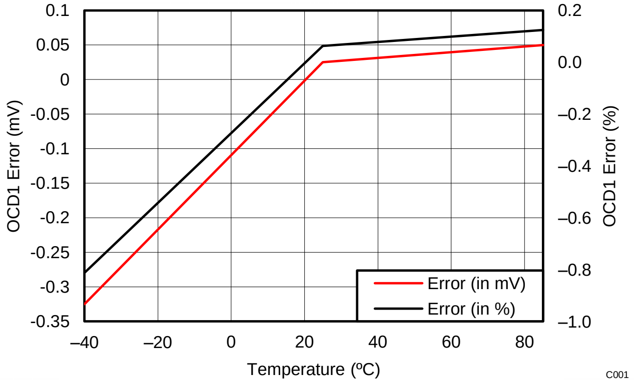


图 5. OCD1 Error at 40-mV Threshold

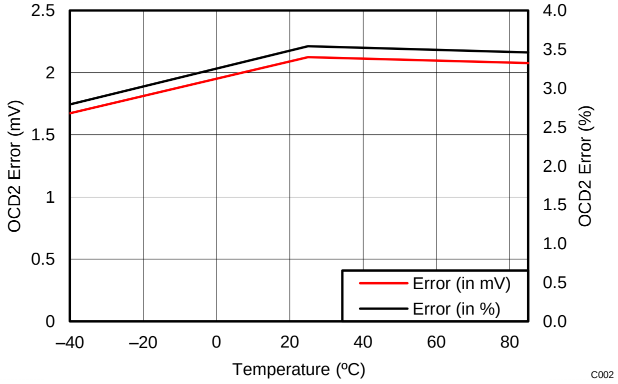


图 6. OCD2 Error at 60-mV Threshold

Typical Characteristics (接下页)

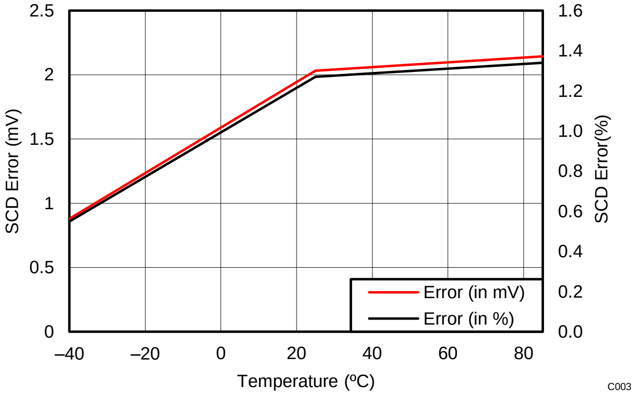


图 7. SCD Error at 160-mV Threshold

8 Detailed Description

8.1 Overview

The bq77904 and bq77905 families are full-feature stackable primary protectors for Li-ion/Li-Polymer batteries. The devices implement a suite of protections, including:

- Cell voltage: overvoltage, undervoltage
- Current: Overcurrent discharge 1 and 2, short circuit discharge
- Temperature: overtemperature and undertemperature in charge and discharge
- PCB: cell open-wire connection
- FET body diode protection

Protection thresholds and delays are factory-programmed and available in a variety of configurations.

The bq77904 supports 3-series-to–4-series cell configuration and bq77905 supports 3-series-to–5-series cell configuration. Up to four devices can be stacked to support ≥6-series cell configurations, providing protections up to 20-series cell configurations.

The device has built-in CHG and DSG drivers for low-side N-channel FET protection, which automatically open up the CHG and/or DSG FETs after protection delay time when a fault is detected. A set of CHG/DSG overrides is provided to allow disabling of CHG and/or DSG driver externally. Although the host system can use this function to disable the FETs' control, the main use of these pins is to channel down the FET control signal from the upper device to the lower device in a cascading configuration in ≥6-series battery packs.

8.1.1 Device Functionality Summary

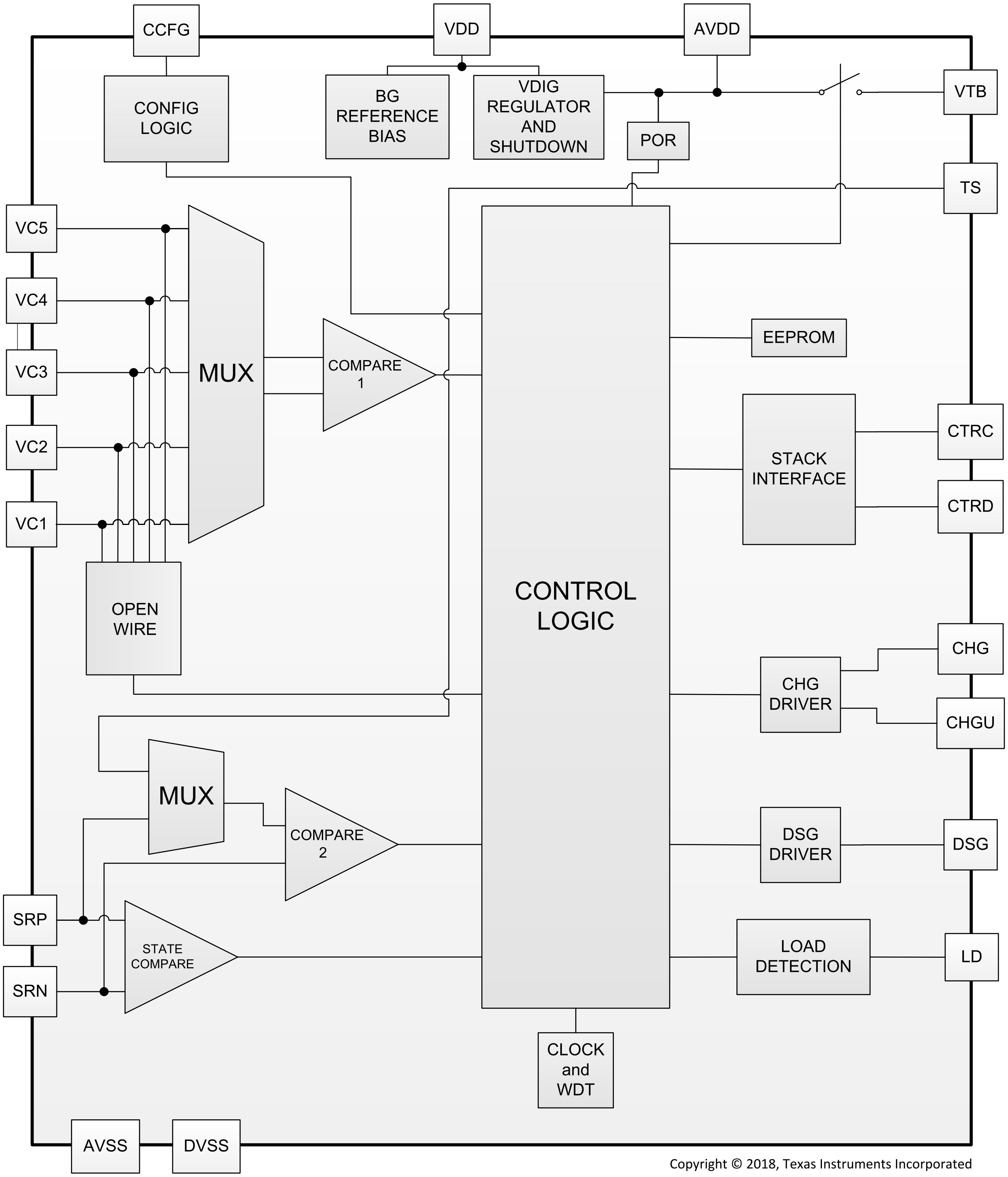
In this and subsequent sections, a number of abbreviations are used to identify specific fault conditions. The fault descriptor abbreviations and their meanings are defined in 表 3.

表 3. Device Functionality Summary

FAULT DESCRIPTOR		FAULT DETECTION THRESHOLD and DELAY OPTIONS		FAULT RECOVERY METHOD and SETTING OPTIONS	
OV	Overvoltage	3 V to 4.575 V (25-mV step)	0.5, 1, 2, 4.5 s	Hysteresis	0, 100, 200, 400 mV
UV	Undervoltage	1.2 V to 3 V (100-mV step for < 2.5 V, 50-mV step for ≥ 2.5 V)	1, 2, 4.5, 9 s	Hysteresis OR Hysteresis + Load Removal	200, 400 mV
OW	Open wire (cell to pcb disconnection)	0 (disabled), 100, 200, or 400 nA	4.5 s	Restore bad VCx to pcb connection	VCx > V_{OW}
OTD(1)	Overtemperature during discharge	65°C or 70°C	4.5 s	Hysteresis	10°C
OTC(1)	Overtemperature during charge	45°C or 50°C	4.5 s	Hysteresis	10°C
UTD(1)	Undertemperature during discharge	–20°C or –10°C	4.5 s	Hysteresis	10°C
UTC (1)	Undertemperature during charge	–5°C or 0°C	4.5s	Hysteresis	10°C
OCD1	Overcurrent1 during discharge	10 mV to 85 mV (5-mV step)	10, 20, 45, 90, 180, 350, 700, 1420 ms	Delay OR Delay + Load Removal OR Load Removal	1 s or 9 s
OCD2	Overcurrent1 during discharge	20 mV to 170 mV (10-mV step)	5, 10, 20, 45, 90, 180, 350, 700 ms		
SCD	Short circuit discharge	40 mV to 340 mV (20-mV step)	360 µs		
CTRC	CHG signal override control	Disable via external control or via CHGU signal from the upper device in the stack configuration.	t_{CTRDEG_ON}	Enable via external control or via CHGU signal from the upper device in the stack configuration.	t_{CTRDEG_OFF}
CTRD	DSG signal override control	Disable via external control or via DSG signal from the upper device in the stack configuration.	t_{CTRDEG_ON}	Enable via external control or via DSG signal from the upper device in the stack configuration.	t_{CTRDEG_OFF}

(1) These thresholds are target based on temperature, but they are dependent on external components that could vary based on customer selection. The circuit is based on a 103AT NTC thermistor connected to TS and VSS, and a 10-kΩ resistor connected to VTB and TS. Actual thresholds must be determined in mV. Refers to the overtemperature and undertemperature mV threshold in the Electrical Characteristics table.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Protection Summary

The bq77904 and bq77905 have two comparators. Both are time multiplexed to detect all protection fault conditions. Each of the comparators runs on a time-multiplexed schedule and cycles through the assigned protection-fault checks. Comparator 1 checks for OV, UV, and OW protection faults. Comparator 2 checks for OCD1, OCD2, SCD, OTC, OTD, UTC, and UTD protection faults. For OV, UV, and OW protection faults, every cell is checked individually in round-robin fashion, starting with cell 1 and ending with the highest-selected cell. The number of the highest cell is configured using the CCFG pin.

Devices can be ordered with various timing and hysteresis settings. See the *Device Comparison* section for a summary of options available per device type.

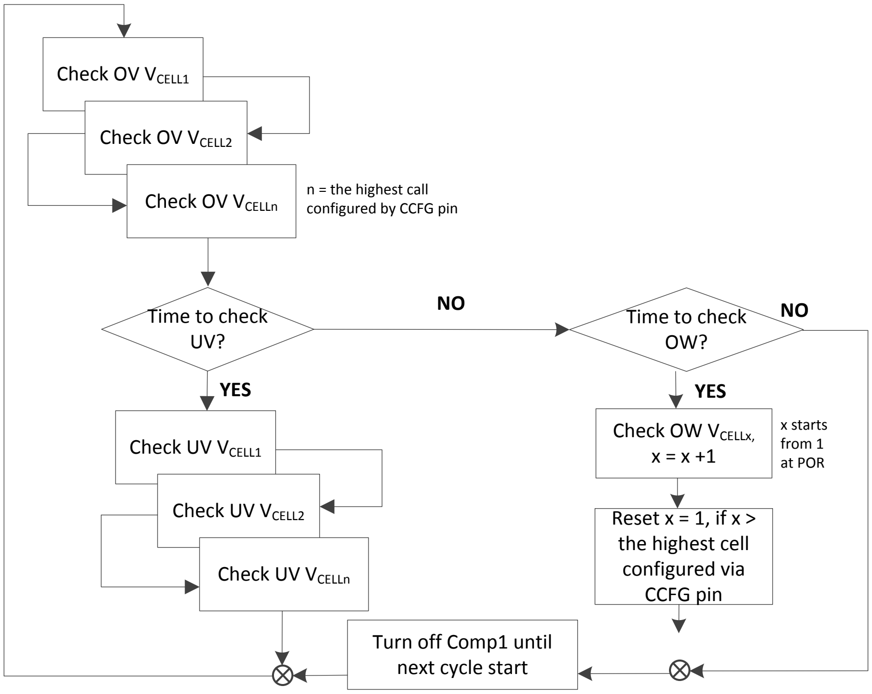


图 8. Comparator 1 Flowchart

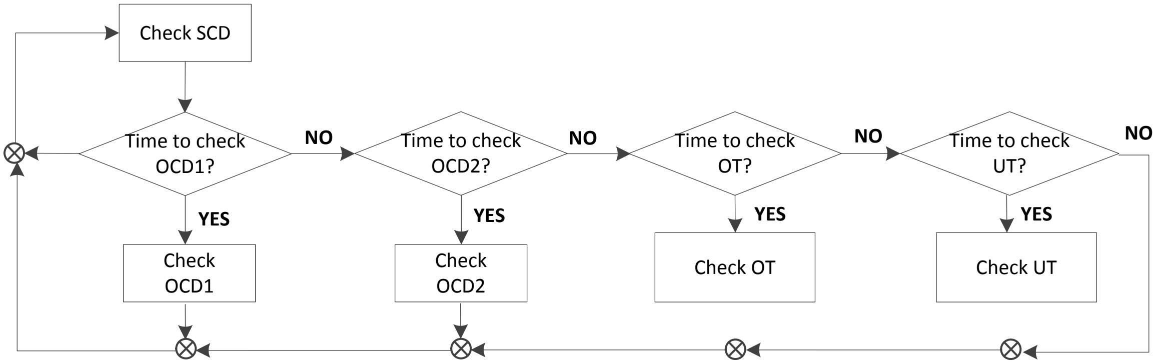


图 9. Comparator 2 Flowchart

Feature Description (接下页)

8.3.2 Fault Operation

8.3.2.1 Operation in OV

An OV fault detection is when at least one of the cell voltages is measured above the OV threshold, V_{OV}. The CHG pin is turned off if the fault condition lasts for a duration of OV Delay, t_{OVn_DELAY}. The OV fault recovers when the voltage of the cell in fault is below the (OV threshold – OV hysteresis, V_{HYS_OV}) for a time of OV Delay.

The bq77904 and bq77905 assume OV fault after device reset.

8.3.2.2 Operation in UV

An UV fault detection is when at least one of the cell voltages is measured below the UV threshold, V_{UV}. The DSG is turned off if the fault condition lasts for a duration of UV Delay, t_{UVn_DELAY}. The UV fault recovers when:

- The cell voltage in fault is above the (UV threshold + UV hysteresis, V_{HYS_UV}) for a time of UV Delay only OR
- The cell voltage in fault is above the (UV threshold + UV hysteresis) for a time of UV Delay AND load removal is detected.

If load removal is enabled as part of the UV recovery requirement, the CHG FET R_{GS} value should change to around 3 MΩ. Refer to the *Using Load Detect for UV Fault Recovery* section of this document for more detail. This requirement applies to load removal enabled for UV recovery only. Therefore, if load removal is selected for current fault recovery, but not for the UV recovery, a lower CHG FET R_{GS} value (typical of 1MΩ) can be used to reduce the CHG FET turn off time.

To minimize supply current, the device disables all overcurrent detection blocks any time the DSG FET is turned off (due to a fault or CTRD being driven to the DISABLED state). Upon recovery from a fault or when CTRD is no longer externally driven, all overcurrent detection blocks reactivate before the DSG FET turns back on.

8.3.2.3 Operation in OW

An OW fault detection is when at least one of the cell voltages is measured below the OW threshold, V_{OW}. Both CHG and DSG are turned off if the fault condition lasts for a duration of OW Delay, t_{OWn_DELAY}. The OW fault recovers when the cell voltage in fault is above the OW threshold + OW hysteresis, V_{OW_HYS} for a time of OW Delay.

The t_{OWn_DELAY} time starts when voltage at a given cell is detected below the V_{OW} threshold and is not from the time that the actual event of open wire occurs. During an open-wire event, it is common that the device detects an undervoltage and/or overvoltage fault before detecting an open-wire fault. This may happen due to the differences in fault thresholds, fault delays, and the VCx pin filter capacitor values. To ensure both CHG and DSG return to normal operation mode, the OW, OV, and UV faults recovery conditions must be met.

8.3.2.4 Operation in OCD1

An OCD1 fault is when the discharge load is high enough that the voltage across the R_{SNS} resistor, (V_{SRP}-V_{SRN}), is measured below the OCD1 voltage threshold, V_{OCD1}. Both CHG and DSG are turned off if the fault condition lasts for a duration of OCD1 Delay, t_{OCD1_DELAY}.

The OCD1 fault recovers when:

- Load removal is detected only, $V_{LD} < V_{LDT}$ OR
- Overcurrent Recovery Timer, t_{CD_REC}, expiration only OR
- Overcurrent Recovery Timer expiration and load removal are detected.

8.3.2.5 Operation in OCD2

An OCD2 fault is when the discharge load is high enough that the voltage across the R_{SNS} resistor, (V_{SRP}-V_{SRN}), is measured below the OCD2 voltage threshold, V_{OCD2}. Both CHG and DSG are turned off if the fault condition lasts for a duration of OCD2 Delay, t_{OCD2_DELAY}.

The OCD2 fault recovers when:

- Load removal detected only, $V_{LD} < V_{LDT}$ OR
- Overcurrent Recovery Timer, t_{CD_REC}, expiration only OR

Feature Description (接下页)

- Overcurrent Recovery Timer expiration and load removal are detected.

8.3.2.6 Operation in SCD

An SCD fault is when the discharge load is high enough that the voltage across the R_{SNS} resistor, (V_{SRP}-V_{SRN}), is measured below the SCD voltage threshold, V_{SCD}. Both CHG and DSG are turned off if the fault condition lasts for a duration of SCD Delay, t_{SCD_DELAY}.

The SCD fault recovers when:

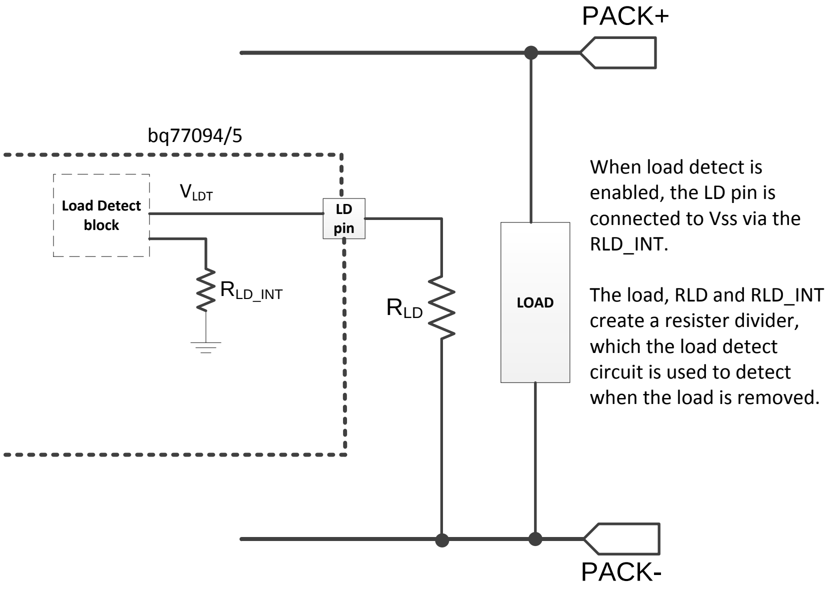
- Load removal detected only, $V_{LD} < V_{LDT}$ OR
- Overcurrent Recovery Timer, t_{CD_REC}, expiration only OR
- Overcurrent Recovery Timer expiration and load removal are detected.

8.3.2.7 Overcurrent Recovery Timer

The timer expiration method activates an internal recovery timer as soon as the initial fault condition exceeds the OCD1/OCD2/SCD time. When the recovery timer reaches its limit, both CHG and DSG drivers are turned back on. If the combination option of timer expiration AND load removal is used, then the load removal condition is only evaluated upon expiration of the recovery timer, which can have an expiration period of t_{CD_REC}.

8.3.2.8 Load Removal Detection

The load removal detection feature is implemented with the LD pin (see 表 4). When no undervoltage fault and current fault conditions are present, the LD pin is held in an open-drain state. Once any UV, OCD1, OCD2, or SCD fault occurs and load removal is selected as part of the recovery conditions, a high impedance pull-down path to VSS is enabled on the LD pin. With an external load still present, the LD pin will be externally pulled high: It is internally clamped to $V_{LDCLAMP}$ and should also be resistor-limited through R_{LD} externally to avoid conducting excessive current. If the LD pin exceeds V_{LDT}, this is interpreted as a *load present condition*. When the load is eventually removed, the internal high-impedance path to VSS should be sufficient to pull the LD pin below V_{LDT} for t_{LD_DEG}. This is interpreted as a *load removed condition* and is one of the recovery mechanisms selectable for undervoltage and overcurrent faults.



When load detect is enabled, the LD pin is connected to Vss via the RLD_INT.

The load, RLD and RLD_INT create a resister divider, which the load detect circuit is used to detect when the load is removed.

图 10. Load Detection Circuit for Current Faults Recovery

表 4. Load State

LD PIN	LOAD STATE
≥ V_{LDT}	Load present
< V_{LOT} for t_{LD_DEG}	Load removed

8.3.2.9 Load Removal Detection in UV

During a UV fault, only the DSG FET driver is turned off while the CHG FET driver remains on. When load removal is selected as part of the UV recovery condition, the active CHG FET driver would alter the resistor divider ratio of the load detection circuit. To ensure the load status can still be detected properly, it is required to increase the CHG FET external R_{GS} value to about 3 MΩ. Refer to the *Using Load Detect for UV Fault Recovery* section for more detail. Note that if load removal is only selected for the current fault recovery (and is not used for UV recovery), it is not required to use a larger CHG FET R_{GS} value.

8.3.2.10 Operation in OTC

An OTC Fault occurs when the temperature increases such that the voltage across an NTC thermistor goes below the OTC voltage threshold, V_{OTC}. CHG is turned off if the fault condition lasts for an OTC delay time, t_{OTC_DELAY}. The state comparator is turned on when CHG is turned off. If a discharge current is detected, the device immediately switches the CHG back on. The response time of the state comparator is typically in 700 µs and should not pose any disturbance in the discharge event. The OTC fault recovers when the voltage across thermistor gets above OTC recovery threshold, V_{OTC_REC}, for OTC delay time.

8.3.2.11 Operation in OTD

An OTD fault is when the temperature increases such that the voltage across an NTC thermistor goes below the OTD voltage threshold, V_{OTD}. Both CHG and DSG are turned off if the fault condition lasts for an OTD delay time, t_{OTD_DELAY}. The OTD fault recovers when the voltage across thermistor gets above OTD recovery threshold, V_{OTD_REC}, a time of an OTD delay.

8.3.2.12 Operation in UTC

A UTC fault occurs when the temperature decreases such that the voltage across an NTC thermistor gets above the UTC voltage threshold, V_{UTC}. CHG is turned off if the fault condition lasts for a time of a UTC delay, t_{UTC_DELAY}. The state comparator is turned on when CHG is turned off. If a discharge current is detected, the device will immediately switch CHG back on. The response time of the state comparator is typically in 700 µs and should not pose any disturbance in the discharge event. The UTC fault recovers when the voltage across thermistor gets below UTC recovery threshold, V_{UTC_REC}, a time of a UTC delay.

8.3.2.13 Operation in UTD

A UTD fault occurs when the temperature decreases such that the voltage across an NTC thermistor goes above the UTD voltage threshold, V_{UTD}. Both CHG and DSG are turned off if the fault condition lasts for a UTD delay time. The UTD fault recovers when the voltage across the thermistor gets below the UTD recovery threshold, V_{UTD_REC}, a time of the UTD delay.

8.3.3 Protection Response and Recovery Summary

表 5 summarizes how each fault condition affects the state of the DSG and CHG output signals, as well as the recovery conditions required to resume charging and/or discharging. As a rule, the CHG and DSG output drivers are enabled only when no respective fault conditions are present. When multiple simultaneous faults (such as an OV and OTD) are present, all faults must be cleared before the FET can resume operation.

表 5. Fault Condition, State, and Recovery Methods

FAULT	FAULT TRIGGER CONDITION	CHG	DSG	RECOVERY METHOD	TRIGGER DELAY	RECOVERY DELAY
CTRC disabled	CTRC disabled for deglitch delay time	OFF	—	CTRC must be enabled for deglitch delay time	t_{CTRDEG_ON}	t_{CTRDEG_OFF}
CTRD disabled	CTRD disabled for deglitch delay time	—	OFF	CTRD must be enabled for deglitch delay time		
OV	V(Cell) rises above V_{OV} for delay time	OFF	—	V(Cell) drops below $V_{OV} – V_{HYS\_OV}$ for delay	t_{OVn_DELAY}	
UV	V(Cell) drops below V_{UV} for delay time	—	OFF	V(Cell) rises above $V_{UV} + V_{HYS\_UV}$ for delay	t_{UVn_DELAY}	
OW	$VC_X – VC_{X–1} < V_{OW}$ for delay time	OFF	OFF	Bad VC_X recovers such that $VC_X – VC_{X–1} > V_{OW} + V_{OW\_HYS}$ for delay	t_{OWn_DELAY}	
OCD1, OCD2, SCD	(VSRP - VSRN) < VOCD1, VOCD2, or VSCD for delay time	OFF	OFF	Recovery delay expires OR LD detects < V_{LDT} OR Recovery delay expires + LD detects < V_{LDT}	t_{OCD1_DELAY}, t_{OCD2_DELAY}, t_{SCD_DELAY},	t_{CD_REC}
OTC(1)	Temperature rises above T_{OTC} for delay time	OFF	—	Temp drops below $T_{OTC} – T_{OTC\_REC}$ for delay	t_{OTC_DELAY}	
OTD(1)	Temperature rises above T_{OTD} for delay time	OFF	OFF	Temp drops below $T_{OTD} – T_{OTD\_REC}$ for delay	t_{OTD_DELAY}	
UTC(1)	Temperature drops below T_{UTC} for delay time	OFF	—	Temperature rises above $T_{UTC} + T_{UTC\_REC}$ for delay	t_{UTC_DELAY}	
UTD(1)	Temp drops below T_{UTD} for delay time	OFF	OFF	Temp rises above $T_{UTD} + T_{UTD\_REC}$ for delay	t_{UTD_DELAY}	

(1) T_{UTC}, T_{UTD}, T_{UTC_REC}, and T_{UTD_REC} correspond to the temperature produced by V_{UTC}, V_{UTD}, V_{UTC_REC}, and V_{UTD_REC} of the selected thermistor resistance.

For bq77904 and bq77905 devices to prevent CHG FET damage, there are times when the CHG FET may be enabled even though an OV, UTC, OTC, or CTRC low event has occurred. See the *State Comparator* section for details.

8.3.4 Configuration CRC Check and Comparator Built-In-Self-Test

To improve reliability, the device has built in CRC check for all the factory-programmable configurations, such as the thresholds and delay time setting. When the device is set up in the factory, a corresponding CRC value is also programmed to the memory. During normal operation, the device compares the configuration setting against the programmed CRC periodically. A CRC error will reset the digital circuitry and increment the CRC fault counter. The digital reset forces the device to reload the configuration as an attempt to correct the configurations. A correct CRC check reduces the CRC fault counter. Three CRC faults counts will turn off both the CHG and DSG drivers. If FETs are opened due to a CRC error, only a POR can recover the FET state and reset the CRC fault.

In addition to the CRC check, the device also has built-in-self-test (BIST) on the comparators. The BIST runs in a scheduler, and each comparator is checked for a period of time. If a fault is detected for the entire check period, the particular comparator is considered at fault, and both the CHG and DSG FETs is turned off. The BIST continues to run by the scheduler even if a BIST fault is detected. If the next BIST result is good, the FET driver resumes normal operation.

The CRC check and BIST check do not affect the normal operation of the device. However, there is not a specific indication when a CRC or BIST error is detected besides turning off the CHG and DSG drivers. If there is no voltage, current, or temperature fault condition present, but CHG and DSG drivers remain off, it is possible that either a CRC or BIST error is detected. Users can power-on reset (POR) the device.

8.3.5 Fault Detection Method

8.3.5.1 Filtered Fault Detection

The device detects a fault once the applicable fault is triggered after accumulating sufficient trigger sample counts. The filtering scheme is based on a simple add/subtract. Starting with the triggered sample count cleared, the counts go up for a sample that is taken across the tested condition (for example, above the fault threshold when looking for a fault) and the counts go down for a sample that is taken before the tested condition (that is, below the fault threshold). 图 11 shows an example of a signal that triggers a fault when accumulating five counts above the fault threshold. Once a fault has been triggered, the triggered sample counts reset, and counts are incremented for every sample that is found to be below the recovery threshold.

注

With a filtered detection, when the input signal falls below the fault threshold, the sample count does not reset, but only counts down as shown in 图 11. Therefore, it is normal to observe a longer delay time if a signal is right at the detection threshold. The noise can push the delay count to be counting up and down, resulting a longer time for the delay counter to reach its final accumulated trigger target.

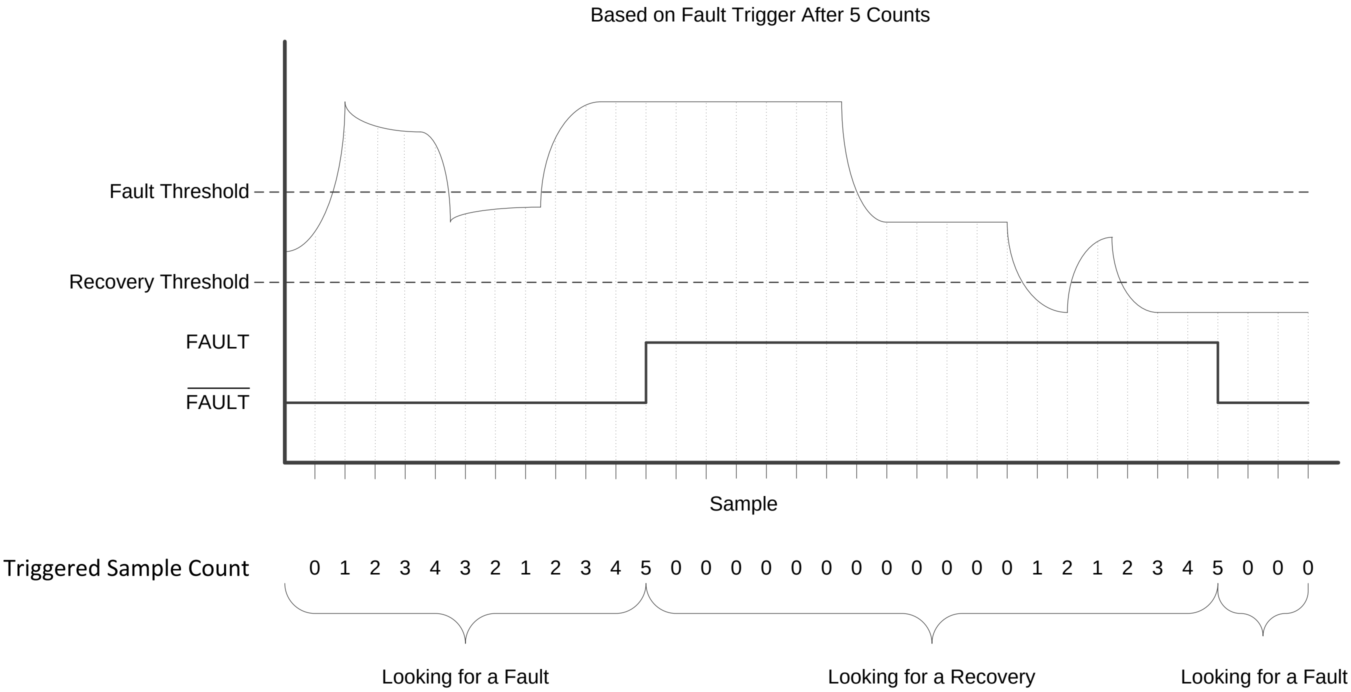


图 11. Fault Trigger Filtering

8.3.6 State Comparator

A small, low-offset analog state comparator monitors the sense-resistor voltage (SRP-SRN) to determine when the pack is in a DISCHARGE state less than a minimum threshold, V_{STATE_D} or a CHARGE state greater than a maximum threshold, V_{STATE_C}. The state comparator is used to turn the CHG FET on to prevent damage or overheating during discharge in fault states that call for having only the CHG FET off, and vice versa for the DSG FET during charging in fault states that call for having only the DSG FET off.

表 6 summarizes when the state comparator is operational. The state comparator is only on during faults detected that call for only one FET driver to be turned off.

表 6. State Comparator Operation Summary

STATE COMP	CHG	DSG	MODE
OFF	ON	ON	Normal

表 6. State Comparator Operation Summary (接下页)

STATE COMP	CHG	DSG	MODE
V_{STATE_C} Detection	ON	OFF	UV, CTRD
V_{STATE_D} Detection	OFF	ON	OV, UTC, OTC, CTRC
OFF	OFF	OFF	OCD1, OCD2, SCD, UTD, OTD, OW

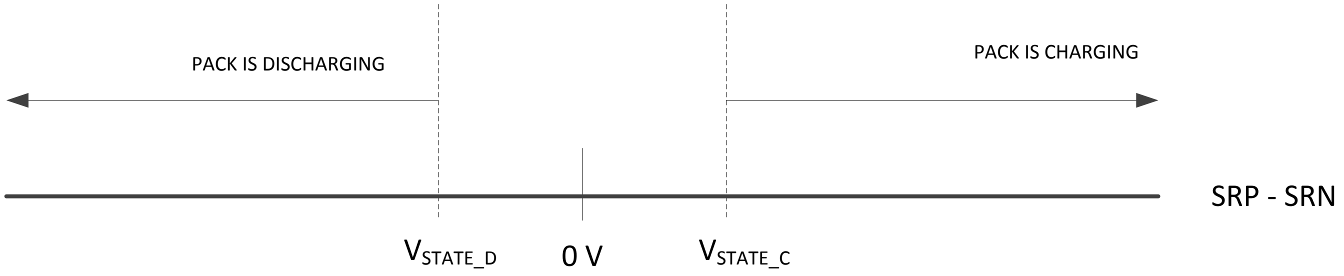


图 12. State Comparator Thresholds

8.3.7 DSG FET Driver Operation

The DSG pin is driven high only when no related faults (UV, OW, OTD, UTD, OCD1, OCD2, SCD, and CTRD are disabled) are present. It is a fast switching driver with a target on resistance of about 15–20 Ω and an off resistance of R_{DSGOFF}. It is designed to allow users to select the optimized R_{GS} value to archive the desirable FET rise and fall time per the application requirement and the choice of FET characteristics. When the DSG FET is turned off, the DSG pin drives low and all overcurrent protections (OCD1, OCD2, SCD) are disabled to better conserve power. These resume operation when the DSF FET is turned on. The device provides FET body diode protection through the state comparator if one FET driver is on and the other FET driver is off.

The DSG driver may be turned on to prevent FET damage if the battery pack is charging while a discharge inhibit fault condition is present. This is done with the state comparator. The state comparator (with the V_{STATE_C} threshold) remains on for the entire duration of a DSG fault with no CHG fault event.

- If (SRP-SRN) ≤ V_{STATE_C} and no charge event is detected, the DSG FET output will remain OFF due to the present of a DSG fault.
- If (SRP-SRN) > V_{STATE_C} and a charge event is detected, the DSG FET output will turn ON for body diode protection.

See the *State Comparator* section for details.

The presence of any related faults, as shown in 图 13, results in the DSGFET_OFF signal.

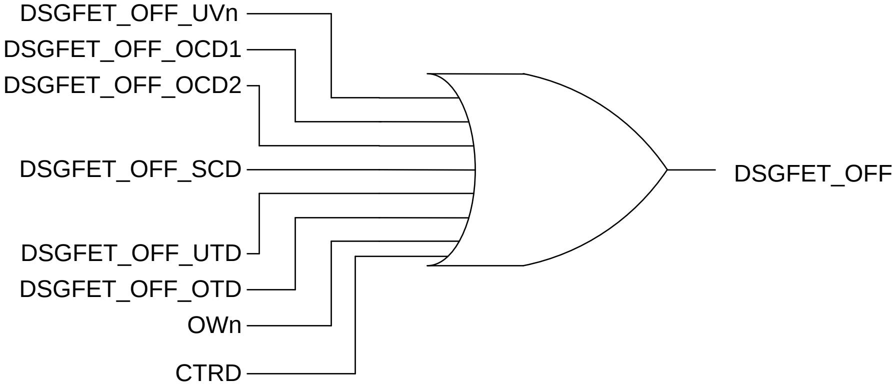


图 13. Faults that Can Qualify DSGFET_OFF

8.3.8 CHG FET Driver Operation

The CHG and CHGU pins are driven high only when no related faults (OV, OW, OTC, UTC, OTD, UTD, OCD1, OCD2, SCD, and CTRC are disabled) are present or the pack has a discharge current where (SRP-SRN) < V_{STATE_D1}. The CHG pin drives the CHG FET, which is for use on the single device configuration or by the bottom device in a stack configuration. The CHGU pin has the same logic state as the CHG pin and is for use in the upper device (in a multi-stack configuration) to provide the drive signal to the CTRC pin of the lower device. The CHGU pin should never connect to the CHG FET directly.

Turning off the CHG pin has no influence on the overcurrent protection circuitry. The CHG pin is designed to switch on quickly and the target on resistance is about 2 kΩ. When the pin is turned off, the CHG driver pin is actively driven low and will fall together with PACK–.

The CHG FET may be turned on to protect the FET's body diode if the pack is discharging, even if a charging inhibit fault condition is present. This is done through the state comparator. The state comparator (with the V_{STATE_D} threshold) remains on for the entire duration of a DSG fault with no CHG fault event.

- If (SRP-SRN) > V_{STATE_D} and no discharge event is detected, the CHG FET output will remain OFF due to the present of a CHG fault.
- If (SRP-SRN) ≤ V_{STATE_D} and a charge event is detected, the CHG FET output will turn ON for body diode protection.

The CHGFET_OFF signal is a result of the presence of any related faults, as shown in 图 14.

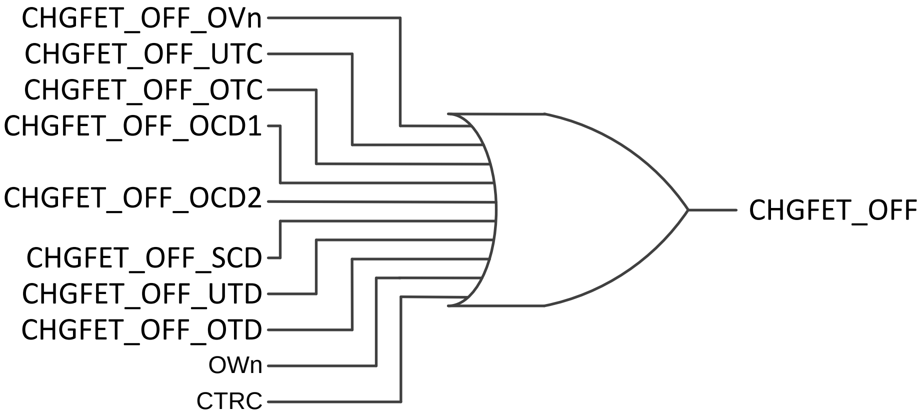


图 14. Faults That Can Qualify CHGFET OFF

8.3.9 External Override of CHG and DSG Drivers

The device allows direct disabling of the CHG and DSG drivers through the CTRC and CTRD pins, respectively. The operation of the CTRC and CTRD pins is shown in 图 15. To support the simple-stack solution for higher-cell count packs, these pins are designed to operate above the device's VDD level. Simply connect a 10-MΩ resistor between a lower device CTRC and CTRD input pins to an upper device CHGU and DSG output pins (see the schematics in *Stacking Implementations*.

CTRC only enables or disables the CHG pin, while CTRD only enables or disables the DSG pin. When the CTRx pin is in the DISABLED region, the respective FET pin will be off, regardless of the state of the protection circuitry. When the CTRx pin is in either ENABLED region, the protection circuitry determines the state of the FET driver.

Both CTRx pins apply the fault-detection filtered method to improve the robustness of the signal detection: The counter counts up if an ENABLED signal is sampled; the counter counts down if a DISABLED signal is sampled. When the counter counts up from 0% to > 70% of its full range, which takes about 7 ms typical of a solid signal, the CTRx pins take the signal as ENABLED. If the counter counts down from 100% to < 30%, of its full range, which takes about 7 ms typical of a solid signal, the CTRx pins take the signal as DISABLED. From a 0 count counter (solid DISABLE), a solid ENABLE signal takes about t_{CTRDEG_ON} time to deglitch. From a 100% count (solid ENABLE), a solid DISABLE signal takes about t_{CTRDEG_OFF} time to deglitch. Although such a filter scheme provides a certain level of noise tolerance, it is highly recommended to shield the CTRx traces and keep the traces as short as possible in the PCB layout design. The CTRx deglitch time will add onto the FET response timing on the OV, UV, and OW faults in a stack configuration. The t_{CTRDEG_OFF} time adds an additional delay to the fault detection timing and the t_{CTRDEG_ON} time adds an additional delay to the fault recovery timing.

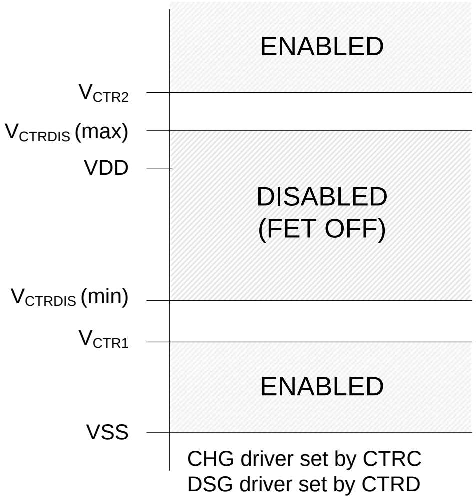


图 15. External Override of CHG and DSG Drivers

8.3.10 Configuring 3-S, 4-S, or 5-S Mode

The bq77904 supports 3-S and 4-S packs, while the bq77905 supports 3-S, 4-S, and 5-S packs. To avoid accidentally detecting a UV fault on unused (shorted) cell inputs, the device must be configured for the specific cell count of the pack. This is set with the configuration pin, CCFG, which is mapped as in 表 7. The device periodically checks the CCFG status and takes t_{CCFG_DEG} time to detect the pin status.

表 7. CCFG Configurations

CCFG	CONFIGURATION	CONNECT TO
< V_{CCFGL} for t_{CCFG_DEG}	3 cells	AVSS
Within V_{CCFGM} for t_{CCFG_DEG}	4 cells	AVDD
> V_{CCFGH} for t_{CCFG_DEG}	5 cells	Floating

The CCFG pin should be tied to the recommended net from 表 7. The device compares the CCFG input voltage to the AVDD voltage and should never be set above the AVDD voltage. When the device configuration is for 5 S, leave the CCFG pin floating. The internal pin bias is approximately 30% of the AVDD voltage for the 5-S configuration. Note that the bq77904 should not be configured in 5-S mode, as this results in a permanent UV fault.

8.3.11 Stacking Implementations

Higher than 5-S cell packs may be supported by daisy-chaining multiple devices. Each device ensures OV, UV, OTC, OTD, UTC, and UTD protections of its directly monitored cells, while any fault conditions automatically disable the global CHG and/or DSG FET driver. Note that upper devices do not provide OCD1, OCD2, or SCD protections, as these are based on pack current. For the bq77904 and bq77905 devices used on the upper stack, the SRP and SRN pins should be shorted to prevent false detection.

表 8. Stacking Implementation Configurations

CONFIGURATION	CHG PIN	CHGU PIN
Bottom or single device	Connect to CHG FET	Leave unconnected
Upper stack	Leave unconnected	Connect to CTRC of the lower device

To configure higher-cell packs, follow this procedure:

- Each device must have a connection on at least three lowest-cell input pins.
- TI recommends to connect a higher-cell count to the upper devices (for example, for a 7-S configuration, connect four cells on the upper device and three cells on the bottom device). This provides a stronger CRTx signal to the bottom device.
- Ensure that each device’s CCFG pin is configured appropriately for its specific number of cells (three, four, or five cells).
- For the bottom device, the CHG pin should be used to drive the CHG FET and leave the CHGU pin unconnected. For the upper device, the CHGU pin should be used to connect to lower device’s CTRC pin with a R_{CTRx} and leave the CHG pin unconnected.
- Connect the upper DSG pins with a R_{CTRx} to the immediate lower device CTRD pin.
- All upper devices should have the SRP and SRN to its AVSS pin.
- If load removal is not used for UV recovery, connect the upper device LD pin to its AVSS pin, as shown in 图 16 and 图 17. Otherwise, refer to 图 24 for proper LD connection.

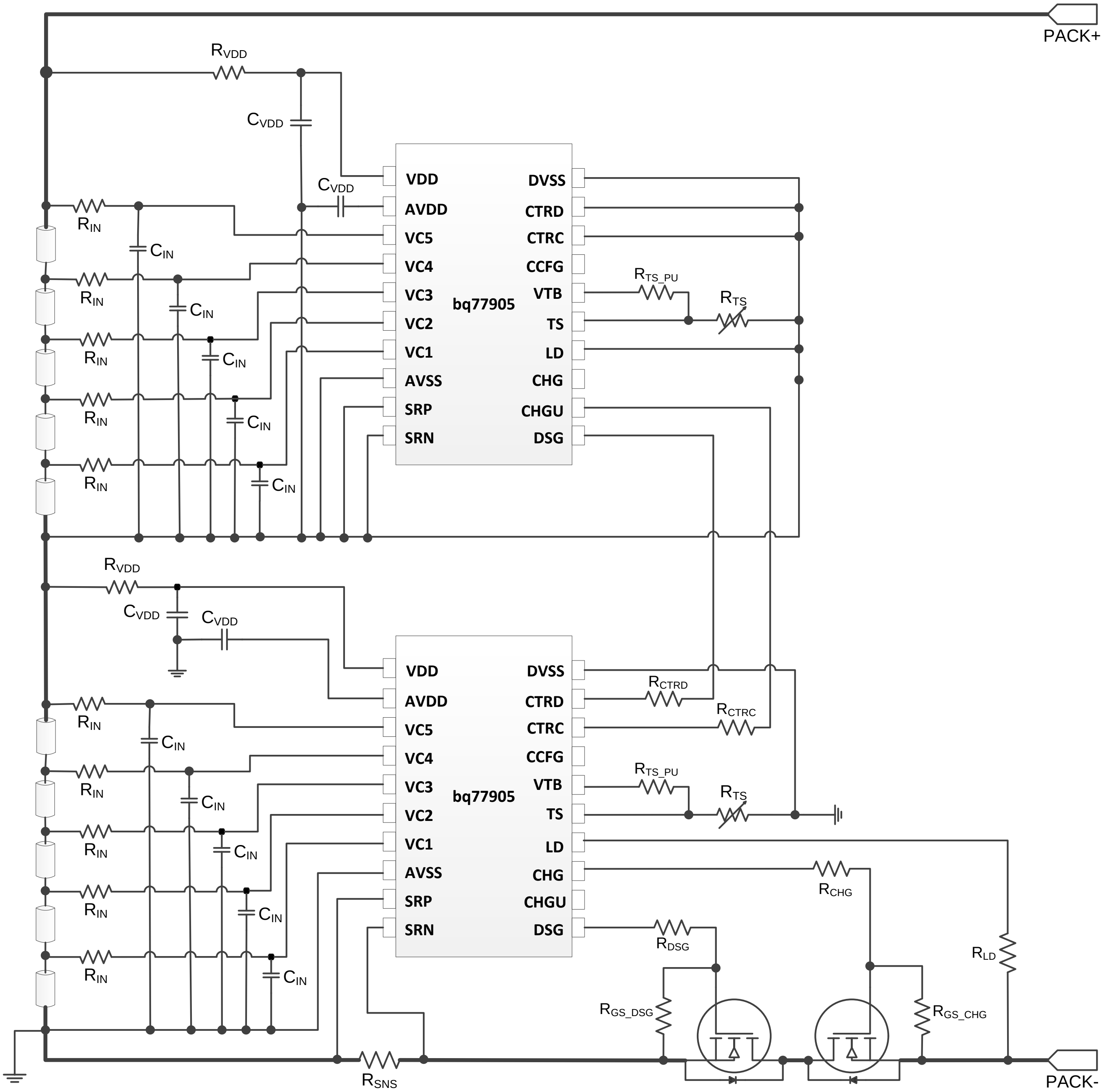


图 16. 10S Pack Using Two bq77905 Devices

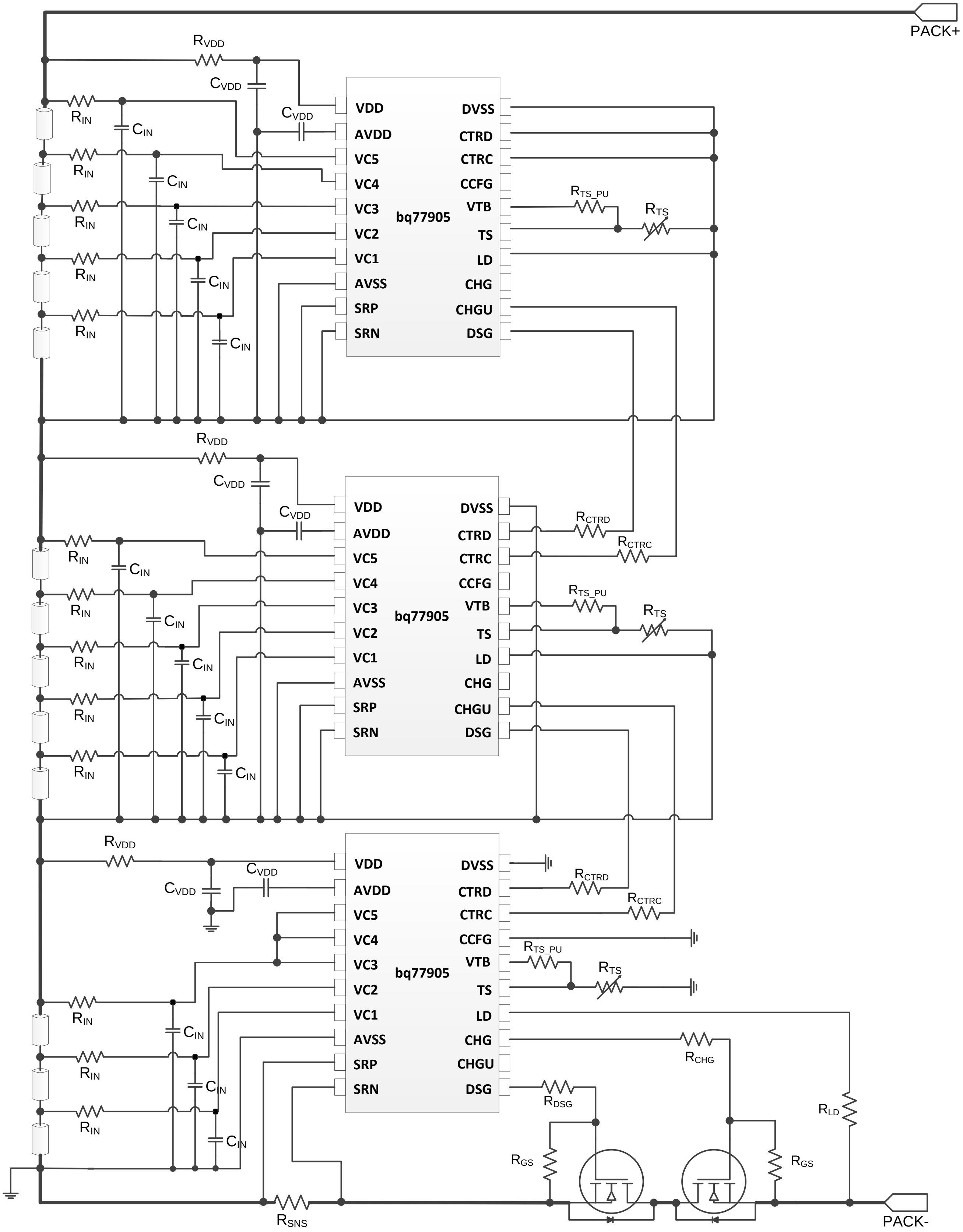


图 17. 13S Pack Using Three bq77905 Devices

8.3.12 Zero-Volt Battery Charging Inhibition

Once the device is powered up, it can pull the CHG pin up if the VDD ≥ V_{SHUT}, which varies from about 1 V per cell on a 3-S configuration to about 0.6 V per cell on a 5-S configuration. If the battery stack voltage falls below V_{SHUT}, the device is in SHUTDOWN mode and the CHG driver is no longer active and charging is not allowed unless VDD rises above V_{POR} again.

8.4 Device Functional Modes

8.4.1 Power Modes

8.4.1.1 Power-On Reset (POR)

The device powers up when VDD ≥ V_{POR}. At POR, the following events occur:

- A typical 5-ms hold-off delay applies to both CHG and DSG drivers, keeping both drivers in the OFF state. This provides time for the internal LDO voltage to ramp up.
- CTRC and CTRD deglitch occurs. During the deglitch time, the CHG and DSG driver remains off. Note that deglitch time masks out the 5-ms hold-off delay.
- The device assumes OV fault at POR; thus, the CHG driver is off for OV recovery time if all the cell voltages are < (V_{OV} – V_{HYS_OV}). The OV recovery time starts after the 5-ms hold-off delay. If the device reset occurs when any cell voltage is above the OV hysteresis range, the CHG driver will remain off until an OV recovery condition is met.

8.4.1.2 FAULT Mode

If any configured protection fault is detected, the device enters the FAULT mode. In this mode, the CHG and/or DSG driver can be turned off depending on the fault. Refer to the fault response summary, Table 5, for detail. When one of the FET drivers (either CHG or DSG) is turned off, while the other FET driver is still on, the state comparator is activated for FET body diode protection.

8.4.1.3 SHUTDOWN Mode

This is the lowest power consumption state of the device when VDD falls below V_{SHUT}. In this mode, all fault detections and theCHG and DSG drivers are disabled. The device will wake up and enter NORMAL mode when VDD rises above V_{POR}.

8.4.1.4 Customer Fast Production Test Modes

The bq7790x device supports the ability to greatly reduce production test time by cutting down on protection fault delay times. To shorten fault times, place the bq7790x device into Customer Test Mode (CTM). CTM is triggered by raising VDD to V_{CTM} voltage above the highest cell input pin (that is, VC5) for t_{CTM_ENTRY} time.

The CTM is expected to be used in single-chip designs only. CTM is not supported for stacked designs. Once the device is in CTM, all fault delay and non-current fault's recovery delay times reduce to a value of t_{CTM_DELAY}. The fault recovery time for overcurrent faults (OCD1, OCD2, and SCD) is reduced to $t_{CTM\_OC\_REC}$.

Verification of protection fault functionality can be accomplished in a reduced time frame in CTM. Reducing the VDD voltage to the same voltage applied to the highest-cell input pin for t_{CTM_ENTRY} will exit CTM.

In CTM, with reduced time for all internal delays, qualification of all faults will be reduced to a single instance. Thus in this mode, fault condition qualification is more susceptible to transients, so take care to have fault conditions clearly and cleanly applied during test mode to avoid false triggering of fault conditions during CTM.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq77904 and bq77905 devices are low-power stackable battery pack protectors with an integrated low-side NMOS FET driver. The bq77904 and bq77905 devices provide voltage, current, temperature, and open-wire protections. All the devices protect and recover without MCU control. The following section highlights several recommended implementation when using these devices.

9.1.1 Recommended System Implementation

9.1.1.1 CHG and DSG FET Rise and Fall Time

The CHG and DSG FET drivers are designed to have fast switching time. Users should select a proper gate resistor (R_{CHG} and R_{DSG} in the reference schematic) to set to the desired rise/fall time.

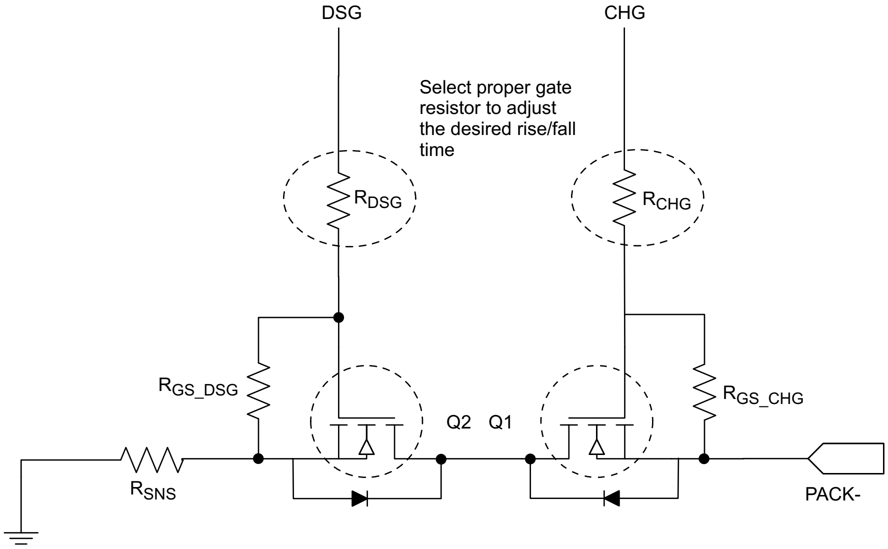
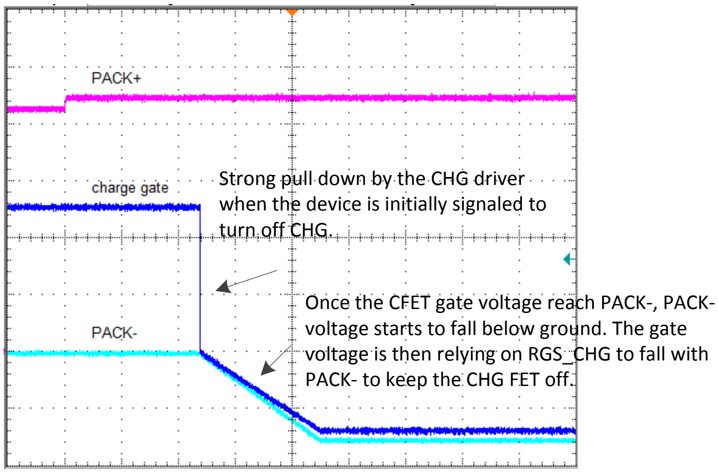


图 18. Select Proper Gate Resistor for FET Rise and Fall Time

The CHG FET fall time is generally slower, because it is connected to the PACK– terminal. The CHG driver will pull to V_{SS} quickly when the driver is signaled to turn off. Once the gate of the CHG FET reaches ground or Vgsth, the PACK– will start to fall below ground and the CHG signal will follow suit in order to turn off the CHG FET. This portion of the fall time is strongly dependent on the FET characteristic, the number of FETs in parallel, and the value of gate-source resistor (R_{GS_CHG}).

Application Information (接下页)



Strong pull down by the CHG driver when the device is initially signaled to turn off CHG.

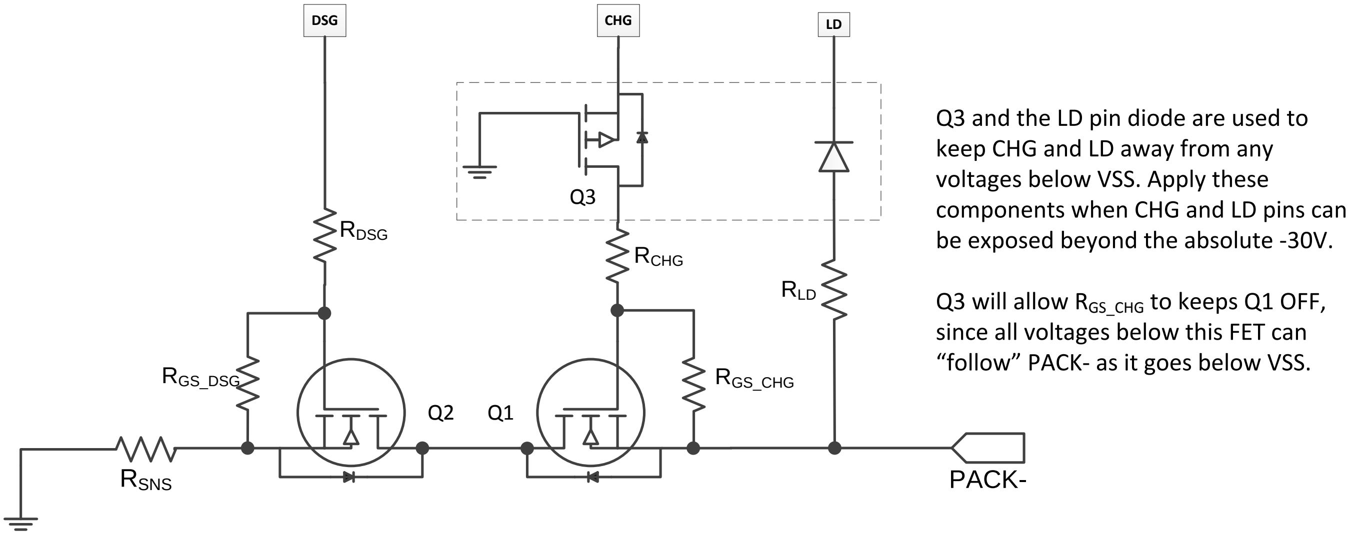
Once the CFET gate voltage reach PACK-, PACK- voltage starts to fall below ground. The gate voltage is then relying on RGS_CHG to fall with PACK- to keep the CHG FET off.

图 19. CHG FET Fall Time

9.1.1.2 Protecting CHG and LD

Because both CHG and LD are connected to the PACK– terminal, these pins are specially designed to sustain an absolute max of –30 V. However, the device can be used in a wide variety of applications, and it is possible to expose the pins lower than –30 V absolute max rating.

To protect the pins, TI recommends to put a PMOS FET in series of the CHG pin and a diode in series of the LD pin as shown below.



Q3 and the LD pin diode are used to keep CHG and LD away from any voltages below VSS. Apply these components when CHG and LD pins can be exposed beyond the absolute -30V.

Q3 will allow R_{GS_CHG} to keeps Q1 OFF, since all voltages below this FET can “follow” PACK- as it goes below VSS.

图 20. Protecting CHG and LD

9.1.1.3 Protecting CHG FET

When the CHG driver is off, CHG is pulled to V_{SS}, the PACK– terminal can be pullup to the PACK+ level when a load is connected. This can put the gate-source voltage above the absolute max of the MOSFET rating. Hence, it is common to place a Zener diode across the CHG FET’s gate-source to protect the CHG FET. Additional components are added when a Zener is used to limit current going into the CHG pin, as well as reducing the impact on rise time. See 图 21 for details.

Application Information (接下页)

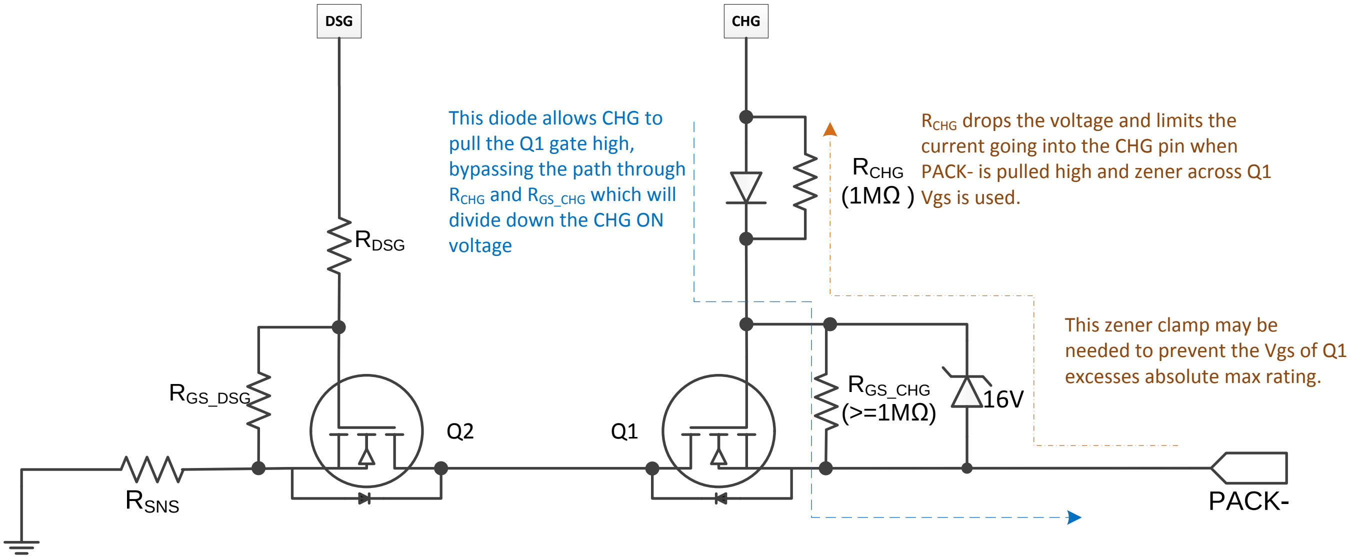


图 21. Protect CHG FET from a High Voltage on PACK–

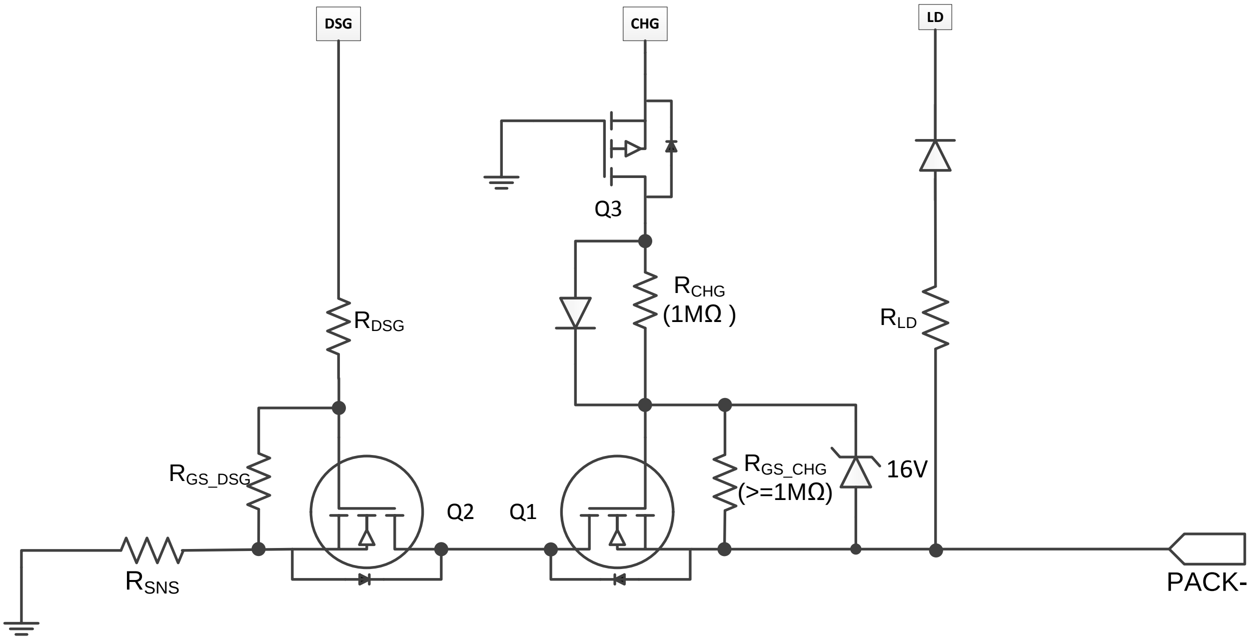


图 22. Optional Components Combining 图 20 and 图 21 Protections

9.1.1.4 Using Load Detect for UV Fault Recovery

A larger CHG FET gate-source resistor is required if load removal is enabled as part of the UV recovery criteria. When the load removal circuit is enabled, the device is internally connected to Vss. Because in a UV fault the CHG driver remains on, it creates a resistor divider path to the load detect circuit.

Application Information (接下页)

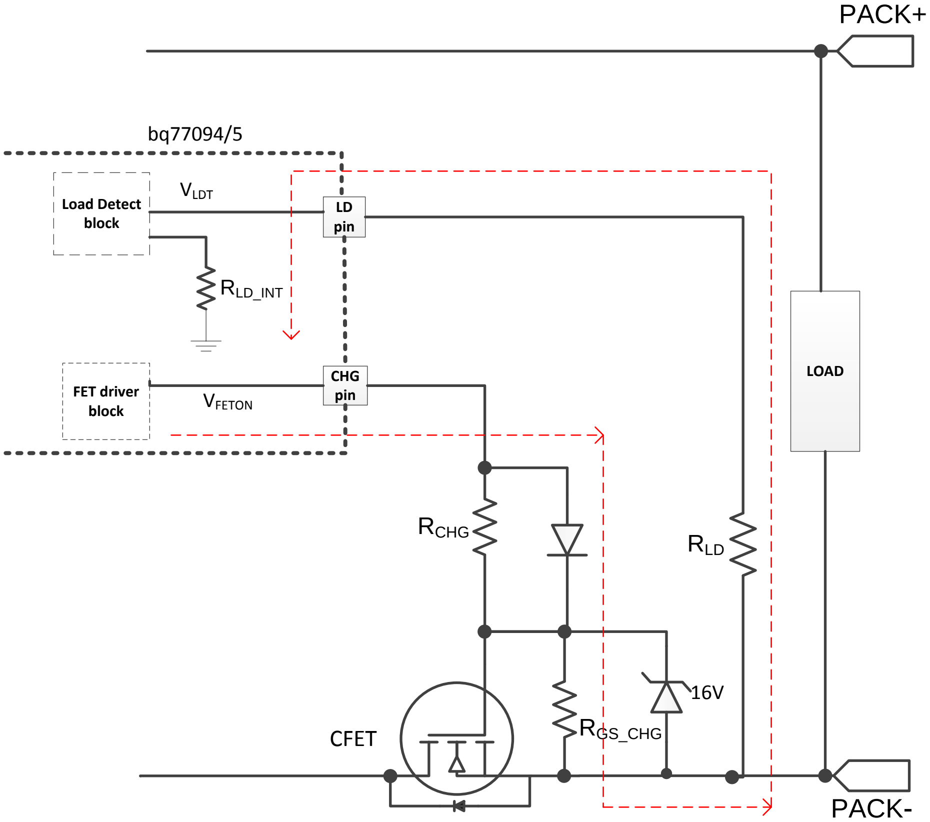


图 23. Load Detect Circuit During UV Fault

To ensure load removal is detected properly during a UV fault, TI recommends to use 3.3 MΩ for R_{GS_CHG} (instead of a typical of 1 MΩ when load removal is NOT required for UV recovery). R_{CHG} can stay in 1 MΩ as recommended when using CHG FET protection components. The CHG FET rise time impact is minimized as described in the *Protecting CHG FET* section. On a stacked configuration, connect the LD pin, as shown in 图 24 if load removal is used for a UV fault recovery. If load detection is not required for a UV fault recovery, a larger value of R_{GS_CHG} can be used (that is, 10 MΩ) and the LD pin on the upper devices can be left floating.

Application Information (接下页)

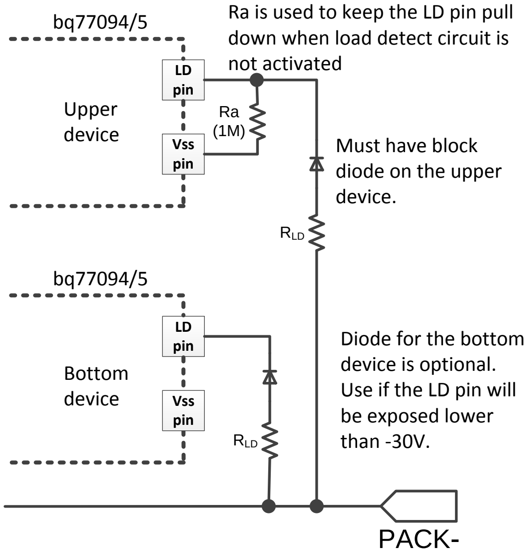


图 24. Simplified Circuit: LD Connection on Upper Device When Using for UV Fault Recovery

9.1.1.5 Temperature Protection

The device detects temperature by checking the voltage divided by R_{TS_PU} and R_{TS}, with the assumption of using 10-KΩ R_{TS_PU} and 103AT NTC for R_{TS}. System designers should always check the thermistor resistance characteristics and refer to the temperature protection threshold specifications in the Electrical Characteristics table to determine if a different pullup resistor should be used. If a different temperature trip point is required, it is possible to scale the threshold using this equation: Temperature Protection Threshold = R_{TS} / (R_{TS} + R_{TS_PU}).

Example: Scale OTC trip points from 50°C to 55°C

The OTC protection can be set to 45°C or 50°C. When the device's OTC threshold is set to 50°C, it is referred to configure the V_{OTC} parameter to 29.38% of VTB (typical), with the assumption of R_{TS_PU} = 10 KΩ and R_{TS} = 103AT or similar NTC (which the NTC resistance at 50°C = 4.16 KΩ). The V_{OTC} specification is the resistor divider ratio of R_{TS_PU} and R_{TS}.

The V_{OTC}, V_{OTD}, V_{UTC}, and V_{UTD} configuration options are fixed in the device; thus, the actual temperature trip point can only adjust by using a different B-value NTC and/or using a different R_{TS_PU}.

In this example, the 103AT NTC resistance at 55°C is 3.536 KΩ. By changing the R_{TS_PU} from 10 KΩ to 8.5 KΩ, users can scale the actual OTC temperature trip point from 50°C to 55°C. Because the R_{TS_PU} value is smaller, this change affects all the other temperature trip points and scales OTD, UTC, and UTD to ~5°C higher as well.

9.1.1.6 Adding Filter to Sense Resistor

Current fault is sense through voltage across a sense resistor. Optional RC filters can be added to the sense resistor to improve stability.

Application Information (接下页)

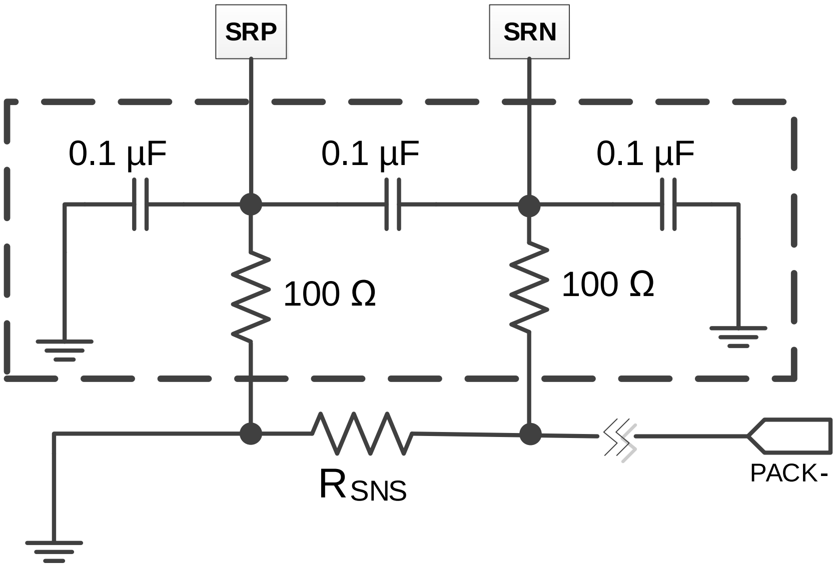


图 25. Optional Filters Improve Current Measurement

9.1.1.7 Using a State Comparator in an Application

The state comparator does not have built-in hysteresis. It is normal to observe the FET body diode protection toggling on and off with the V_{STATE_C1} or V_{STATE_D1} accuracy range. In a typical application, the sense resistor is selected according to the application current, which usually is not close to the state comparator threshold.

9.1.1.7.1 Examples

As an example, using a 5-Ah battery, with 1C-rate (5 A) charge and 2C-rate (10 A) discharge, the sense resistor is 3 mΩ or less. The typical current to turn on the FET body diode protection is 667 mA using this example. Because there is no built-in hysteresis, noise can reset the state comparator counter and toggle off the FET body diode protection and vice versa; thus, it is normal to observe the device toggles the FET body diode protection on or off within a 1-mV to 3-mV range. With a 3-mΩ sense resistor, it is about 330 mA to 1 A. As this behavior is due to noise from the system, the FET toggling behavior usually occurs right at the typical 2-mV state comparator threshold. As current increases or decreases from the typical value, the detection is more solid and has less frequent FET toggling. Using this example, either charge or discharge should provide a solid FET body diode protection detection.

Look at the device behavior during an OV event (and no other fault is detected). In an OV event, CHG FET is off and DSG FET is on. If a discharge of > –1 A occurs, the device would turn on the CHG FET immediately to allow the full discharge current to pass through. Once the overcharged cell is discharged to the OV recovery level, the OV fault is recovered and the CHG driver turns on (or remains on in this scenario) and the state comparator is turned off.

If the discharge current is < 1 A when the device is still in an OV fault, the CHG FET may toggle on and off until the overcharged cell voltage is reduced down to the OV recovery level. When the OV fault recovers, the CHG FET is solidly turned on and the state comparator is off.

Without the FET body diode protection, if a discharge occurs during an OV fault state, the discharge current can only pass through the CHG FET body diode until the OV fault is recovered. This increases the risk of damaging the CHG FET if the MOSFET is not rated to sustain this amount of current through its body diode. It also increases the FET temperature as current is now carried through the body diode.

9.2 Typical Application

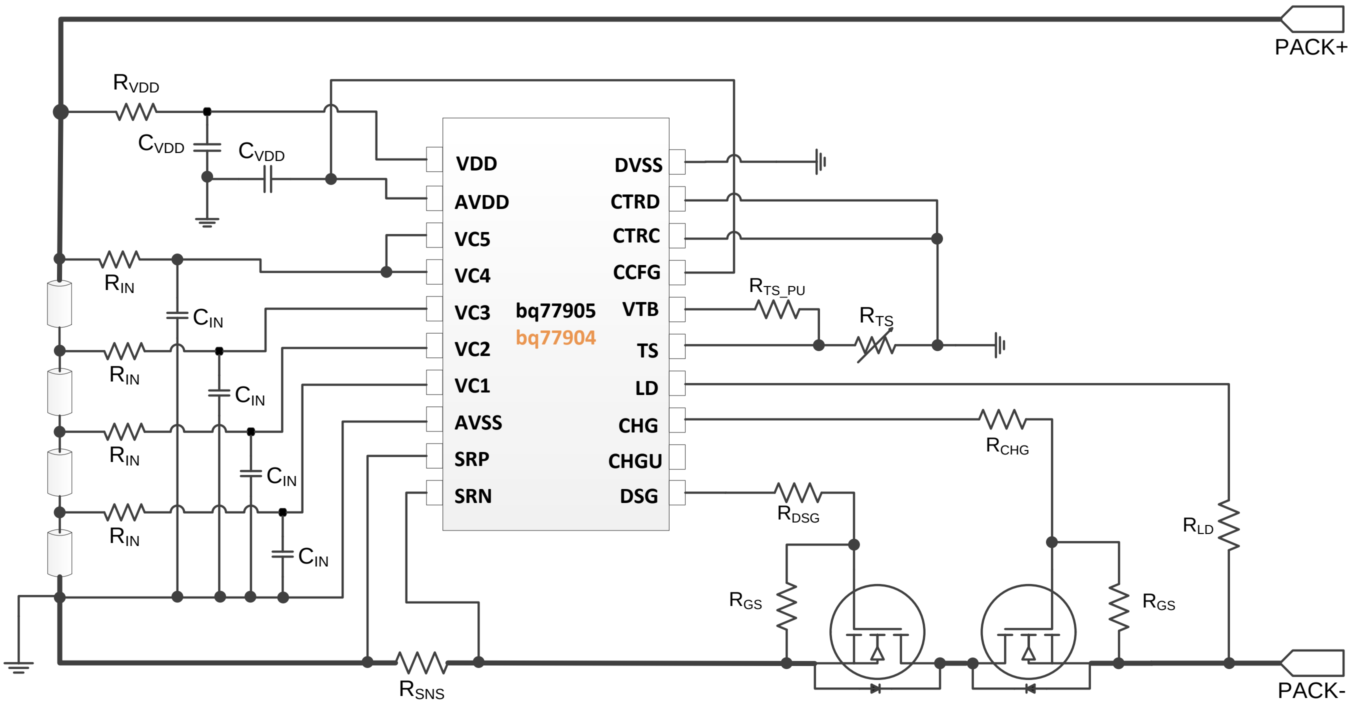


图 26. bq77904 and bq77905 with Four Cells

9.2.1 Design Requirements

For this design example, use the parameters shown in 表 9.

表 9. Design Parameters

PARAMETER	DESCRIPTION		VALUES
R_{IN}	Cell voltage sensing (VCx pins) filter resistor		1 kΩ ±5%
C_{IN}	Cell voltage sensing (VCx pins) filter capacitor		0.1 µF ±10%
R_{VDD}	Supply voltage filter resistor		1 kΩ ±5%
C_{VDD}	Supply voltage filter capacitor		1 µF ±20%
R_{TS}	NTC thermistor		103AT, 10 kΩ ±3%
R_{TS_PU}	Thermistor pullup resistor to VTB pin, assuming using 103AT NTC or NTC with similar resistance-temperature characteristics		10 kΩ ±1%
R_{GS_CHG}	CHG FET gate-source resistor	Load removal is enabled for UV recovery.	3.3 MΩ ±5%
		Load removal is disabled for UV recovery.	1 MΩ ±5%
R_{GS_DSG}	DSG FET gate-source resistor		1 MΩ ±5%
R_{CHG}	CHG gate resistor	System designers should adjust this parameter to meet the desired FET rise/fall time.	1 kΩ ±5%
		If additional components are used to protect the CHG FET and/or to enable load removal detection for UV recovery.	1 MΩ ±5%
R_{DSG}	DSG gate resistor, system designers should adjust this parameter to meet the desired FET rise/fall time.		4.5 kΩ ±5%
R_{CRTC} and R_{CTRD}	CTRC and CTRD current limit resistor		10 MΩ ±5%
R_{LD}	LD resistor for load removal detection		450 KΩ ±5%
R_{SNS}	Current sense resistor for current protection. System designers should change this parameter according to the application current protection requirements.		1 mΩ ±1%

9.2.2 Detailed Design Procedure

The following is the detailed design procedure.

1. Based on the application current, select the proper sense resistor value. The sense resistor should allow detection of the highest current protection, short circuit current.
2. Temperature protection is set with the assumption of using a 103AT NTC (or NTC with similar specification). If a different type of NTC is used, a different R_{TS_PU} may be used for the application. Refer to the actual temperature detection threshold voltage to determine the R_{TS_PU} value.
3. Connect the CCFG pin correctly based on the number of cells in series.
4. Review the Recommended Application Implementation to determine if optional components should be added to the schematic.

9.2.2.1 Design Example

To design the protection for a 36-V Li-ion battery pack using 4.2-V LiCoO2 cells with the following protection requirements:

Voltage Protection

- OV at 4.3 V, recover at 4.1 V
- UV at 2.6 V, recover at 3 V and when load is removed.

Current Protection

- OCD1 at 40 A with 300-ms–400-ms delay
- OCD2 at 80 A with the shortest delay option
- SCD at 100 A with < 500-µs delay
- Requires load removal for recovery

Temperature Protection

- Charge – OTC at 50°C, UTC at –5°C
- Discharge – OTD at 70°C, UTD at –10°C

To start the design:

1. Start the schematic.
   - A 36-V pack using $LiCoO_2$ cells requires 10-S configuration; thus, two bq77905 devices in a stackable configuration is needed.
   - Follow the 10-S reference schematic in this document. Follow the recommended design parameters listed in the *Design Requirements* section of this document.
   - The power FET used in this type of application usually has an absolute of 20 V Vgs. For a 36-V pack design, TI recommends to use the additional components to protect the CHG FET Vgs. See the *Using Load Detect for UV Fault Recovery* section for details.
   - Because load removal for UV recovery is required, a 3-MΩ R_{GS_CHG} should be used for the schematic.
2. Decide the value of the sense resistor, R_{SNS}.
   - When selecting the value of R_{SNS}, ensure the voltage drop across SRP and SRN is within the available current protection threshold range.
   - In this example, select R_{SNS} = 1 mΩ (any value ≤ 2 mΩ will work in this example).
3. Determine all of the bq77905 protection configurations (see 表 10).
4. Review the available released or preview devices in the *Device Comparison* section to determine if a suitable option is available. If not, contact TI representative for further assistance.

表 10. Design Example Configuration

Protection	Threshold	Hysteresis	Delay	Recovery Method
OV	4.3 V	200 mV	1 s (default setting)	Hysteresis
UV	2.6 V	400 mV	1 s (default setting)	Hysteresis + load removal
OW	100 nA (default setting)	—	—	$(VC_x – VC_{x–1})$ > 600 mV (typical)
OCD1	40 mV	—	350 ms	Load removal only

表 10. Design Example Configuration (接下页)

Protection	Threshold	Hysteresis	Delay	Recovery Method
OCD2	80 mV	—	5 ms	Load removal only
SCD	100 mV	—	Fixed at 360 µs	Load removal only
OTC	50°C	10°C	4.5 s	Hysteresis
OTD	70°C	10°C	4.5 s	Hysteresis
UTC	–5°C	10°C	4.5 s	Hysteresis
UTD	–10°C	10°C	4.5 s	Hysteresis

9.2.3 Application Curves

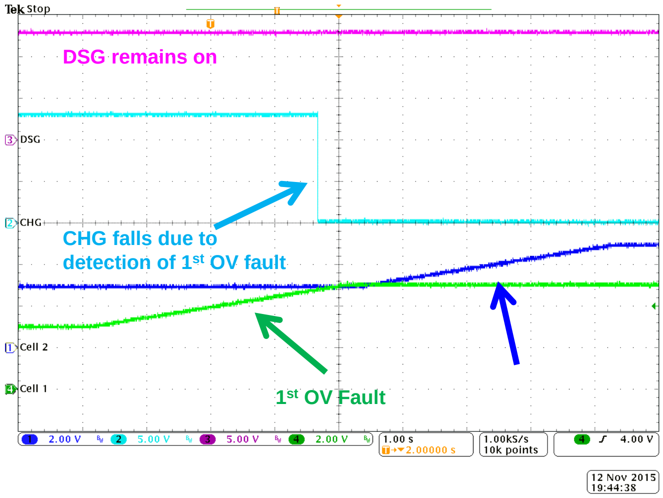


图 27. OV Fault Protection

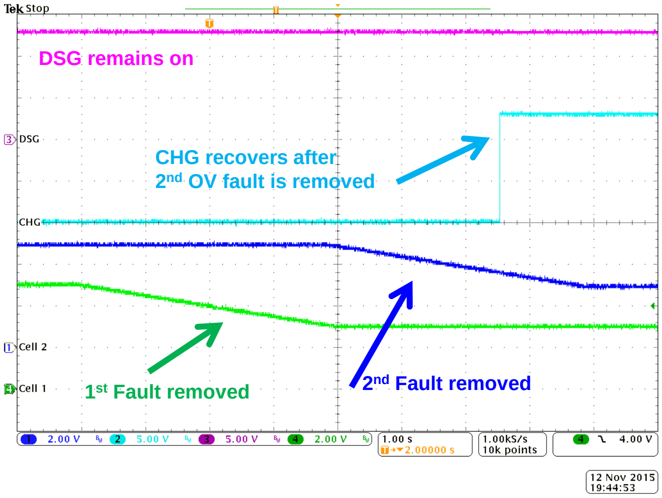


图 28. OV Fault Recovery

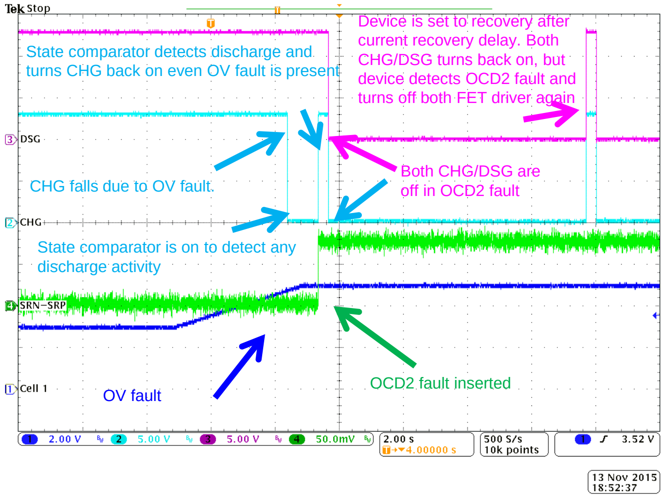


图 29. OV and OCD2 Faults Protection

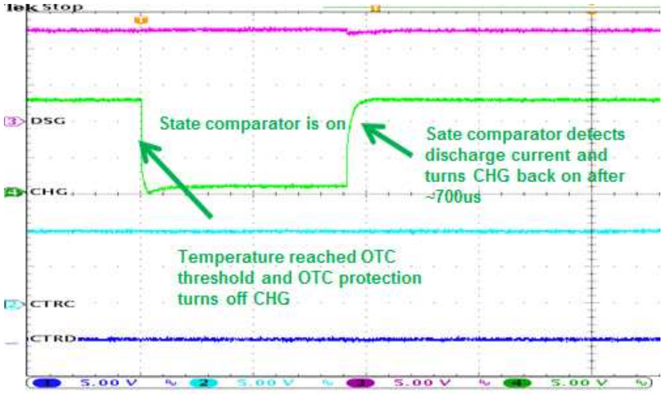
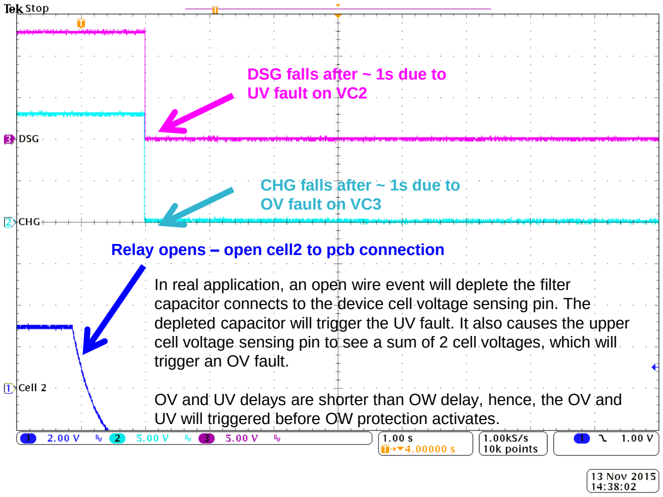


图 30. Detect OTC Fault While in 30-A Discharge



DSG falls after ~ 1s due to UV fault on VC2

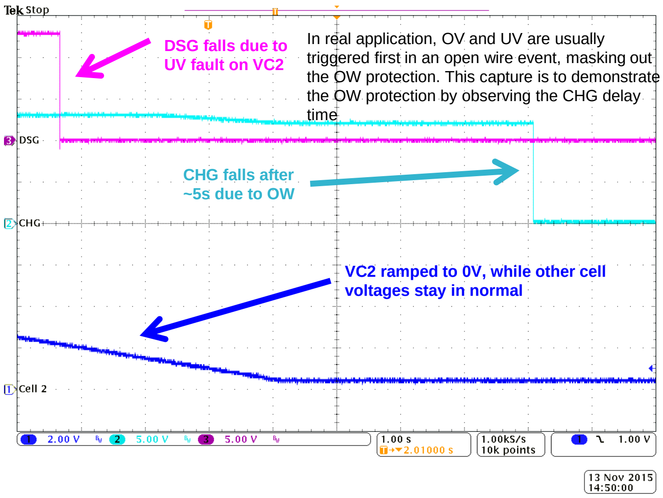
CHG falls after ~ 1s due to OV fault on VC3

Relay opens – open cell2 to pcb connection

In real application, an open wire event will deplete the filter capacitor connects to the device cell voltage sensing pin. The depleted capacitor will trigger the UV fault. It also causes the upper cell voltage sensing pin to see a sum of 2 cell voltages, which will trigger an OV fault.

OV and UV delays are shorter than OW delay, hence, the OV and UV will triggered before OW protection activates.

图 31. OW Fault Protection—Open Cell2 To PCB Connection



DSG falls due to UV fault on VC2

In real application, OV and UV are usually triggered first in an open wire event, masking out the OW protection. This capture is to demonstrate the OW protection by observing the CHG delay time

CHG falls after ~5s due to OW

VC2 ramped to 0V, while other cell voltages stay in normal

图 32. OW Fault Protection—Ramping Down Cell2 Voltage

9.3 System Examples

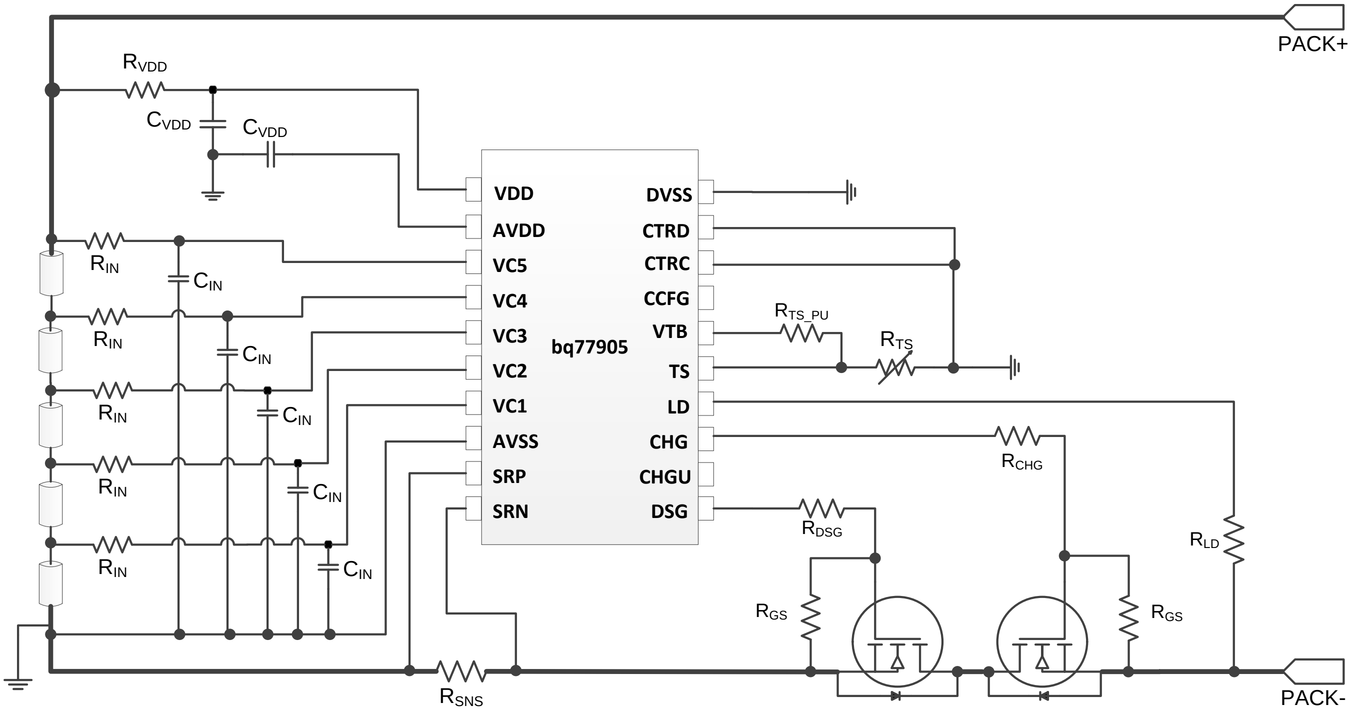


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图 33. bq77905 with Five Cells

10 Power Supply Recommendations

The recommended cell voltage range is up to 5 V. If three cells in series are connecting to bq77905, the unused VCx pins should be shorted to the highest unused VCx pin. The recommended VDD range is from 3 V–25 V. This implies the device is still operational when cell voltage is depleted down to approximately 1.5-V range.

11 Layout

11.1 Layout Guidelines

1. Match SRN and SRP traces.
2. R_{IN} filters, VDD, AVDD filters, and the C_{VDD} capacitor should be placed close to the device pins.
3. Separate the device ground plane (low current ground) from the high current path. Filter capacitors should reference to the low current ground path or device Vss.
4. In a stack configuration, the R_{CTRD} and R_{CTRC} should be placed closer to the lower device CTRD and CTRC pins.
5. R_{GS} should be placed near the FETs.

11.2 Layout Example

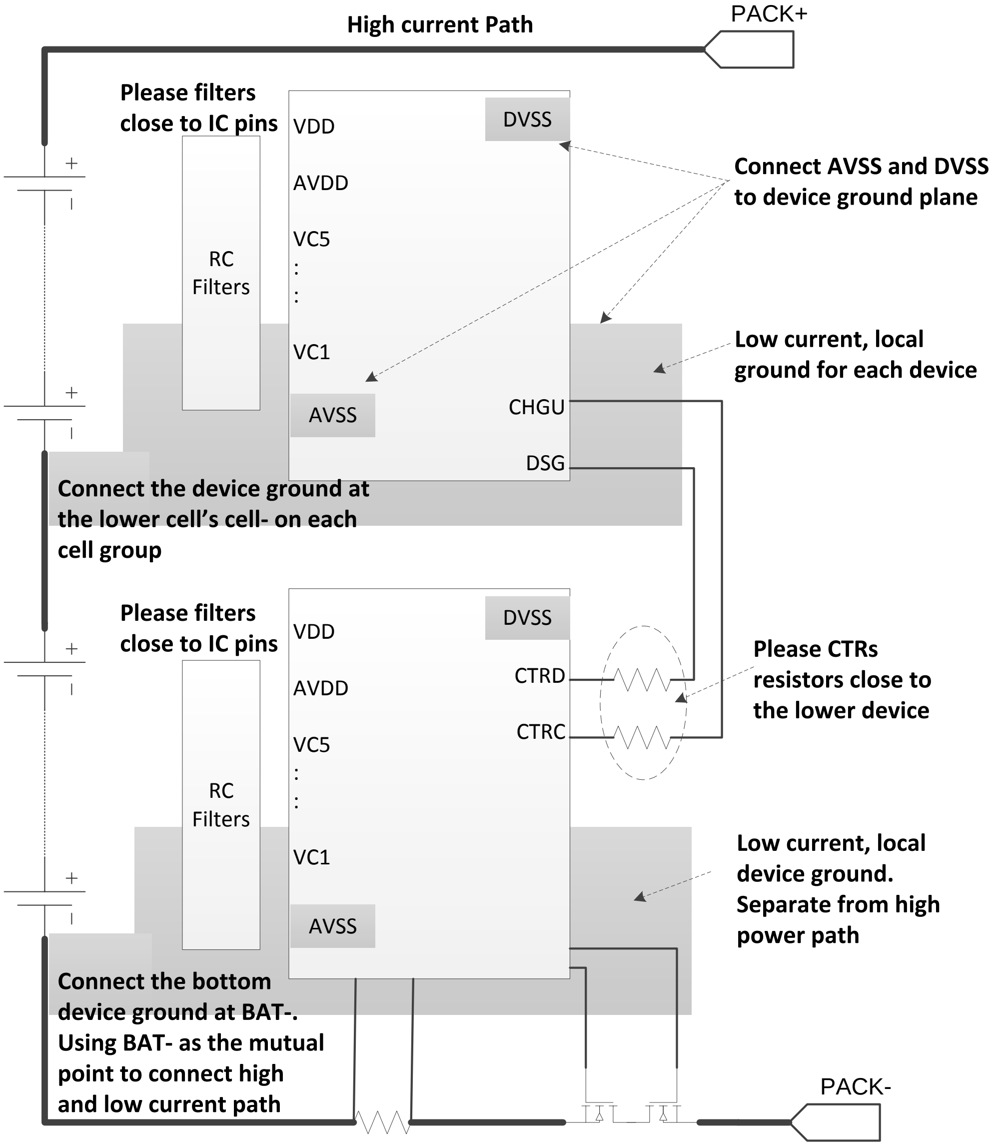

图 34. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **11.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
bq77904	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq77905	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。***此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ7790400PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790400	Samples
BQ7790400PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790400	Samples
BQ7790500PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790500	Samples
BQ7790500PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790500	Samples
BQ7790502PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790502	Samples
BQ7790502PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790502	Samples
BQ7790503PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790503	Samples
BQ7790503PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790503	Samples
BQ7790505PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790505	Samples
BQ7790505PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790505	Samples
BQ7790508PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790508	Samples
BQ7790508PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790508	Samples
BQ7790509PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790509	Samples
BQ7790509PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790509	Samples
BQ7790511PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790511	Samples
BQ7790511PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790511	Samples
BQ7790512PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790512	Samples
BQ7790512PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790512	Samples
BQ7790518PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790518	Samples
BQ7790518PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790518	Samples

PACKAGE OPTION ADDENDUM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ7790521PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790521	Samples
BQ7790521PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790521	Samples
BQ7790522PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790522	Samples
BQ7790522PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B7790522	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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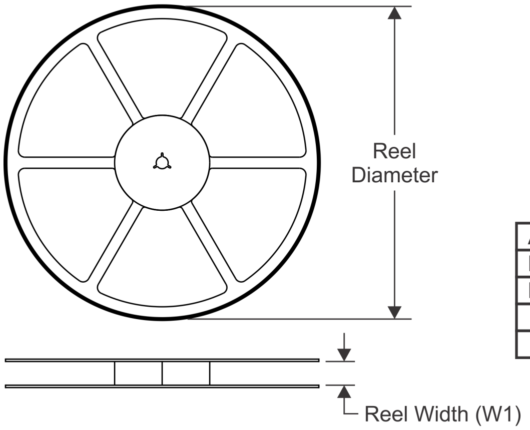
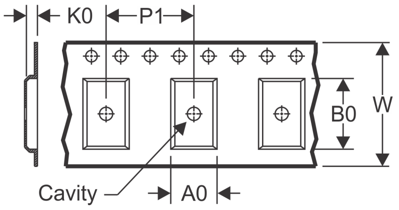
TAPE AND REEL INFORMATION

REEL DIMENSIONS

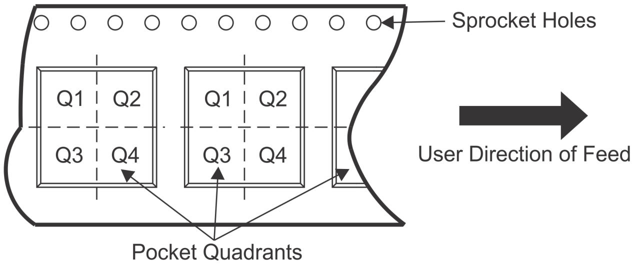


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

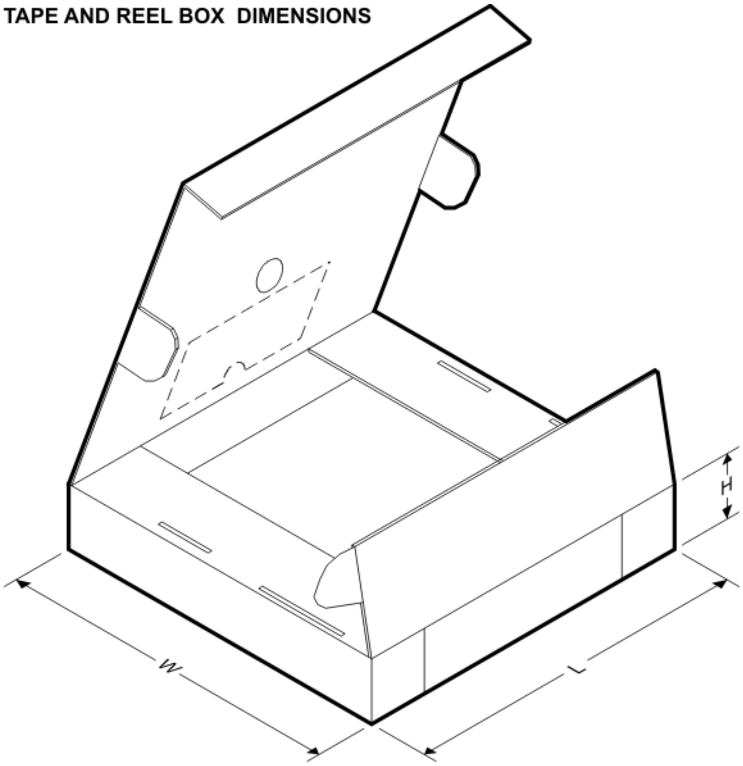
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ7790400PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BQ7790500PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BQ7790502PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BQ7790503PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BQ7790505PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BQ7790508PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BQ7790509PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BQ7790511PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BQ7790512PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BQ7790518PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BQ7790521PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BQ7790522PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

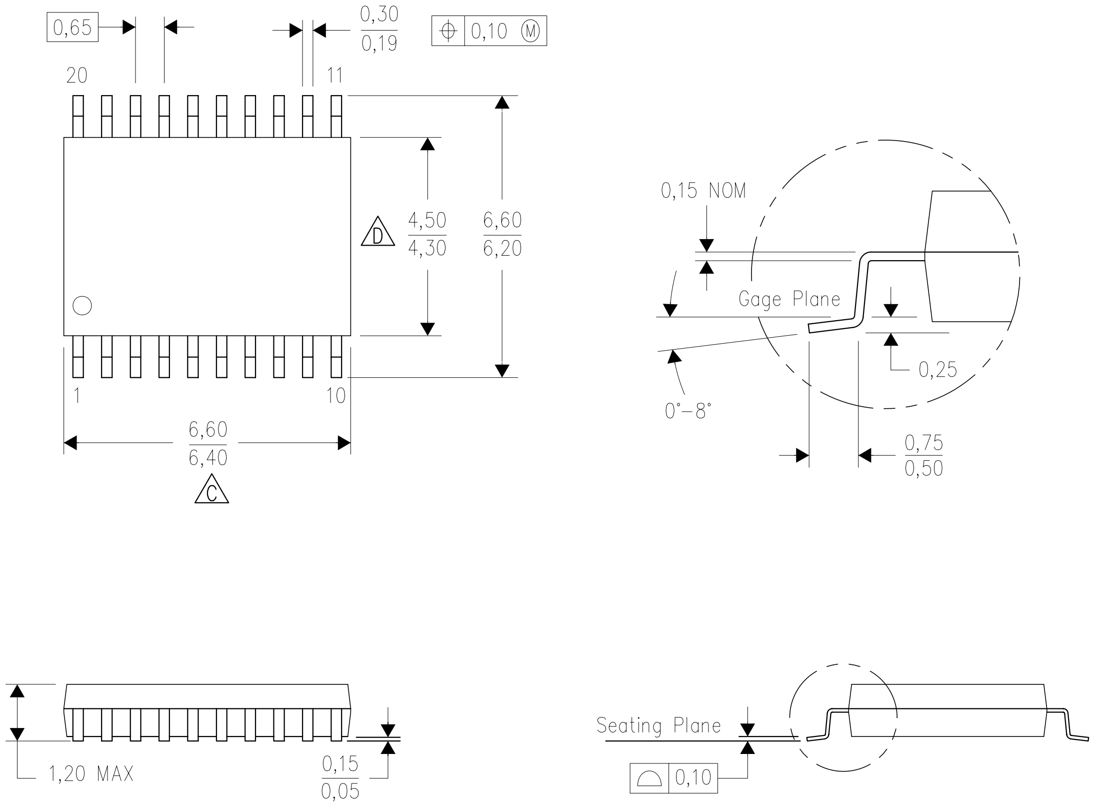
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ7790400PWR	TSSOP	PW	20	2000	350.0	350.0	43.0
BQ7790500PWR	TSSOP	PW	20	2000	350.0	350.0	43.0
BQ7790502PWR	TSSOP	PW	20	2000	350.0	350.0	43.0
BQ7790503PWR	TSSOP	PW	20	2000	350.0	350.0	43.0
BQ7790505PWR	TSSOP	PW	20	2000	350.0	350.0	43.0
BQ7790508PWR	TSSOP	PW	20	2000	350.0	350.0	43.0
BQ7790509PWR	TSSOP	PW	20	2000	350.0	350.0	43.0
BQ7790511PWR	TSSOP	PW	20	2000	350.0	350.0	43.0
BQ7790512PWR	TSSOP	PW	20	2000	350.0	350.0	43.0
BQ7790518PWR	TSSOP	PW	20	2000	853.0	449.0	35.0
BQ7790521PWR	TSSOP	PW	20	2000	853.0	449.0	35.0
BQ7790522PWR	TSSOP	PW	20	2000	853.0	449.0	35.0

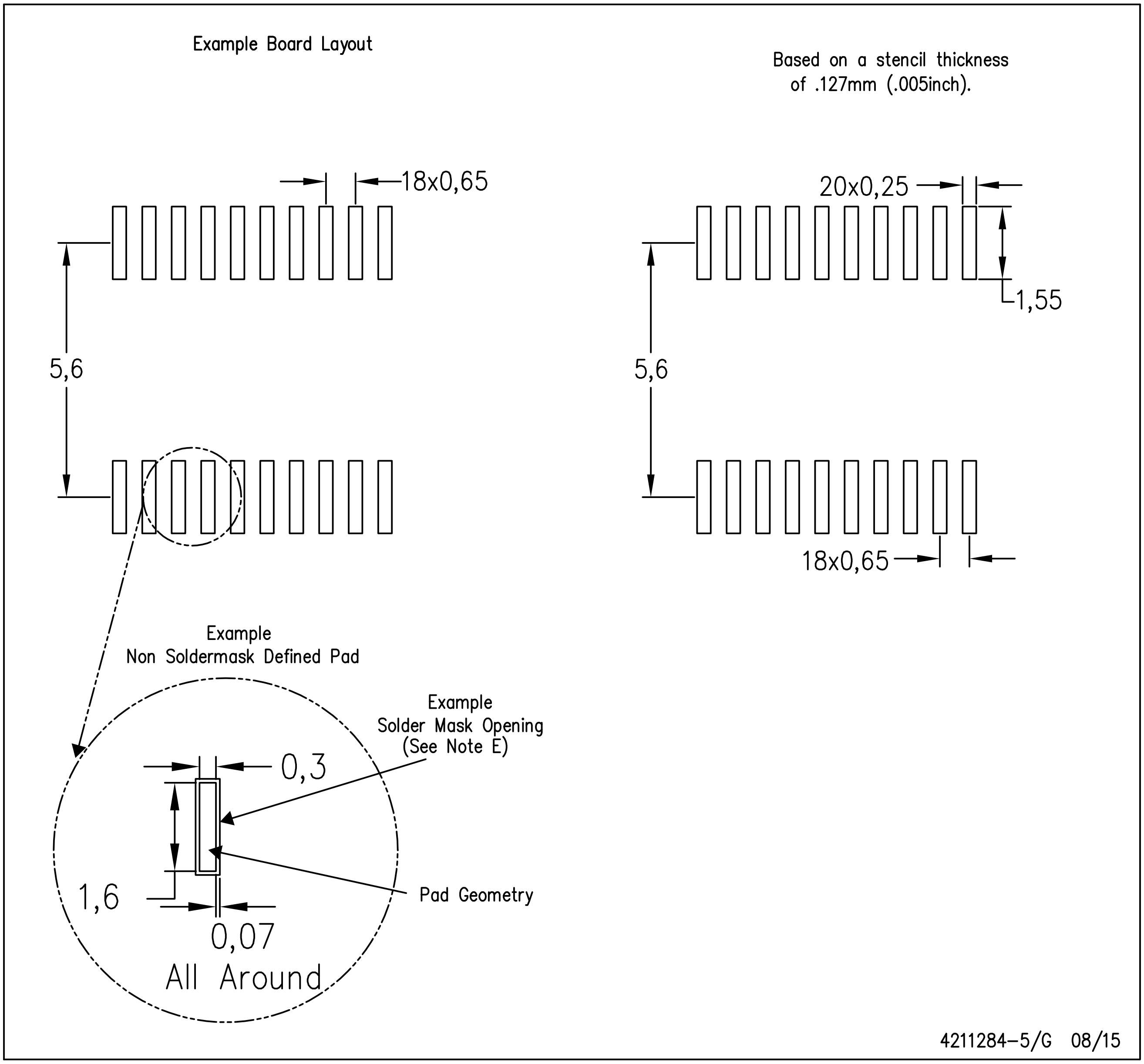
PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



4040064-5/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC-7351 is recommended for alternate design.

D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.

E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

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