# 适用于 2 节串联锂离子电池且具有自动电池平衡功能的 BQ29209-Q1 电压保护

## 1 特性

- 2 节串联电池二级保护
- 带外部使能控制的自动电量失衡校正
  - ±30mV 使能阈值，0mV 禁用阈值（典型值）
- 外部电容控制的延迟计时器
- 外部电阻控制的电量平衡电流
- 低功耗 $I_{CC}$ < 3µA（典型值）（$V_{CELL}$（总电压）< $V_{PROTECT}$）
- 内部电量平衡功能可处理高达 15mA 的电流
- 支持外部电量平衡模式
- 高精度过压保护：
  - ±25mV（$T_A$ = 0°C 至 60°C）
- 固定过压保护阈值：4.30V
- 小型 8 引脚 DRB 封装
- 符合汽车类 AEC Q100 2 级标准

## 2 应用

- 锂离子电池组二级保护
  - 紧急呼叫 (eCall)
  - 笔记本电脑
  - 电动工具
  - 便携式设备和仪器
  - 备用电池系统

## 3 说明

BQ29209-Q1 器件是一款用于 2 节串联锂离子电池组的二级过压保护 IC，具有高精度精密过压检测电路和自动电量失衡校正功能。

该 IC 将 2 节串联电池组中每节电池的电压与出厂设定的内部参考电压进行比较。如果任一电池达到过压状态，OUT 引脚由低电平转换为高电平状态。

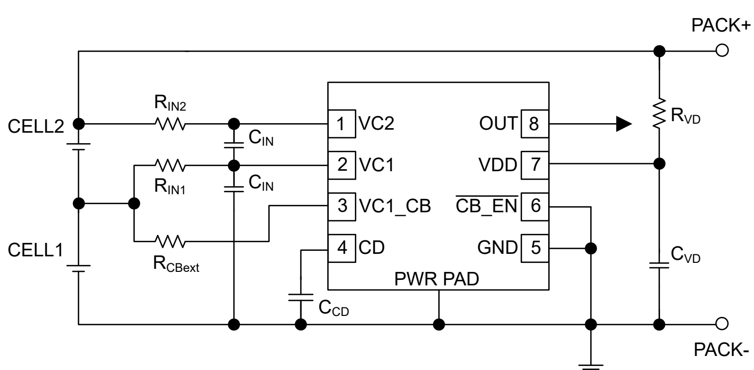
BQ29209-Q1 可执行基于电压的自动电量失衡校正。当电池电压与内部参考电压相差 30mV（标称值）或以上时，启动电量平衡；当电池电压与内部参考电压相差 0mV（标称值）时，停止电量平衡。电量平衡功能由 CB_EN 引脚使能和禁用。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| BQ29209-Q1 | VSON (8) | 3.00mm × 3.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



# 目录



## 4 修订历史记录

**Changes from Revision B (November 2018) to Revision C** — **Page**

- Added a clarification regarding operation if GND is not connected first in sequence ... 8

**Changes from Revision A (March 2016) to Revision B** — **Page**

- 已更改 更改了*简化原理图* 中的组件名称 ... 1
- Changed a component name in *Recommended Operating Conditions* ... 4
- Added the value of internal cell balancing switch resistances to *Electrical Characteristics* ... 5
- Changed resistor names ... 6
- Added Figure 5 to clarify the cell balancing description; updated the equations ... 9
- Changed values and component names in Figure 10 ... 12
- Changed component names and values used in the design example ... 12
- Changed external cell balancing figure, equations, and description ... 13

**Changes from Original (June 2015) to Revision A** — **Page**

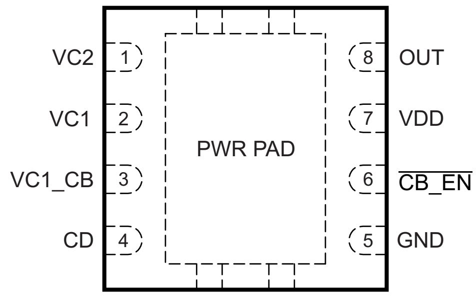
- 已更改 更改了电阻器 $R_{VD}$ 位置，向*简化原理图* 添加了 PACK+ 和 PACK- ... 1
- Deleted the Lead Temperature (soldering) from the *Absolute Maximum Ratings* table ... 3
- Changed resistor $R_{VD}$ location in Figure 10 ... 12
- Added title to Table 1 ... 12
- Changed resistor $R_{VD}$ location, added PACK+ and PACK– in Figure 12 ... 14

# 5 Device Options

| $T_A$ | PART NUMBER | OVP |
|---|---|---|
| –40°C to +105°C | BQ29209-Q1 | 4.3 V |

# 6 Pin Configuration and Functions

**DRB Package**
**8-Pin VSON**
**Top View**




### Pin Functions

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| $\overline{\text{CB\_EN}}$ | 6 | Cell balance enable |
| CD | 4 | Connection to external capacitor for programmable delay time |
| GND | 5 | Ground pin |
| OUT | 8 | Output |
| Thermal Pad | PWR PAD | GND pin to be connected to the PWRPAD on the printed circuit board for proper operation |
| VC1 | 2 | Sense voltage input for bottom cell |
| VC1_CB | 3 | Cell balance input for bottom cell |
| VC2 | 1 | Sense voltage input for top cell |
| VDD | 7 | Power supply |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

Over-operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage range, $V_{MAX}$ | VDD–GND | –0.3 | 16 | V |
| Input voltage range, $V_{IN}$ | VC2–GND, VC1–GND | –0.3 | 16 | V |
| | VC2–VC1, CD–GND | –0.3 | 8 | V |
| | $\overline{\text{CB\_EN}}$–GND | –0.3 | 16 | V |
| Output voltage range, $V_{OUT}$ | OUT–GND | –0.3 | 16 | V |
| Continuous total power dissipation, $P_{TOT}$ | | See *Thermal Information*. | | |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 (1) | | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins (VC2, CD, OUT, and GND) | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, VDD | | 4 | | 10 | V |
| Input voltage range | VC2–VC1, VC1–GND | 0 | | 5 | V |
| Delay time capacitance, $t_{d(CD)}$ | $C_{CD}$ (See Figure 10.) | | 0.1 | | µF |
| Voltage monitor filter resistance | $R_{IN}$ (See Figure 10.) | 100 | 1K | | Ω |
| Voltage monitor filter capacitance | $C_{IN}$ (See Figure 10.) | 0.01 | 0.1 | | µF |
| Supply voltage filter resistance | $R_{VD}$ (See Figure 10.) | | 100 | 1K | Ω |
| Supply voltage filter capacitance | $C_{VD}$ (See Figure 10.) | | 0.1 | | µF |
| Cell balance resistance | $R_{CBext}$ (See Figure 10 and *Protection (OUT) Timing*.) | 100 | | 4.7K | Ω |
| Operating ambient temperature range, $T_A$ | | –40 | | 105 | °C |

## 7.4 Thermal Information

| THERMAL METRIC (1) | | BQ29209-Q1 | UNIT |
|---|---|---|---|
| | | DRB | |
| | | 8 PINS | |
| $R_{θJA}$ | Junction-to-ambient thermal resistance | 50.5 | °C/W |
| $R_{θJC(top)}$ | Junction-to-case(top) thermal resistance | 25.1 | °C/W |
| $R_{θJB}$ | Junction-to-board thermal resistance | 19.3 | °C/W |
| $ψ_{JT}$ | Junction-to-top characterization parameter | 0.7 | °C/W |
| $ψ_{JB}$ | Junction-to-board characterization parameter | 18.9 | °C/W |
| $R_{θJC(bot)}$ | Junction-to-case(bottom) thermal resistance | 5.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

Typical values stated where $T_A$ = 25°C and VDD = 7.2 V. Minimum and maximum values stated where $T_A$ = –40°C to 105°C and VDD = 4 V to 10 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{PROTECT}$ | Overvoltage detection voltage | | | 4.3 | | V |
| $V_{HYS}$ | Overvoltage detection hysteresis | | 200 | 300 | 400 | mV |
| $V_{OA}$ | Overvoltage detection accuracy | $T_A$ = 25°C | –10 | | 10 | mV |
| $V_{OA\_DRIFT}$ | Overvoltage threshold temperature drift | $T_A$ = 0°C to 60°C | –0.4 | | 0.4 | mV°/C |
| | | $T_A$ = –40°C to 110°C | –0.6 | | 0.6 | |
| $X_{DELAY}$ | Overvoltage delay time scale factor | $T_A$ = 0°C to 60°C<br>Note: Does not include external capacitor variation. | 6 | 9 | 12 | s/µF |
| | | $T_A$ = –40°C to 110°C<br>Note: Does not include external capacitor variation. | 5.5 | 9 | 13.5 | |

## Electrical Characteristics (continued)

Typical values stated where $T_A$ = 25°C and VDD = 7.2 V. Minimum and maximum values stated where $T_A$ = –40°C to 105°C and VDD = 4 V to 10 V (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $X_{DELAY\_CTM}$ (1) | Overvoltage delay time scale factor in Customer Test Mode | | | 0.08 | | s/µF |
| $I_{CD(CHG)}$ | Overvoltage detection charging current | | | 150 | | nA |
| $I_{CD(DSG)}$ | Overvoltage detection discharging current | | | 60 | | µA |
| $V_{CD}$ | Overvoltage detection external capacitor comparator threshold | | | 1.2 | | V |
| $I_{CC}$ | Supply current | (VC2–VC1) = (VC1–GND) = 3.5 V (See Figure 8.) | | 3 | 6 | µA |
| $V_{OUT}$ | OUT pin drive voltage | (VC2–VC1) or (VC1–GND) > $V_{PROTECT}$, VDD = 10 V, $I_{OH}$ = 0 | 6 | 8.25 | 9.5 | V |
| | | (VC2–VC1) or (VC1–GND) = $V_{PROTECT}$, VDD = $V_{PROTECT}$, $I_{OH}$ = –100 µA, $T_A$ = 0°C to 60°C | 1.75 | 2.5 | | V |
| | | (VC2–VC1) and (VC1–GND) < $V_{PROTECT}$ , $I_{OL}$ = 100 µA, $T_A$ = 25°C | | | 200 | mV |
| | | (VC2–VC1) and (VC1–GND) < $V_{PROTECT}$ , $I_{OL}$ = 0 µA, $T_A$ = 25°C | | 0 | 10 | mV |
| | | VC2 = VC1 = VDD = 4 V, $I_{OL}$ = 100 µA | | | 200 | mV |
| $I_{OH}$ | High-level output current | OUT = 1.75 V, (VC2–VC1) or (VC1–GND) = $V_{PROTECT}$, VDD = $V_{PROTECT}$ to 10 V, $T_A$ = 0°C to 60°C | –100 | | | µA |
| $I_{OL}$ | Low-level output current | OUT = 0.05 V, (VC2–VC1) or (VC1–GND) < $V_{PROTECT}$, VDD = $V_{PROTECT}$ to 10 V, $T_A$ = 0°C to 60°C | 30 | | 85 | µA |
| $I_{OH\_ZV}$ | High-level short-circuit output current | OUT = 0 V, (VC2–VC1) = (VC1–GND) = $V_{PROTECT}$ VDD = 4 to 10 V | | | –8 | mA |
| $I_{IN}$ | Input current at VCx pins | Measured at VC1, (VC2–VC1) = (VC1–GND) = 3.5 V, $T_A$ = 0°C to 60°C (See Figure 8.) | –0.2 | | 0.2 | µA |
| | | Measured at VC2, (VC2–VC1) = (VC1–GND) = 3.5 V, $T_A$ = 0°C to 60°C (See Figure 8.) | | | 2.5 | µA |
| $V_{MM\_DET\_ON}$ | Cell mismatch detection threshold for turning ON | (VC2–VC1) versus (VC1–GND) and vice-versa when cell balancing is enabled. VC2 = VDD = 7.6 V | 17 | 30 | 45 | mV |
| $V_{MM\_DET\_OFF}$ | Cell mismatch detection threshold for turning OFF | Delta between (VC2–VC1) and (VC1–GND) when cell balancing is disabled. VC2 = VDD = 7.6 V | –9 | 0 | 9 | mV |
| $V_{CB\_EN\_ON}$ | Cell balance enable ON threshold | Active LOW pin at $\overline{CB\_EN}$ | | | 1 | V |
| $V_{CB\_EN\_OFF}$ | Cell balance enable OFF threshold | Active HIGH at $\overline{CB\_EN}$ | 2.2 | | | V |
| $I_{CB\_EN}$ | Cell balance enable ON input current | $\overline{CB\_EN}$ = GND (See Figure 9.) | | | 0.2 | µA |
| $R_{CB1int}$ | Internal cell balance switch resistance | $\overline{CB\_EN}$ = GND | | 300 | | Ω |
| $R_{CB2int}$ | Internal cell balance switch resistance | $\overline{CB\_EN}$ = GND | | 235 | | Ω |

(1) Specified by design. Not 100% tested in production.

## 7.6 Recommended Cell Balancing Configurations

Typical values stated where $T_A$ = 25°C and (VC2–VC1), (VC1–GND) = 3.8 V. Minimum and maximum values stated where $T_A$ = –40°C to 105°C, VDD = 4 V to 10 V, and (VC2–VC1), (VC1–GND) = 3 V to 4.2 V. All values assume recommended supply voltage filter resistance $R_{VD}$ of 100 Ω and 5% accurate or better cell balance resistor $R_{CBext}$.

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CB}$ | Cell balance input current | $R_{CBext}$ = 4700 Ω | 0.5 | 0.75 | 1 | mA |
| | | $R_{CBext}$ = 2200 Ω | 1 | 1.5 | 2 | |
| | | $R_{CBext}$ = 910 Ω | 2 | 3 | 4 | |
| | | $R_{CBext}$ = 560 Ω | 3 | 4.5 | 6 | |
| | | $R_{CBext}$ = 360 Ω | 3.5 | 6 | 8.5 | |
| | | $R_{CBext}$ = 240 Ω | 4 | 7.5 | 11 | |
| | | $R_{CBext}$ = 120 Ω | 5 | 10 | 15 | |

## 7.7 Typical Characteristics

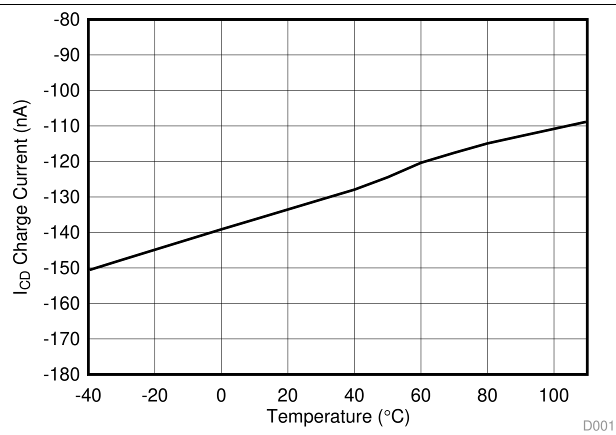



**Figure 1. $I_{CD}$ Charge Current**

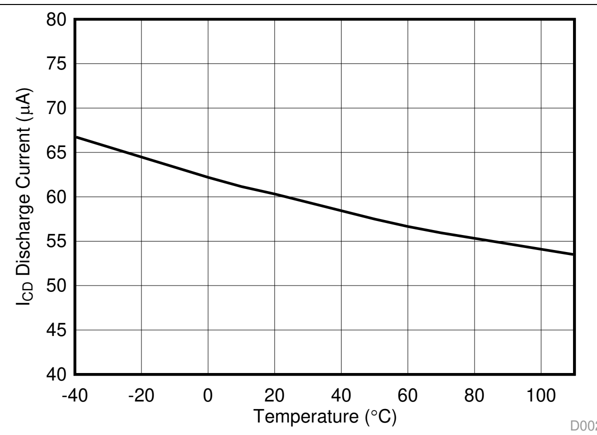



**Figure 2. $I_{CD}$ Discharge Current**

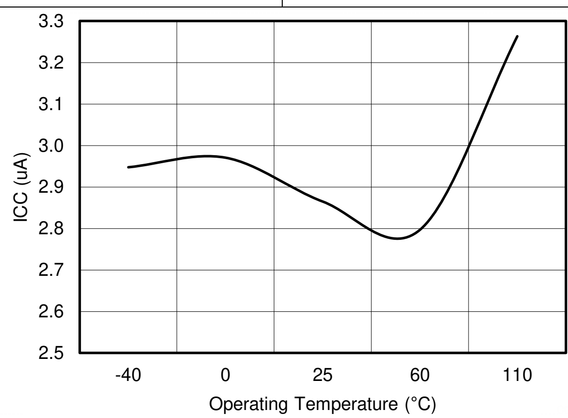



**Figure 3. Average ICC During Normal Operation Across Operational Temperature**

# 8 Detailed Description

## 8.1 Overview

The BQ29209-Q1 provides overvoltage protection and cell balancing for 2-series cell lithium-ion battery packs.

### 8.1.1 Voltage Protection

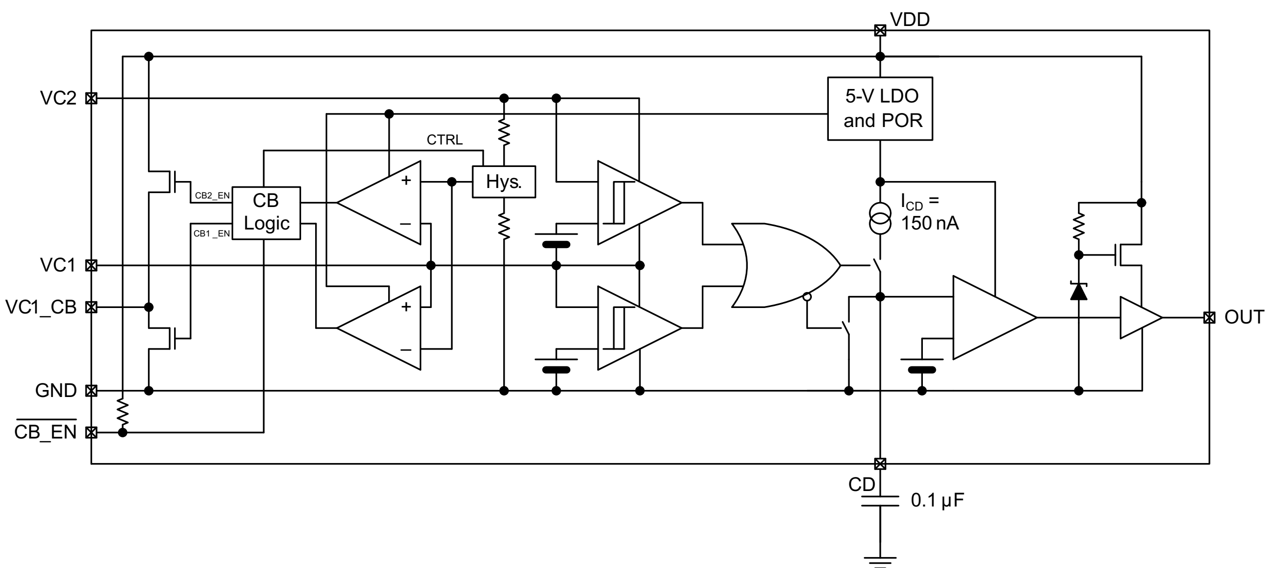
Each cell voltage is continuously compared to a factory configured internal reference threshold. If either cell reaches an overvoltage condition, the BQ29209-Q1 device starts a timer that provides a delay proportional to the capacitance on the CD pin. Upon expiration of the internal timer, the OUT pin changes from a low to high state.

### 8.1.2 Cell Balancing

If enabled, the BQ29209-Q1 performs automatic cell-balance correction where the two cells are automatically corrected for voltage imbalance by loading the cell with the higher voltage with a small balancing current. When the cells are measured to be equal within nominally 0 mV, the load current is removed. It will be re-applied if the imbalance exceeds nominally 30 mV. The cell mismatch correction circuitry is enabled by pulling the $\overline{\text{CB\_EN}}$ pin low, and disabled when $\overline{\text{CB\_EN}}$ is pulled to greater than 2.2 V, for example, VDD.

If the internal cell balancing current of up to 15 mA is insufficient, the BQ29209-Q1 may be configured via external circuitry to support much higher external cell balancing current.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Protection (OUT) Timing

Sizing the external capacitor is based on the desired delay time as follows:

$$C_{CD} = \frac{t_d}{X_{DELAY}}$$

Where $t_d$ is the desired delay time and $X_{DELAY}$ is the overvoltage delay time scale factor, expressed in seconds per microfarad. $X_{DELAY}$ is nominally 9 s/µF. For example, if a nominal delay of 3 seconds is desired, use a $C_{CD}$ capacitor that is 3 s / 9 s/µF = 0.33 µF.

The delay time is calculated as follows:

$$t_d = C_{CD} \times X_{DELAY}$$

## Feature Description (continued)

If the cell overvoltage condition is removed before the external capacitor reaches the reference voltage, the internal current source is disabled and an internal discharge block is employed to discharge the external capacitor down to 0 V. In this instance, the OUT pin remains in a low state.

### 8.3.2 Cell Voltage > $V_{PROTECT}$

When one or both of the cell voltages rises above $V_{PROTECT}$, the internal comparator is tripped, and the delay begins to count to $t_d$. If the input remains above $V_{PROTECT}$ for the duration of $t_d$, the BQ29209-Q1 output changes from a low to a high state, by means of an internal pull-up network, to a regulated voltage of no more than 9.5 V when $I_{OH}$ = 0 mA.

The external delay capacitor should charge up to no more than the internal LDO voltage (approximately 5 V typically), and will fully discharge in approximately under 100 ms when the overvoltage condition is removed.

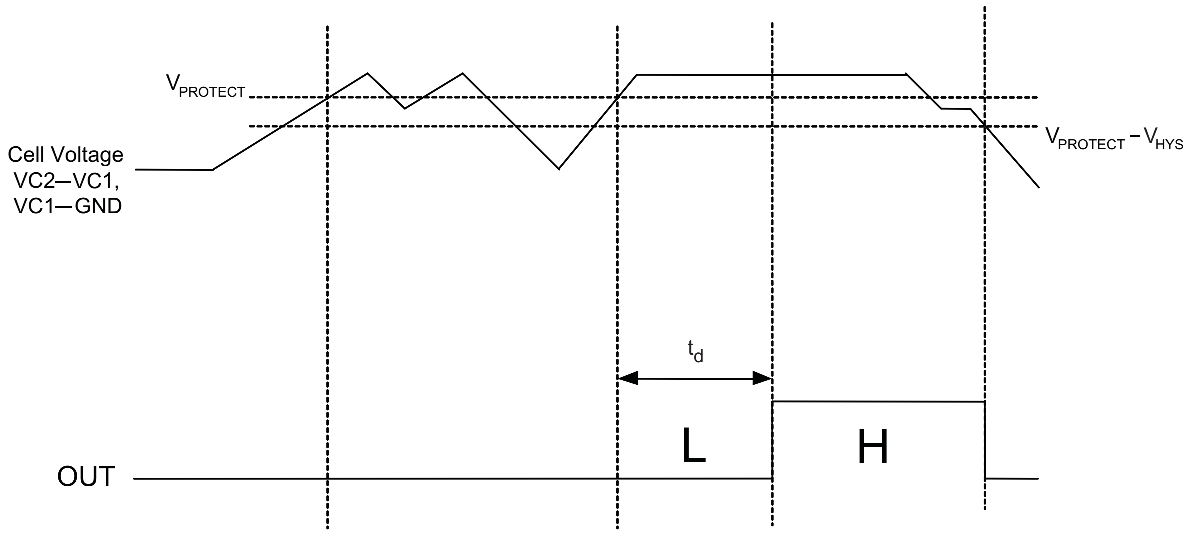



**Figure 4. Timing for Overvoltage Sensing**

### 8.3.3 Cell Connection Sequence

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**NOTE**

Before connecting the cells, populate the overvoltage delay timing capacitor, $C_{CD}$.

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The recommended cell connection sequence begins from the bottom of the stack, as follows:

1. GND
2. VC1
3. VC2

While not advised, connecting the cells in a sequence other than that described above does not result in errant activity on the OUT pin. For example:

1. GND
2. VC2 or VC1
3. Remaining VCx pin

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**NOTE**

Using any cell connection sequence that does not connect GND first may result in increased leakage current drawn by the VDD pin.

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## Feature Description (continued)

### 8.3.4 Cell Balance Enable Control

To avoid prematurely discharging the cells, it is recommended to turn off (pull high) the active-low Cell Balance Enable Control pin at lower state-of-charge (SOC) levels.

### 8.3.5 Cell Balance Configuration

The following cell balancing details relate to Figure 5.

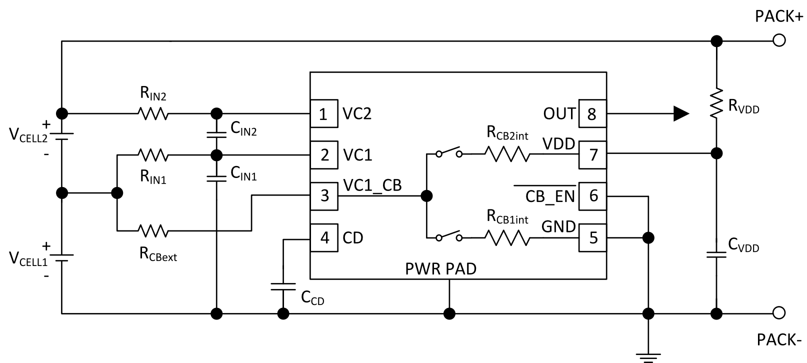



**Figure 5. Simplified Schematic for Cell Balancing Description**

The cell balancing current may be calculated as follows:

For Cell 1 balancing current, $I_{CB1}$:

$$I_{CB1} = \frac{V_{CELL1}}{R_{CBext} + R_{CB1int}} \tag{1}$$

For Cell 2 balancing current, $I_{CB2}$:

$$I_{CB2} = \frac{V_{CELL2}}{R_{CBext} + R_{CB2int} + R_{VDD}} \tag{2}$$

Where:

$R_{CBext}$ = resistor connected between the top of Cell 1 and the VC1_CB pin

$R_{IN1}$ = resistor connected between the top of Cell 1 and the VC1 pin

$R_{IN2}$ = resistor connected between the top of Cell 2 and the VC2 pin

$R_{VDD}$ = resistor connected between the top of Cell 2 and the VDD pin

### 8.3.6 Cell Imbalance Auto-Detection (Via Cell Voltage)

The $V_{MM\_DET\_ON}$ and $V_{MM\_DET\_OFF}$ specifications are calibrated where VDD = VC2 = 7.6 V and VC1 = 3.8 V. The recommended range of cell balancing is VC2 and VDD between 6.0 V and 8.4 V, and VC1 between 3 V and 4.2 V. Below VDD = 6 V, it is recommended to pull $\overline{\text{CB\_EN}}$ high to disable the cell balancing function.

## Feature Description (continued)

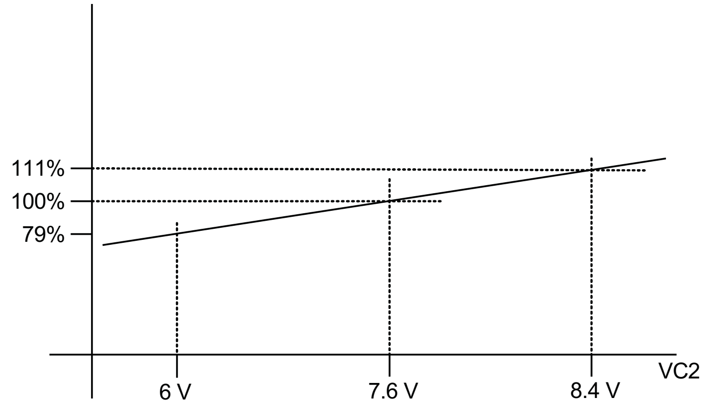



**Figure 6. $V_{MM\_DET\_ON}$ and $V_{MM\_DET\_OFF}$ Threshold**

### 8.3.7 Customer Test Mode

Customer Test Mode (CTM) helps to greatly reduce the overvoltage detection delay time and enable quicker customer production testing. This mode is intended for quick-pass board-level verification tests, and, as such, individual cell overvoltage levels may deviate slightly from the specifications ($V_{PROTECT}$, $V_{OA}$). If accurate overvoltage thresholds are to be tested, use the standard delay settings that are intended for normal use.

To enter CTM, VDD should be set to approximately 9.5 V higher than VC2. When CTM is entered, the device switches from the normal overvoltage delay time scale factor, $X_{DELAY}$, to a significantly reduced factor of approximately 0.08, thereby reducing the delay time during an overvoltage condition.

**CAUTION**

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into CTM. Also, avoid exceeding absolute maximum voltages for the individual cell voltages (VC1–GND) and (VC2–VC1). Stressing the pins beyond the rated limits may cause permanent damage to the device.

To exit CTM, power off the device and then power it back on.

## Feature Description (continued)

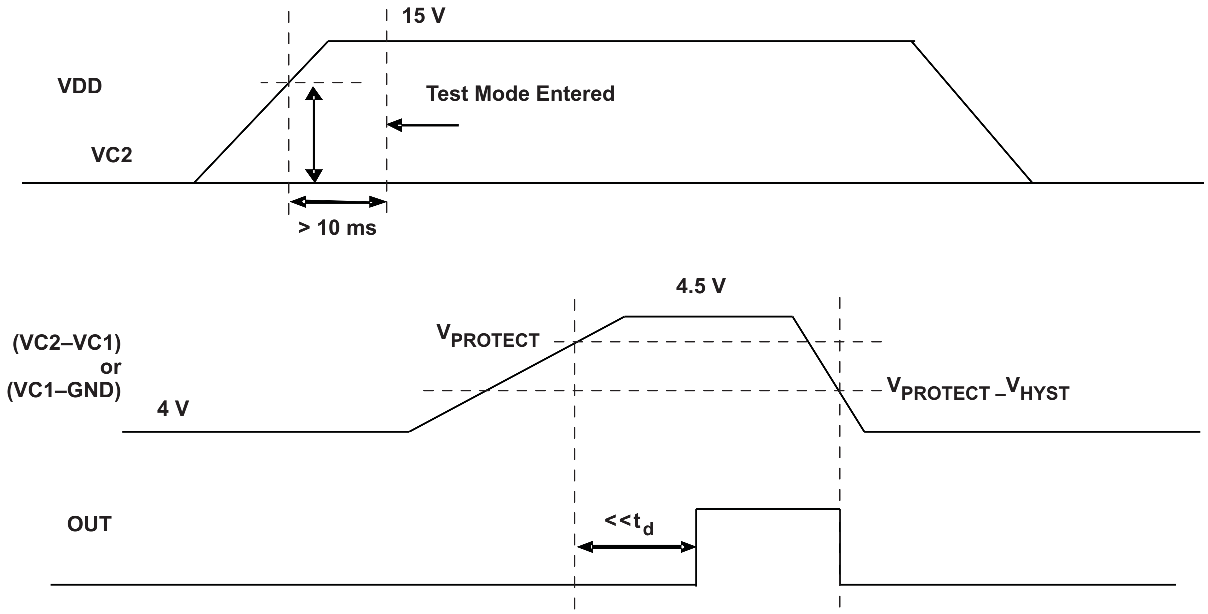



**Figure 7. Voltage Test Limits**

### 8.3.8 Test Conditions

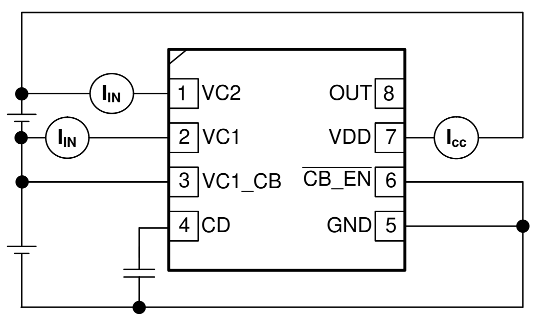



**Figure 8. $I_{CC}$, $I_{IN}$ Measurement**

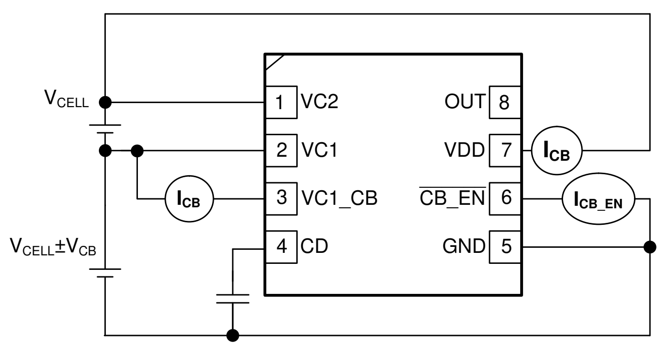



**Figure 9. $I_{CB}$ Measurement**

## 8.4 Device Functional Modes

This device monitors the voltage of the cells connected to the VCx pins and depending on these voltages and the overall battery voltage at VDD the device enters different operating modes.

### 8.4.1 NORMAL Mode

The device is operating in NORMAL mode when the cell voltage range is between the over-charge detection threshold ($V_{PROTECT}$) and the minimum supply voltage.

If this condition is satisfied, the device turns OFF the OUT pin.

### 8.4.2 PROTECTION Mode

The device is operating in PROTECTION mode when the cell over voltage protection feature has been triggered. See *Cell Voltage > $V_{PROTECT}$* for more details on this feature.

If this condition is satisfied, the device turns ON the OUT pin.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The BQ29209-Q1 is designed to be used in 2-series Li-Ion battery packs and with the option to include voltage-based cell balancing. The number of parallel cells or the overall capacity of the battery only affects the cell balancing circuit due to the level of potential imbalance that needs to be corrected.

## 9.2 Typical Applications

### 9.2.1 Battery Connection

Figure 10 shows the configuration for the 2-series cell battery connection with cell balancing enabled.

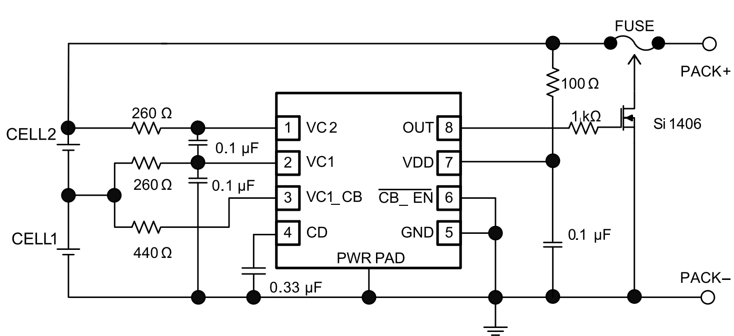



**Figure 10. 2-Series Cell Configuration**

#### *9.2.1.1 Design Requirements*

For this design example, use the parameters listed in Table 1.

## Typical Applications (continued)

**Table 1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE at $T_A$ = 25°C |
|---|---|
| Input voltage range | 4 V to 10 V |
| Overvoltage Protection (OVT) | 4.3 V |
| Overvoltage detection delay time | 3 s |
| Overvoltage detection delay timer capacitor | 0.33 µF |
| Cell Balancing Enabled | Yes |
| Cell Balancing Current, $I_{CB1}$ and $I_{CB2}$ | 5 mA (targeted at a nominal cell voltage of 3.8 V) |
| Cell Balancing Resistors, $R_{CBext}$, $R_{IN1}$, $R_{IN2}$ and $R_{VD}$ | $R_{CBext}$ = 440 Ω, $R_{IN1}$ = 260 Ω, $R_{IN2}$ = 260 Ω, $R_{VD}$ = 100 Ω |

#### *9.2.1.2 Detailed Design Procedure*

The BQ29209-Q1 has limited features but there are some key calculations to be made when selecting external component values.

- Calculate the required $C_{CD}$ capacitor value for the voltage protection delay time. Care should be taken to evaluate the tolerances of the capacitor and the BQ29209-Q1 to ensure system specifications are met.
- Calculate the cell balancing resistor values to provide a suitable level of balancing current that will, at a minimum, counter act an increase in imbalance during normal operation of the battery. Care should be taken to ensure any connectivity resistance is also considered as this will also reduce the balancing current level.

#### *9.2.1.3 Application Curve*

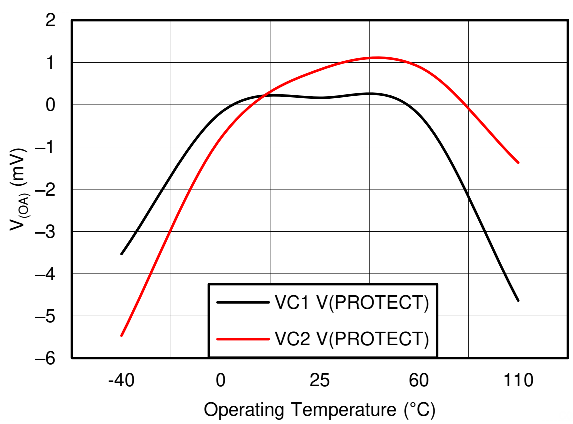



**Figure 11. Average $V_{PROTECT}$ Accuracy ($V_{OA}$) Across Operation Temperature**

## 9.3 System Example

### 9.3.1 External Cell Balancing

Higher cell balancing currents can be supported by means of a simple external network, as shown in Figure 12.

## System Example (continued)

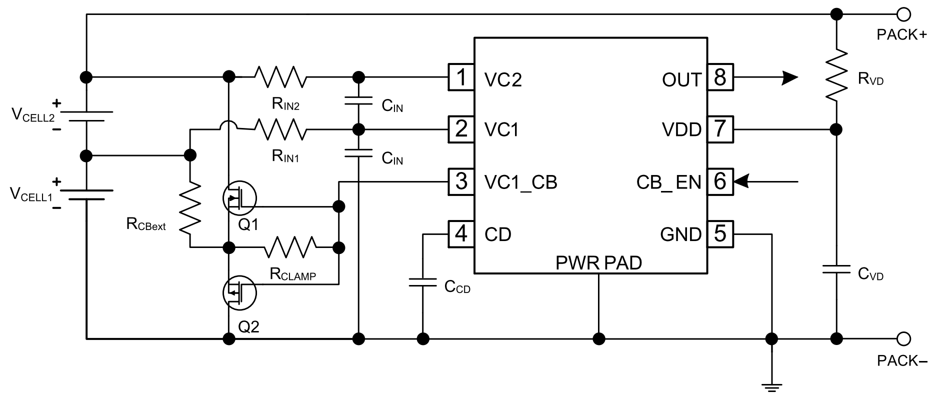



**Figure 12. External Cell Balancing Configuration**

The VC1_CB pin is tri-stated when cell balancing is disabled, is driven low by the internal logic to enable balancing on CELL1, and is driven high by the internal logic to enable balancing on CELL2. $R_{CLAMP}$ ensures that both Q1 and Q2 remain off when balancing is disabled, and should be sized above 2 kΩ to prevent excessive internal device current when the balancing network is activated. If $R_{CLAMP}$ is too small, then the gate-source voltage required to enable the external FETs cannot be achieved. $R_{CBext}$ determines the value of the balancing current, and is dependent on the voltage of the balanced cell and the specific Q1 and Q2 transistors used in the design (due to the transistors operating in saturation mode during balancing). The balancing currents (assuming the current through $R_{CLAMP}$ is not significant) are given as follows:

$$I_{CB1} = \frac{(V_{CELL1} - V_{SG\_Q2})}{R_{CBext}} \quad (3)$$

$$I_{CB2} = \frac{(V_{CELL2} - V_{GS\_Q1})}{R_{CBext}} \quad (4)$$

## 10 Power Supply Recommendations

The recommended power supply for this device is a maximum 10-V operation on the VDD input pin.

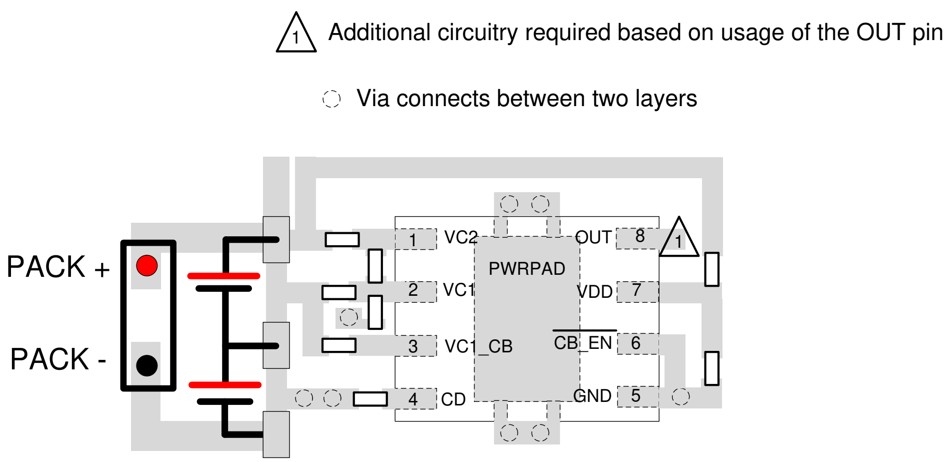
# 11 Layout

## 11.1 Layout Guidelines

The following are the recommended layout guidelines:

1. Ensure the input filters to the VC1 and VC2 pins are as close to the IC as possible to improve noise immunity.
2. If the OUT pin is used to control a high current path, for example: to blow a chemical fuse, then care should be taken to ensure the high current path creates minimal interference of the BQ29209-Q1 voltage sense inputs.
3. The input RC filter on the VDD pin should be close to the terminal of the IC.

## 11.2 Layout Example



# 12 器件和文档支持

## 12.1 接收文档更新通知

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## 12.2 社区资源

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## 12.3 商标

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## 12.4 静电放电警告

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## 12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。此信息是针对指定器件可提供的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ29209TDRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 209Q1 | Samples |
| BQ29209TDRBTQ1 | ACTIVE | SON | DRB | 8 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 209Q1 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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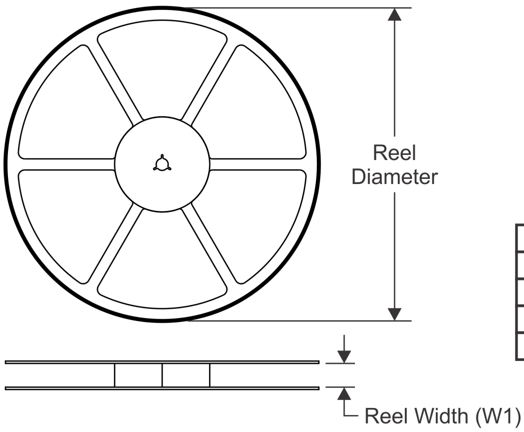
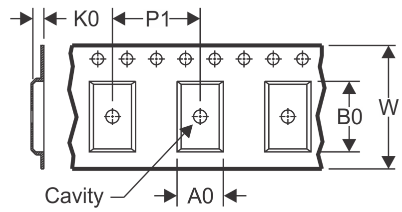
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

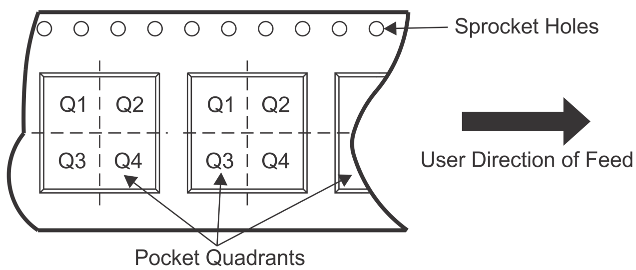



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

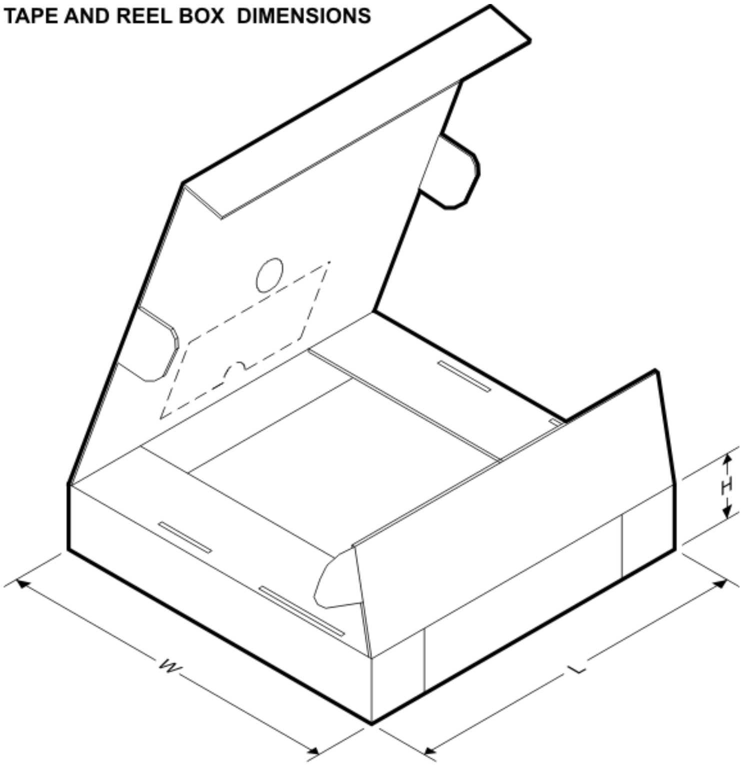
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ29209TDRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ29209TDRBTQ1 | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

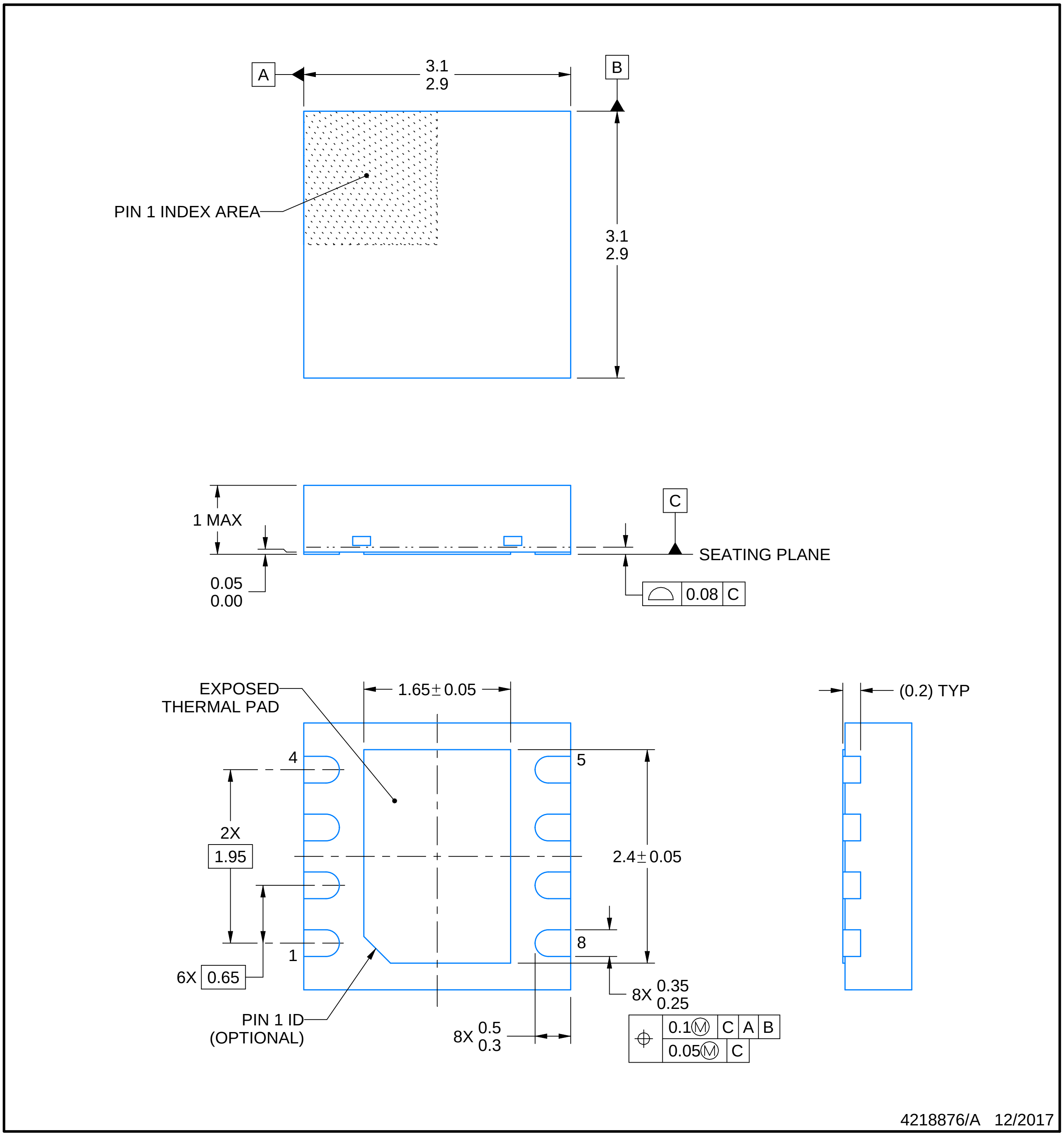
## TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

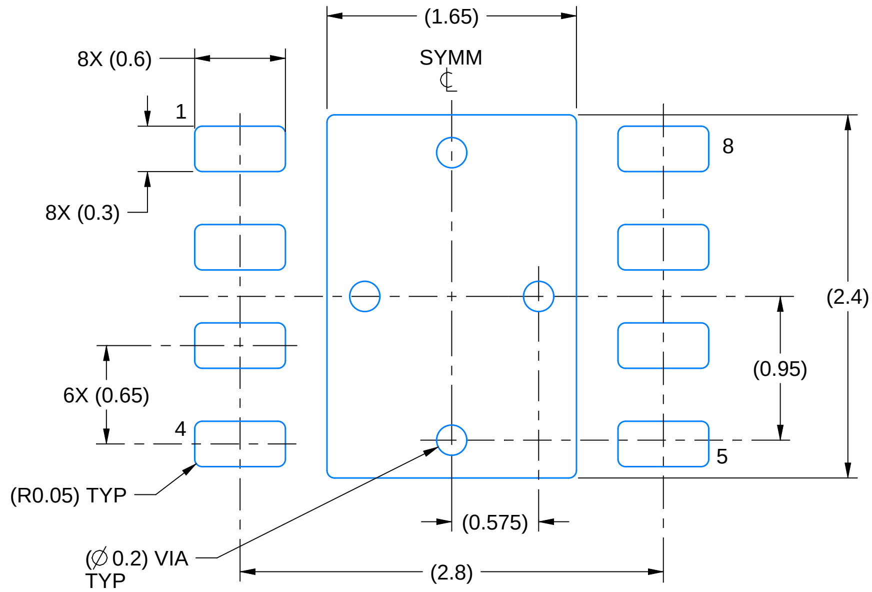
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ29209TDRBRQ1 | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ29209TDRBTQ1 | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

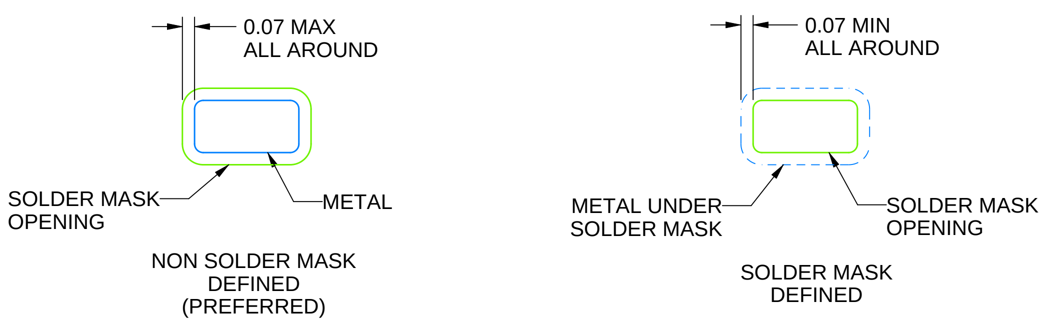



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X




SOLDER MASK DETAILS

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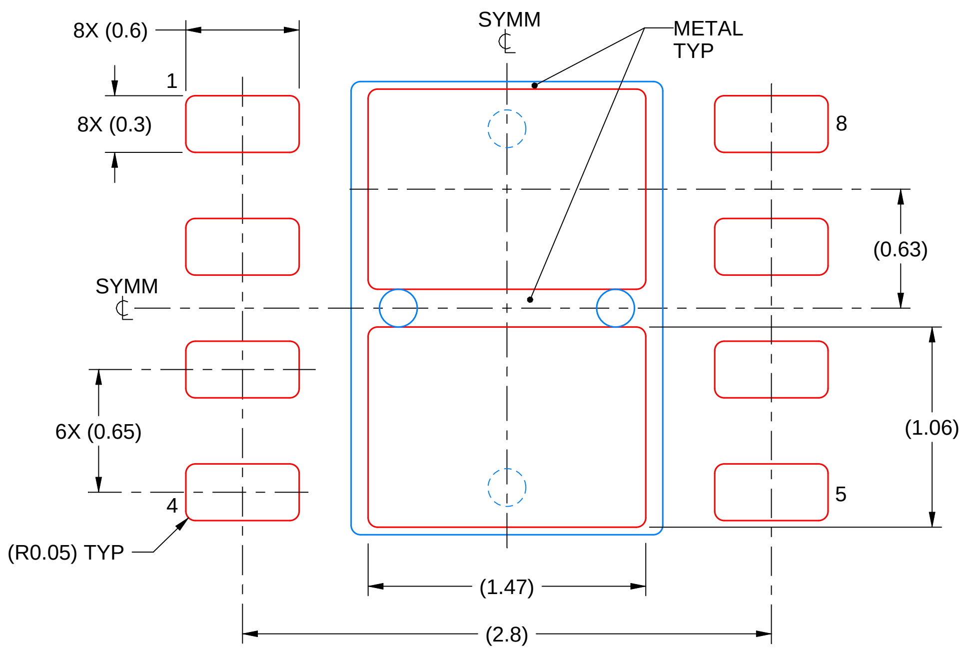
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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