# TMUX1119 5V、低泄漏电流、2:1 精密开关

## 1 特性

- 宽电源电压范围：1.08V 至 5.5V
- 低泄漏电流：3pA
- 低导通电阻：1.8Ω
- 低电荷注入：–6pC
- 工作温度范围：-40°C 至 +125°C
- 兼容 1.8V 逻辑电平
- 失效防护逻辑
- 轨至轨运行
- 双向信号路径
- 先断后合开关
- ESD 保护 HBM：2000V

## 2 应用

- 超声波扫描仪
- 患者监护和诊断
- 血糖监测仪
- 光学模块
- 光纤传输
- 远程无线电单元
- 数据采集系统
- 半导体测试设备
- 工厂自动化和工业控制
- 流量变送器
- 可编程逻辑控制器 (PLC)
- 模拟输入模块
- 电池测试

## 3 说明

TMUX1119是一种互补金属氧化物半导体 (CMOS) 单极双投 (2:1) 开关。1.08V 至 5.5V 的宽电源电压工作范围 可支持 医疗设备到工业系统的大量应用。该器件可在源极 (Sx) 和漏极 (D) 引脚上支持从 GND 到 $V_{DD}$ 范围的双向模拟和数字信号。所有逻辑输入均具有兼容 1.8V 逻辑电平的阈值，当器件在有效电源电压范围内运行时，这些阈值可确保 TTL 和 CMOS 逻辑兼容性。失效防护逻辑 电路允许在电源引脚之前的控制引脚上施加电压，从而保护器件免受潜在的损害。

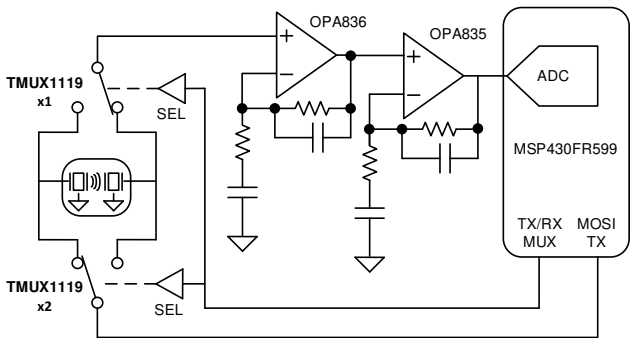
TMUX1119 是精密开关和多路复用器器件系列的一部分。这些器件具有非常低的导通和关断泄漏电流以及较低的电荷注入，因此可用于高精度测量 应用的高速串行链路的稳定性。3nA 的低电源电流和小型封装选项使其可用于便携式 应用的热管理优化而设计。中实现高功率密度、高效率和稳健性。

器件信息(1)

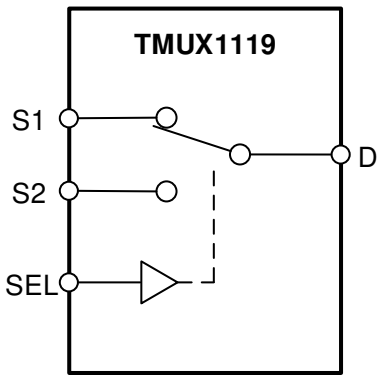
| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TMUX1119 | SC70 (6) | 2.00mm × 1.25mm |
| | SOT-23 (6)(2) | 2.90mm x 1.60mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。
(2) 产品预览

应用示例




方框图



# 目录



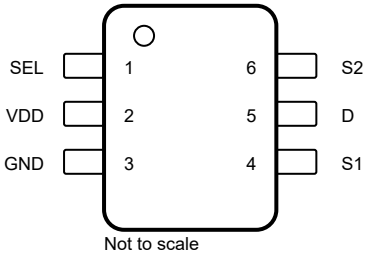
## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| Changes from Original (December 2018) to Revision A | Page |
|---|---|
| • 将数据表标题从“精密模拟多路复用器”更改为“精密开关” | 1 |
| • 更改了*应用* 列表 | 1 |
| • Changed Thermal Information for DCK package | 4 |

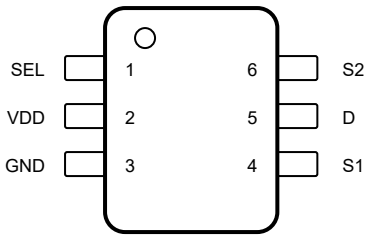
# 5 Pin Configuration and Functions

**DCK Package**
**6-Pin SC70**
**Top View**




Not to scale

**DBV Package**
**6-Pin SOT-23**
**Top View**

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Product Preview

**Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| SEL | 1 | I | Select pin: controls state of the switch according to 表 1. (Logic Low = S1 to D, Logic High = S2 to D) |
| VDD | 2 | P | Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between $V_{DD}$ and GND. |
| GND | 3 | P | Ground (0 V) reference |
| S1 | 4 | I/O | Source pin 1. Can be an input or output. |
| D | 5 | I/O | Drain pin. Can be an input or output. |
| S2 | 6 | I/O | Source pin 2. Can be an input or output. |

(1) I = input, O = output, I/O = input and output, P = power

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | –0.5 | 6 | V |
| $V_{SEL}$ or $V_{EN}$ | Logic control input pin voltage (SEL) | –0.5 | 6 | V |
| $I_{SEL}$ or $I_{EN}$ | Logic control input pin current (SEL) | –30 | 30 | mA |
| $V_S$ or $V_D$ | Source or drain voltage (Sx, D) | –0.5 | $V_{DD}$+0.5 | V |
| $I_S$ or $I_{D\ (CONT)}$ | Source or drain continuous current (Sx, D) | –30 | 30 | mA |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |
| $T_J$ | Junction temperature | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.08 | | 5.5 | V |
| $V_S$ or $V_D$ | Signal path input/output voltage (source or drain pin) (Sx, D) | 0 | | $V_{DD}$ | V |
| $V_{SEL}$ | Logic control input pin voltage (SEL) | 0 | | 5.5 | V |
| $T_A$ | Ambient temperature | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TMUX1119 SC70 (DCK) 6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 243.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 206.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 128.3 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 107.8 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 128.0 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics ($V_{DD}$ = 5 V ±10 %)

at $T_A$ = 25°C, $V_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to On-Resistance | 25°C | | 1.8 | 4 | Ω |
| | | | –40°C to +85°C | | | 4.5 | Ω |
| | | | –40°C to +125°C | | | 4.9 | Ω |
| $\Delta R_{ON}$ | On-resistance matching between channels | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to On-Resistance | 25°C | | 0.13 | | Ω |
| | | | –40°C to +85°C | | | 0.4 | Ω |
| | | | –40°C to +125°C | | | 0.5 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to On-Resistance | 25°C | | 0.85 | | Ω |
| | | | –40°C to +85°C | | | 1.4 | Ω |
| | | | –40°C to +125°C | | | 1.6 | Ω |
| $I_{S(OFF)}$ | Source off leakage current (1) | $V_{DD}$ = 5 V<br>Switch Off<br>$V_D$ = 4.5 V / 1.5 V<br>$V_S$ = 1.5 V / 4.5 V<br>Refer to Off-Leakage Current | 25°C | –0.08 | ±0.005 | 0.08 | nA |
| | | | –40°C to +85°C | –0.3 | | 0.3 | nA |
| | | | –40°C to +125°C | –0.9 | | 0.9 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | Channel on leakage current | $V_{DD}$ = 5 V<br>Switch On<br>$V_D$ = $V_S$ = 2.5 V<br>Refer to On-Leakage Current | 25°C | –0.025 | ±0.003 | 0.025 | nA |
| | | | –40°C to +85°C | –0.3 | | 0.3 | nA |
| | | | –40°C to +125°C | –0.95 | | 0.95 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | Channel on leakage current | $V_{DD}$ = 5 V<br>Switch On<br>$V_D$ = $V_S$ = 4.5 V / 1.5 V<br>Refer to On-Leakage Current | 25°C | –0.1 | ±0.01 | 0.1 | nA |
| | | | –40°C to +85°C | –0.35 | | 0.35 | nA |
| | | | –40°C to +125°C | –2 | | 2 | nA |
| **LOGIC INPUTS (SEL)** | | | | | | | |
| $V_{IH}$ | Input logic high | | –40°C to +125°C | 1.49 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | –40°C to +125°C | 0 | | 0.87 | V |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | 25°C | | ±0.005 | | µA |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | –40°C to +125°C | | | ±0.05 | µA |
| $C_{IN}$ | Logic input capacitance | | 25°C | | 1 | | pF |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | | 2 | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | Logic inputs = 0 V or 5.5 V | 25°C | | 0.003 | | µA |
| | | | –40°C to +125°C | | | 1 | µA |

(1) When $V_S$ is 4.5 V, $V_D$ is 1.5 V, and vice versa.

## Electrical Characteristics ($V_{DD}$ = 5 V ±10 %) (continued)

at $T_A$ = 25°C, $V_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $t_{TRAN}$ | Switching time between channels | $V_S$ = 3 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to Transition Time | 25°C | | 12 | | ns |
| | | | –40°C to +85°C | | | 18 | ns |
| | | | –40°C to +125°C | | | 19 | ns |
| $t_{OPEN}$ (BBM) | Break before make time | $V_S$ = 3 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to Break-Before-Make | 25°C | | 8 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $Q_C$ | Charge Injection | $V_D$ = 1 V<br>$R_S$ = 0 Ω, $C_L$ = 1 nF<br>Refer to Charge Injection | 25°C | | –6 | | pC |
| $O_{ISO}$ | Off Isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to Off Isolation | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to Off Isolation | 25°C | | –45 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to Crosstalk | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to Crosstalk | 25°C | | –45 | | dB |
| BW | Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>Refer to Bandwidth | 25°C | | 250 | | MHz |
| $C_{SOFF}$ | Source off capacitance | f = 1 MHz | 25°C | | 6 | | pF |
| $C_{SON}$<br>$C_{DON}$ | On capacitance | f = 1 MHz | 25°C | | 20 | | pF |

## 6.6 Electrical Characteristics ($V_{DD}$ = 3.3 V ±10 %)

at $T_A$ = 25°C, $V_{DD}$ = 3.3 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to On-Resistance | 25°C | | 3.7 | 8.8 | Ω |
| | | | –40°C to +85°C | | | 9.5 | Ω |
| | | | –40°C to +125°C | | | 9.8 | Ω |
| $\Delta R_{ON}$ | On-resistance matching between channels | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to On-Resistance | 25°C | | 0.13 | | Ω |
| | | | –40°C to +85°C | | | 0.4 | Ω |
| | | | –40°C to +125°C | | | 0.5 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to On-Resistance | 25°C | | 1.9 | | Ω |
| | | | –40°C to +85°C | | 2 | | Ω |
| | | | –40°C to +125°C | | 2.2 | | Ω |
| $I_{S(OFF)}$ | Source off leakage current (1) | $V_{DD}$ = 3.3 V<br>Switch Off<br>$V_D$ = 3 V / 1 V<br>$V_S$ = 1 V / 3 V<br>Refer to Off-Leakage Current | 25°C | –0.05 | ±0.001 | 0.05 | nA |
| | | | –40°C to +85°C | –0.1 | | 0.1 | nA |
| | | | –40°C to +125°C | –0.5 | | 0.5 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | Channel on leakage current | $V_{DD}$ = 3.3 V<br>Switch On<br>$V_D$ = $V_S$ = 3 V / 1 V<br>Refer to On-Leakage Current | 25°C | –0.1 | ±0.005 | 0.1 | nA |
| | | | –40°C to +85°C | –0.35 | | 0.35 | nA |
| | | | –40°C to +125°C | –2 | | 2 | nA |
| **LOGIC INPUTS (SEL)** | | | | | | | |
| $V_{IH}$ | Input logic high | | –40°C to +125°C | 1.35 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | –40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | 25°C | | ±0.005 | | µA |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | -40°C to 125°C | | | ±0.05 | µA |
| $C_{IN}$ | Logic input capacitance | | 25°C | | 1 | | pF |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | | 2 | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | Logic inputs = 0 V or 5.5 V | 25°C | | 0.003 | | µA |
| | | | –40°C to +125°C | | | 0.8 | µA |

(1) When $V_S$ is 3 V, $V_D$ is 1 V, and vice versa.

## Electrical Characteristics ($V_{DD}$ = 3.3 V ±10 %) (continued)

at $T_A$ = 25°C, $V_{DD}$ = 3.3 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $t_{TRAN}$ | Switching time between channels | $V_S$ = 2 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to Transition Time | 25°C | | 14 | | ns |
| | | | –40°C to +85°C | | | 20 | ns |
| | | | –40°C to +125°C | | | 21 | ns |
| $t_{OPEN}$ (BBM) | Break before make time | $V_S$ = 2 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to Break-Before-Make | 25°C | | 9 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $Q_C$ | Charge Injection | $V_D$ = 1 V<br>$R_S$ = 0 Ω, $C_L$ = 1 nF<br>Refer to Charge Injection | 25°C | | –6 | | pC |
| $O_{ISO}$ | Off Isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to Off Isolation | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to Off Isolation | 25°C | | –45 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to Crosstalk | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to Crosstalk | 25°C | | –45 | | dB |
| BW | Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>Refer to Bandwidth | 25°C | | 250 | | MHz |
| $C_{SOFF}$ | Source off capacitance | f = 1 MHz | 25°C | | 6 | | pF |
| $C_{SON}$<br>$C_{DON}$ | On capacitance | f = 1 MHz | 25°C | | 20 | | pF |

## 6.7 Electrical Characteristics ($V_{DD}$ = 1.8 V ±10 %)

at $T_A$ = 25°C, $V_{DD}$ = 1.8 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to On-Resistance | 25°C | | 40 | | Ω |
| | | | –40°C to +85°C | | | 80 | Ω |
| | | | –40°C to +125°C | | | 80 | Ω |
| $\Delta R_{ON}$ | On-resistance matching between channels | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to On-Resistance | 25°C | | 0.4 | | Ω |
| | | | –40°C to +85°C | | | 1.5 | Ω |
| | | | –40°C to +125°C | | | 1.5 | Ω |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 1.98 V<br>Switch Off<br>$V_D$ = 1.62 V / 1 V<br>$V_S$ = 1 V / 1.62 V<br>Refer to Off-Leakage Current | 25°C | –0.05 | ±0.003 | 0.05 | nA |
| | | | –40°C to +85°C | –0.1 | | 0.1 | nA |
| | | | –40°C to +125°C | –0.5 | | 0.5 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | Channel on leakage current | $V_{DD}$ = 1.98 V<br>Switch On<br>$V_D$ = $V_S$ = 1.62 V / 1 V<br>Refer to On-Leakage Current | 25°C | –0.1 | ±0.005 | 0.1 | nA |
| | | | –40°C to +85°C | –0.5 | | 0.5 | nA |
| | | | –40°C to +125°C | –2 | | 2 | nA |
| **LOGIC INPUTS (SEL)** | | | | | | | |
| $V_{IH}$ | Input logic high | | –40°C to +125°C | 1.07 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | –40°C to +125°C | 0 | | 0.68 | V |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | 25°C | | ±0.005 | | µA |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | –40°C to +125°C | | | ±0.05 | µA |
| $C_{IN}$ | Logic input capacitance | | 25°C | | 1 | | pF |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | | 2 | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | Logic inputs = 0 V or 5.5 V | 25°C | | 0.001 | | µA |
| | | | –40°C to +125°C | | | 0.85 | µA |

(1) When $V_S$ is 1.62 V, $V_D$ is 1 V, and vice versa.

## Electrical Characteristics ($V_{DD}$ = 1.8 V ±10 %) (continued)

at $T_A$ = 25°C, $V_{DD}$ = 1.8 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $t_{TRAN}$ | Transition time between channels | $V_S$ = 1 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to Transition Time | 25°C | | 28 | | ns |
| | | | –40°C to +85°C | | | 44 | ns |
| | | | –40°C to +125°C | | | 44 | ns |
| $t_{OPEN}$ (BBM) | Break before make time | $V_S$ = 1 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to Break-Before-Make | 25°C | | 16 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $Q_C$ | Charge Injection | $V_D$ = 1 V<br>$R_S$ = 0 Ω, $C_L$ = 1 nF<br>Refer to Charge Injection | 25°C | | –3 | | pC |
| $O_{ISO}$ | Off Isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to Off Isolation | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to Off Isolation | 25°C | | –45 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to Crosstalk | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to Crosstalk | 25°C | | –45 | | dB |
| BW | Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF | 25°C | | 250 | | MHz |
| $C_{SOFF}$ | Source off capacitance | f = 1 MHz | 25°C | | 6 | | pF |
| $C_{SON}$<br>$C_{DON}$ | On capacitance | f = 1 MHz | 25°C | | 20 | | pF |

## 6.8 Electrical Characteristics ($V_{DD}$ = 1.2 V ±10 %)

at $T_A$ = 25°C, $V_{DD}$ = 1.2 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to On-Resistance | 25°C | | 70 | | Ω |
| | | | –40°C to +85°C | | | 105 | Ω |
| | | | –40°C to +125°C | | | 105 | Ω |
| $\Delta R_{ON}$ | On-resistance matching between channels | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to On-Resistance | 25°C | | 0.4 | | Ω |
| | | | –40°C to +85°C | | | 1.5 | Ω |
| | | | –40°C to +125°C | | | 1.5 | Ω |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 1.32 V<br>Switch Off<br>$V_D$ = 1 V / 0.8 V<br>$V_S$ = 0.8 V / 1 V<br>Refer to Off-Leakage Current | 25°C | –0.05 | ±0.003 | 0.05 | nA |
| | | | –40°C to +85°C | –0.1 | | 0.1 | nA |
| | | | –40°C to +125°C | –0.5 | | 0.5 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | Channel on leakage current | $V_{DD}$ = 1.32 V<br>Switch On<br>$V_D$ = $V_S$ = 1 V / 0.8 V<br>Refer to On-Leakage Current | 25°C | –0.1 | ±0.005 | 0.1 | nA |
| | | | –40°C to +85°C | –0.5 | | 0.5 | nA |
| | | | –40°C to +125°C | –2 | | 2 | nA |
| **LOGIC INPUTS (SEL)** | | | | | | | |
| $V_{IH}$ | Input logic high | | –40°C to +125°C | 0.96 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | –40°C to +125°C | 0 | | 0.36 | V |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | 25°C | | ±0.005 | | µA |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | –40°C to +125°C | | | ±0.05 | µA |
| $C_{IN}$ | Logic input capacitance | | 25°C | | 1 | | pF |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | | 2 | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | Logic inputs = 0 V or 5.5 V | 25°C | | 0.003 | | µA |
| | | | –40°C to +125°C | | | 0.7 | µA |

(1) When $V_S$ is 1 V, $V_D$ is 0.8 V, and vice versa.

## Electrical Characteristics ($V_{DD}$ = 1.2 V ±10 %) (continued)

at $T_A$ = 25°C, $V_{DD}$ = 1.2 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $t_{TRAN}$ | Transition time between channels | $V_S$ = 1 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to Transition Time | 25°C | | 55 | | ns |
| | | | –40°C to +85°C | | | 190 | ns |
| | | | –40°C to +125°C | | | 190 | ns |
| $t_{OPEN}$ (BBM) | Break before make time | $V_S$ = 1 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to Break-Before-Make | 25°C | | 28 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $Q_C$ | Charge Injection | $V_D$ = 1 V<br>$R_S$ = 0 Ω, $C_L$ = 1 nF<br>Refer to Charge Injection | 25°C | | –2 | | pC |
| $O_{ISO}$ | Off Isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to Off Isolation | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to Off Isolation | 25°C | | –45 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to Crosstalk | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to Crosstalk | 25°C | | –45 | | dB |
| BW | Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF | 25°C | | 250 | | MHz |
| $C_{SOFF}$ | Source off capacitance | f = 1 MHz | 25°C | | 6 | | pF |
| $C_{SON}$<br>$C_{DON}$ | On capacitance | f = 1 MHz | 25°C | | 20 | | pF |

## 6.9 Typical Characteristics

at $T_A$ = 25°C, $V_{DD}$ = 5 V (unless otherwise noted)

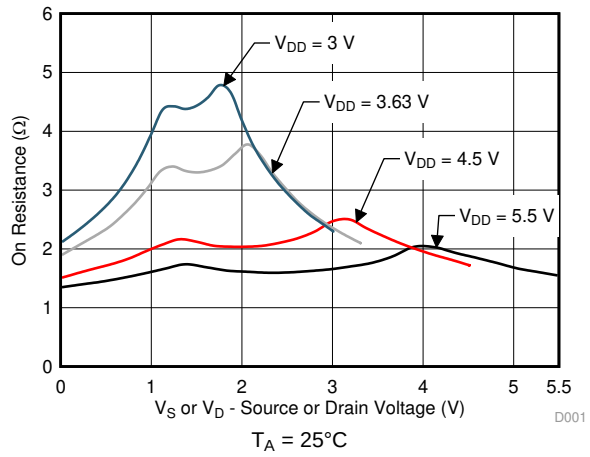



**图 1. On-Resistance vs Source or Drain Voltage**

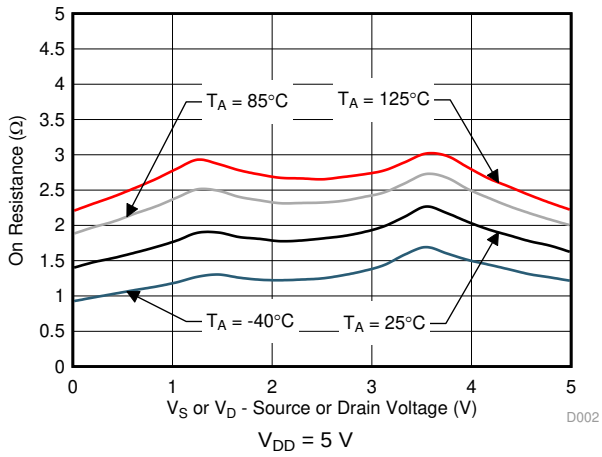



**图 2. On-Resistance vs Temperature**

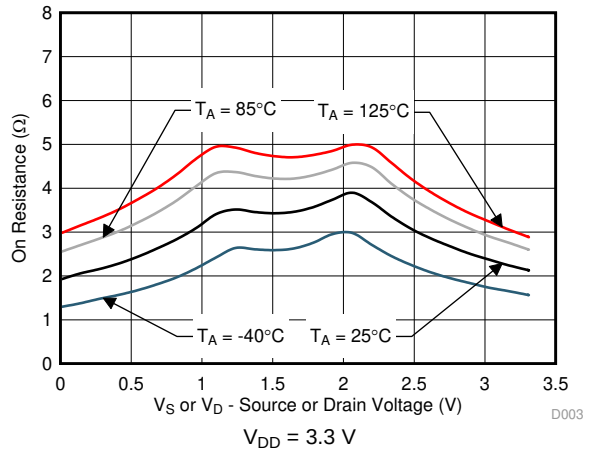



**图 3. On-Resistance vs Temperature**

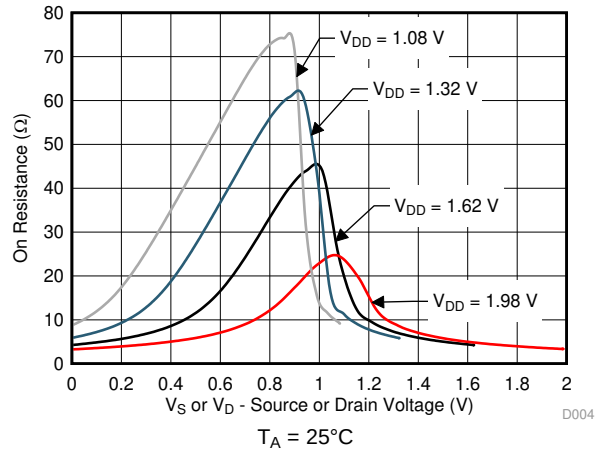



**图 4. On-Resistance vs Source or Drain Voltage**

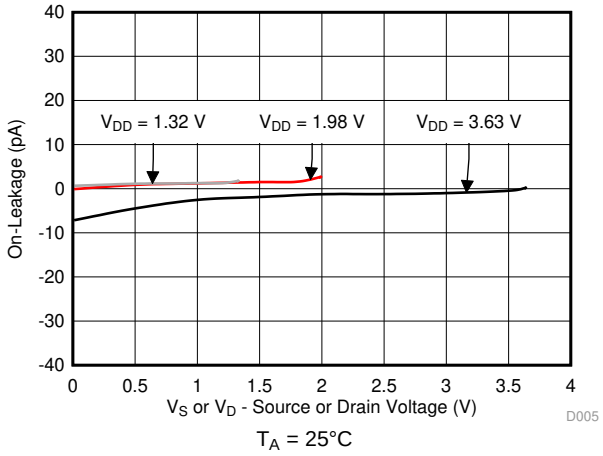



**图 5. On-Leakage vs Source or Drain Voltage**

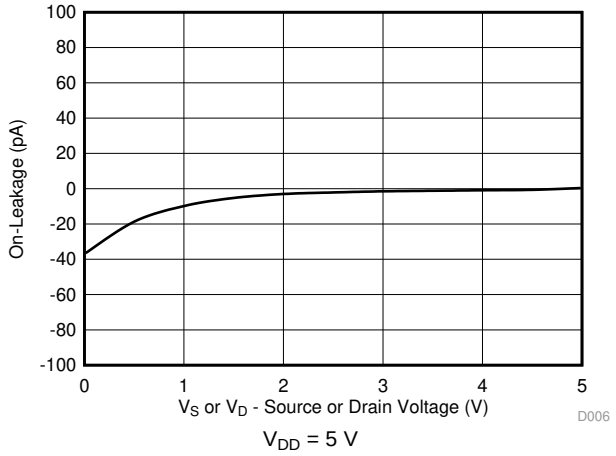
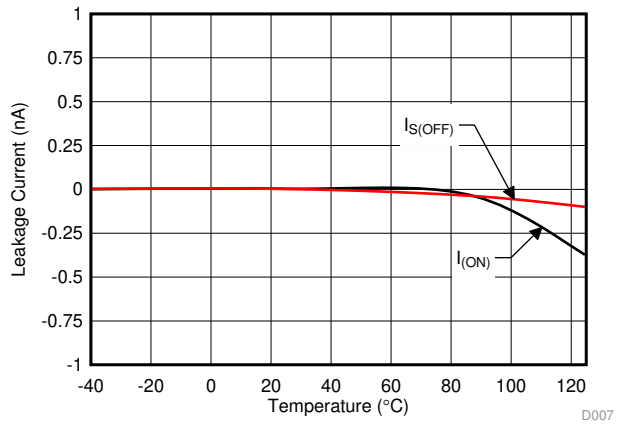


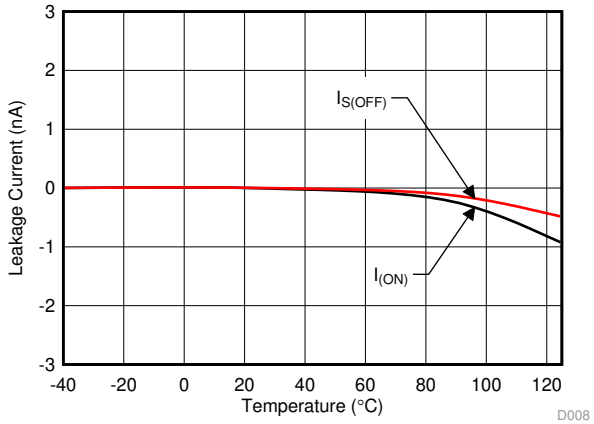

**图 6. On-Leakage vs Source or Drain Voltage**

## Typical Characteristics (接下页)



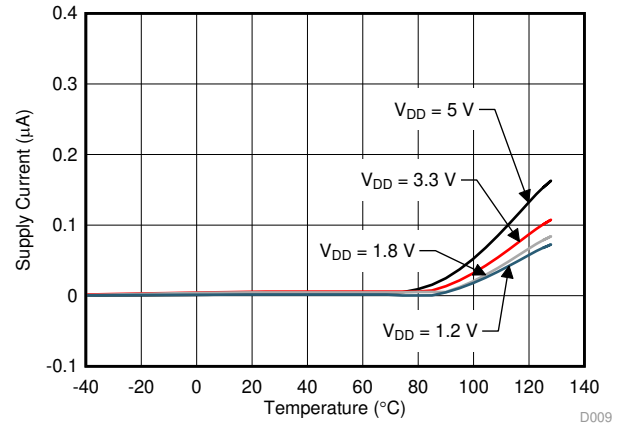

$V_{DD}$ = 3.3 V

**图 7. Leakage Current vs Temperature**



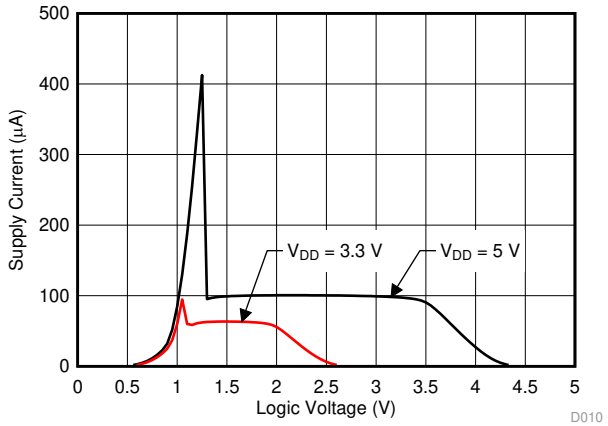

$V_{DD}$ = 5 V

**图 8. Leakage Current vs Temperature**



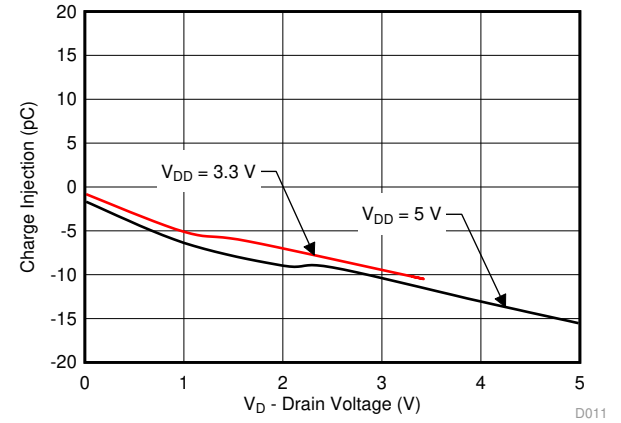

$V_{SEL}$ = 5.5 V

**图 9. Supply Current vs Temperature**



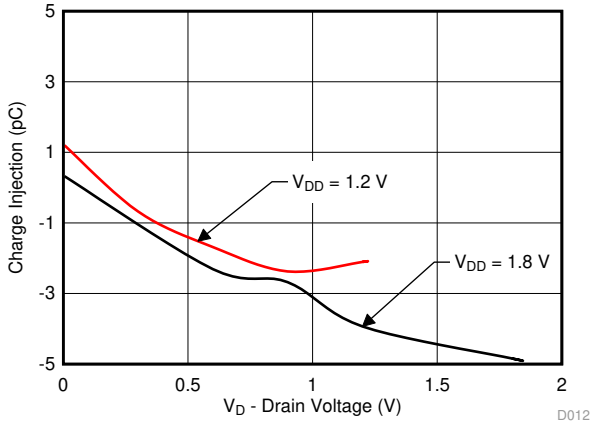

$T_A$ = 25°C

**图 10. Supply Current vs Logic Voltage**




$T_A$ = -40°C to 125°C

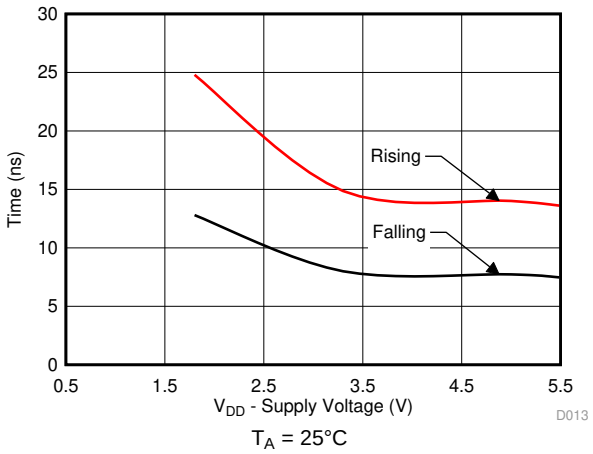
**图 11. Charge Injection vs Drain Voltage**




$T_A$ = -40°C to 125°C

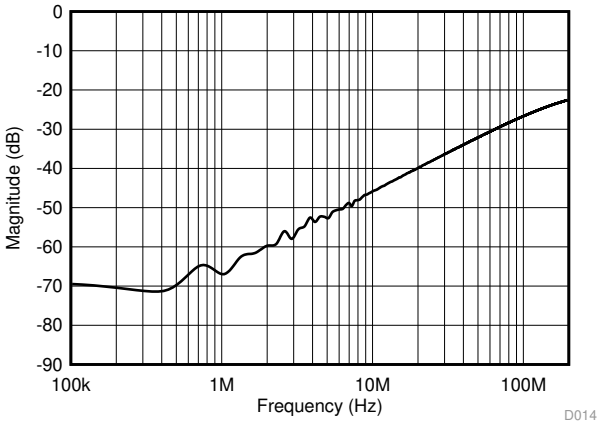
**图 12. Charge Injection vs Drain Voltage**

## Typical Characteristics (接下页)



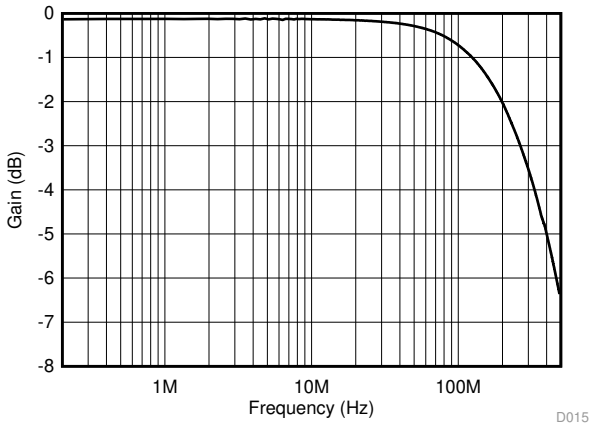

$T_A$ = 25°C

**图 13. Output $T_{TRANSITION}$ vs Supply Voltage**




$T_A$ = 25°C

**图 14. Xtalk and Off-Isolation vs Frequency**




$T_A$ = 25°C

**图 15. On Response vs Frequency**

# 7 Parameter Measurement Information

## 7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol $R_{ON}$ is used to denote on-resistance. The measurement setup used to measure $R_{ON}$ is shown in 图 16. Voltage (V) and current ($I_{SD}$) are measured using this setup, and $R_{ON}$ is computed with $R_{ON} = V / I_{SD}$:

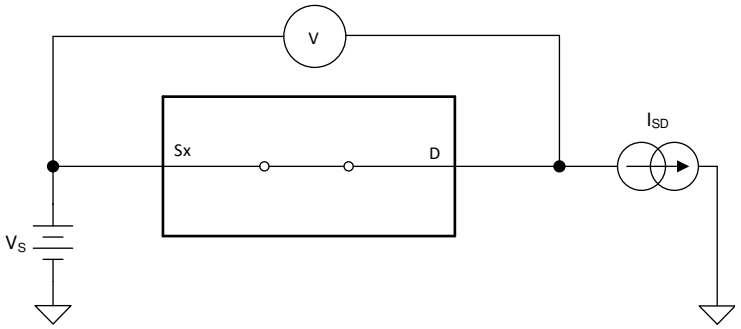



**图 16. On-Resistance Measurement Setup**

## 7.2 Off-Leakage Current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

The setup used to measure off-leakage current is shown in 图 17.

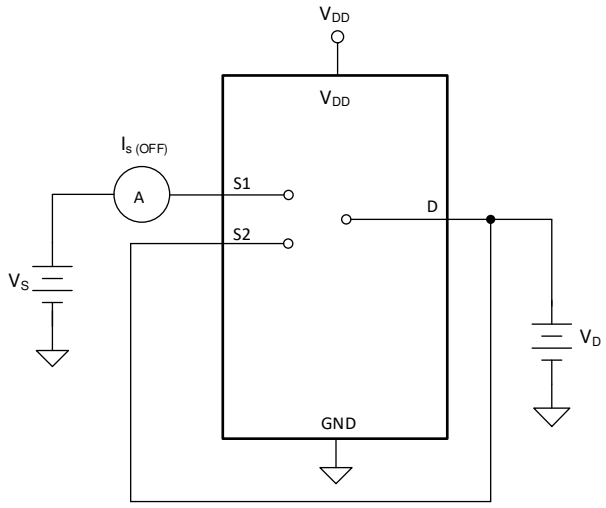



**图 17. Off-Leakage Measurement Setup**

## 7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 图 18 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

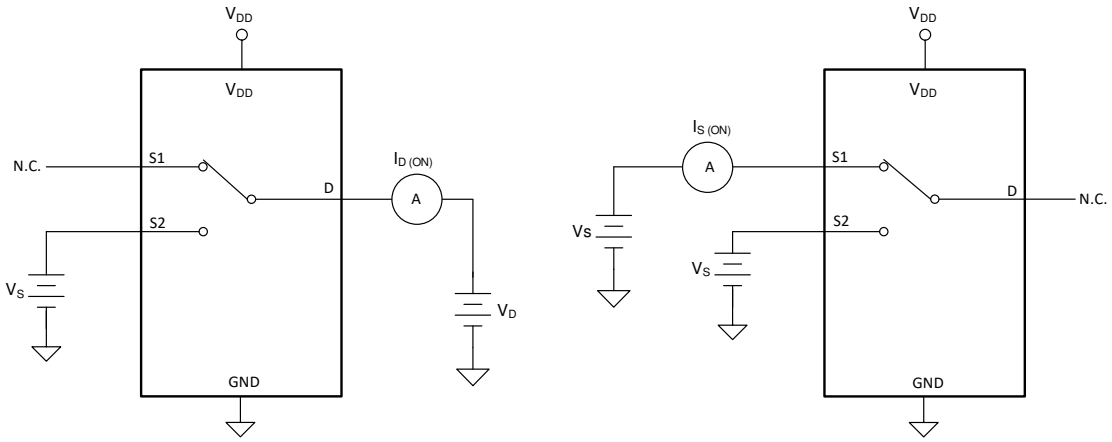



**图 18. On-Leakage Measurement Setup**

## 7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 19 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

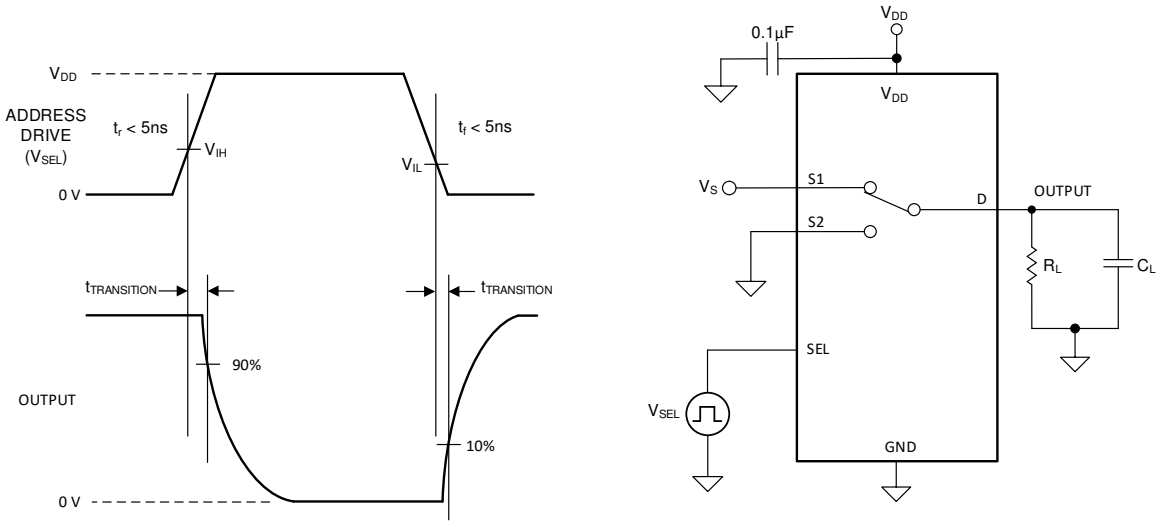



**图 19. Transition-Time Measurement Setup**

## 7.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 20 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

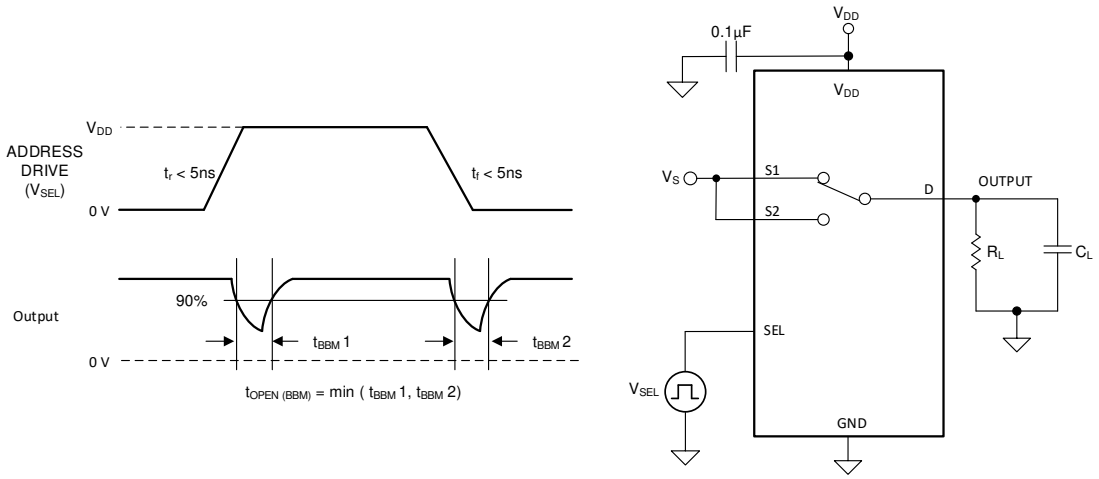



**图 20. Break-Before-Make Delay Measurement Setup**

## 7.6 Charge Injection

The TMUX1119 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol $Q_C$. 图 21 shows the setup used to measure charge injection from Drain (D) to Source (Sx).

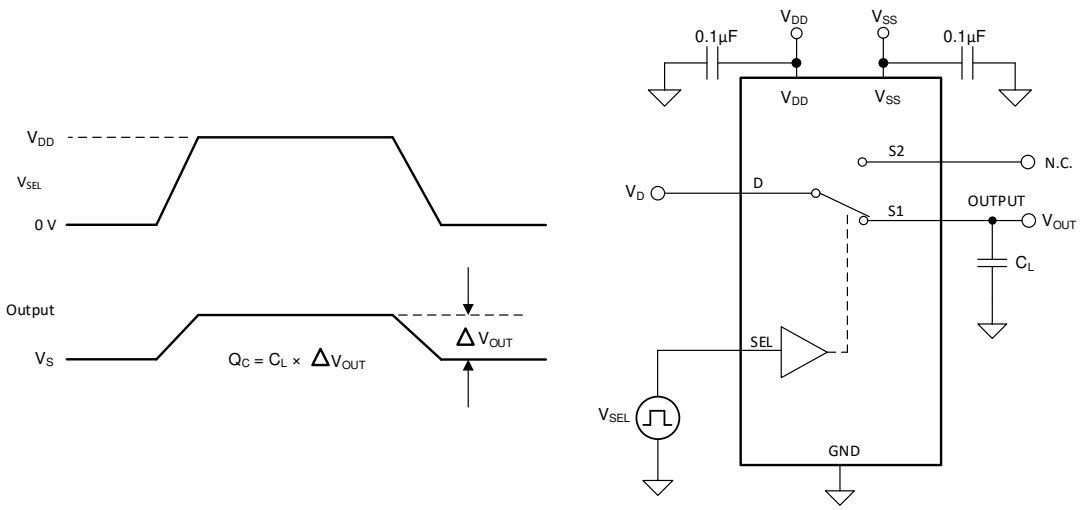



**图 21. Charge-Injection Measurement Setup**

## 7.7 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 图 22 shows the setup used to measure, and the equation used to calculate off isolation.

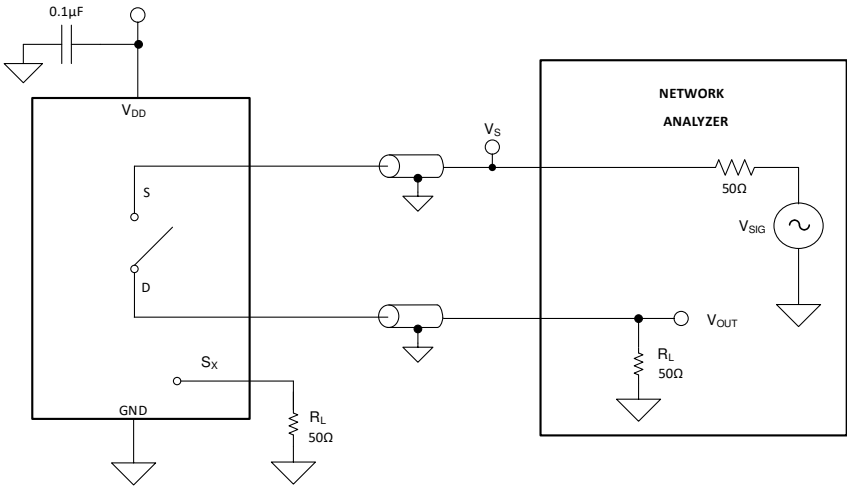



**图 22. Off Isolation Measurement Setup**

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

## 7.8 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 图 23 shows the setup used to measure, and the equation used to calculate crosstalk.

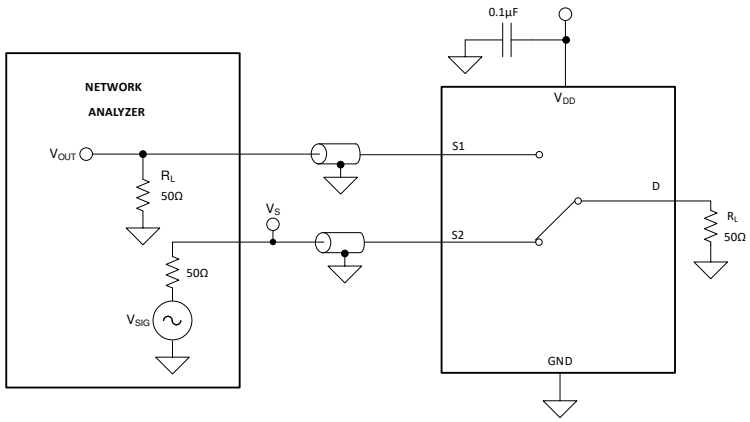



**图 23. Crosstalk Measurement Setup**

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

## 7.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 图 24 shows the setup used to measure bandwidth.

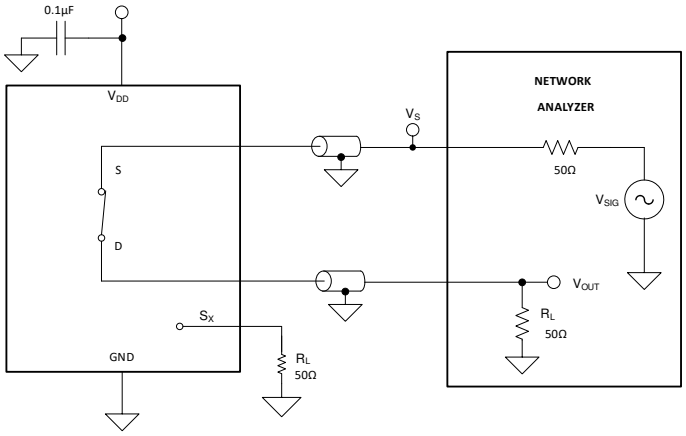



**图 24. Bandwidth Measurement Setup**

# 8 Detailed Description

## 8.1 Overview

The TMUX1119 is an 2:1, 1-ch. (SPDT), analog switch where the input is controlled with a single select (SEL) control pin.

## 8.2 Functional Block Diagram

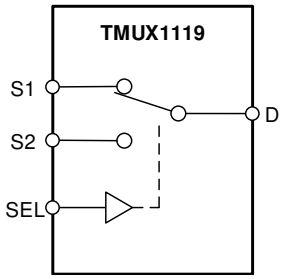



**图 25. TMUX1119 Functional Block Diagram**

## 8.3 Feature Description

### 8.3.1 Bidirectional Operation

The TMUX1119 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). The device has very similar characteristics in both directions and supports both analog and digital signals.

### 8.3.2 Rail to Rail Operation

The valid signal path input/output voltage for TMUX1119 ranges from GND to $V_{DD}$.

### 8.3.3 1.8 V Logic Compatible Inputs

The TMUX1119 has 1.8-V logic compatible control for the logic control input (SEL). The logic input threshold scales with supply but still provide 1.8-V logic control when operating at 5.5 V supply voltage. 1.8-V logic level inputs allow the TMUX1119 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*

### 8.3.4 Fail-Safe Logic

The TMUX1119 supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pin of the TMUX1119 to be ramped to 5.5 V while $V_{DD}$ = 0 V. Additionally, the feature enables operation of the TMUX1119 with $V_{DD}$ = 1.2 V while allowing the select pin to interface with a logic level of another device up to 5.5 V.

## Feature Description (接下页)

### 8.3.5 Ultra-low Leakage Current

The TMUX1119 provides extremely low on-leakage and off-leakage currents. The TMUX1119 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents. 图 26 shows typical leakage currents of the TMUX1119 versus temperature.

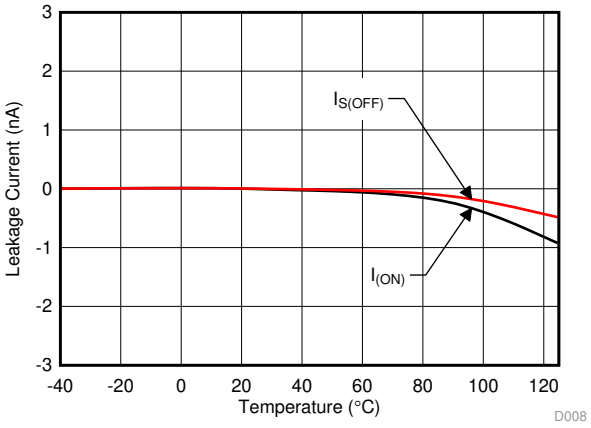



**图 26. Leakage Current vs Temperature**

### 8.3.6 Ultra-low Charge Injection

The TMUX1119 has a transmission gate topology, as shown in 图 27. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

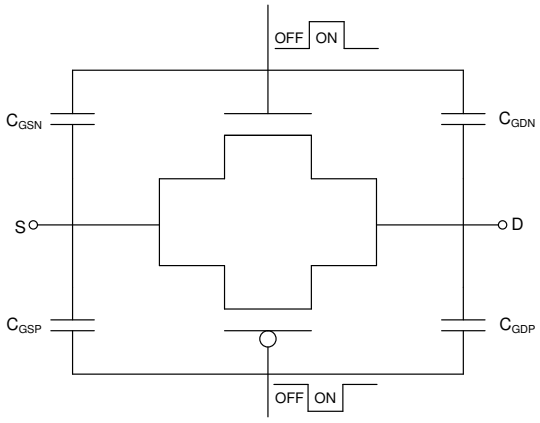



**图 27. Transmission Gate Topology**

## Feature Description (接下页)

The TMUX1119 has special charge-injection cancellation circuitry that reduces the drain-to-source charge injection to -6 pC at $V_D$ = 1 V as shown in 图 28.

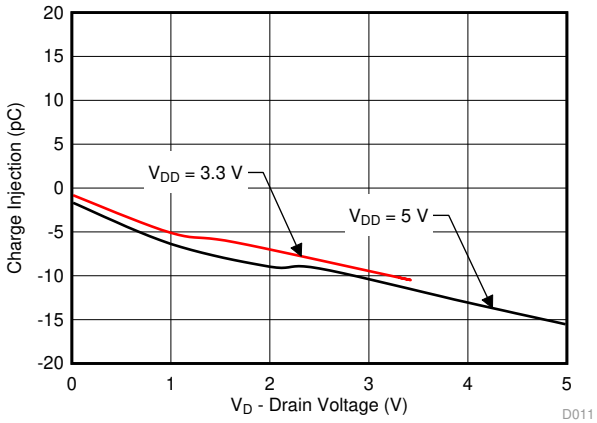



**图 28. Charge Injection vs Drain Voltage**

## 8.4 Device Functional Modes

The select (SEL) pin of the TMUX1119 controls which switch is connected to the drain of the device. When a given input is not selected, that source pin is in high impedance mode (HI-Z). The control pins can be as high as 5.5 V.

## 8.5 Truth Tables

**表 1. TMUX1119 Truth Table**

| CONTROL LOGIC (SEL) | Selected Source (Sx) Connected To Drain (D) Pin |
|---|---|
| 0 | S1 |
| 1 | S2 |

# 9 Application and Implementation

**注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TMUX11xx family offers ulta-low input/output leakage currents and low charge injection. These devices operate up to 5.5 V, and offer true rail-to-rail input and output of both analog and digital signals. The TMUX1119 has a low on-capacitance which allows faster settling time when multiplexing inputs in the time domain. These features make the TMUX11xx devices a family of precision, high-performance switches and multiplexers for low-voltage applications.

## 9.2 Typical Application

图 29 shows an ultrasonic gas meter front end. The ultrasonic front end design utilizes time of flight (TOF) measurement to determine the amount of gas flowing in a pipe. The circuit utilizes the MSP430FR5994, two ultra low power operational amplifiers, OPA835 and OPA836, along with two TMUX1119, 2:1 precision switches.

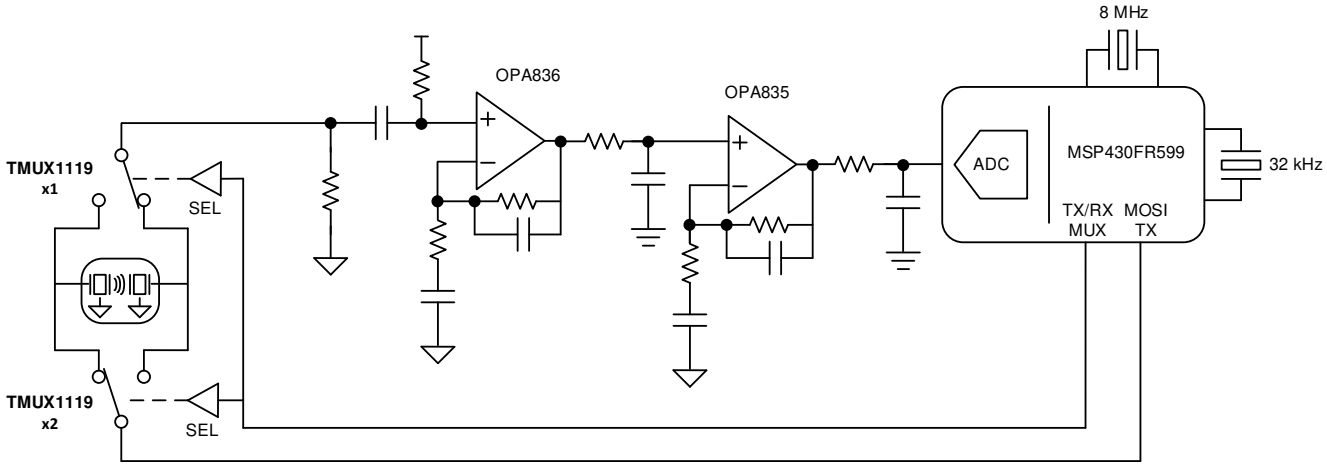



**图 29. Ultrasonic Gas Meter System**

## 9.3 Design Requirements

For this design example, use the parameters listed in 表 2.

**表 2. Design Parameters**

| PARAMETERS | VALUES |
|---|---|
| Supply ($V_{DD}$) | 5 V |
| I/O signal range | 0 V to $V_{DD}$ (Rail to Rail) |
| Control logic thresholds | 1.8 V compatible |
| Single-shot standard deviation (STD) | <2 ns |
| Zero-flow drift (ZFD) | <1 ns |

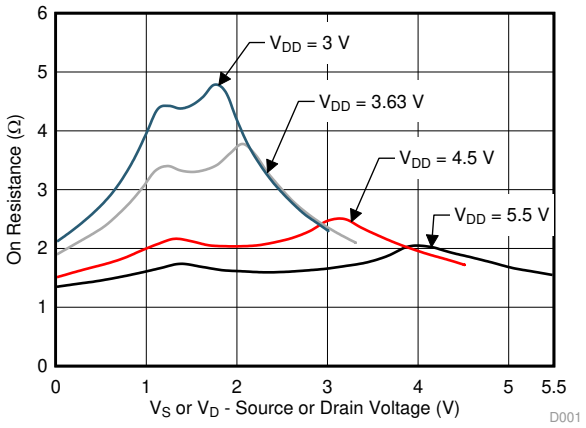
## 9.4 Detailed Design Procedure

The TMUX1119 can be operated without any external components except for the supply decoupling capacitors. All inputs passing through the switch must fall within the recommend operating conditions of the TMUX1119, including signal range and continuous current. For this design with a supply of 5 V the signal range can be 0 V to 5 V, and the max continuous current can be 30 mA.

The TMUX1119 device is a bidirectional, single-pole double-throw (SPDT) switch that offers low on-resistance, low leakage, and low power. These features make this device suitable for portable and power sensitive applications such as ultrasonic gas metering systems. The two TMUX1119 devices are used to switch the transmission and reception signals from the MCU to the two transceivers in an efficient manner without distortion. Exceptional on-resistance flatness, leakage performance, and charge injection allows the TMUX1119 to be utilized in place of the TS5A9411 in *Ultrasonic Gas Meter Front-End With MSP430™ Reference Design*. For a more detailed analysis of the entire system refer to the *reference design*.

## 9.5 Application Curve

The TMUX1119 is capable of switching signals with minimal distortion because of the ultra-low leakage currents and excellent On-resistance flatness. 图 30 shows how the on-resistance fo the TMUX1119 varies with different supply voltages.




$T_A$ = 25°C

**图 30. On-Leakage vs Source or Drain Voltage**

# 10 Power Supply Recommendations

The TMUX1119 operates across a wide supply range of 1.08 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the $V_{DD}$ supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from $V_{DD}$ to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

# 11 Layout

## 11.1 Layout Guidelines

### 11.1.1 Layout Information

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 31 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

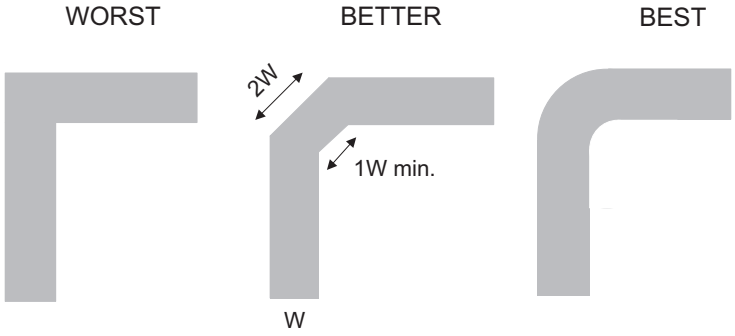



**图 31. Trace Example**

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

图 32 illustrates an example of a PCB layout with the TMUX1119. Some key considerations are:

- Decouple the $V_{DD}$ pin with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the $V_{DD}$ supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

## 11.2 Layout Example

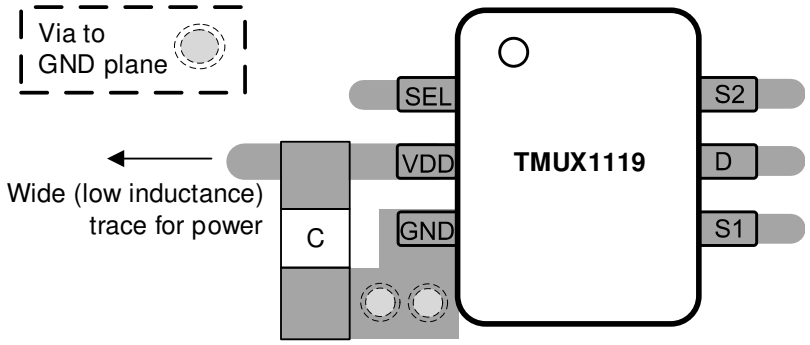



**图 32. TMUX1119 Layout Example**

# 12 器件和文档支持

## 12.1 文档支持

### 12.1.1 相关文档

德州仪器 (TI)，*《采用 MSP430™ 的超声波燃气表前端参考设计》*。

德州仪器 (TI)，*《真差分 4 x 2 多路复用器、模拟前端、同步采样 ADC 电路》*。

德州仪器 (TI)，*《使用低 CON 多路复用器改善稳定性问题》*。

德州仪器 (TI)，*《使用 1.8V 逻辑多路复用器和开关简化设计》*。

德州仪器 (TI)，*《利用关断保护信号开关消除电源排序》*。

德州仪器 (TI)，*《高电压模拟多路复用器的系统级保护》*。

德州仪器 (TI)，*《QFN/SON PCB 连接》*。

德州仪器 (TI)，*《四方扁平封装无引线逻辑封装》*。

## 12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

## 12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 12.4 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 12.5 商标

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## 12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMUX1119DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 26HT | Samples |
| TMUX1119DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | 1DF | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

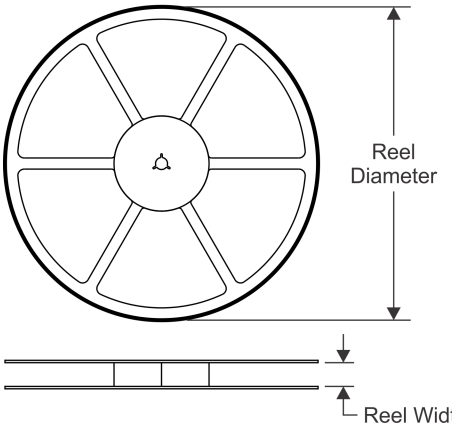
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

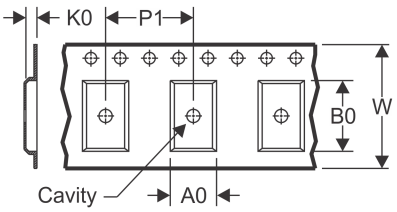
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

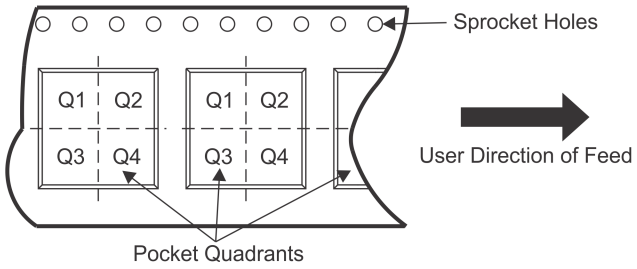



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

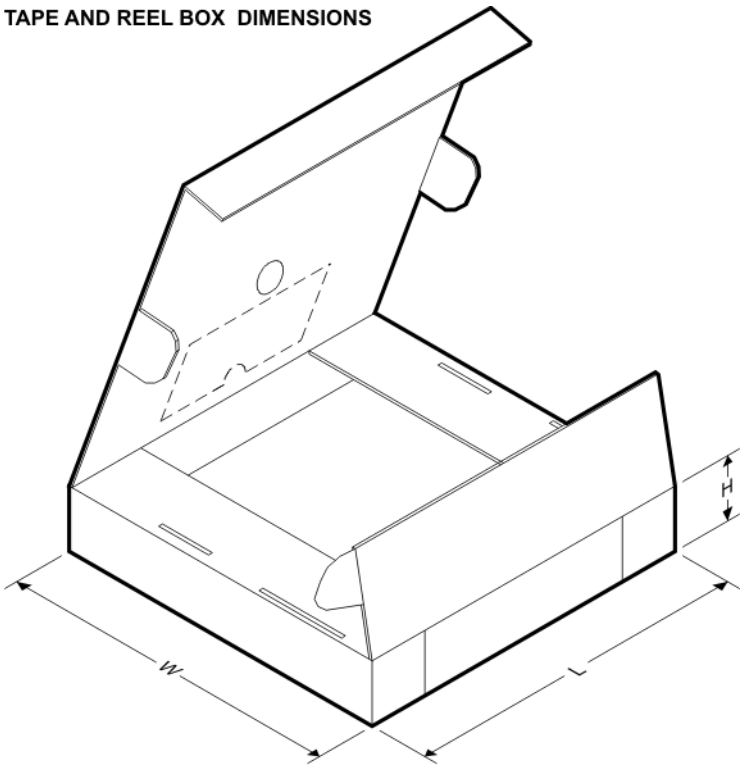
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMUX1119DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TMUX1119DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

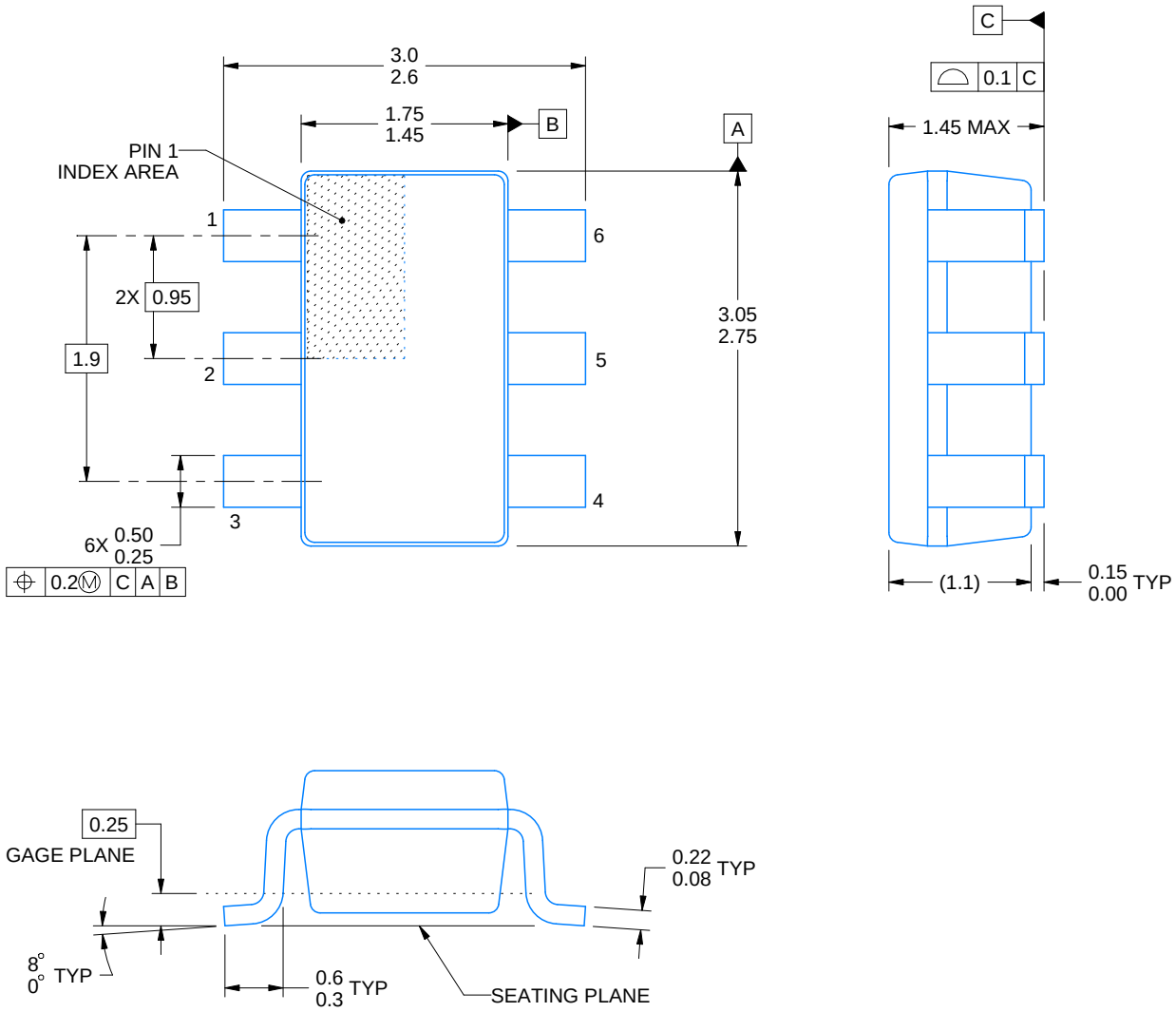
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMUX1119DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TMUX1119DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

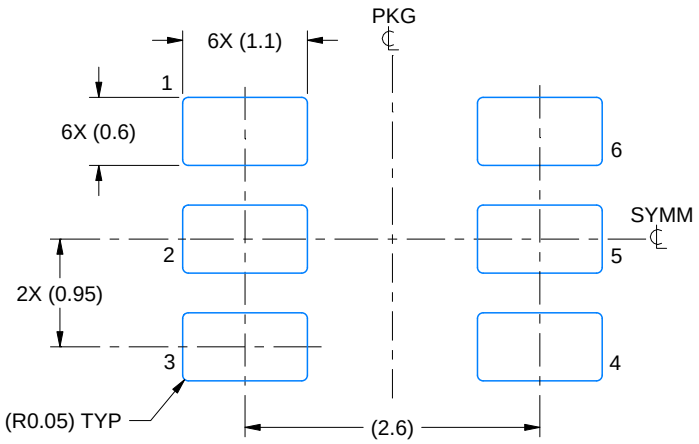
SMALL OUTLINE TRANSISTOR



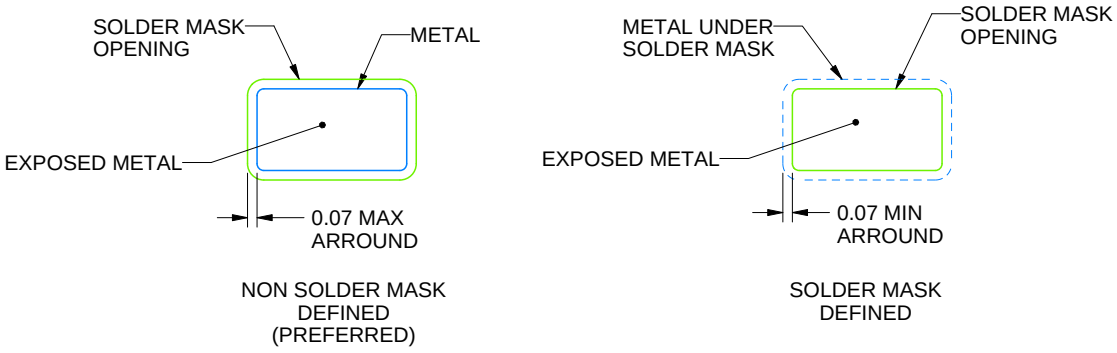

4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

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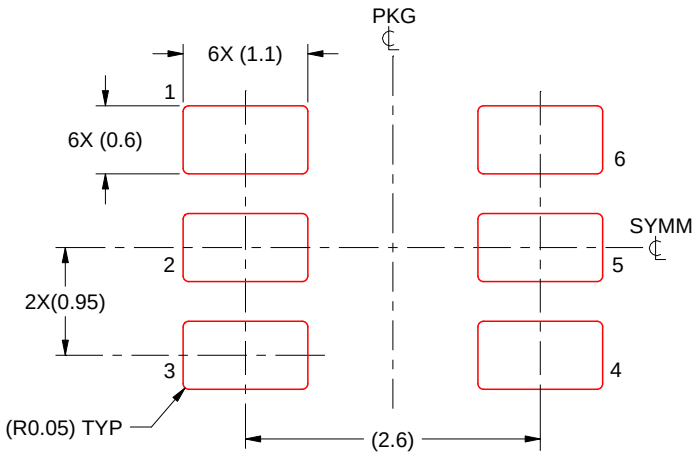
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



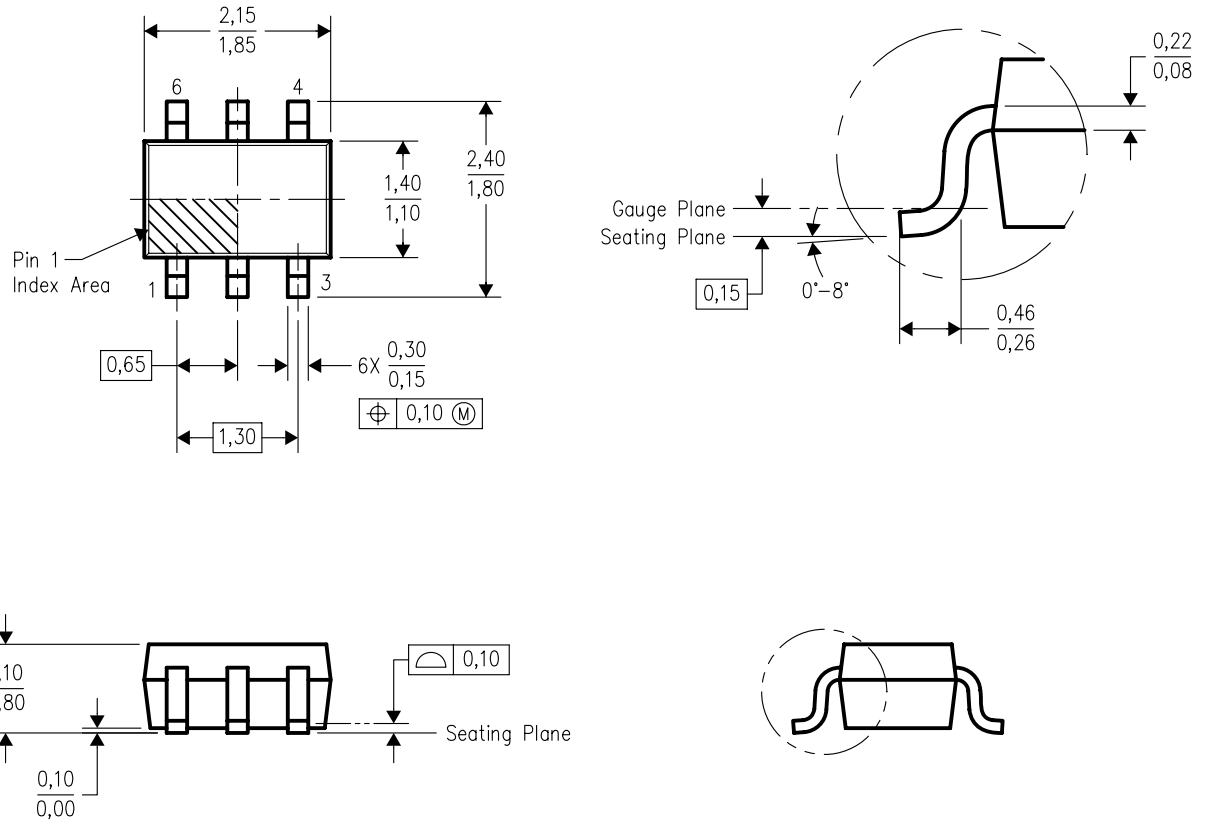

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

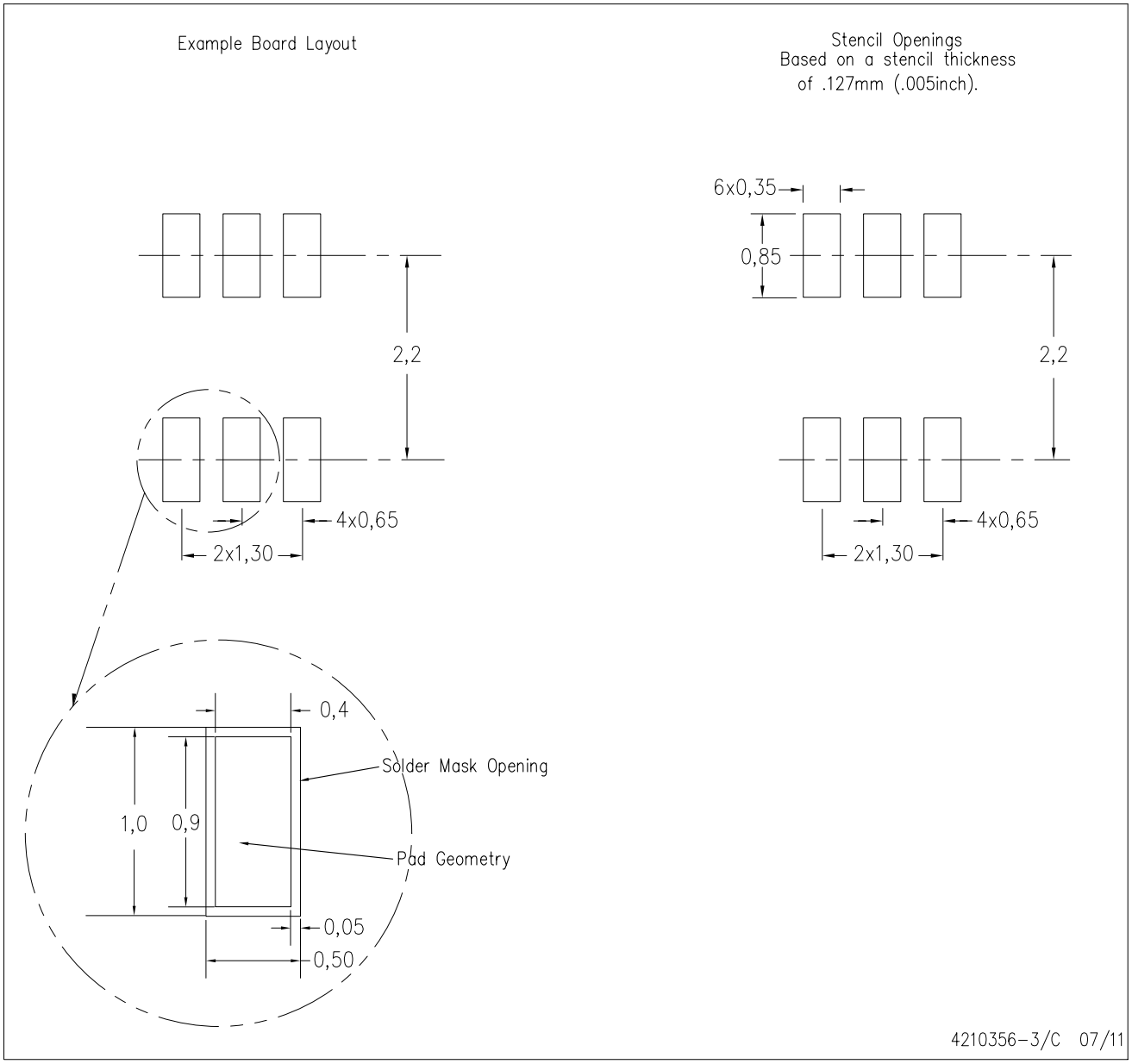
## DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE




4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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