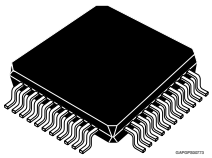
L9924L

Automotive vehicle conform truck car alternator regulator IC with LIN

Datasheet - production data



TQFP44EP

Features

- AEC-Q100 qualified
- System in package smart power alternator regulator and 8-bit microcontroller (non-monolithic approach)
- Protected high/low side field pre-driver for external MOS
- Field short circuit protection
- Regulated voltage driven by ECU (programmable protocol driven)
- Regulated voltage thermally compensated (without protocol)
- Lamp driver (wake up and warning detection)
- Diagnostic via LIN
- LIN 2.1 interface for programming and control
- Self start function
- Load response control (LRC)
- Field monitor (FM) output
- Thermal shutdown
- Package TQFP44EP (10 x 10 mm)

Description

The L9924L is a controlled multifunctional alternator regulator intended to be used in cars, commercial and agricultural vehicles, with support for 12 V and 24 V systems. The control can be achieved through different communication protocols: LIN, RCV, PCM, C_term, BSS. It is a System-In-Package solution with smart power alternator regulator IC coupled with a 8-bit microcontroller (non-monolithic approach). It includes the control section, fault diagnostic circuit which drives a warning lamp, and the protection against short circuits.

This device regulates in closed loop the output of an automotive generator by controlling the field winding current by means of a Pulse-Width Modulation (PWM) of an external high side or low side driver at fixed frequency.

This is information on a product in full production. www.st.com

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1 Application schematics

Figure 1. Low-side configuration 12 V

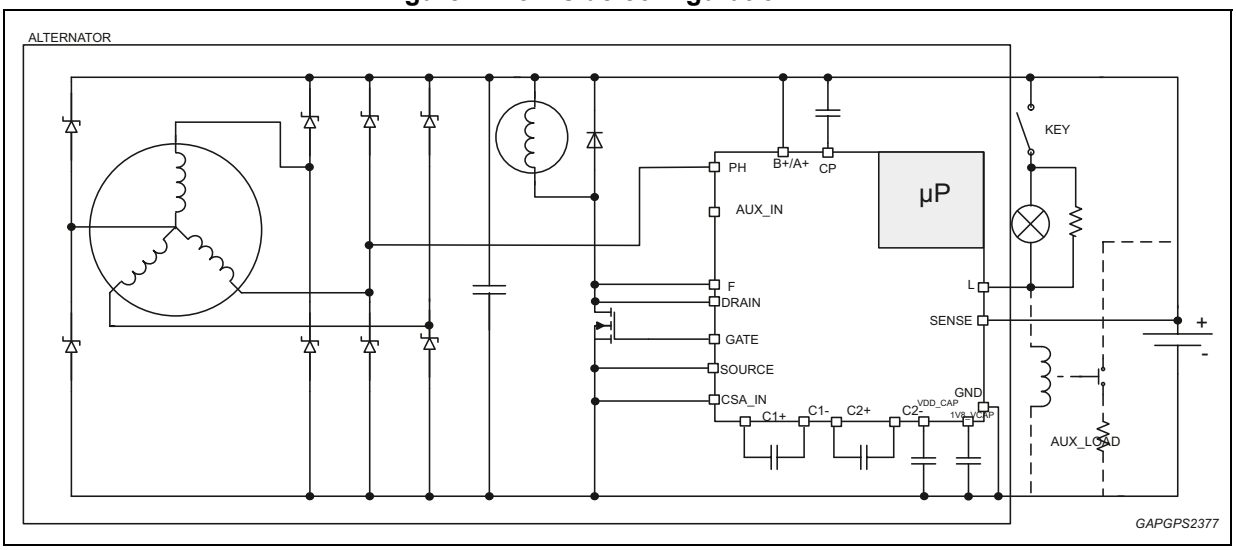


Figure 2. High-side configuration 12 V

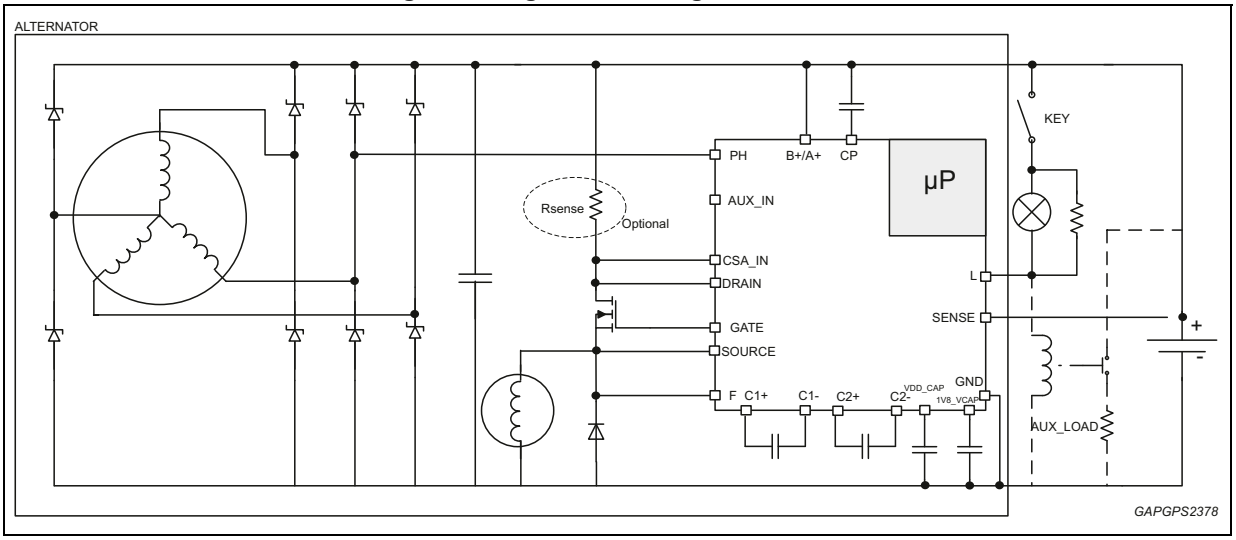
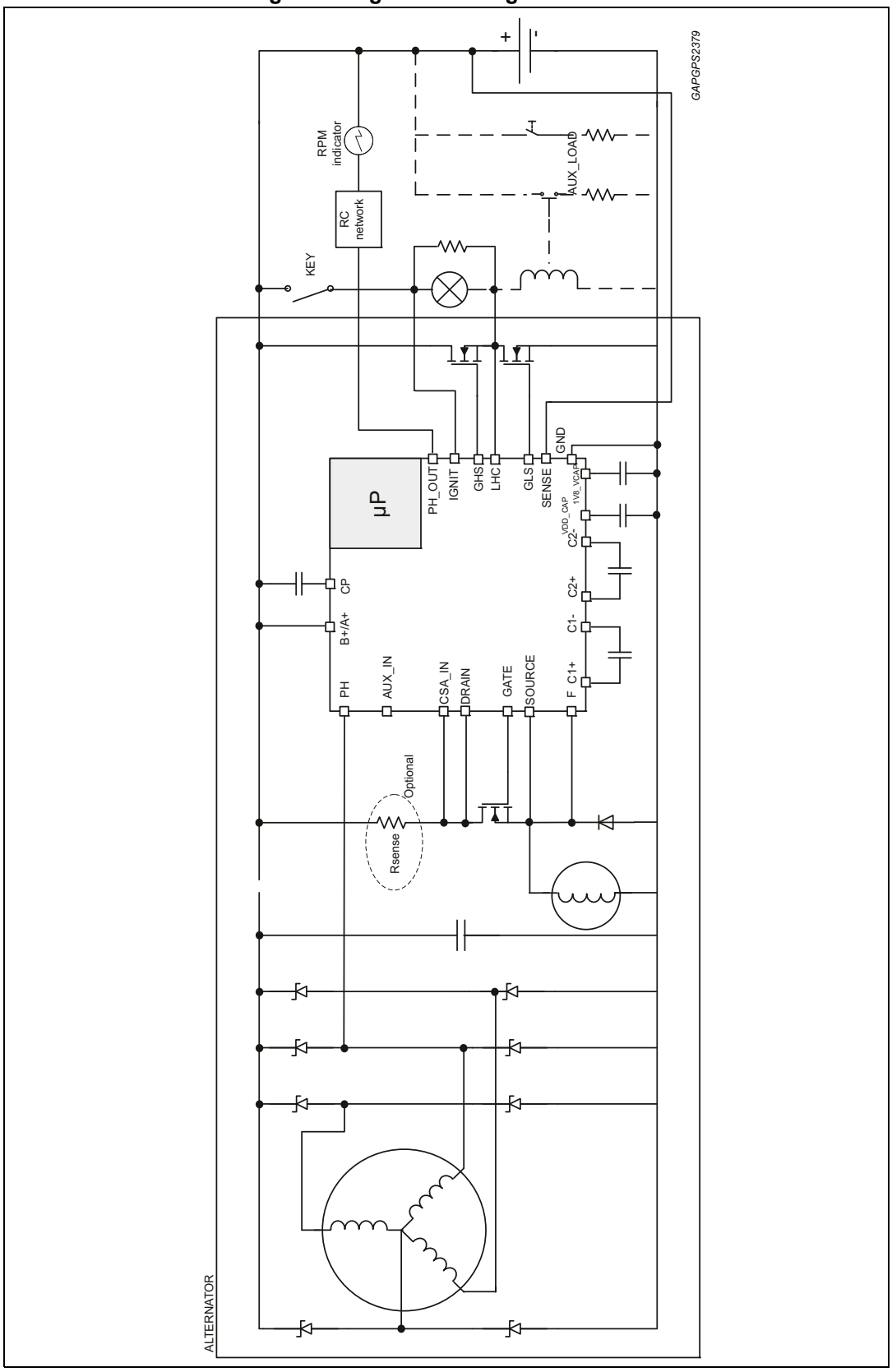
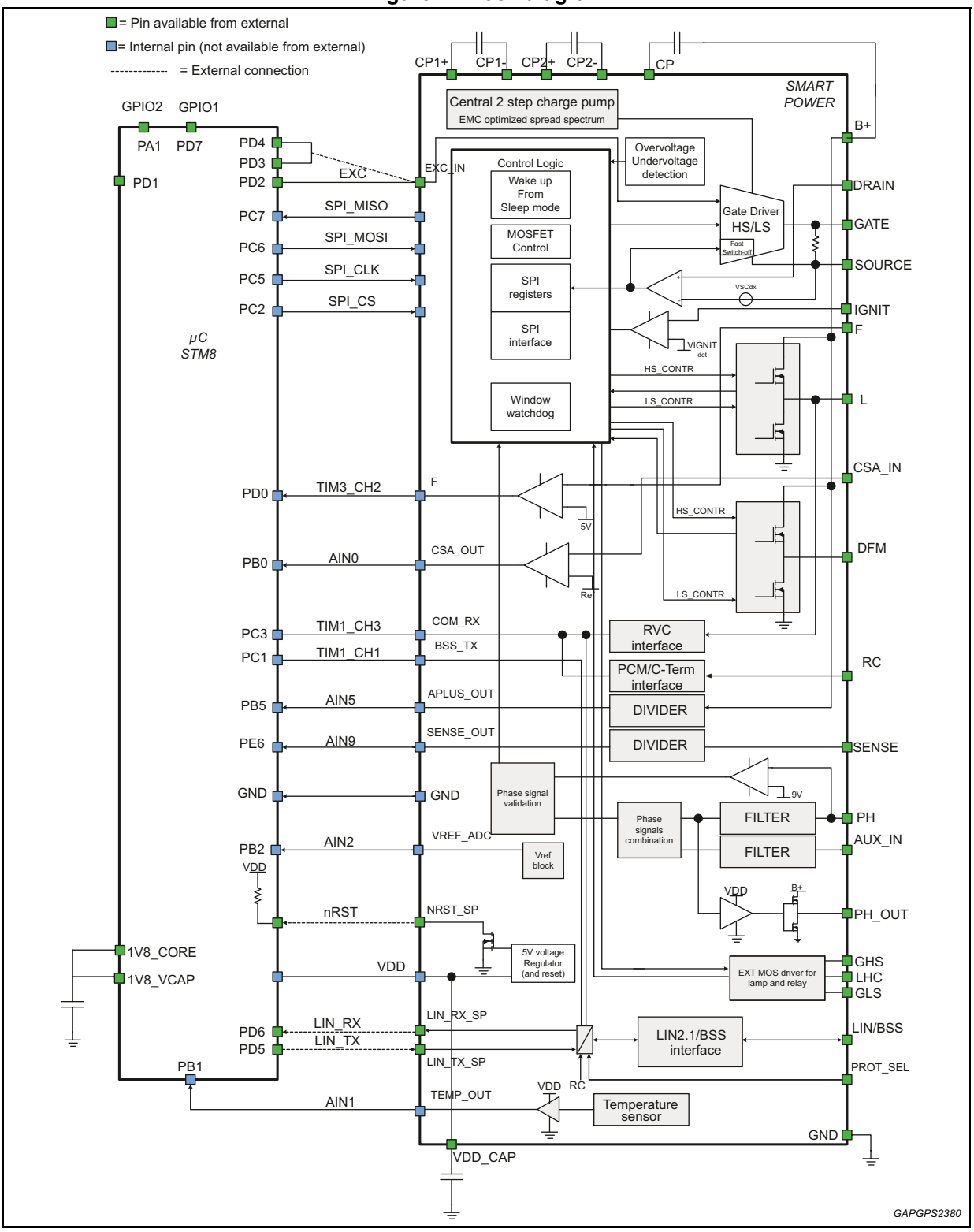


Figure 3. High-side configuration 24 V



2 Block diagram

Figure 4. Block diagram



3 Pin description

Figure 5. Pin connection diagram

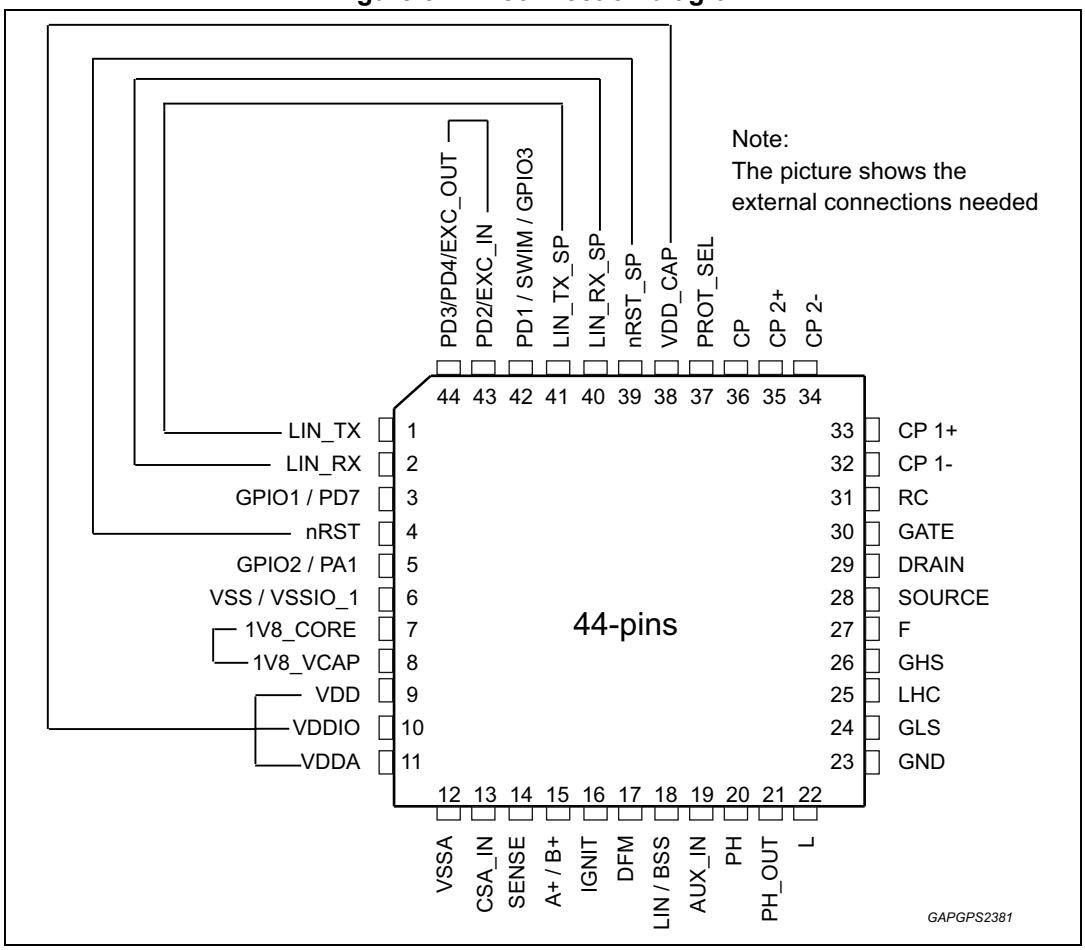


Table 1. Pin function

N°	Pin name	Function
1	LIN_TX	LIN transmitter (µC output)
2	LIN_RX	LIN receiver (µC input)
3	PD7/TLI/GPIO1	General purpose Input/output (PD7) / Top level interrupt
4	nRST	Reset (µC)
5	PA1/GPIO2	General purpose Input/output (PA1)
6	VSS / VSSIO_1	Digital ground / I/O ground
7	1V8_CORE	1.8 V Core
8	1V8_VCAP	1.8 V regulator capacitor(470 to 3300nF)
9	VDD	Digital power supply
10	VDDIO	I/O power supply

Table 1. Pin function (continued)

N°	Pin name	Function
11	VDDA	Analog power supply (connect to 100nF//1uF for decoupling)
12	VSSA	Analog ground
13	CSA_IN	Current sense ampl. Input
14	SENSE	Battery sensing with dedicated wire
15	A+ /B+	Battery sense / Device power supply
16	IGNIT	Ignition terminal
17	DFM	Field Monitor (PWM signal going to ECU)
18	LIN/BSS	LIN / BSS (coming from ECU)
19	AUX_IN	Auxiliary input
20	PH	Phase sense input
21	PH_OUT	Filtered Phase signal
22	L	Key sensing and Warning Lamp terminal output
23	GND	Regulator ground
N°	PIN	Function
24	GLS	Gate driver of ext Low Side MOS used for Lamp
25	LHC	Key sensing and Warning Lamp terminal output in case of ext MOS used for lamp driving
26	GHS	Gate driver of ext High Side MOS used for Relay
27	F	Field activity monitor (for High side and low side configuration)
28	SOURCE	External MOS Source
29	DRAIN	External MOS Drain
30	GATE	External MOS Gate
31	RC	C-Terminal / PCM (PWM signal input coming from ECU)
32	CP1-	Charge pump pin for capacitor 1, negative side
33	CP1+	Charge pump pin for capacitor 1, positive side
34	CP2-	Charge pump pin for capacitor 2, negative side
35	CP2+	Charge pump pin for capacitor 2, positive side
36	CP	Charge pump output
37	PROT_SEL	Protocol selection
38	VDD_CAP	5V capacitor(5V regulator output)
39	nRST_SP	Reset (Smart Power)
40	LIN_RX_SP	LIN receiver (smart power output)
41	LIN_TX_SP	LIN transmitter (smart power input)
42	PD1/SWIM/GPIO3	Single Wire Interface Module (for µC programming) General purpose Input/output (PD1)

Table 1. Pin function (continued)

N°	Pin name	Function
43	PD2/EXC_IN	Excitation input: connect to PD3/PD4/EXC_OUT
44	PD3/PD4/EXC_OUT	Excitation output: connect to PD2/EXC_IN

As shown in the picture, the following pin groups must be connected through external wiring.

Table 2. Group of pins externally connected

Signal	Pins			
VDD	9 (VDD)	10 (VDDIO)	11 (VDDA)	38 (VDD_CAP)
GND	23 (GND)	6 (VSS/VSSIO_1)	12 (VSS_A)	Exposed PAD
V18	7 (1V8_CORE)	8 (V8_VCAP)		
nRST	4 (nRST)	39 (nRST_SP)		
LIN_TX	1 (LIN_TX)	41 (LIN_TX_SP)		
LIN_RX	2 (LIN_RX)	40 (LIN_RX_SP)		

VDD and GND pins in the block diagram are generic references to the relevant pin groups of the above table.

4 Electrical specifications

4.1 Absolute maximum ratings

T_j = -40 to 155 °C, unless otherwise specified.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VB_{DC}	DC supply voltage	48	V
VB_{LD}	Transient supply voltage (load dump) t < 500 ms	65	V
T_j	Junction temperature range	-40 to 155	°C
T_{stg}, T_{case}	Storage and case temperature range	-40 to 155	°C
P_{TOT}	Total power dissipation	1.25	W
VB_R	Reverse battery voltage @ 25 °C, T = 15 sec	-2.5	V
VPH_{min}	Normal working condition reverse voltage (PH Bplus. GND)	-1.5	V
ESD_{HBM}	ESD HBM (Internal pins)	±2	kV
ESD_{HBM}	ESD HBM (All global pins)	±4	kV
ESD_{HBM}	LIN pin	±6	kV

Table 4. Maximum ratings

N°	Pin	Condition	Min.	Max.	Unit
1	LIN_TX	-	-0.2	V_{DD}+0.2	V
2	LIN_RX	-	-0.2	V_{DD}+0.2	V
3	PD7/TLI/GPIO1	-	-0.2	V_{DD}+0.2	V
4	nRST	-	-0.2	V_{DD}+0.3	V
5	PA1/GPIO2	-	-0.2	V_{DD}+0.2	V
6	VSS / VSSIO_1	-	-	-	V
7	1V8_CORE	-	-0.2	2.7	
8	1V8_VCAP	-	-0.2	2.0	V
9	VDD	-	-0.2	6.5	V
10	VDDIO	-	-0.2	6.5	V
11	VDDA	-	-0.3	6.5	V
12	VSSA	-	-	-	-
13	CSA_IN	-	-0.3	+48	V
14	SENSE	-	-20	+48	V
15	A+/B+	Reverse battery voltage @ 25 °C, T = 15 s	-2.5	+48	V
16	IGNIT	-	-20	+48	V
17	DFM	-	-0.3	+48	V

Table 4. Maximum ratings (continued)

N°	Pin	Condition	Min.	Max.	Unit
18	LIN/BSS	-	-20	+40	V
19	AUX_IN	-	-20	+48	V
20	PH	-	-20	+48	V
21	PH_OUT	-	-0.3	+48	V
22	L	-	-0.3	+48	V
23	GND	-	-	-	-
24	GLS	-	-0.3	+13.5	V
25	LHC	-	-0.3	+48	V
26	GHS	-	max[-0.3; V(LHC)-0.6]	min[+48; V(LHC)+13.5]	V
27	F	-	-2	+48	V
28	SOURCE	-	-2	+48	V
29	DRAIN	-	-2.5	+48	V
30	GATE	-	V(SOURCE)-0.6	min[+48; V(SOURCE)+13.5]	V
31	RC	-	-1.5	+48	V
32	CP1-	-	-0.3	+48	V
33	CP1+	-	max[-0.3; V(A+/B+)-0.3]	V(A+/B+)+20	V
34	CP2-	-	-0.3	+48	V
35	CP2+	-	max[-0.3; V(A+/B+)-0.6]	V(A+/B+)+20	V
36	CP	-	max[-0.3; V(A+/B+)-0.3]	V(A+/B+)+20	V
37	PROT_SEL	-	-0.3	6.5	V
38	VDD_CAP	-	-0.2	6.5	V
39	nRST_SP	-	-0.3	V_{DD}+0.3	V
40	LIN_RX_SP	-	-0.3	V_{DD}+0.3	V
41	LIN_TX_SP	-	-0.3	6.5	V
42	PD1/SWIM/GPIO3	-	-0.2	V_{DD}+0.2	V
43	PD2/EXC_IN	-	-0.2	min[6.5; V_{DD}+0.3]	V
44	PD3/PD4/EXC_OUT	-	-0.2	V_{DD}+0.2	V

4.1.1 EEPROMs parameters

Table 5. Flash program memory

#	Parameter	Test condition	Value	Unit
1	Erase/Write cycles	T_{amb} = 25 °C	2500	Cycles
2		T_{amb} = 55 °C	1500	
3		T_{amb} = 125 °C	300	
4	Retention	T_{amb} = 55 °C	20	Years

Table 6. Data memory

#	Parameter	Test condition	Value	Unit
1	Erase/Write cycles	T_{amb} = 25 °C	280000	Cycles
2		T_{amb} = 55 °C	170000	
3		T_{amb} = 125 °C	10000	
4	Retention	T_{amb} = 55 °C	2	Years

4.2 Thermal data

Table 7. Thermal data

#	Symbol	Parameter	Max.	Unit
1	$R_{th_j\text{-}case}$	Thermal resistance junction-to-case	1	°C/W
2	T_{pad}	Exposed pad temperature	140	°C

4.3 Electrical characteristics

4.3.1 Pin "A+/B+"

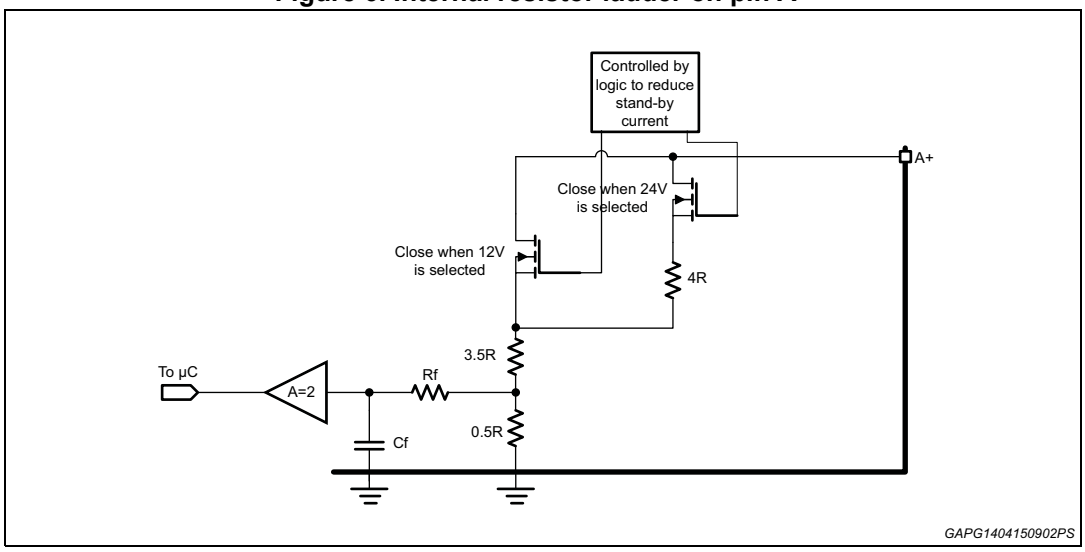
This pin is both the primary power supply (B+) and the default battery sense (A+)

The device is supplied by the battery through A+/B+ pin and it remains in stand-by condition with a current consumption of $IB_{stby12V/24V}$ until there is activity on one or more wake-up sources.

Table 8. Pin "A+/B+" electrical characteristics

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	VB_{OVR}	Operating Voltage Range	-	6	-	40	V
2	$IB_{stby12V}$	12-V stand-by current consumption	V(A+/B+) = 12.6 V 6 wake-up sources active V(PH)=V(AUX_IN)=V(GND) LIN_BSS tied to A+/B+ RC pin tied to A+/B+ through a resistor	-	-	255	µA
3	$IB_{stby24V}$	24-V stand-by current consumption	V(A+/B+) = 25.2 V 6 wake-up sources active V(PH)=V(AUX_IN)=V(GND) LIN_BSS pin tied to A+/B+; RC pin tied to A+/B+ through a resistor	-	-	265	µA
4	VB_{IntOvp}	Over-voltage protection threshold (12-V systems)	[0x2].12 = SEL24V_EN = b0	16.5	17.6	19	V
		Over-voltage protection threshold (24-V systems)	[0x2].12 = SEL24V_EN = b1	33	35.5	38	V
5	VB_{low}	A+/B+ under-voltage	-	4.5	5.3	6	V
6	αB	Resistor divider attenuation	[0x2].12 = SEL24V_EN = 0	3.96	4	4.04	V/V
			[0x2].12 = SEL24V_EN = 1	7.925	8	8.069	V/V
7	εB	Resistor divider accuracy	[0x2].12 = SEL24V_EN = 1	-	-	0.9	%
8	fB_p	Pole frequency	-	520	860	1570	Hz

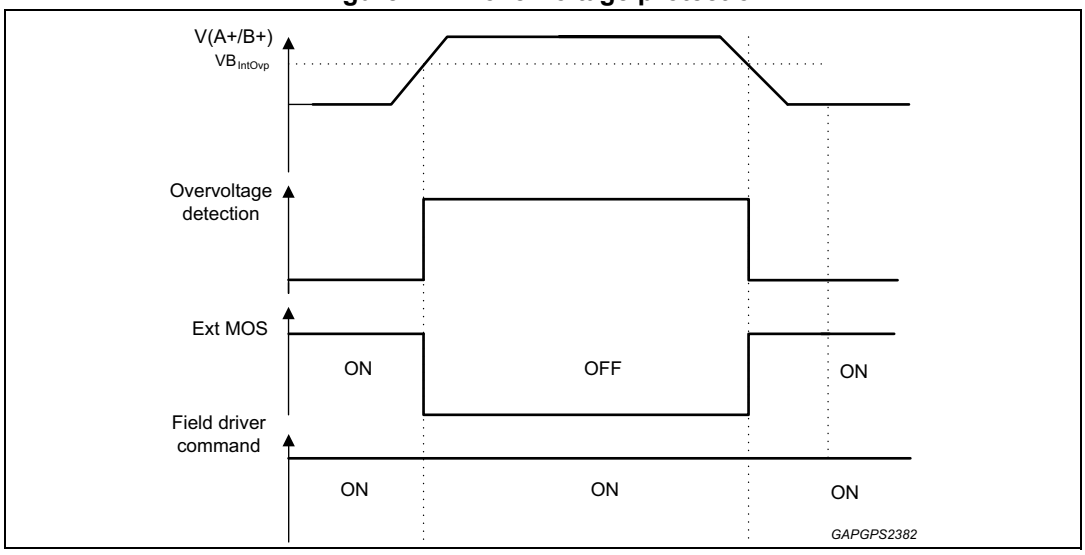
Figure 6. Internal resistor ladder on pin A+



When the A+ voltage drops below VB_{low} the whole device is turned-off and could be initialized by a Power-On Reset (PORn).

If A+/B+ voltage overcomes the VB_{IntOvp} value, the system switches the field excitation off and sets bit 7 of SPI read register 0x12 [12.4.6]: it's up to the application software to take the appropriate actions (lamp on, drivers off, etc.).
A+/B+ signal, suitably conditioned and filtered by an 'active' divider equipped with a low-pass filter, is forwarded to µC pin AIN5.

Figure 7. VB overvoltage protection



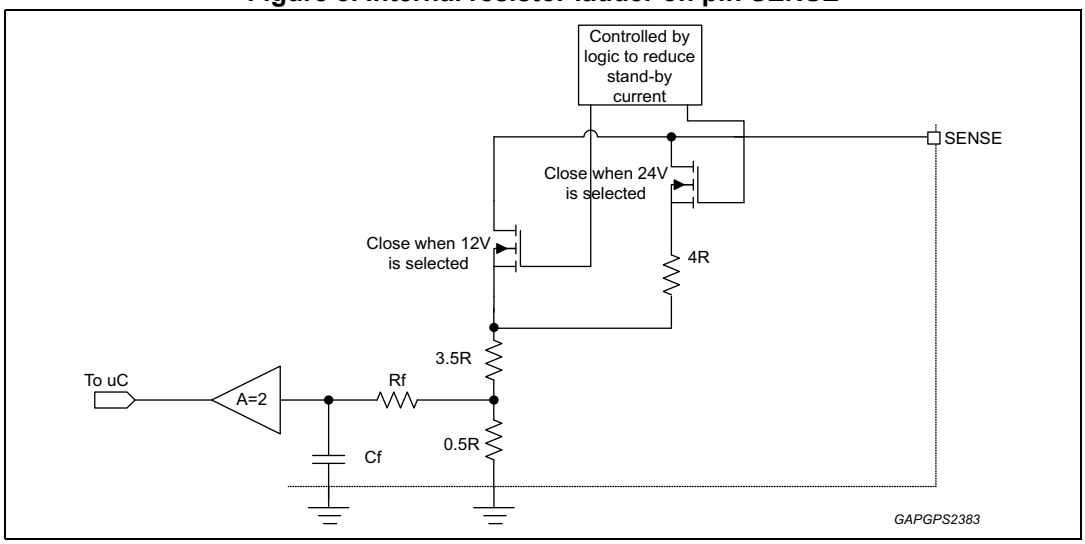
4.3.2 Pin "SENSE"

The system battery can be alternatively sensed using the SENSE input, instead of A+ sensing path.

A suitable resistor ladder can be selected by means of bit 12 of SPI write register 0x02, depending on the device operating mode (12 V or 24 V [12.4.11]).

The signal, before being forwarded to µC pin AIN9, is filtered through single pole low-pass filter.

Figure 8. Internal resistor ladder on pin SENSE



A similar block is used to bring A+ pin voltage to AIN5 microcontroller analog input.

Table 9. Electrical characteristics pin "SENSE"

#	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
1	αS	Resistor divider attenuation	[0x2].12 = SEL24V_EN = 0	3.96	4	4.04	V/V
			[0x2].12 = SEL24V_EN = 1	7.925	8	8.069	V/V
2	εS	Resistor divider accuracy	[0x2].12 = SEL24V_EN = 1	-	-	0.9	%
3	fS_p	Pole frequency	-	520	860	1570	Hz

4.3.3 Pin “IGNIT”

The IGNIT pin is an input used as additional signal to wake-up the device. The signal applied to IGNIT is compared to a threshold $VIGNIT_{detx}$ to manage the device wake-up. If not used this pin must be tied to GND.

Table 10. Electrical characteristics pin “IGNIT”

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	$VIGNIT_{det1}$	24-V threshold input voltage	[0x2].12 = SEL24V_EN = b1	11	13	15	V
2	$VIGNIT_{det2}$	12-V threshold input voltage	[0x2].12 = SEL24V_EN = b0	6	8	10	V
3	$IGNIT_{pull\text{-}dw}$	Pull-down current	28 V<(IGNIT) ≤ $VIGNIT_{det2}$	-	20	250	µA

4.3.4 Pin “PROT_SEL”

This pin is used together with RC to select the used protocol.The pull-up resistor present in Active mode is turned into pull-down one in power stand-by mode to limit current consumption.

Table 11. Electrical characteristics pin “PROT_SEL”

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	$VPSEL_L$	Low level input voltage	-	-	-	1.3	V
2	$VPSEL_H$	High level input voltage	-	2.3	-	V_{DD}	V
3	$VPSEL_{Hyst}$	Input hysteresis	-	-	0.4	-	V
4	RPSEL	Pull-up/pull-down resistor	Active mode Pull-up to internal 3.3-V power rail V(PROT_SEL) = V(GND) RPSEL = -3.3 V/I(PROT_SEL)	-	100	-	kΩ

Table 11. Electrical characteristics pin “PROT_SEL” (continued)

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5	$IPSEL_{PU}$	Pull-up current	Active mode RPSEL current when pull-up to internal 3.3-V power rail V(PROT_SEL)=V(GND)	-	-33	-	µA
6	$IPSEL_{PD}$	Pull-down current	Power Stand-by mode RPSEL current when pull-down to GND V(PROT_SEL) = V_{DD}	-	33	-	µA

4.3.5 Pin “LIN/BSS”

This pin can be used for both LIN and BSS communication protocols. In order to allow the pin sharing between LIN and BSS protocol (the internal pull-up resistor necessary for LIN is not used by BSS protocol), it is necessary to select the desired protocol using the PROT_SEL pin, RC pin and control internal pull-up resistor by bit 4 of SPI register 0x08.

Table 12. Electrical characteristics pin PROT_SEL and RC pin protocol

PROT_SEL PIN level	RC PIN level	PROTOCOL SELECTED
Low	Low	LIN
Low	High (through ext pull-up resistor)	BSS
High	High (through ext pull-up resistor for PCM and C-Term) Low (for RVC)	All other protocols
High	High	Reserved

Because of the internal pull-up resistor, when not used (no LIN or BSS protocol) the pin should be left open and the “wake-up by LIN” function must be disabled by SPI.

LIN general requirements:

- Speed communication up to 20 kbit/s (100 kbit/s for Flash).
- LIN 2.1 compliant (SAEJ2602 compatible) transceiver.
- Functional range from +40 V to -18 V DC at LIN/BSS pin.
- GND disconnection fail safe at module level.
- Off mode: does not disturb network.
- GND shift operation at system level.
- Micro controller interface with CMOS compatible I/O pins.
- ESD: Immunity against automotive transients per ISO7637 specification
- Matched output slopes and propagation delay
- In order to further reduce the current consumption in standby mode, the integrated LIN bus interface offers an ultra low current consumption.

Pins involved in both LIN and BSS protocols management are:

- LIN_RX_SP: smart power output, which stands for RxD
- LIN_TX_SP: smart power input, which stands for TxD
- LIN/BSS: transceiver bus from ECU
- LIN_RX: µC input to be connected to LIN_RX_SP
- LIN_TX: µC output to be connected to LIN_TX_SP

LIN Error Handling

The device provides the following 3 error handling features which aren't described in the LIN Spec. V2.1, but implemented in several stand-alone LIN transceivers/microcontrollers to switch the application back to normal operation mode.

- Dominant TxD time out

  In case TxD is in dominant state (i.e. low level) for more than $t_{dom(TXD)}$=12ms (typical value) the transmitter will be disabled. The status won't be latched and can be read through bit 12 (read only) of 0x12 SPI register. The transmitter remains disabled until TxD changes to recessive state (i.e. high level) for more than 12µs. This error detection can be enabled by setting bit 1 of 0x08 SPI register.

- Permanent recessive LIN/BSS bus

  In case TxD changes to dominant (i.e. low level) state and RxD signal does not follow within $t_{rec(LIN)}$ = 40 µs (typical value) the transmitter will be disabled. The status bit won't be latched and can be read through bit 11 (read only) of 0x12 SPI register. The transmitter remains disabled until TxD changes to recessive state (i.e. high level) for more than 12 µs.

- Permanent dominant LIN/BSS bus

  In case the bus state is dominant (i.e. LIN/BSS at low level) for more than $t_{dom(LIN)}$ = 12 ms (typical value) a permanent dominant status will be detected. The status won't be latched and can be read through bit 13 (read only) of 0x12 SPI register. The transmitter will not be switched off. This error detection can be enabled by setting bit 1 of 0x08 SPI register.

Note: a normal wake up caused by a message on the bus will start the voltage regulator and the microcontroller to switch the application back to normal operation mode.

Wake-up by LIN/BSS bus

In power standby mode the device can receive a wake-up from LIN/BSS bus. Two different conditions can be differentiated:

- Normal wake-up

  A normal wake-up occurs when the device was previously asked to enter Power Stand-by mode while LIN/BSS bus was in recessive (i.e. high level) state. A level at LIN bus crossing V_{Thwkup} longer than t_{linbus} = 5 µs (typical value) will switch the device into Active mode and will turn the LIN/BSS receiver on as well to process coming message frames. An event is generated at the RxD pin.

- Wake-up from LIN/BSS bus in short-to-GND condition

  This wake-up condition isn't supported by the device and must be carefully avoided into application. In case the device was asked to enter Power Stand-by mode while LIN/BSS bus was recognized in dominant (i.e. low level) state, the command must be preceded by the LIN/BSS wake-up disable command (bit 12 in 0x04 SPI register).

When the device is in Active mode through any other available wake-up source, the LIN/BSS wake-up can be restored.

Compatible to LIN 2.1 for Baud rates up to 20 kBit/s (Up to 100 kbit/s for Flash Mode).

Table 13. Electrical characteristics pin "LIN/BSS"

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
LIN/BSS receiver							
1	V_{TXDLOW}	TxD input voltage dominant level	-	-	-	1.3	V
2	$V_{TXDHIGH}$	Input voltage recessive level	-	2.3	-	V_{DD}	V
3	V_{TXDHYS}	TxD input hysteresis	-	-	0.5	-	V
4	I_{TXDPU}	TxD input pull-up current	Active mode Pull-up to internal 3.3-V power rail V(TxD)=V(GND) I_{TXDPU}=-3.3 V/100 kΩ	-60	-33	-5	µA
5	I_{TXDPD}	TxD input pull-down current	Power Stand-by mode V(TxD) = V_{DD}	5	33	60	µA
6	V_{RXDLOW}	TxD output voltage dominant level	I(RxD) = 2 mA	-	0.2	0.5	V
7	$V_{RXDHIGH}$	TxD output voltage recessive level	I(RxD) = 2 mA	V_{DD}-0.4V	-	-	V
8	V_{Thdom}	Receiver threshold voltage recessive to dominant state	V(A+/B+) =12 V	0.4 V(A+/B+)	0.45 V(A+/B+)	0.5 V(A+/B+)	V
9	V_{Threc}	Receiver threshold voltage dominant to recessive state	V(A+/B+) =12 V	0.5 V(A+/B+)	0.55 V(A+/B+)	0.6 V(A+/B+)	V
10	V_{Thhys}	Receiver threshold hysteresis	V(B+/A+) =12 V, $V_{Threc} - V_{Thdom}$	0.07 V(A+/B+)	0.1 V(A+/B+)	0.175 V(A+/B+)	V
11	V_{Thcnt}	Receiver tolerance center value	V(B+/A+) =12 V, $(V_{Threc} + V_{Thdom})/2$	0.475 V(A+/B+)	0.5 V(A+/B+)	0.525 V(A+/B+)	V
12	V_{Thwkup}	Receiver wakeup threshold voltage	Wake-up by LIN/BSS active, Power Stand-by mode, recessive-to-dominant edge, V(A+/B+)-3.5 V<40 V	V(A+/B+) -3.5	V(A+/B+) -2.5	V(A+/B+) -1.5	V
13	t_{linbus}	Time for wakeup via bus	Wake-up by LIN/BSS active, Power Stand-by mode, recessive-to-dominant edge	-	5	-	µs
LIN/BSS DC parameters							
14	$I_{LINDomSC}$	Transmitter input current limit in dominant state	V(TxD)=V_{TXDLOW} V(LIN/BSS) =V(A+/B+) =33 V	40	100	180	mA

Table 13. Electrical characteristics pin "LIN/BSS" (continued)

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
15	$I_{bus_PAS_dom}$	Input leakage current at the receiver with pull-up resistor	V(A+/B+) =12 V [0x08].4 = LIN_PU_DIS = b0 V(TxD) = $V_{TXDHIGH}$ V(LIN/BSS) = V(GND)	-1	-	-	mA
16	$I_{bus_PAS_NoPU_dom}$	Input leakage current at the receiver w/o pull-up resistor	V(A+/B+) =12 V [0x08].4 = LIN_PU_DIS = b1 V(TxD) = $V_{TXDHIGH}$ V(LIN/BSS) = V(GND)	-0.85	-	-	mA
17	$I_{bus_PAS_rec}$	Transmitter input current in recessive state	V(TxD) = $V_{TXDHIGH}$ V(LIN/BSS) > 8 V V(A+/B+) < 33 V V(A+/B+)≤V(LIN/BSS)<V(A+/B+)+0.3	-	-	20	µA
18	$I_{bus_NO_GND}$	Input current in case of device GND loss	V(A+/B+)=V(GND) = 12 V 0 V < V(LIN/BSS) < 33 V	0	-	2	mA
19	I_{bus}	Input current in case of device A+/B+ loss	V(A+/B+) = V(GND) 0 V < V(LIN/BSS) < 33 V	-	-	3.5	mA
LIN/BSS transmitter							
20	V_{LINdom}	LIN/BSS bus voltage level in dominant state	V(TxD)=V_{TXDLOW} I(LIN/BSS) = 40 mA	-	-	1.35	V
21	V_{LINrec}	LIN/BSS bus voltage level in recessive state	V(A+/B+) =12 V V(TxD) = $V_{TXDHIGH}$ I(LIN/BSS) = -10 µA	0.8 V(A+/B+)	-	-	V
22	R_{LINup}	LIN/BSS bus pull up resistor	V(LIN/BSS) = V(GND)	20	40	60	kΩ
LIN/BSS timing							
23	SRf	LIN/BSS bus slew rate falling edge	V(A+/B+)=12V From 20% to 80% of V(LIN/BSS) (Rbus,Cbus) = (1 kΩ, 1 nF)	1	2	3	V/µs
24	t_{RXpd}	LIN/BSS-to-RxD receiver	t_{RXDpdf}=t[0,5*V(RxD)] - t[0,45*V(LIN/BSS)] t_{RXDpdr}=t[0,5*V(RxD)]- t[0,55*V(LIN/BSS)] t_{RXDpd}=max(t_{RXDpdr}, t_{RXDpdf}) CRXD = 20 pF V(A+/B+) = 12 V (Rbus,Cbus) = (1 kΩ,1 nF), (660 Ω,6.8 nF), (500 Ω,10nF)	-	-	6	µs
25	t_{RXDpd_sym}	t_{RXDpd} symmetry (t_{RXDpdr} Vs. t_{RXDpdf})	tRXpd_sym = tRXpdr – tRXpdf	-4	-	4	µs

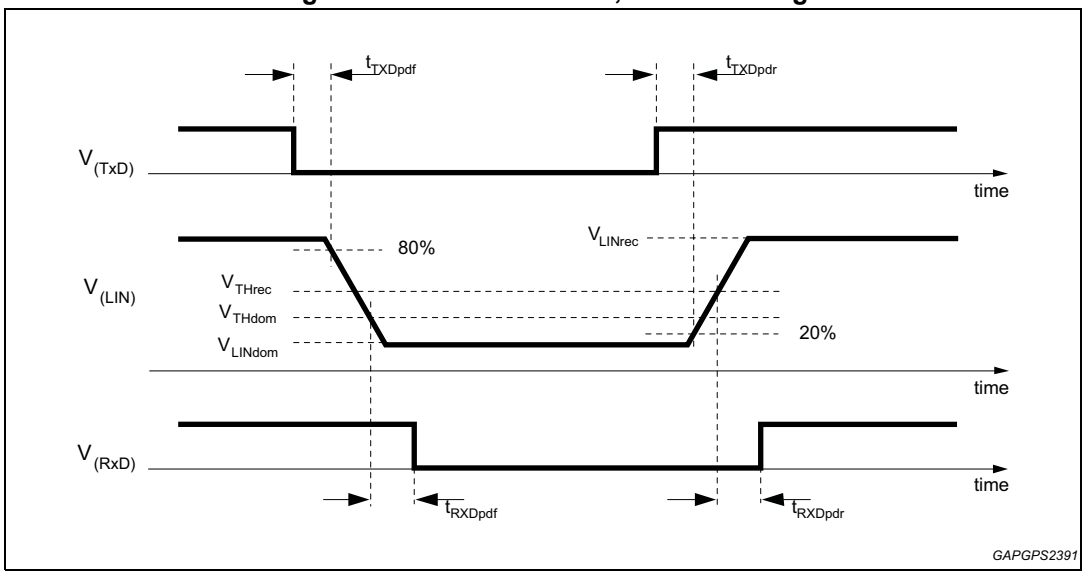
Table 13. Electrical characteristics pin "LIN/BSS" (continued)

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
26	t_{LINpd}	TxD-to-LIN/BBS transmitter propagation delay time	t_{LINpdf}=t[0,45*V(LIN/BSS)] - t[0,5*V(TxD)] t_{LINpdr}=t[0,55*V(LIN/BSS)] - t[0,5*V(TxD)] t_{LINpd}=max($t_{LINpdr,tLINpdf}$) V(A+/B+) = 12 V (Rbus,Cbus) = (1 kΩ,1 nF), (660 Ω,6.8 nF), (500 Ω,10 nF)	-	-	10	µs
27	t_{LINpd_sym}	t_{LINpd} symmetry (t_{LINpdr} Vs. t_{LINpdf})	t_{LINpd_sym}=t_{LINpdr}-t_{LINpdf}	-4	-	4	µs
28	D1	Duty cycle 1	THRec(max)=0,744*V(A+/B+) THDom(max)=0,581*V(A+/B+) V(A+/B+)={7, 18}V t_{bit} = 50 µs D1=$t_{bus_rec(min)}$/(2*t_{bit}) (Rbus,Cbus) = (1 kΩ,1 nF), (660 Ω,6.8 nF), (500 Ω,10nF)	0.396	-	-	-
29	D2	Duty cycle 2	TTHRec(min)=0,284*V(A+/B+) THDom(min)=0,422*V(A+/B+) V(A+/B+) = {7.6, 18} V t_{bit} =50 µs D2=t_{bus_rec}(max)/(2*t_{bit}) (Rbus,Cbus) = (1 kΩ,1 nF), (660 Ω,6.8 nF), (500 Ω,10nF)	-	-	0.581	-
30	D3	Duty cycle 3	THRec(max)=0,778*V(A+/B+) THDom(max)=0,616*V(A+/B+) V(A+/B+) = {7, 18}V t_{bit} = 96 µs; D3 = $t_{bus_rec(min)}$/(2*t_{bit}); (Rbus,Cbus) = (1 kΩ,1 nF), (660 Ω,6.8 nF), (500 Ω,10nF)	0.417	-	-	-
31	D4	Duty cycle 4	THRec(min)=0,251*V(A+/B+) THDom(min)=0,389*V(A+/B+) V(A+/B+) = {7.6, 18}V; t_{bit} = 96 µs; D4 = $t_{bus_rec(max)}$/(2*t_{bit}); (Rbus,Cbus) = (1 kΩ,1 nF), (660 Ω,6.8 nF), (500 Ω,10nF)	-	-	0.590	-
32	$t_{dom(TXD)}$	TXD input dominant time-out	-	-	12	-	ms

Table 13. Electrical characteristics pin "LIN/BSS" (continued)

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
33	$t_{dom(LIN)}$	LIN/BSS bus dominant time-out	-	-	12	-	ms
34	$t_{rec(LIN)}$	LIN/BSS bus recessive time-out	-	-	40	-	µs

Figure 9. LIN/BSS transmit, receive timing



4.3.6 Pin "DFM"

DFM is an output pin used to export a copy of the field PWM signal to external devices to allow a better system control. The DFM is internally connected to a low-side and to a high-side that can be independently configured by the µC by properly setting SPI write registers 0x04 and 0x05 [*12.4.13*] [*12.4.14*].

Bits 4 and 5 of SPI register 0x04 are available to set DFM output configuration:

Table 14. DFM output configuration

DFM bit1	DFM bit 0	DFM output configuration
0	0	DFM output disabled
0	1	Low side driver enabled
1	0	High side driver enabled
1	1	Push-pull enabled

Table 15. Electrical characteristics pin "DFM"

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	VML	Low-side saturation voltage	I(DFM) = 5 mA	0.90	1.15	1.40	V
2	IML_{lim}	Low-side current limitation	-	25	50	75	mA
3	VMH	High side saturation voltage	I(DFM) = -5 mA.Charge pump in OFF state	0.20	0.35	0.60	V
4	IMH_{lim}	High-side current limitation	-	-75	-50	-25	mA
5	$tML_{OCfilter}$	Low-side current limitation filter time	-	-	30	-	µs
6	$tMH_{OCfilter}$	High-side current limitation filter time	-	-	30	-	µs
7	VM_{TM}	Turbo mode threshold voltage	-	42	46	50	V

This pin can be used to notify the TURBO mode selection; TURBO mode bit (bit 4 of register 0x14, [*12.4.8*]) is set when the voltage on DFM pin goes above the VM_{TM} and V(A+/B+)< VB_{IntOvp}.

TURBO mode can be used by the application SW to skip all the delays to accelerate test procedures.

4.3.7 Pin "PH"

The PH pin is an input for the phase signal coming from alternator's stator output. The internal comparator detects the presence of the phase signal when V(PH) > VP_{HTh}. The squared signal is forwarded to a period measurement unit that provides suitable timing data to the µC to compute the rotor speed.

If the phase signal falls below the VP_{prTh1}/VP_{prTh2} threshold the phase regulation request (bit 12 of SPI register 0x13 is set [*12.4.7*]).

The device exits the stand-by mode when an activity is detected on PH pin (i.e. V(PH)>VP_{HTh}) independently on the status of other wake-up sources.

Table 16. Electrical characteristics pin "PH"

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	VP_{HTh}	High voltage comparator threshold	V(AUX_IN)=V(GND)	200	280	360	mV
2	VP_{LTh}	Low voltage comparator threshold	V(AUX_IN)=V(GND)	120	190	260	mV
3	tP_{SR}	Spike rejection time	Analogue filter	-	30	-	µs
4	$IP_{pull\text{-}dw}$	Pull-down current	V(PH) = 28 V	-	2	-	mA
5	$RP_{pull\text{-}dw}$	Passive pull-down resistance	-	-	20	-	kΩ
6	VP_{prTh1}	12-V phase regulation voltage threshold	[0x2].12 = SEL24V_EN=b0	7	8	9	V
7	VP_{prTh2}	24-V phase regulation voltage threshold	[0x2].12 = SEL24V_EN=b1	20	22.5	25	V

4.3.8 Pin "AUX_IN"

The AUX_IN pin can be used as auxiliary phase input signal in addition to PH pin. If not used, AUX_IN pin must be tied to ground. It's forbidden to replace AUX_IN pin with PH pin.

Table 17. Electrical characteristics pin "AUX_IN"

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	$VAUX_{HTh}$	High voltage comparator threshold	V(PH) = 1.150 V	200	280	360	mV
2	$VAUX_{LTh}$	Low voltage comparator threshold	V(PH) = 1.150 V	120	190	260	mV
3	$tAUX_{SR}$	Spike rejection time	Analogue filter	-	30	-	µs
4	$IAUX_{pull\text{-}dw}$	Pull-down current	V(AUX_IN) = 28 V	-	50	-	µA

4.3.9 Pin "GATE"

The external power MOS provides a PWM regulated current to flow from the system battery into the field coil for system voltage regulation. The GATE pin provides the necessary current to turn-on and turn-off the external power MOS.

The gate-source-voltage of the external power MOS is limited by the driver circuit.

In order to drive different kinds of external power MOS and to adjust the gate currents according to environmental changes (e.g. temperature, emission levels, excitation signal edges duration) the gate charging and discharging currents are programmable via SPI, register 0x03 [*12.4.12*].

When the voltage between DRAIN an SOURCE pins become greater than V_{SCdx} the device switches the external power MOS off, activating a fast gate discharging current.

Table 18. Electrical characteristics pin "GATE"

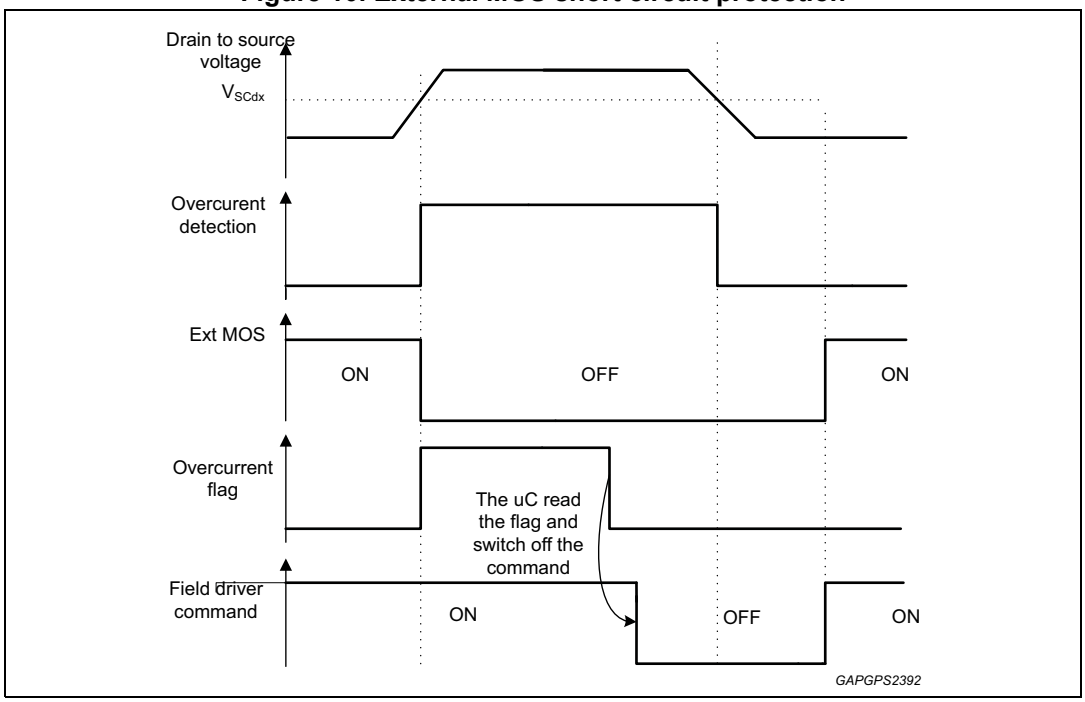
#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Drivers for external high/low side power MOS							
1	$I_{GHx(on)}$	Turn on current (SOURCE stage)	T_j = 25 °C	-	0 -> -11.55, -1.65 steps	-	mA
1	$I_{GHx(off)}$	Turn off current (SINK stage)	T_j = 25 °C		0 -> +11.55, +1.65 steps	-	mA
9	V_{GHxH}	High level voltage	V(A+/B+) = 6 V	V(SOURCE) +7V	-	-	V
			V(A+/B+) = 12 V	V(SOURCE) +9	V(SOURCE) +11	V_{SOURCE} +13	V
			V(A+/B+) = 24 V	V(SOURCE) +9	V(SOURCE) +11	V_{SOURCE} +13	V
10	R_{GSHx}	Gate-source passive discharge resistance	-	-	100	-	kΩ

4.3.10 Pin "DRAIN" and "SOURCE"

The device monitors the voltage between pins DRAIN and SOURCE in order to provide short circuit protection to the external Power MOS.

When the gate-to-source voltage exceeds the VGS_{th} value, the monitoring of the drain-to-source voltage becomes active and in case the voltage drop over the external power MOS exceeds the threshold voltage V_{SCdx} the gate driver will automatically switch the external MOS transistor off and the corresponding drain-to-source monitoring flag will be set in the SPI (bit 9 of read register 0x12 [*12.4.6*]). In order to turn the external MOS driver back on, the µC needs to read (and then clear) the diagnostic bit.

Figure 10. External MOS short circuit protection



The threshold voltage V_{SCdx} can be programmed in 4 steps between 0.5 V and 2 V with the SPI (write register 0x03).

The drain source monitoring has a filter time $T_{scfilter}$ and is only active when the corresponding gate driver is in source condition.

Table 19. Electrical characteristics pin "DRAIN" and "SOURCE"

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	V_{SCd1}	Drain-to source voltage threshold 1	-	0.4	0.5	0.6	V
2	V_{SCd2}	Drain-to source voltage threshold 2	-	0.9	1.0	1.1	V
3	V_{SCd3}	Drain-to source voltage threshold 3	-	1.35	1.5	1.65	V
4	V_{SCd4}	Drain-to source voltage threshold 4	-	1.8	2.0	2.2	V

Table 19. Electrical characteristics pin "DRAIN" and "SOURCE" (continued)

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5	VGS_{th}	Gate to source voltage threshold for drain-to source voltage monitoring	-	4.7	5	5.3	V
6	$t_{SCfilter}$	Short circuit filter time	Analogue filter	-	15	-	µs

4.3.11 Pin "F"

F pin is an input used to import a feedback of the field driver activity. The signal coming from field is compared to a threshold VF_{det} and forwarded to a µC timer port.

The F signal behavior is related to the system configuration (low side or high side).

Table 20. Electrical characteristics pin "F"

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	VF_{det}	Voltage threshold input comparator	-	-	4.2	-	V

4.3.12 Pin "CSA_IN"

The CSA_IN pin is an input dedicated to rotor current sensing in high side configuration only.

The rotor current can be measured by means of an external sense resistor.

The current sense amplifier output is connected to the µC AIN0 analog input.

R_{sense} must be inserted between MOS drain and A+/B+, keeping all connections towards CSA_IN A+/B+ EPONA pins as short as possible.

Figure 11. High-side configuration.

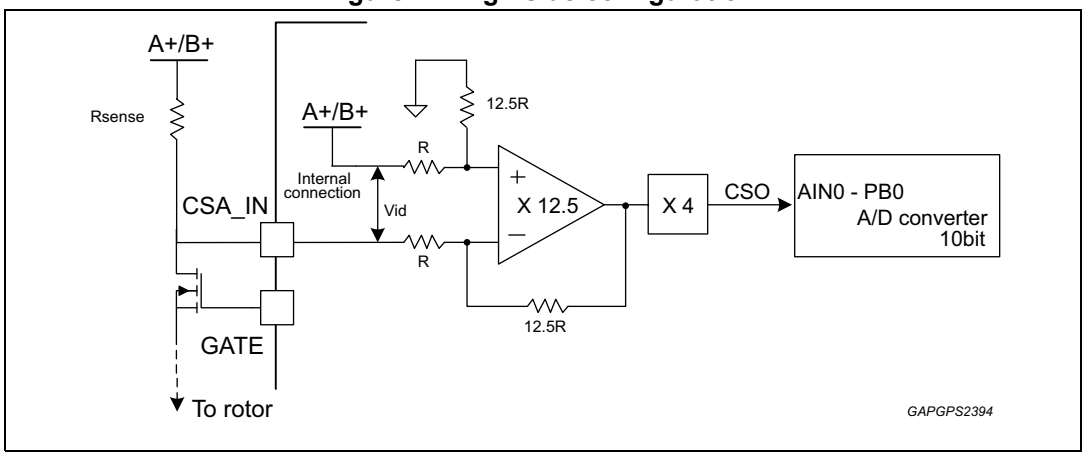


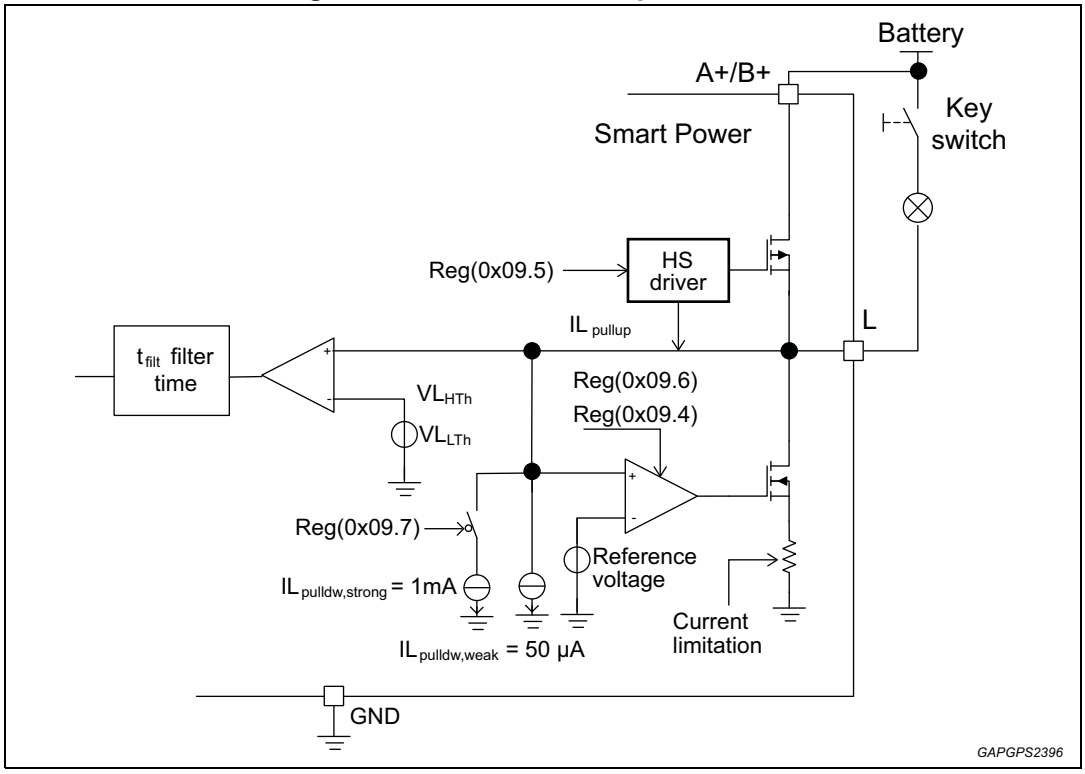
Table 21. Electrical characteristics pin "CSA_IN"

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	$Gain_{HS}$	Differential voltage gain	HS configuration	-	50	-	-
2	V_{IDM_HS}	HS differential input voltage	HS configuration $Gain_{HS}$ = 50 V/V ± 12% V_{ICM_HS} = 12 V V_{IDM_HS} = V(A+/B+)-V(CSA_IN)	15	-	90	mV
			HS configuration $Gain_{HS}$ = 50 V/V ± 12% V_{ICM_HS} = 24 V V_{IDM_HS} = V(A+/B+)-V(CSA_IN)	25	-	90	mV
3	V_{ICM_HS}	Common mode input voltage in high side configuration	High side configuration only	-	V(A+/B+)	-	V
4	V_{CSOH}	Output high level	HS configuration I(CSA_OUT) = -400 µA	V_{DD}-0.4	V_{DD}	-	V
5	V_{CSOL}	Output low level	HS configuration I(CSA_OUT) = 400 µA	-	0.1	0.4	V
6	R	CSA_IN series resistance	-	-	36	-	kΩ

4.3.13 Pin "L"

L pin is used to drive the fault indicator lamp and the optional auxiliary load relay (lamp drive mode).

Figure 12. L interface in lamp drive mode



The device exits the stand-by mode when the switch "Key" (see *Figure 12*) is closed (i.e. $V(L) > VL_{HTh}$).

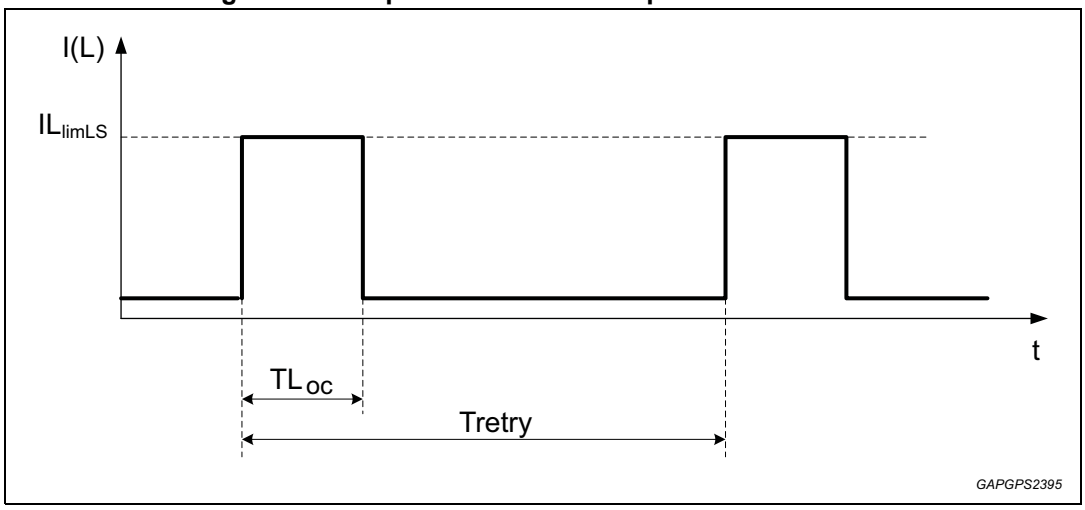
The lamp is driven by an internal low side N-channel MOSFET whereas the relay is driven by an internal high-side N-channel MOSFET.

The current in low side driver is limited to IL_{limLS} for a time tL_{OC}, then the driver is switched off and bit 2 of SPI read register 0x12 is set [*12.4.6*]; it can again be turned on by means of a µC command.

The maximum power dissipation allowed is P_{retry}.

The application software must wait the proper time before turning the lamp driver on again respecting the max power dissipation over a retry period.

Figure 13. Lamp driver overcurrent protection function



The minimum T_{retry} can be calculated in the following way:

$$T_{retry} = \frac{IL_{limLS} \cdot TL_{oc} \cdot V(A+/B+)}{P_{retry}}$$

The high side driver is switched off if the current overcomes the IL_{OVCHS} for $tL_{filterHS}$ time and bit 3 of SPI read register 0x12 is set [*12.4.6*].

Low-side and the high-side have independent commands through bits 4 and 5 of SPI write register 0x09 [*12.4.17*]. High-side has a protection in case its turn-on occurs with a V(L) voltage exceeding V(A+/B+) by VLrevHS. In this case the high-side is internally forced into off-state (high-side recirculation is not possible).

The L pin can be used for the RVC protocol (RVC drive mode) if the suitable configuration has been selected setting bit 6 of SPI write register 0x09 [*12.4.17*] to change the gate control in alarm condition for the low side MOS connected to the pin (drain voltage regulation at $VL_{RVC,\ fault}$.

To reduce, in lamp drive mode, the power dissipation in the lamp driver while it is on, the following strategy is implemented: after key-on, as soon as the L pin voltage overcomes VL_{HTh}, after t_{filt} time it is brought to VL_{sat} voltage (between its drain and source), then the key status is verified every t_{wait} time intervals within a $t_{chk,to}$ time window.

During this window, if the key is switched on the L voltage reaches the VL_{key_chk} value and immediately returns to the VL_{sat} value before the window expiration whereas, if the key is no longer active, the L voltage cannot increase and remains to VL_{sat} voltage level.

Note: *If a bulb is connected on the L pin, the in-rush phase can generate an over-current fault leading to the impossibility of bulb turn-on. In this case the software must use a "lamp soft switch-on procedure", see below example Figure 14.*

Figure 14. Flow chart of soft L switch-on

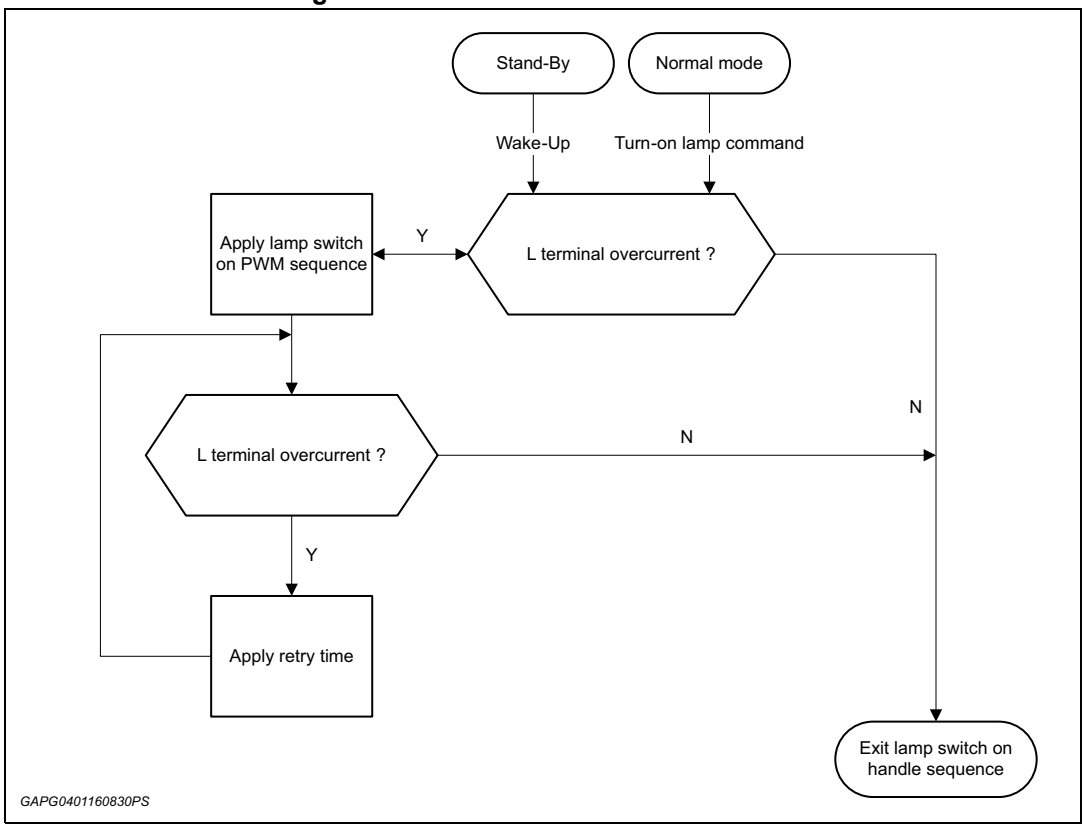


Figure 15. Example of soft L switch-on

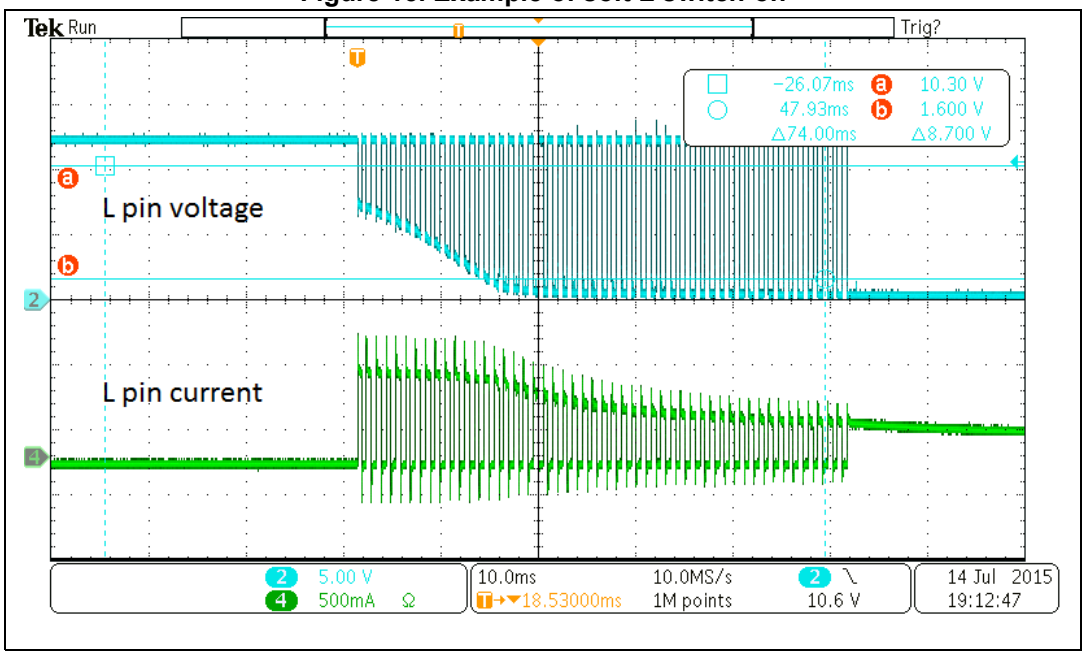


Figure 16. Fault indicator lamp drive in alarm condition and key engaged

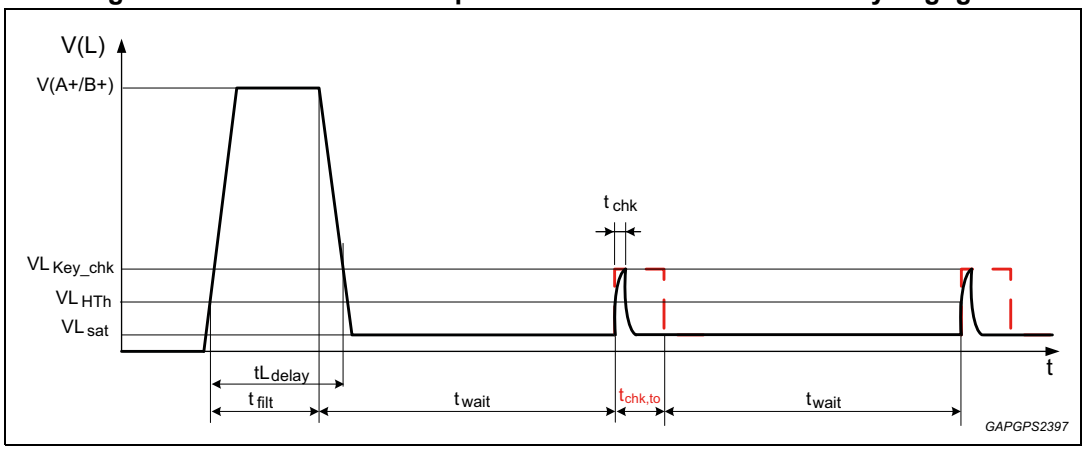


Table 22. Electrical characteristics pin "L"

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	VL_{sat}	Lamp driver saturation voltage	Lamp drive mode I(L) = 0.3 A (1)	-	-	0.5	V
2	$VL_{RVC,fault}$	RVC protocol alarm voltage	RVC drive mode I(L) = 10 mA (1)	-	-	1.0	V
3	VL_{Key_chk}	Lamp driver threshold voltage to check key presence	Lamp drive mode I(L) = 250 mA	-	1.0	-	V
4	$IL_{pulldw,weak}$	Weak pull-down current	Reg(0x09.4) = b0 Reg(0x09.7) = b1 I(L)<0 @ V(L) = 0.7 V $IL_{pulldw,weak} = -IL_{pullup} + I(L)$	-	50	-	µA
5	IL_{pulldw}	Pull-down current (total)	Reg(0x09.4) = b0 Reg(0x09.7) = b0 I(L)>0 @ V(L) = 0.7 V $IL_{pulldw}=IL_{pulldw,weak} + IL_{pulldw,strong}=$ $=-IL_{pullup} + I(L)$	-	1	-	mA
6	IL_{pullup} (1)	Pull-up current	Active mode Reg(0x09.5) = b0 IL_{pullup} = I(L)<0 @ V(L) = V(GND) Current from HS driver injected into L pin	-	-150	-	µA
7	$t_{chk,to}$	Key presence check time-out window	Lamp drive mode digital window time-out	-	-	1	ms
8	t_{chk}	Key presence check time window	Key switch engaged Analogue time I(L) = +250 mA	-	45	-	µs

Table 22. Electrical characteristics pin "L" (continued)

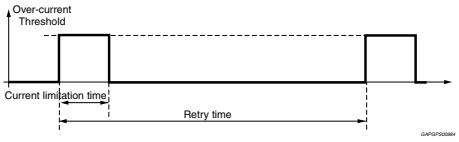
#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
9	t_{wait}	Key presence check time interval	Lamp drive mode, digital window time	-	40	-	ms
10	t_{filt}	Key-on filter time	Both lamp and RVC drive modes Analogue time V(L) = V(A+/B+) = 12 V	-	45	-	µs
11	VL_{HTh}	High voltage threshold key-ON receiver detector	-	0.7	0.8	0.9	V
12	VL_{LTh}	Low voltage threshold key-ON receiver detector	-	0.7	0.8	0.9	V
13	$IL_{lamp,limLS}$	Low-side lamp driver limitation current	Lamp drive mode V(L) = 12 V	0.5	-	1	A
14	$IL_{RVC,limLS}$ (2)	Low-side RVC driver limitation current	RVC drive mode V(L) = 5 V	70	-	150	mA
15	tL_{delay}	Turn-on delay time	Both lamp and RVC drive modes Analogue time V(L) = 12 V	-	-	120	µs
16	tL_{OC}	Maximum time duration of low-side linear current limitation	Lamp drive mode Digital window time 	-	-	2	ms
17	P_{retry} (3)	Max power dissipation during retrying period	For information only	-	-	300	mW
18	VH_{sat}	Relay driver saturation voltage	I(L) = -0.3 A	-	-	1	V
19	IL_{OVCHS}	High-side over-current threshold	-	-1	-	-0.4	A
20	$tL_{filterHS}$	High-side over current filter time	Analogue filter time	-	15	-	µs

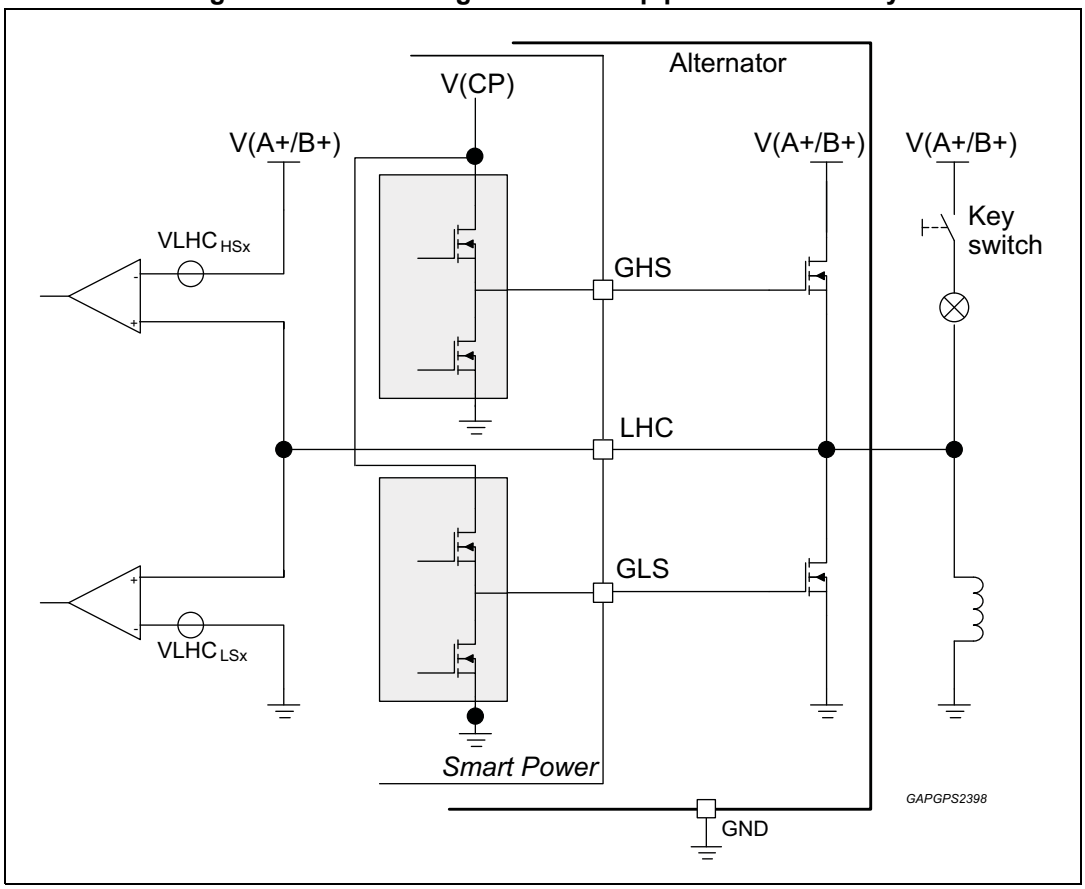
Table 22. Electrical characteristics pin "L" (continued)

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
21	$tL_{filterLS}$	Low-side current limitation filter time	Analogue filter time	-	40	-	µs
22	VL_{revHS}	High-side reverted bias protection over-drive	High-side turn-on $I(L)>IL_{pulldw}$ to cause high-side turn-off [i.e. V(L)-V(A+/B+)>0 V]	-	550	-	mV

1. In Power Stand-by mode the pull-up current is -5µA,min.
2. In case of L pin used for RVC protocol (RVC drive mode) I(L)= 20mA,max.
3. The microcontroller application software must take care to respect the value in item #17

4.3.14 Pin "GHS" and "GLS"

Figure 17. External high current lamp pre-driver circuitry



A high current external MOS driver is available in case the lamp/relay system requires more current than the internal MOS can deliver. The GHS and GLS pins are dedicated to drive the external MOSs' gates providing the necessary current.

The gate-source-voltage of the external Power-MOS is limited by the driver circuit.

Table 23. Electrical characteristics pin "GHS" and "GLS"

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Drivers for external high side power MOS							
1	$IGHS_{ON}$	Turn ON current (SOURCE stage)	T_j = 25 °C, V(LHC) don't care, V(GHS) = V(LHC)	-	-1.65	-	mA
2	$IGHS_{OFF}$	Turn OFF current (SINK stage)	T_j = 25 °C, V(LHC) don't care, V(GHS) - V(LHC) = VGHS	-	1.65	-	mA
3	$IGLS_{ON}$	Turn ON current (SOURCE stage)	T_j = 25°C, $VLHC_{fault}$<V(LHC)<$VLHC_{LSx}$, V(GLS)=V(GND)	-	-1.65	-	mA
4	$IGLS_{OFF}$	Turn OFF current (SINK stage)	T_j = 25 °C, V(LHC) don't care, V(GLS)-V(GND) = VGLS	-	1.65	-	mA
5	VGHS	High level voltage for gate of High-side driver	V(A+/B+) = 7 V CP_LOW = b0 V(LHC) = V(A+/B+) I(CP) = 0 µA	V(LHC) +5.5	-	-	V
			V(A+/B+) = 12 V CP_LOW = b0 V(LHC) = V(A+/B+) I(CP) = 0 µA	V(LHC) +9	V(LHC) +11	V(LHC) +13	V
			V(A+/B+) = 24 V CP_LOW = b0 V(LHC) = V(A+/B+) I(CP) = 0 µA	V(LHC) +9	V(LHC) +11	V(LHC) +13	V
6	VGLS	High level voltage for gate of Low-side driver	V(A+/B+) = 7 V CP_LOW = b0 VLHCfault<V(LHC)<VLHCLS2 I(CP)=0µA	7	-	-	V
			V(A+/B+) = 12 V CP_LOW = b0 $VLHC_{fault}$<V(LHC)<$VLHC_{LS2}$ I(CP) = 0 µA	9	11	13	V
			V(A+/B+) = 24 V CP_LOW = b0 $VLHC_{fault}$<V(LHC)<$VLHC_{LS2}$ I(CP) = 0 µA	9	11	13	V

The values in items 5 and 6 for VGHS and VGLS are valid only when the charge pump has been activated and it is working properly, otherwise they cannot be guaranteed.
The suggested external MOS used to drive the lamp is a self-protected PowerMOS like ST VND5N07.

4.3.15 Pin "LHC"

This pin must be used in place of L pin, to connect the lamp when externals MOS are used to drive the lamp and the auxiliary load relay. It acts like the L pin, when the switch "Key" (see *Figure 18*) is closed (i.e. V(LHC)>$VLHC_{HTh}$) the device exits stand-by condition. The presence of the key is detected in alarm condition by regulating the voltage on LHC pin to $VLHC_{fault}$=1.26 V (typ.), when suggested external low-side MOS is biased at its typical current.

The voltage of this pin is monitored respect to GND and A+/B+ in order to protect the external high side and low side MOS. When the external low side is turned on, if its drain (i.e. LHC) voltage becomes greater than $VLHC_{LSx}$ respect to GND the external power is switched off and bit 0 of SPI read register 0x12 is set [*12.4.6*].

When the external high side is turned on, if its drain (i.e. A+/B+) voltage becomes greater than $VLHC_{HSx}$ respect to LHC the external power is switched off and bit 1 of SPI read register 0x12 is set [*12.4.6*].

$VLHC_{LSx}$ and $VLHC_{HSx}$ thresholds can be selected by means of bits 0 and 1 of SPI write register 0x09 [*12.4.17*].

These diagnostic functions take place when GLS voltage with respect to GND is higher than $VGLS_{Th}$ parameter for low side MOS and when GHS voltage with respect to LHC is higher than $VGHs_{Th}$ parameter for high side MOS.

Table 24. Electrical characteristics pin "LHC"

#	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
1	$ILHC_{pulldw}$	Pull down current	Reg(0x09.2) = b0 Reg(0x09.7) = b0 I(LHC) > 0 @ V(LHC) = 0.7 V $ILHC_{pulldw}$=$ILHC_{pulldw,weak}$ + $ILHC_{pulldw,strong}$=-$ILHC_{pullup}$ + I(LHC)	-	1	-	mA
2	$ILHC_{pulldw,weak}$	Weak pull-down current	Reg(0x09.2) = b0 Reg(0x09.7) = b1 I(LHC) < 0 @ V(LHC) = 0.7 V $ILHC_{pulldw,weak}$=-$ILHC_{pullup}$ + I(LHC)	-	50	-	µA
3	$ILHC_{pullup}$	Pull-up current	Reg(0x09.3) = b0 $ILHC_{pullup}$=I(LHC)<0 @ V(LHC)=V(GND) Current from HS driver injected into LHC pin	-400	-	-	µA
4	$VLHC_{fault}$	LHC alarm voltage	External low-side PowerMOS: VND5N07 I(D)=ID_{typ}	-	1.26	-	V
5	$VLHC_{HTh}$	High Voltage Threshold key-on detector	-	0.8	0.9	1.0	V
6	$VLHC_{LTh}$	Low Voltage Threshold key-on detector	-	0.7	0.8	0.9	V
7	$TLHC_{delay}$	Turn-on delay time	-	-	-	100	µs

Table 24. Electrical characteristics pin "LHC" (continued)

#	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
8	$VLHC_{LS1}$	Low side drain voltage with respect to GND, threshold 1	Reg(0x09.0) = b1	1.8	2.0	2.2	V
9	$VLHC_{LS2}$	Low side drain voltage with respect to GND, threshold 2	Reg(0x09.0) = b0	1.35	1.5	1.65	V
10	$VLHC_{HS1}$	High side drain voltage with respect to LHC, threshold 1	Reg(0x09.1) = b1	0.85	1.0	1.2	V
11	$VLHC_{HS2}$	High side drain voltage with respect to LHC, threshold 2	Reg(0x09.1) = b0	1.35	1.5	1.65	V
12	$VGLS_{Th}$	Low side gate voltage respect to GND threshold	-	4.5	5.0	5.5	V
13	$VGHS_{Th}$	High side gate voltage respect to LHC threshold	-	4.5	5.0	5.5	V

Note: If GHS, GLH and LHC pins are not used they must be connected to GND: in this case the system recognizes that the lamp is connected to L pin and not to LHC pin.

4.3.16 Pin "RC"

Figure 18. RC pin connection on alternator

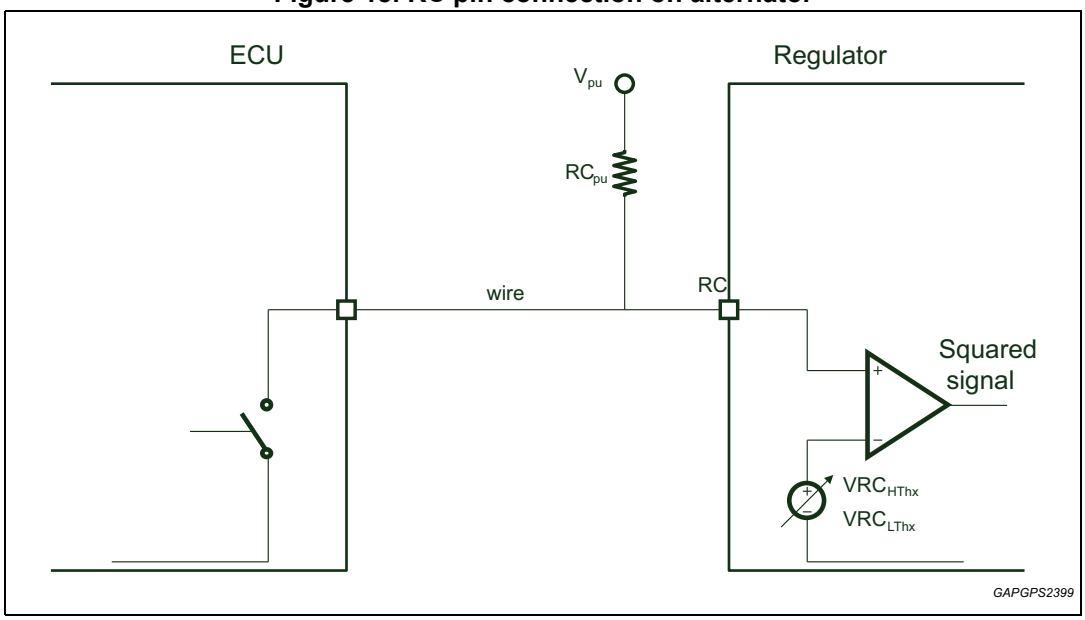
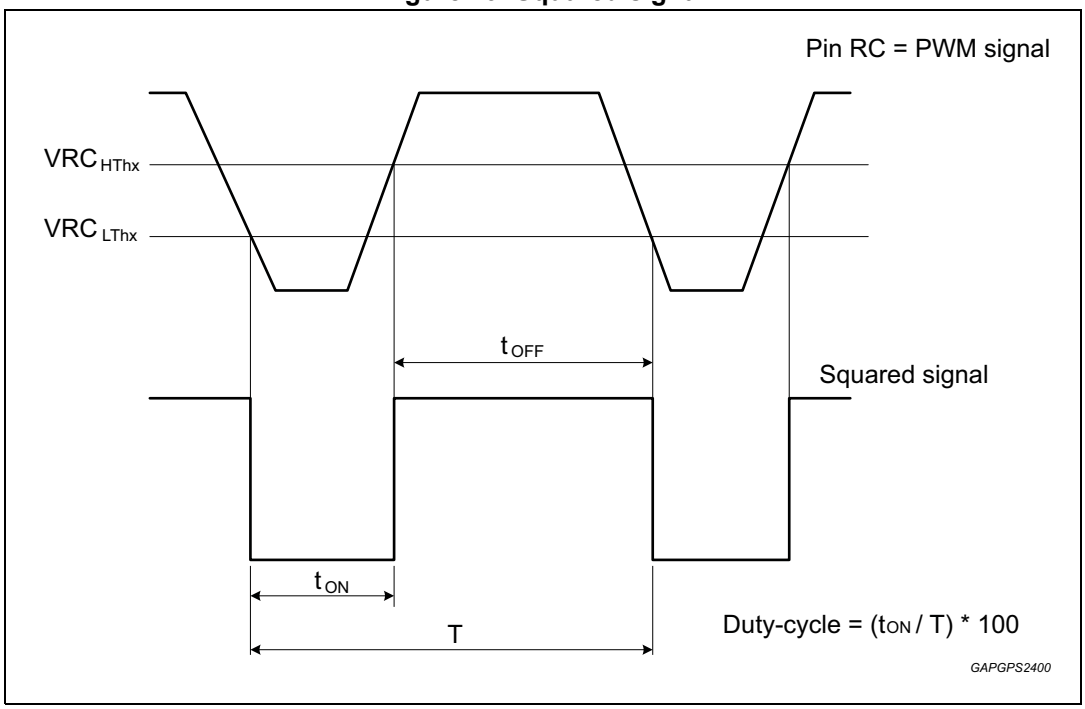


Figure 19. Squared signal



The RC pin is a protocol input to be used for both PCM and C-Term protocols; both external component RC_{pu} and the V_{pu} supply voltage must be chosen depending on the addressed protocol. In addition RC allows to hardware select, along with PROT_SEL pin, one among possible protocols that can be managed by regulator.

Table 25. Electrical characteristics pin "RC"

#	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
1	VRC_{HTh1} (1)	High level threshold voltage 1	-	3.1	3.3	3.5	V
2	VRC_{LTh1} (1)	Low level threshold voltage 1 (SPI configurable)	-	1.3	1.5	1.7	V
3	VRC_{hyst1}	Voltage threshold hysteresis 1	-	-	1.8	-	V
4	VRC_{HTh2} (1)	High level threshold voltage 2	SPI default	3.1	3.3	3.5	V
5	VRC_{LTh2} (1)	Low level threshold voltage 2 (SPI configurable)	SPI default	2.3	2.5	2.7	V
6	VRC_{hyst2}	Voltage threshold hysteresis 2	SPI default	-	0.8	-	V
7	VRC_{LTh_WU}	Low level threshold voltage for wake-up	Power stand-by mode RC falling edge wake-up	2.3	2.5	2.7	V
8	VRC_{HTh_WU}	High level threshold voltage for wake-up	Power stand-by mode RC rising edge wake-up	3.1	3.3	3.5	V
9	fRC_{VR}	Valid frequency range	-	100	-	500	Hz
10	tRC_{MIN}	Communication rejected with t_{ON} or t_{OFF} < tRC_{MIN}	-	10	20	35	µs

1. VRC_{HThx} and VRC_{LThx} parameters are in tracking

4.3.17 VREF_ADC

At VREF_ADC pad of the smart power it is available a precise voltage supplied to the AIN2 pin of the microcontroller [11] to allow a software calibration of the conversion obtained with the ADC.

Figure 20. Internal voltage reference for ADC

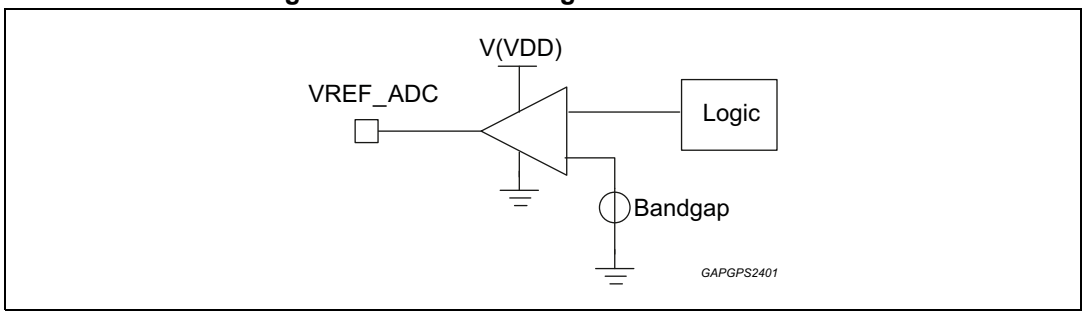


Table 26. Electrical characteristics "VREF_ADC"

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	$VREF_{ADC}$	Output voltage	-	4.257	4,3	4.343	V

4.3.18 Pin "PH_OUT"

The PH_OUT pin exports the filtered PH signal. PH_OUT is driven by a push pull output and must withstand 48V as absolute voltage.

Table 27. Electrical characteristics pin "PH_OUT"

#	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
1	$VPHO_L$	Low side saturation voltage	I(PH_OUT) = 5 mA	0.90	1.15	1.40	V
2	$IPHO_{L,LIM}$	Low-side current limitation	-	25	-	50	mA
3	$VPHO_H$	High side saturation voltage	I(PH_OUT) = -5 mA Charge pump in OFF state	0.90	1.15	1.40	V
4	$IPHO_{H,LIM}$	High-side current limitation	-	-50	-	-25	mA
5	$tPHO_L$	Low side current limitation filter time	Analogue symmetrical filter time	-	30	-	µs
6	$tPHO_H$	High side current limitation filter time	Analogue symmetrical filter time	-	30	-	µs

If the PH_OUT current exceeds the $IPHO_{X,LIM}$ value, then the bit 10 of SPI register 0x12 is set [*12.4.6*]

4.3.19 Charge pump output

The two-stage charge pump is supplied by A+/B+ pin. External flying capacitors are used to achieve the requested charge pump current capability. This current capability has a current limitation. In both standby mode and thermal shutdown the charge pump is disabled.

In case the charge pump output voltage V(CP) remains lower than $V_{CP,LOW}$ for longer than $t_{CP,LOW}$ parameter a charge pump low output fault condition is latched and bit 8 of SPI register 0x12 is set. [*12.4.6*]

The following capacitors are suggested: CP1 = 22nF, CP2 = 22nF, CP = 100nF. CP must be connected between CP and A+/B+ pins

Table 28. Charge pump output electrical characteristics

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	V_{CP}	Charge pump output voltage (both 12-V and 24-V systems)	V(A+/B+) ≥ 12 V I(CP) = -13 mA $I_{CP,TAIL}$ = 128 mA	V(A+/B+)+11	V(A+/B+)+13	V(A+/B+)+15	V
2	I_{CP}	Charge pump output current	I_{CP} = I(CP) < 0 assuring V(CP)-V(A+/B+)>$V_{CP,LOW}$ 45 mA ≤ $I_{CP,TAIL}$ ≤ 128 mA	-	-	-13	mA
3	$V_{CP,LOW}$	Charge-pump-low voltage threshold	-	V(A+/B+)+4.7	V(A+/B+)+5.4	V(A+/B+)+6.1	V

Table 28. Charge pump output electrical characteristics (continued)

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
4	f_{CP}	Charge pump oscillator clock frequency	No wobbling		800		kHz
5	$t_{CP,LOW}$	Charge-pump-low filter time	Digital filter time		10		µs
6	$I_{CP,TAIL}$	Charge pump tail current	Reg(0x03<13:12>) = b00 → 128mA (default)	45		128	mA

Charge pump must be switched on only in high side configurations because:

- a charge pump in off-state (default) asserts a charge pump low output fault condition
- the charge pump low output fault disables GATE pin driver (i.e. Field Power MOS is kept off)

Charge pump can be kept switched off in low side configurations. The charge pump generator tail current $I_{CP,TAIL}$ can be selected via SPI register 0x03 among the following typical values:

- 128 mA (Default)
- 77 mA
- 96 mA
- 45 mA

4.3.20 5-V (VDD) voltage regulator

The device contains a fully protected low drop voltage regulator designed for fast transient response.

The voltage regulator provides a 5-V stable VDD supply voltage at VDD/VDD_CAP pins and up to 50 mA continuous load current to supply the µC. In addition the 5-V regulator drives the internal 5-V loads as I/O structures. The VDD voltage regulator is protected against overload and over-temperature. The output voltage precision is ±2% (incl. temperature drift and line-/load regulation) for the whole output current operating range; the output voltage is stable for ceramic load capacitors greater than C_{VDD}= 680 nF (typ. ±10%) close to the device VDD_CAP pin.

Table 29. 5-V (VDD) voltage regulator electrical characteristics

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	V_{DD}	Output voltage	V(A+/B+) > 6V -50 mA ≤ I(VDD_CAP) ≤ 0 mA	-	5.0	-	V
2	εV_{DD}	Output voltage tolerance	V(A+/B+) > 6 V -50 mA ≤ I(VDD_CAP) ≤ 0 mA	-3.8	-	+3.8	%
3	C_{VDD}	Compensation capacitor	C_{VDD} to be connected as close as possible to VDD_CAP pin	612	680	1000	nF
4	I_{VDD}	Output current	Max continuous load current	-50	-	-	mA
5	$I_{VDDinrush}$	Inrush current capability	V(A+/B+) > 6 V V(VDD_CAP) > V_{RTL}	-50	-	-	mA

Table 29. 5-V (VDD) voltage regulator electrical characteristics (continued)

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
6	$I_{VDDpeak}$	Peak output current	V(A+/B+) > 6 V V(VDD_CAP)>V_{RTL}	-75	-	-	mA
7	$I_{VDDshort}$	Short circuit output current	Current limitation	-185	-130	-75	mA
8	V_{DDLiR}	Line regulation voltage	6 V ≤ V(A+/B+) ≤ 40 V I(VDD_CAP) = -30 mA constant during test	-3.8	-	+3.8	%
9	t_{TSD}	Deactivation time after thermal shut-down	-	0.8	1.0	1.5	ms
10	V_{DDFAIL}	Output voltage fail threshold	VDD_CAP pin forced when regulator is disabled	-	2	-	V
11	$t_{VDDSHTstart}$	Start-up short-to-ground detection time	V(VDD_CAP) < V_{DDFAIL} during regulator start-up	3.4	4.0	7.0	ms
12	$t_{VDDFAIL}$ (1)	Short-to-ground detection time	V(VDD_CAP) < V_{DDFAIL}	1.7	2.0	3.5	µs
13	dV_{DD}/dt	dV(VDD_CAP)/dt @ 5-V regulator switch-on	C_{VDD_CAP} = 680 nF I(VDD_CAP) = -3.5 mA Slope from: 0.5 V → 1 V 1 V → 0.9*V_{DD} If current limitation is reached, then the slope is controlled by current limitation and output capacitor	5	-	50	V/ms

1. If short-to-ground time exceeds $t_{VDDFAIL}$ then VDD regulator is permanently kept off and only a Power-On Reset (PORn) can restart functionality.

4.3.21 Reset output (nRST_SP)

In case VDD pin regulator is turned on and the voltage exceeds the VDD reset threshold voltage V_{RTH}, the reset pin nRST_SP is pulled up by STM8 internal pull-up resistor (nRST side) to VDD pin voltage after a 2ms (typ.) reset delay time. This is necessary to provide a suitable microcontroller startup phase when the system is switched on.

A reset pulse t_{RP} (typ. 2ms) is generated in case of:

- VDD pin voltage lower than V_{RTL} parameter
- Watchdog failure

Table 30. Reset output (nRST_SP) electrical characteristics

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	V_{RTH}	VDD reset threshold voltage	V(VDD) increasing	4.5	4.7	4.9	V
2	V_{RTL}	VDD reset threshold voltage	V(VDD) decreasing	4.4	4.6	4.8	V
3	V_{RTHyst}	VDD threshold voltage hysteresis	-	-	0.1	-	V
4	V_{RESETL}	nRST_SP low output voltage	V(VDD) > 1 V	-	0.2	0.4	V

Table 30. Reset output (nRST_SP) electrical characteristics (continued)

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5	t_{RR}	nRST_SP reaction time	I(nRST_SP) = 1 mA	-	15	-	µs
6	t_{RP}	nRST_SP pulse time	I(nRST_SP) = 1 mA	1.3	2.4	3.4	ms
7	t_{VDDUV}	VDD under-voltage filter time	Digital filter time	15	25	40	µs

4.3.22 Temperature sensor

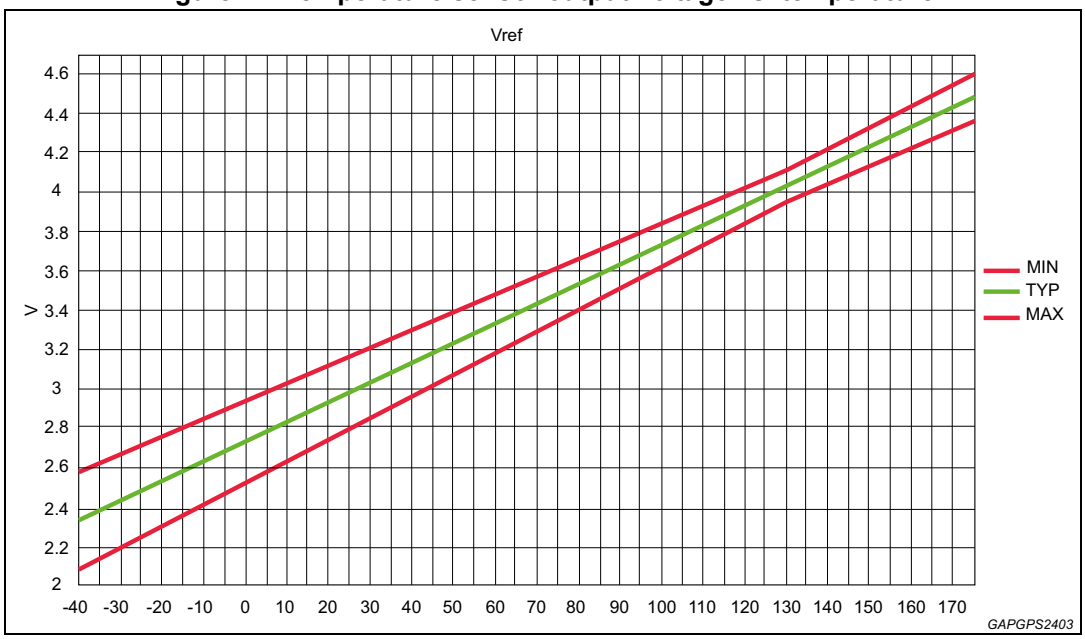
The sensor generates a voltage proportional to the absolute temperature of the die and makes it available at TEMP_OUT pin. It works over the whole temperature range, with a resolution of 10.5 mV ±1 mV/ºK.

The sensor output voltage is forwarded to pin AIN1 of the microcontroller [*11*] to allow temperature check.

Table 31. Temperature sensor (TEMP_OUT)

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	V_{TEMP}	Output voltage	T = 130 ºC	4.041	4.098	4.155	V
2	ε_{TEMP}	Voltage temperature drift	-40 °C ≤ T ≤ 130 °C	9.5	10.5	11.5	mV/K

Figure 21. Temperature sensor output voltage vs. temperature



Note: The voltage output of the sensor is related to the absolute temperature of the silicon junctions. Junction temperature and ambient temperature must be related taking into account the power dissipated by the device and the thermal resistance Rthje between the silicon and the environment around the application board.

Typical curve expressions (V_{TEMP_OUT} in V, T in °C):

$V_{TEMP_OUT} = \varepsilon_{TEMP} \cdot T + (V_{TEMP} - 130 \cdot \varepsilon_{TEMP}) = 10.5 \cdot 10^{-3} \cdot T + 2.733$

$T[°C] = \varepsilon_{TEMP}^{-1} \cdot V_{TEMP_OUT} + 130 - V_{TEMP} / \varepsilon_{TEMP} = 95.24 \cdot V_{TEMP_OUT} - 260.3$

5 Warning, alarms and faults

As general approach, the device provides embedded and automatic safety checks: in this way any critical condition is automatically managed by hardware without the need of the application software that has the task to signal the event and to apply, if possible, the proper restore procedure or to keep the system in a safe status.

5.1 System error flags

The following events, signaled in SPI read register 0x12 [*12.4.5*] are foreseen:

Table 32. System error flags

Bit	Description	Action
EXTP_OC	Excitation overcurrent [*4.3.10*]	HW and SW This flag has an effect also on CP_LOW bit
THSD	Overtemperature	None
PHO_OC	Phase out overcurrent [*4.3.18*]	HW and SW
CP_LOW	Charge pump low voltage [*4.3.19*]	HW and SW
APLUS_OV	Battery overvoltage [*4.3.1*]	HW and SW
APLUS_UV	Battery undervoltage [*4.3.1*]	None
LIN_PERM_DOM	LIN Permanent Dominant	HW and SW
LIN_TXD_DOM	LIN Dominant TXD	HW and SW
LIN_PERM_REC	LIN Permanent Recessive	HW and SW
DFM_OC	DFM overcurrent [*4.3.6*]	HW and SW
L_HS_OC	L High-side overcurrent [*4.3.13*]	HW and SW
L_LS_OC	L Low-side overcurrent [*4.3.15*]	HW and SW
LHC_HS_OC	LHC High-side overcurrent [*4.3.15*]	HW and SW
LHC_LS_OC	LHC Low-side overcurrent [*4.3.15*]	HW and SW

5.2 Lamp

The dashboard lamp (L or LHC) is used to notify faulty events to the driver.

At start-up the lamp driver is, by default, switched on and must be switched off just after crank.

The lamp must be activated if one or more of the following conditions are present:

- Excitation overcurrent (signaled in register 0x12)
- Battery overvoltage (signaled in register 0x12)
- Discrepancy between the applied excitation and the effective field excitation. A short to battery is not signaled by any flag of SPI registers but can be detected by comparing the two excitations [*4.3.11*]
- Phase error: persistent absence of phase signal [*12.4.7*]
- Phase regulation error: a persistent phase regulation request [*12.4.7*]

Any of the above condition, before causing a lamp warning, must be confirmed for a lamp confirmation time (hundreds of milliseconds).

When all above error conditions disappear, after a lamp-off confirmation time (hundreds of microseconds), the lamp is switched off.

6 Watchdog

In order to support system safety, the Smart Power logic provides an embedded windowed watchdog block able to operate either on the Smart Power analog blocks or on the microcontroller; this approach guarantees system control also when the microcontroller is not powered or doesn't work at all.

A watchdog is a unit designed to reset the system if a refresh operation is not accomplished within a specified time window: if the refresh is not done at all or if it is done before or later, the unit switches the power stage off and, if suitably configured, resets the microcontroller.

In this way the system is able to prevent either SW or HW errors:

- SW: the code flow is lost or in a deadlock
- HW: the microcontroller is stopped for any reason

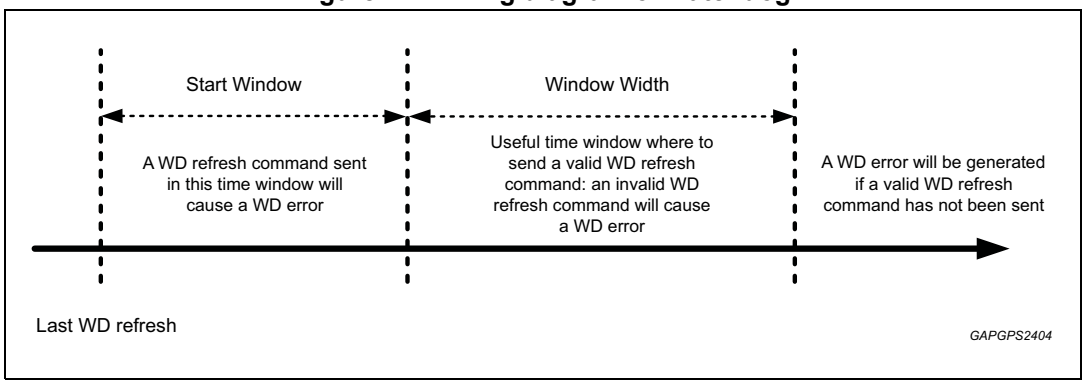
To handle the Smart Power watchdog the following parameters need to be defined:

- start window:
  - it is the time interval, after the last refresh, where the watchdog refresh cannot be accomplished. A refresh in this interval causes a watch dog error occurrence; this feature detects a condition where the code falls into a never ending loop including a refresh operation or an accelerated system clock
- operating window:
  - it is the time interval, after the start window, where the watchdog refresh must be accomplished. A refresh after this interval causes a watch dog error occurrence; this feature detects a condition where the code falls into a never ending loop excluding a refresh operation or a decelerated system clock
- windows resolution:
  - the watchdog timing resolution is configurable to better fit system needs
- refresh words:
  - to improve safety, when refreshing the watchdog, the system must alternate two different keywords

Watchdog configuration and refresh are handled by the microcontroller by writing suitable data in the SPI watchdog registers [*12.4.15*] [*12.4.19*].

The following picture shows a timing diagram of watchdog behavior:

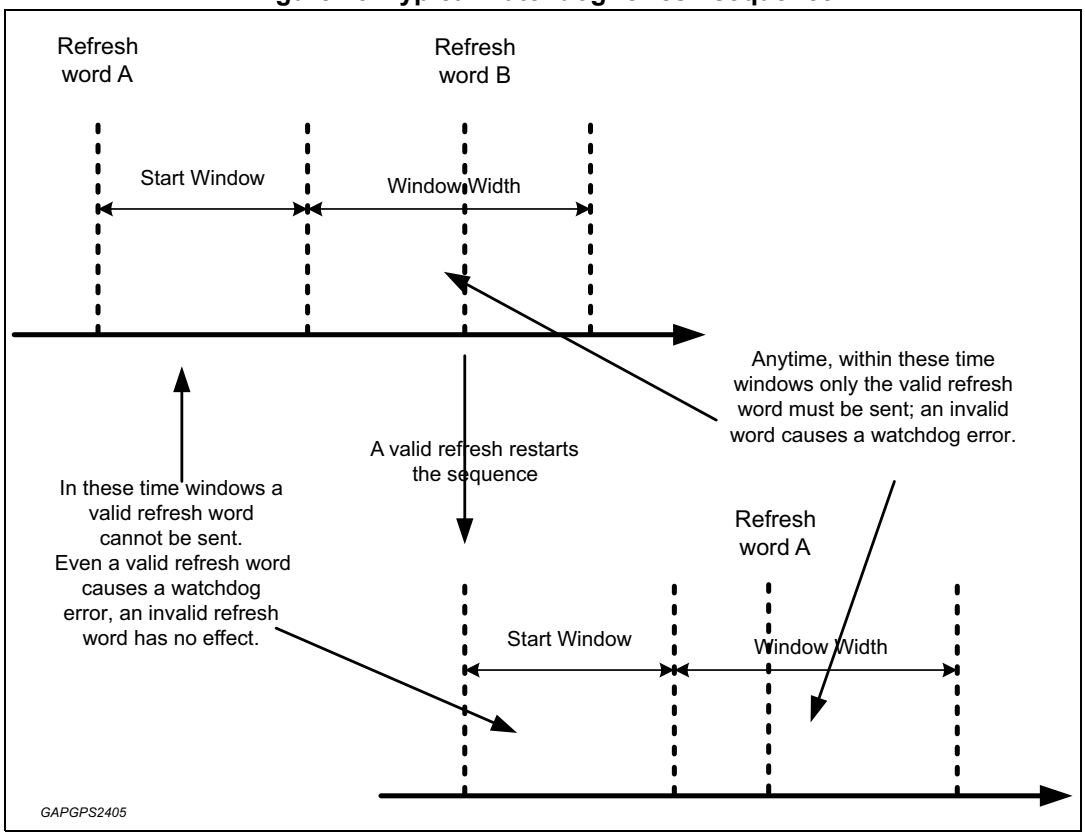
Figure 22. Timing diagram of watchdog



Once the watchdog has been correctly refreshed the above sequence restarts.

The following picture illustrates a typical watchdog refresh sequence.

Figure 23. Typical watchdog refresh sequence



6.1 Power stage watchdog handling

When a watchdog error occurs, the power stage is in the following conditions:

- Excitation off
- DFM off (the relevant SPI bits are cleared)
- LIN TX off (the relevant SPI bit is cleared)
- Lamp drivers:
  - on/off or off/on. The relevant outputs are conditioned by the relevant activation bits in SPI register (L_HS_EN and L_LS_EN) that cannot be on at the same time and with a default value of 1 for LS and 0 for HS. The effective lamp status is conditioned by L_KEY status.
- High current lamp drivers:
  - on/off or off/on. The relevant outputs are conditioned by the relevant activation bits in SPI register (LHC_HS_EN and LHC_LS_EN) that cannot be on at the same time and with a default value of 1 for LS and 0 for HS. The effective lamp status is conditioned by LHC_KEY status.

6.2 Watchdog error

A watch error occurs when the correct refresh word isn't sent in the correct time window; on its occurrence the following behaviors are possible:

- The Smart Power logic switches all the outputs off without resetting the microcontroller
- The Smart Power logic switches all the outputs off and resets the microcontroller

On startup the system has 500 ms to configure or to disable the watchdog before an error. The configuration is accomplished by writing the relevant SPI register.

On Power On reset the watchdog is configured to switch the outputs off leaving alive the microcontroller whereas on Wakeup the watchdog keeps the configuration available before entering the stand-by mode; this choice makes easier test and debug activities.

6.3 Watchdog freeze

The 500 ms watchdog startup window can be frozen by setting the INIT bit in the relevant register: this option can be useful to give some more time to the software to accomplish system initialization or to keep the watchdog frozen. In this condition it can be activated by clearing the INIT bit.

6.4 Persistent watchdog failure

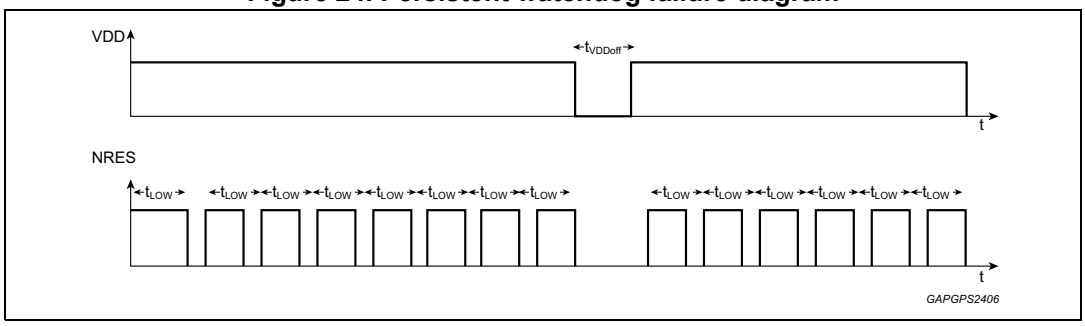
If, for any reason (HW or SW), the microcontroller is not in the condition to configure or to freeze the watchdog unit the Smart Power logic will apply two sequences of 7 reset trials before entering an idle state with the system definitively powered off. To eventually recover the system, if possible, it is necessary to do a power on reset.

The picture shows the sequence: VDD is applied and NRES is released: after 7 consecutive watchdog error occurrences VDD is released and a new 5 trials sequence is applied.

At the end of the sequence the Smart Power status depends on the key(s) status:

- All keys off: the Smart Power enters the stand-by status
- At least one key is on: the Smart Power remains alive with the power stages off

Figure 24. Persistent watchdog failure diagram



The watchdog reset count can be read and cleared through the relevant SPI register.

7 Thermal shutdown

Thermal shutdown is automatically accomplished by the Smart Power logic when the junction temperature reaches 200 degrees.

Table 33. Thermal shutdown electrical characteristics

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	Tsd	Thermal shutdown	Guaranteed by design	185	200	215	°C
2	Thyst	Hysteresis	-	3	6	9	

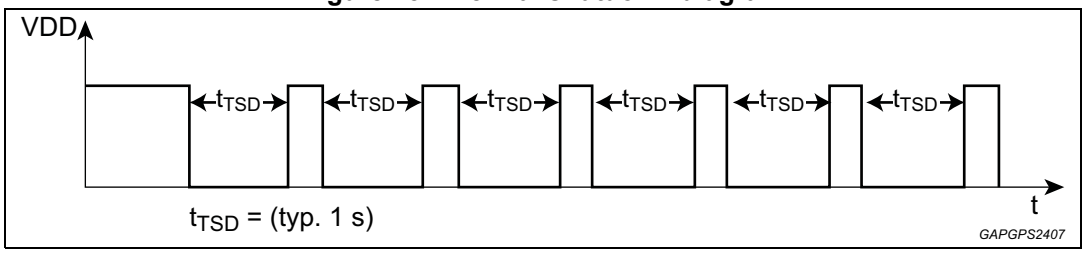
The system is brought in a safe condition and the microcontroller is powered off for a t_{TSD} time interval to allow the system temperature to decrease

After the delay the microcontroller is powered again and will find bit 5 of SPI read register 0x12 set.

After 6 trials the system is definitively powered off and can be resumed, if possible, only with a Power On Reset; the thermal shutdown reset counter can be read and cleared through the relevant SPI register.

A thermal shutdown condition should never occur and the device SW should keep under control the junction temperature and take the appropriate actions.

Figure 25. Thermal shutdown diagram



8 Turbo mode

During alternator and/or regulator production test it could be useful to reduce the system timings in order to save time; for this reason it is possible to set system in TURBO MODE status [see *4.3.6*].

In this condition the application SW should reduce or cancel internal timeouts (e.g. lamp alarm) thus accelerating the test procedures.

9 Communication configurations

The device supports different communication protocols on LIN/BSS pin for LIN and BSS protocol, L pin for RVC protocol and RC pin for PCM and C-TERM protocols.

All protocols are mutually exclusive and can be activated through a combination of pins and SPI bit settings; besides, LIN is available or not according to the device option.

The following table shows how to configure the system:

Table 34. How to configure the system

Protocol	Pin		SPI settings		Comment
	PROT_SEL	RC	lin_prot_in_use Reg 0x08 – bit3	RVC_EN Reg 0x09 – bit6	
LIN	0	0	1	X	LIN circuitry is enabled and LIN_TX_SP/LIN_RX_SP SmartPower pins are active. µC TIM1_CH3 pin is grounded If the LIN option is not available, the SmartPower LIN_RX_SP pin is grounded
BSS	0	1	1	X	BSS circuitry is enabled to carry the incoming signal to µC TIM1_CH3 pin LIN_RX_SP SmartPower pin is grounded
PCM C-TERM	1(1)	X	X	0	PCM/C-TERM interface is enabled to carry the incoming signal to µC TIM1_CH3 pin LIN_RX_SP SmartPower pin is grounded
RVC	1*	X	X	1	RVC interface is enabled to carry the incoming signal to µC TIM1_CH3 pin LIN_RX_SP SmartPower pin is grounded

1. PROT_SEL pin has an internal 100k pull-up resistor.

10 ADC channels

As already mentioned, 5 ADC channels of the µC are dedicated to monitor the system status; this chapter outlines some details about voltage ranges.

Table 35. ADC channels

Signal	Description	ADC channel	Range
TEMP	Temperature	1	0-5 V (4.88 mV/lsb) with 10 mV/°K – See relevant chapter [*4.3.22*]
VREF	Reference voltage	2	4.3 V ±1% [*4.3.17*]
CSA_IN	Current sense amplifier	0	0-100 mV [*4.3.12*]
B+	Battery voltage	5	0-20 V for 12 V configuration (19.5 mV/lsb), 0-40 V for 24 V configuration (39.1 mV/lsb) [*4.3.1*] [*4.3.2*]
SENSE	Field voltage	9	

11 Microcontroller non volatile memories

STM8AF6268 microcontroller embedded into EPONA has two non-volatile memories:

- Flash Program Memory (32k bytes): it is used to store the application code and calibration parameters (if any).
- EEPROM Data Memory (1k bytes): it can be used to store calibration data (if any) or some other data that need to be preserved.

The main parameters that characterize EEPROMs is the retention time and the maximum number of erase/write cycles: after the minimum guaranteed retention time and above the maximum number of erase/write cycles, the data stored in the memory are no longer guaranteed; for this reason, the program memory is trimmed to maximize the data retention time at the expense of erase/write cycles' number whereas the data memory is trimmed to maximize the erase/write cycles' number without compromising the retention time.

12 SPI interface

SPI interface is the communication channel between the microcontroller (Master) and the Smart Power (Slave).

It consists of an input shift register, an output shift register and four control signals. MOSI (Master Output Slave Input) is the data input line for the Smart Power input shift register. MISO (Master Input Slave Output) is the data output line from the Smart Power output shift register. SCK is the clock source input while CSN is the active low chip select input.

12.1 SPI protocol

All SPI communications are executed in exact 24-bit increments. The EPONA contains a data validation method through the SCK input to avoid transmission with a bit number not equal to 24 bits from being written to the device. The SCK input counts the number of received clocks and should the clock counter exceed or count fewer than 24 clocks, the received message is discarded without changes to internal registers.

The general format of the 24-bit transmission frame for SPI interface is shown here below:

Bit Position																								
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
GSW									RPAR	Data Bits														MISO
R/W	ADDR					RESERVED			WPAR	Data Bits														MOSI

Data to the device (i.e. MOSI) consists of:

R/W Read/Write selection bit

ADDR [4-0] Register address bits

RESERVED -

WPAR Parity bit

DATA [13-0] In write operation these bit are the data to be written to the destination register; in read operation these bits define a key (0x0A5) to enable the read and clear feature of some bits

Data returned from the device (i.e. MISO) consists of:

GSW Global Status word

RPAR Parity bit

DATA [13-0] Data bit read from the addressed register

The communications is controlled through CSN, enabling and disabling communication. When CSN is at logic high, all SPI communication I/O is tri-stated and no data is accepted. On the falling edge of CSN the data to be transmitted on MISO are latched and therefore the

latches are cleared. On the rising edge of SCLK the MOSI data are sampled and the MISO data are up-dated. The MOSI pin receives serial data from the master with MSB first. Likewise for MISO, data is read MSB first, LSB last. A failed transmission is indicated in the bit 23 of the MISO frame.

See next paragraphs for further details.

12.2 SPI electrical characteristics

12.2.1 CSN input

Table 36. CSN input electrical characteristics

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	$V_{in\ L}$	CSN voltage low level	-	-	-	1.3	V
2	$VCSN_H$	CSN voltage high level	-	2.3		V_{DD}	V
3	$VCSN_{Hyst}$	CSN hysteresis	-	-	0.4	-	V
4	$RCSN_{pu}$	CSN pull-up resistor	Pull-up in Active/pull-down in Stand-by. Pull-up to internal 3.3-V power rail. V(CSN)=V(GND) $RCSN_{PU}$ = -3.3 V/I(CSN)	-	100	-	kΩ

12.2.2 SCK, MOSI input

Table 37. SCK, MOSI input electrical characteristics

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	t_{set}	Delay time from standby to active mode	Switching from standby to active mode. Time until output drivers are enabled after CSN going to high.	-	160	300	µs
2	$V_{in\ L}$	Input voltage low level	-	-	-	1.3	V
3	$V_{in\ H}$	Input voltage high level	-	2.3		V_{DD}	V
4	$V_{in\ Hyst}$	Input hysteresis	-	-	0.4	-	V
5	$R_{in\ PD}$	Input pull-down resistor	V(in) = $V_{in\ L,MAX}$ $R_{in\ PD}$ = V(in)/I(in)	-	100	-	kΩ

12.2.3 MISO output

Table 38. MISO output electrical characteristics

#	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1	$VMISO_L$	MISO low level	I(MISO) = 2 mA	-	0.2	0.4	V
2	$VMISO_H$	MISO high level	I(MISO) = -2 mA	V_{DD}-0.5	-	V_{DD}	V
3	$IMISO_{Leak}$	MISO leakage current	Tri-state leakage V(MISO) = V(GND) V(MISO) = V(VDD)	-2	-	2	µA

12.3 SPI timing

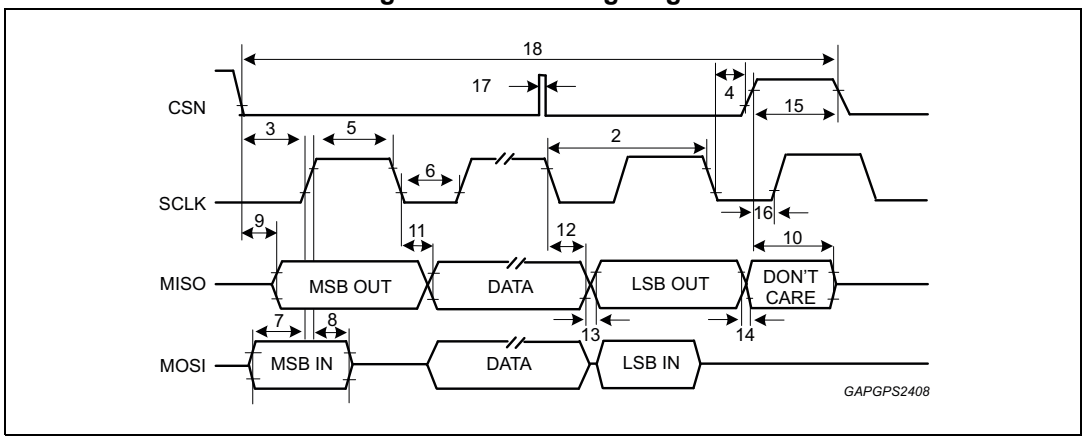
All electrical characteristics are valid for the following conditions unless otherwise noted.

T_j = -40 to 155 °C, 6 V ≤ VB ≤ 40 V

Table 39. SPI timing characteristics

#	Symbol	Parameter	Test condition	Min	Max	Units
1	f_{op}	Transfer frequency	Design Information	-	2	MHz
2	t_{sclk}	SCLK period	Design Information	500	-	ns
3	t_{lead}	Enable lead time	Design Information	1500	-	ns
4	t_{lag}	Enable lag time	Design Information	50	-	ns
5	t_{sclkhs}	SCLK high time	Design Information	200	-	ns
6	t_{sclkls}	SCLK low time	Design Information	200	-	ns
7	t_{sus}	MOSI input setup time	Design Information	20	-	ns
8	t_{hs}	MOSI input hold time	Design Information	20	-	ns
9	t_a	MISO access time	50	-	60	ns
10	t_{dis}	MISO disable time	50 pF load	-	100	ns
11	t_{vs}	MISO output valid time	50 pF load	-	66	ns
12	t_{ho}	MISO output hold time	50 pF load	0	-	ns
13	t_r	MISO rise time	50 pF load	-	30	ns
14	t_f	MISO fall time	50 pF load	-	30	ns
15	t_{csn}	CSN negated time	Design Information	1500	-	ns
16	t_{sh}	SCLK hold time	Design Information	20	-	ns
17	t_{csgrt}	CSN noise glitch rejection time	-	-	TBC	ns
18	T_{intfrm}	SPI inter-frame time	Design Information	15		µs

Figure 26. SPI timing diagram



12.4 SPI registers

L9924L registers, accessed through SPI interface, can be distinguished in

- READ ONLY REGISTER/BITS (RO): these registers/bits are used to give system status and configuration information.
  Status bits in read register contain the latched status of the relevant information.
- READ AND CLEAR REGISTER/BITS (RC): these registers/bits are used to give system status and configuration information.
  Status bits in read register contain the latched status of the relevant information.
  These bits are automatically cleared by a read operation if the data field of the SPI word transmitted by the microcontroller to the Smart Power is 0x0A5.
- READ/WRITE REGISTERS (RW): these register are used to set system configuration and parameters and to activate/deactivate system outputs.
  A write operation returns the previous register value.
- WRITE ONLY REGISTERS (WO)/BITS, when read back don't return the previously written value.

In some read/write registers there are read only bits.
Some registers are locked and a write access must be preceded by an unlock operation.

Table 40. SPI register

Register	R/W	ID	Description
SYSTEM / UNLOCK [*12.4.10*]	R/W	0x01	This register can be used to unlock some protected system configurations
SYSTEM OPERATION [*12.4.11*]	R/W	0x02	This LOCKED register is used to configure the system behavior
EXTERNAL POWER MOS [*12.4.12*]	R/W	0x03	This register is used to configure the parameter of the external power MOS driver
WAKE-UP SOURCES AND DFM GEN SETUP [*12.4.13*]	R/W	0x04	This register is used to enable or disable the wake-up sources and configure the parameter of the DFM signal (frequency and polarity)
DFMONITOR PWM D.C. [*12.4.14*]	R/W	0x05	This register is used to configure the parameter of the DFM signal duty cycle

Table 40. SPI register (continued)

Register	R/W	ID	Description
WATCHDOG CONFIG [12.4.15]	R/W	0x06	This LOCKED register is used to configure the Smart Power embedded watchdog
RESERVED – WRITE ONLY	W	0x07	-
CP-SPREAD-SPECTR & LINBITS SETTINGS [12.4.16]	R/W	0x08	This register is used to set charge pump modulation and some LIN parameter
DRV SETTINGS [12.4.17]	R/W	0x09	Output on/off
RESERVED	R/W	0x0A	-
TEST MODE STATUS [12.4.18]	R	0x0B	This register notifies the Smart Power working status
WATCHDOG REFRESH [12.4.19]	R/W	0x0F	This register is used to refresh the watchdog in order to prevent system reset
WAKE UP SOURCES [12.4.5]	R	0x11	This register contains a snapshot of system status at startup
LAMP LIN GENERAL STATUS [12.4.6]	R	0x12	This register contains diagnostic data
PH-SENSE [12.4.7]	R	0x13	This register contains the last phase measurement
WD_TS_RES_CNT [12.4.8]	R	0x14	Watch dog and thermal shutdown reset count
DEVICE INFO [12.4.9]	R	0x1F	Device ID, silicon revision, device settings

12.4.1 Register read operation

The transmit/receive 24 bits message pair of a register read operation is composed as follows:

Table 41. Register read operation

SPI TX message (MOSI)		SPI RX message (MISO)	
Bit	**Description**	**Bit**	**Description**
23	0 (Read cmd)	23-15	GSW
22-18	Read Register ID	14	Parity
17-15	0 - Reserved	13-0	Data
14	Parity (odd)	-	-
13-0	0x0A5 for read and clear operation	-	-

12.4.2 Register write operation

The transmit/receive 24 bits message pair of a register write operation is composed as follows:

Table 42. Register write operation

SPI TX message (MOSI)		SPI RX message (MISO)	
Bit	**Description**	**Bit**	**Description**
23	1 (Write cmd)	23-15	GSW
22-18	Write Register ID	14	Parity
17-15	0 - Reserved	13-0	Previous register content
14	Parity (odd)	-	-
13-0	Data to write	-	-

Parity

The parity bit is computed to give an odd number of bit set to 1 in the 24 bits message.

Lock/Unlock

Some registers are write protected in order to prevent writing of undesired data; to write such registers it is necessary to unlock them by writing the corresponding unlock bit in register 0x01.

After unlock the protected register it must be immediately written! Any read/write access to any register resets the lock status.

12.4.3 GSW: global status word

At any read or write access, the first 9 upper bits of the returned 24 bits frame contain the Global Status Word that summarizes some status bits:

Table 43. GSW: global status word

GSW Bit	Frame Bit	Register name	Reset value	Description
8	23	PREV_SPI_FAILED	0	Prev. SPI Frame Discarded
7	22	LIN_EVENT	0	LIN event occurrence (LIN_PERM_DOM | LIN_TXD_DOM | LIN_PERM_REC)
6	21	EXC_OC	0	Excitation overcurrent (EXTP_OC)
5	20	L/LHC_OC	0	L or LHC overcurrent (L_LS_OC or L_HS_OC or LHC_LS_OC or LHC_HS_OC)
4	19	DFM_PHASE_OUT_OC	0	DFM or phase out overcurrent (DFM_OC | PHO_OC)
3	18	CP_LOW	0	Charge pump low (CP_LOW)
2	17	KEY_GEN	0	L_key OR LHC_key OR IGNT_KEY

Table 43. GSW: global status word (continued)

GSW Bit	Frame Bit	Register name	Reset value	Description
1	16	APLUS	0	A+ overvoltage or undervoltage (APLUS_OV | APLUS_UV)
0	15	PHsense New Measure is Available	0	A valid phase measurement value is available. This bit is cleared by a read operation of register 0x13 After power on, this bit is set also at the first rising edge of the input phase signal: in this case the register data are don't care and must be discarded

12.4.4 SPI errors

An SPI error occurs after at least one of the following conditions is matched:

- Parity error
- Invalid address
- Write only register read attempt
- Wrong bits number

The PREV_SPI_FAILED bit of GSW notifies an error in the previous received SPI frame.

12.4.5 WAKEUP SOURCE register [0x11]

This registers returns some information about wakeup/reset exit status condition and KEY input status

Table 44. WAKEUP SOURCE register [0x11]

Bit	Register name	Reset value	Description
13	RESERVED	-	-
12	IGNIT_KEY(1)	-	0: IGNIT input OFF 1: IGNIT input ON
11	L_KEY(1)	-	0: L input OFF 1: L input ON Always 0 if RVC_EN = 1 (bit 6 of register 0x08)
10	LHC_KEY(1)	-	0: LHC input OFF 1: LHC input ON
9	VDD_UV	0 (RC)	The previous µC reset has been caused by a VDD undervoltage event (< 4.7V)
8	RESERVED	-	-

Table 44. WAKEUP SOURCE register [0x11] (continued)

Bit	Register name	Reset value	Description
7	WDG_FAIL_SWT_OFF_PWR_STG	0 (RC)	If the watchdog has been configured to switch the power off instead to reset the microcontroller, this bit notifies that the power stage has been switched off after a watchdog failure occurrence (see register 0x02) This bit must be cleared with a read and clear operation to enable the field excitation
6	WDG_FAIL_RESET_UP	0 (RC)	When 1 notifies that the system reset has been caused by the SmartPower watchdog
5	WKUP_BY_L	0 (RO)	Wakeup source Notification These bits contain the latched status of the relevant input pin after a system wake-up. If more than one bit is set the wake-up source signal cannot be unambiguously identified
4	WKUP_BY_LHC	0 (RO)	-
3	WKUP_BY_IGNIT		
2	WKUP_BY_PH		
1	WKUP_BY_RC(2)		
0	WKUP_BY_LIN(2)		

1. These bits report the current status of the relevant input without any latch logic.
2. If the wakeup is triggered by a protocol line edge it is possible that the microcontroller loses the first data frame because of the time it takes to wakeup and to initialize the whole system; the protocol transmitter node must take into account this eventuality.

Warning: if the relevant wake-up source are disabled (WKUP_SOURCE_IGNIT_DISABLE, WKUP_SOURCE_LHC_DISABLE and WKUP_SOURCE_L_DISABLE bits of register 0x04) these bits are cleared independently of the effective status of the pins

12.4.6 LAMP LIN GENERAL STATUS register [0x12]

This register returns system status flags:

- 0: the notification is not present
- 1: the notification is present. The register read operation clears the notification

Table 45. LAMP LIN GENERAL STATUS register [0x12]

Bit	Register name	Reset value	Description
13	LIN_PERM_DOM	0 (RC)	LIN Permanent Dominant
12	LIN_TXD_DOM	0 (RC)	LIN Dominant TXD
11	LIN_PERM_REC	0 (RC)	LIN Permanent Recessive
10	PHO_OC [*4.3.18*]	0 (RC)	Phase out overcurrent (low side or high side)
9	EXTP_OC(1) [*4.3.10*]	0 (RC)	External MOS overcurrent
8	CP_LOW [*4.3.19*]	1 (RC)	Low Voltage on CP pin After a wakeup this bit is 1 because the CP_ENABLE (bit 11 of register 0x03 [*12.4.12*) has not yet been set. To clear this bit, the CP_ENABLE must be set, then the status register must be read with the clear option after a suitable time interval.
7	APLUS_OV [*4.3.1*]	0 (RC)	Overvoltage A+
6	APLUS_UV	0 (RC)	Undervoltage A+
5	THSD	0 (RC)	Overtemperature(2)
4	DFM_OC(1)	0 (RC)	Over current DFM (high side or low side driver)
3	L_HS_OC(1) [*4.3.13*]	0 (RC)	L High side driver overcurrent
2	L_LS_OC (1)[*4.3.13*]	0 (RC)	L Low side driver overcurrent
1	LHC_HS_OC(1)	0 (RC)	LHC High side driver overcurrent
0	LHC_LS_OC(1)	0 (RC)	LHC Low side driver overcurrent

1. A driver is immediately switched off at the occurrence of an overcurrent event and remains “locked” until the suitable restore procedure is applied:

   - Switch the output off with the relevant SPI command (L, LHC and DFM) or remove the excitation signal (power MOS)

   - Clear the alarm flags with the read and clear command

   - Switch the output on with the relevant SPI command (L, LHC and DFM) or apply the excitation signal (power MOS)

2. The over-temperature condition automatically causes a power off (thermal shutdown): the THSD bit can be read by the microcontroller at power up in order to know the history of the system; if the bit is set it means that the previous power off was caused by an over-temperature occurrence.

12.4.7 PH-SENSE register [0x13]

L9924L system provides a Phase Period Measurement block: the input phase signal (or signals) is (are) suitably filtered and processed.

Table 46. PH-SENSE register [0x13]

Bit	Register name	Reset value	Description
13	PH-Sense Measurement Timed - OUT	0	This bit indicates the absence of rotation or a too slow rotation The timeout is notified to the microcontroller by setting bit 0 of GSW word. The flag is cleared by reading this register
12	PHASE_REGULATION_REQUEST	1	This bit, valid only when a new phase value has been notified (GSW.0=1) indicates that the phase input voltage has been below the threshold for at least 4 periods.
11	Reserved	-	-
10-0	RPM_PHASE_PERIOD	-	This register contains the phase sense measurement expressed into 64 us units. A new available measurement or is notified to the microcontroller by setting bit 0 of GSW word. The new measurement notification is cleared by reading this register

The logic measures the time interval (PhaseMeas), in 64 us units, corresponding to 4 periods (PhasePeriod = PhaseMeas / 4) of the phase signal: this time can be easily converted into the rotor speed according to the number of pole pairs (N_p):

$$\text{RotorSpeed (rpm)} = \frac{60}{Np \cdot PhasePeriod} = \frac{60}{Np \cdot (PhaseMeas{:}4)} = \frac{240}{Np \cdot PhaseMeas} = \frac{240}{Np \cdot PhaseVal \cdot 64\mu s}$$

For example, at 3000 rpm, in a system with 6 pole pairs, we obtain the following data:

Table 47. Example in a system with 6 pole pairs at 3000 rpm

Parameter	Value
Rotor frequency	50 Hz (3000 rpm / 60)
Phase frequency	300 Hz (50 * 6)
Phase period	3.33 ms
4 phase periods	13.33 ms
Phase measurement	208 (13.33 ms / 64 µs)

Therefore, reading the 208 value and applying the above formula we can compute:

$RotorSpeed_{rpm}$ = 240 / (6 * 208 * 64 µs) ˜= 3004 rpm

The following table shows the RPM ranges corresponding to different pole pairs values:

Table 48. RPM ranges corresponding to different pole pairs values

Pole pairs	Rotor speed - RPM		2x Ratio Motor speed - RPM		3x Ratio Motor speed - RPM	
	min	max	min	max	min	max
4	458	117187	229	58593	153	39062
5	366	93750	183	46875	122	31250
6	305	78125	152	39062	102	26041
7	262	66964	131	33482	87	22321
8	229	58593	114	29296	76	19531
9	204	52083	102	26041	68	17361
10	183	46875	91	23437	61	15625

The maximum RPM values don't correspond to the minimum value of the register (1) but to the 64 µsec timer resolution: it can be considered a sort of 15.625 kHz sampling rate thus giving a maximum input signal frequency of roughly 8.3 kHz.

Incoming phase signal with a frequency under the specified minimum values lead to a timeout condition, incoming phase signal with a frequency above the specified maximum values lead to wrong results.

12.4.8 WATCHDOG / THERMAL SHUTDOWN RESET COUNT register [0x14]

Any reset event triggered by the watch dog or by the thermal shutdown circuitry increment a counter in this register.

If needed, at system boot the SW can read the register to know the system history.

Table 49. WATCHDOG / THERMAL SHUTDOWN RESET COUNT register [0x14]

Bit	Register name	Reset value	Description
13-12	Reserved	-	-
10-8	THERMAL_SHUTDOWN_EVENTS_COUNT	0 (RC)	Thermal shutdown reset counter
7-5	Reserved	-	-
4	TURBO_MODE	0 (RO)	When set, this bit notifies that the Smart Power has detected the turbo-mode configuration
3-0	WDG_uC_RESET_EVENTS_COUNT	0 (RC)	Watch dog reset counter

12.4.9 DEVICE ID register [0x1F]

This register contains chip and communication protocol configuration:

Table 50. DEVICE ID register [0x1F]

Bit	Register name	Reset value	Description
13	Reserved	-	-
12	Reserved	-	-
11	LIN_PROT_DENIED_OTP	RO	0: LIN available 1: LIN not available
10	APPL_24V_DENIED_OTP	RO	0: 24V supported 1: 24V not supported
9	ProtSel	RO	PROT_SEL pin image
8	RC	RO	RC pin image: if the pin is used for a communication protocol its value follows the status of the line
7-0	Sil_Revision	RO	Silicon revision

12.4.10 SYSTEM / UNLOCK register [0x01]

This register contains some unlock bits to allow a write access to the relevant bits of register 0x02 or register 0x06.

Table 51. SYSTEM / UNLOCK register [0x01]

Bit	Register name	Reset value	Description
13	Reserved	-	-
12	UNLOCK_SEL24V_EN	0 (WO	Write 1 to enable the write access to SEL24V_EN bit of register 2
11	Reserved	-	-
10	UNLOCK WDG Config REG_06	0 (WO)	Write 1 to enable the write access to the WDG Config register (0x06)
9	UNLOCK WDG: Init Time-Out Disable	0 (WO)	Writing '1' to this bit enables a write access to the WDG INIT ENABLE bit of System Operation register (0x02)
8	UNLOCK_WDG_FAIL_REST_µC	0 (WO)	Writing '1' to this bit enables a write access to the WDG_FAIL_REST-uC bit of System Operation register (0x02)
7-5	Reserved	-	-
4	UNLOCK EPONA Cfg-REGs SW Reset Capability	0 (WO)	Writing '1' to this bit enables a write access to the SW_RESET bit of System Operation register (0x02)
3-1	Reserved	-	-
0	UNLOCK_SYST_POWER_OFF	0 (WO)	Writing '1' to this bit enables a write access to the POWER_OFF bit of System Operation register (0x02)

The bits of this register are write only (WO) and their value isn't latched: any successive read attempt returns 0.

A write access to a locked bit must be preceded by the relevant unlock operation: if a read/write access to any other register is done the unlock condition is lost and a write access to a locked bit will have no effect.

12.4.11 SYSTEM OPERATION register [0x02]

By writing this register it is possible to configure the system behavior related to watchdog and reset. The configuration bits are locked and any write access must be preceded by an unlock operation.

Table 52. SYSTEM OPERATION register [0x02]

Bit	Register name	Reset value	Description
13	Reserved	-	
12	SEL24V_EN (LOCKED)	0	Set this bit to configure 24V support. This option is possible only if the relevant OTP bit is set
11	Reserved	-	
10	Reserved	-	
9	WDG_INIT_ENABLE (LOCKED)	0/1(1)	Write 1 to disable the initial 500 ms watchdog timeout
8	WDG_FAIL_REST_uC (LOCKED)	0/1(1)	When 0 a watchdog failure can only switch the power stage off, when 1 a watchdog failure switches the power stage off and resets the microcontroller
7-5	Reserved	-	
4	Apply EPONA Cfg-REGs SW Reset (LOCKED)	0(2)	Write 1 to force a default condition (SW RESET) corresponding to the reset status. This command doesn't clear the content of bits 8 and 9 and doesn't clear the content of read and read and clear bits.
3-1	Reserved	-	
0	POWER_OFF (LOCKED)(3)	0	Writing 1 the system enters standby mode if no key input is active.

1. On power on reset the value of these bit is 0, on wakeup the bits maintain the last programmed values (if any); these bits are not cleared by the SW reset command.
2. After a SW reset the Watchdog is also initialized and, if not previously disabled, must be programmed and refreshed to avoid a watchdog error occurrence.
3. The POWER_OFF command is ignored if at least one, among the enabled wake-up sources (see register 0x04) is active. It's up to the application SW ti implement the appropriate power off sequence

12.4.12 External POWER MOS register [0x03]

This register is used to configure Smart Power behavior

Table 53. EXTERNAL POWER MOS register [0x03]

Bit	Register name	Reset value	Description
13-12	CP_ITAIL	0	This two bits field set the charge pump generator tail current: 0. 128 mA 1. 77 mA 2. 96 mA 3. 45 mA An application has to select the appropriate current as trade-off between the needed current and the switching noise [*4.3.19*]
11	CP_Enable(1)(2)	0	To ensure low current in standby coming from µC (POFF).
10	UV_DIS	0	To disable B+ Undervoltage Detection In some conditions the regulation strategy (LRC, Phase regulation, etc) could lead to an undervoltage status: in order to avoid an immediate stand-by condition activation, the undervoltage detection must be disabled
9	VCLTH_SEL	0	RC Protocol V Low Level Threshold selection
8	EXTP_LS	0	Excitation Low Side configuration selection
7-5	EXTP_TOFFCURR	0	Turn off current strength [*4.3.9*]: 0: 1.65 mA 1: 0 mA 2: 4.95 mA 3: 3.3 mA 4: 8.25 mA 5: 6.6 mA 6: 11.55 mA 7: 9.0 mA

Table 53. EXTERNAL POWER MOS register [0x03] (continued)

Bit	Register name	Reset value	Description
4-2	EXTP_TONCURR	0	Turn on current strength [4.3.9]: 0: 0 mA 1: 1.65 mA 2: 3.3 mA 3: 4.95 mA 4: 6.6 mA 5: 8.25 mA 6: 9.0 mA 7: 11.55 mA
1-0	EXTP_VSCD	0	Overcurrent threshold value specified in terms of voltages thresholds [4.3.9]: 0 0.5 V 1 1.0 V 2 1.5 V 3 2.0 V

1. Charge pump is not activated if an overvoltage/undervoltage condition is present.
2. Charge pump typically takes about 30 us to reach an active level; the application SW should monitor the CP_LOW condition to verify the effective status of the circuitry.

12.4.13 WAKE-UP sources and DFM GEN setup register [0x04]

This register is used to configure DFM frequency and polarity [4.3.6] and to enable or disable the wake-up sources.

Table 54. WAKE-UP sources and DFM GEN setup register [0x04]

Bit	Register name	Reset value	Description
13	Reserved	-	-
12	WKUP_SOURCE_LIN_DISABLE	0	When set this bit prevent the LIN/BSS receiver to generate a wake-up
11	WKUP_SOURCE_RC_DISABLE	0	When set this bit prevent the RC receiver to generate a wake-up
10	WKUP_SOURCE_IGNIT_DISABLE	0	When set, this bit inhibits pin IGNIT to generate a system wake-up
9	WKUP_SOURCE_LHC_DISABLE	0	When set, this bit inhibits pin LHC to generate a system wake-up
8	WKUP_SOURCE_L_DISABLE	0	When set, this bit inhibits pin L to generate a system wake-up
7	Reserved	-	-

Table 54. WAKE-UP sources and DFM GEN setup register [0x04] (continued)

Bit	Register name	Reset value	Description
6	DFM_polarity	1	1: the output PWM signal begins with an active pulse and is followed by the inactive interval 0: the output PWM signal begins with the inactive interval followed by the active pulse
5-4	DFM_DRV_SEL	0	DFM output configuration: 0. DFM output disabled 1. Low side driver enabled 2. High side driver enabled 3. Push-pull enabled
3-0	DFM_freq	0x0F	DFM signal frequency from 100 Hz to 400Hz with 25 Hz steps: – 0000: 100 Hz – 0001: 125 Hz – … – 1011: 375 Hz – 1100-1110: 400 Hz – 1111: DFM OFF (default)

When set, the receiver stage of the corresponding pin is disabled and cannot neither detect a wakeup condition nor change the relevant status bit in register 0x11 (IGNIT_KEY, LHC_KEY, L_KEY); the output stage, when present, isn't affected by the disable bit and is always enabled.

For example, if a wake-up by lamp is disabled, the system is still able to drive the lamp output but cannot exit from stand-by because of a L-input transition and the pin status isn't available on register 0x11, but can drive the lamp output.

In these conditions, if the application needs, after wake-up, to use the L-input it has to clear the relevant wake-up disable bit.

The following sequence can be applied:

- … exit from stand by (caused by some other source); in this condition the L-interface cannot receive any protocol but the lamp, if present, can be properly handled
- Clear the WKUP_SOURCE_L_DISABLE bit in order to enable the interface
- Wait for the interface activation time (~100 µs)
- Run the application
- Set the WKUP_SOURCE_L_DISABLE bit in order to disable the interface to generate a wakeup
- Enter standby

The stand-by exit by phase cannot be disabled. Disabling wake-up sources contributes to reduce the stand-by power consumption

12.4.14 DFM PWM DUTY CYCLE register [0x05]

This register is used to configure DFM duty cycle [4.3.6].

Table 55. DFM PWM DUTY CYCLE register [0x05]

Bit	Register name	Reset value	Description
13-10	Reserved	-	-
9-0	DFM_DC_PERC	0	Duty cycle value (see next table)

The duty cycle resolution changes according to the frequency:

Table 56. Duty cycle resolution changes according to the frequency

Frequency (Hz)	100% value	Resolution %	Frequency (Hz)	100% value	Resolution %
100	625	1.6	275	455	2.19
125	500	2	300	833	1.2
150	417	2.39	325	770	1.29
175	357	2.8	350	715	1.39
200	625	1.6	375	668	1.49
225	555	1.8	400	625	1.6
250	500	2			

Example: at 275 Hz, to apply a 37% duty cycle the value to write is 168 thus obtaining an effective duty cycle of 36.9%.

12.4.15 WATCHDOG CONFIG register [0x06]

Writing to this LOCKED register it is possible to configure the watchdog window parameters (see the relevant chapter for more details):

- Resolution
- Start point
- Duration

Table 57. WATCHDOG CONFIG register [0x06]

Bit	Register name	Reset value	Description
13-12	WDG_Timer_Resolution	3	00: 512 µs 01: 1024 µs 10: 2048 µs 11: 2048 µs (def value)
11-6	WDG_Valid_Window_Start	0x20	According to the resolution (512/1024/2048 µs) this parameter defines the watchdog Window start point: 0-32.256/0-64.512/0-129.024 µs The default value is 32 that, with the 2048 µs default resolution gives a 65.536 ms def value
5-0	WDG_Window_Duration	0x20	According to the resolution (512/1024/2048 µs) this parameter defines the watchdog Window duration: 0-32.256/0-64.512/0-129.024 µs The default value is 32 that, with the 2048 µs default resolution gives a 65.536 ms def value

12.4.16 CP-SPREAD-SPECTRUM & LIN SETTING register [0x08]

This register is used to activate/deactivate the spread spectrum strategy for the charge pump module and to choose the relevant modulation frequency; it also contains some LIN setting.

Table 58. CP-SPREAD-SPECTRUM & LIN SETTING register [0x08]

Bit	Bit Name	Reset Value	Description
13	Reserved	-	-
12	WOBBLE_MODE_DIS	0	CP wobble mode disable: 0: Pseudo-random wobble is active, (Default) 1: Wobble mode is off
11	WOBBLE_FREQUENCY	0	CP wobble frequency selector: 0: 8 kHz (Default) 1: 16 kHz
10-5	Reserved	-	-
4	LIN_PU_DIS	0	LIN pull-up resistor disable bit: 0: LIN pull-up resistor is enabled (Default) 1: LIN pull-up resistor is disabled
3	LIN_IN_USE (1)	0	LIN transceiver enable bit: 0: LIN transceiver is disabled (Default) 1: LIN transceiver is enabled. This mode is effective only when respective OTP protection bit isn't programmed. OTP protection status can be acquired by reading LIN_PROT_OTP bit in [0x1F] register
2	SPI_LINRX_ONLY	0	LIN receiver-only enable bit: 0: Both LIN receiver and transmitter are available (Default) 1: LIN transmitter is unavailable
1	SPI_LINTX_TOUT (1)	0	LIN TX dominant 12ms time-out enable bit: 0: LIN TX dominant time-out detection is disabled (Default) 1: LIN TX dominant time-out detection is enabled
0	LINFLASH	0	LIN flash mode enable bit: 0: Flash mode is disabled (Default) 1: Flash mode is enabled. This mode allows to increase standard high-speed data rate (>19.2kb/s)

1. In order to establish LIN traffic and related error handling it is mandatory LIN_IN_USE=1: write 0x0008 ' [0x08] register, SPI TX frame 0xA00008. Conversely SPI_LINTX_TOUT bit can be optionally set to enable here below 12-ms LIN error handling features:
"LIN bus 12-ms permanent dominant, notified into LIN_PERM_DOM R/O bit in [0x12] register
"LIN TX dominant 12-ms time-out, notified into LIN_TX_DOM R/O bit in [0x12] register
In this case: write 0x000A ' [0x08] register, SPI TX frame 0xA0400A.

12.4.17 DRV SETTINGS register [0x09]

Table 59. DRV SETTINGS register [0x09]

Bit	Register name	Reset value	Description
13	Reserved	-	-
12	CSA_ENABLE(1)	-	Curr. Sense Amplifier Enable
11-8	Reserved	-	-
7	L_LHC_PULLDW_DIS(2)	0	L/LHC active pull down disable
6	RVC_EN	0	RVC protocol selection [*4.3.13*]
5	L_HS_EN(3)	0	Turn on L-High side [*4.3.13*]
4	L_LS_EN(4)	1	Turn on L-Low side [*4.3.13*]
3	LHC_HS_EN(3)	0	Turn on LHC-High side
2	LHC_LS_EN(4)	1	Turn on LHC-Low side
1	VLHC_HS1_SEL	0	Over current threshold selection High side [*4.3.15*]
0	VLHC_LS1_SEL	0	Over current threshold selection Low side [*4.3.15*]

1. Current Sense Amplifier CANNOT be enabled before EXTP_LS (bit 8 of [0x03] register) has been configured.
2. If this bit is active any standby request will be ignored.
3. High Side drivers need charge pump activation.
4. After power-up, the Smart power logic will automatically activates the line (L or LHC) corresponding to the detected KEY signal (KEY or LH-KEY). Both L_LS_EN and LHC_LS_EN bit are set at 1 independently on effective status of the relevant the input that can be understood reading the wakeup source register.

   HIGH side and LOW side drivers of L and LHC outputs CANNOT be activated at the same time: the Smart Power has an embedded control logic to prevent the software from applying a wrong command. In this case the outputs are off but the bits keep the programmed value. When switching from low side to high side or vice versa, it is necessary to switch both the drivers off and then to activate the desired driver.
   The default values L and LHC LS drivers are set to 1 in order to let the system to quickly switch the lamp(s) on without waiting any SW command.
   If the input receive is not engaged or the relevant wake-up source is disabled (see register 0x04), the driver is off even if the bit is 1.

   As specified in the relevant paragraph (Pin “L”), in case of overcurrent, the lamp output is automatically turned off. In this case, before a new trial it is necessary to apply a suitable delay

12.4.18 TEST MODE STATUS register [0x0B]

It is a reserved read-only test register: in test mode it returns 1 otherwise 0. The application could read this register to check if the device is working in a correct condition.

12.4.19 WATCHDOG REFRESH register [0x0F]

This register must be suitably written to refresh the watchdog; it also contains the current watchdog counter value.

Table 60. WATCHDOG REFRESH register [0x0F]

Bit	Register name	Reset value	Description
13-10	Reserved	-	
9-8	WDG_Refr_CODE	0	Watchdog refresh code: – 00: not valid – 01: word A (first refresh word to send to the device) – 10: word B – 11: not valid Words A and B must be sent alternatively
7-0	WDG_Timer	0 (RO)	Watchdog current counter value. The resolution is specified by bits 13 and 12 of watchdog config register. The counter is cleared on watchdog error occurrence. These bits are read only: any write attempt will have no effect

12.5 SPI sequence example

This paragraph shows a simple Smart Power command sequence for a system in the following conditions:

- L-key active
- 5 ms square wave input applied to phase input
- Watchdog disabled (test mode)

Table 61. SPI sequence examples

Operation	MOSI	MISO	Comment
Read and Clear wakeup source register (0x11)	4440A5	060A20	GSW: – CP-LOW (charge pump not yet activated) – Key active DATA – L-KEY (key status) – VDD-UV – WKUP_BY_L (wake up source)
Read and Clear general status register (0x12)	4840A5	060100	GSW: – CP-LOW (charge pump not yet activated) – Key active DATA: CP-LOW

Table 61. SPI sequence examples (continued)

Operation	MOSI	MISO	Comment
Read config register (0x1F)	7C0000	0600F1	GSW: – CP-LOW (charge pump not yet activated) – Key active DATA – LIN not available – 24 V not supported – Silicon revision = 0xF – Device ID = 1
Write 0x800 to system operation register (0x03): charge pump enable	8C4800	064000	GSW: – CP-LOW (charge pump not yet activated) – Key active
Read And Clear general status register (0x12)	4840A5	060100	GSW: – CP-LOW (charge pump not yet activated) – Key active DATA: CP-LOW (still set because of deglitch time)
Read general status register (0x12	484000	020000	GSW: Key active CP-LOW cleared because of previous clear command and previous charge pump activation
Write 0x6C to DFM setup register (0x04): Polarity 1 - High side – 400Hz	90406C	020000	GSW: Key active DATA – Polarity 1 (default) – DFM OFF (0x0F)
Write 0x3E to DFM duty cycle register (0x05): 3E = 62 -> 10%	94403E	020000	GSW: Key active DATA: 0
Write 0x1000 to drv settings register (0x09): lamps off and CSA enable	45000	020014	GSW: Key active DATA – L_LS_ENABLE (default) – LHC_LS_ENABLE (default)
Read phase register (0x13)	4C0000	02D800	GSW: – Key active – Phase notification DATA: 0x1800=6144 – First phase -> Discard
Wait 22 ms (4 phase periods plus a 2 ms margin)	-	-	-
Read phase register (0x13)	4C0000	029138	GSW: – Key active – Phase notification DATA – Phase regulation request (bit 12) – 0x138=312 -> 19.969 ms ~20 ms correspond to 4 periods

Table 61. SPI sequence examples (continued)

Operation	MOSI	MISO	Comment
Read phase register (0x13)	4C0000	025138	GSW: Key active DATA: as before Phase notification is no longer present because of previous read operation. Data are not significant
Wait 22 ms (4 phase periods plus a 2 ms margin)			
Write 0x10 to unlock register (0x01): unlock SW reset bit	840010	02C000	GSW: – Key active – Phase notification (new data available)
Write 0x10 to system operation register (0x02): SW reset cmd	880010	02C000	GSW: – Key active – Phase notification (new data available – reg 0x13 not read)
Remove L key			
Write 1 to unlock register (0x01): unlock stand by bit	840001	04C000	GSW: – CP-LOW (because of prev SW reset) – Phase notification (new data available – reg 0x13 not read) Key flag no longer present
Write 1 to system operation register (0x02): unlock stand by bit	880001	04C000	See above

13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

13.1 TQFP44 (10x10x1.0 mm exp. pad down) package information

Figure 27. TQFP44 (10x10x1.0 mm exp. pad down) package outline

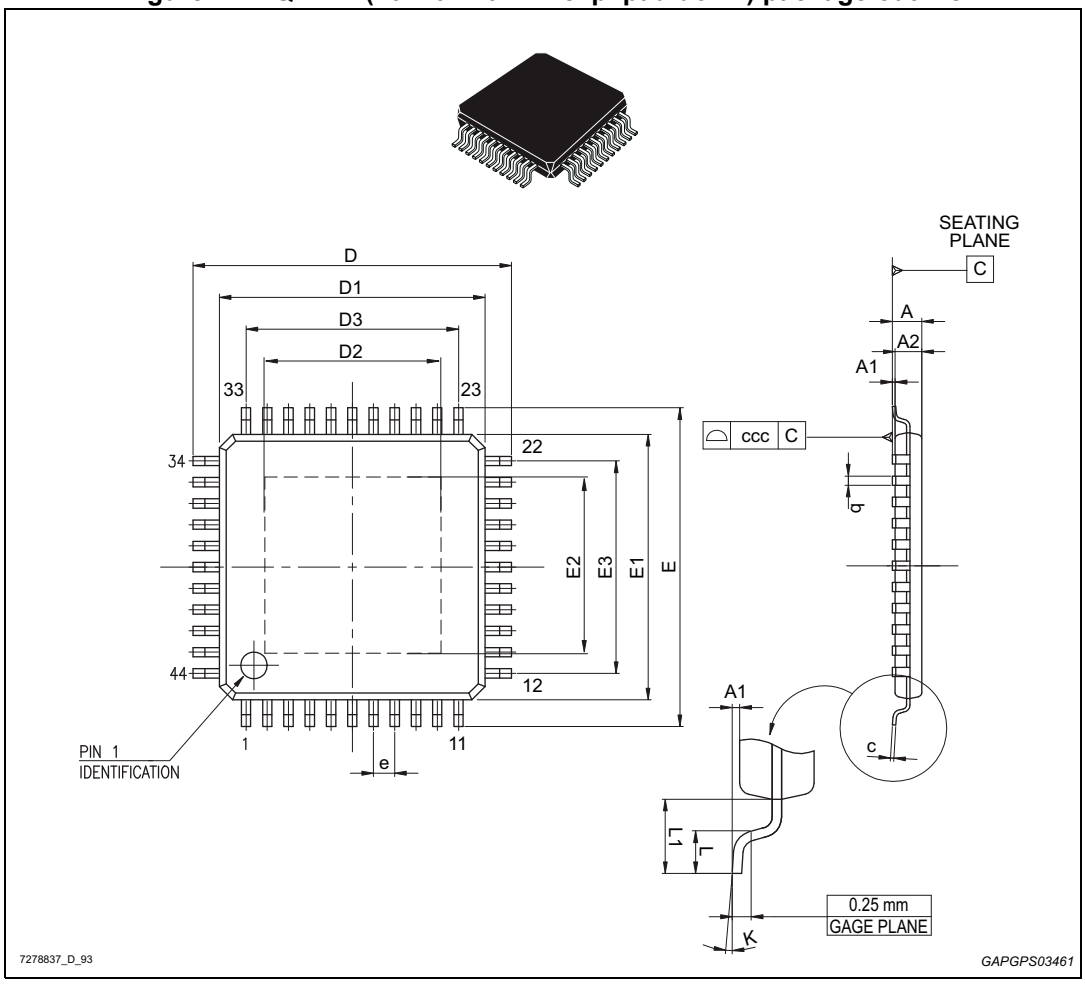
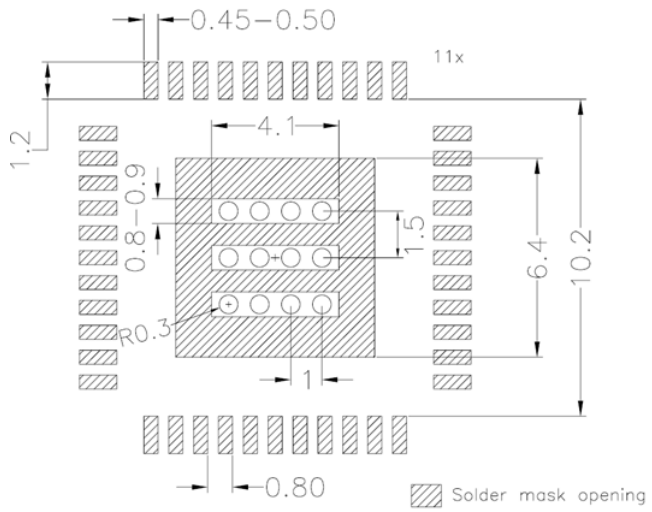


Table 62. TQFP44 (10x10x1.0 mm exp. pad down) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	0.37	0.45	0.012	0.015	0.018
c	0.09	-	0.20	0.004	-	0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D2	5.85	-	6.05	0.230	-	0.238
D3	-	8.00	-	-	0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E2	5.85	-	6.05	0.230	-	0.238
E3	-	8.00	-	-	0.315	-
e	-	0.80	-	-	0.031	-
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	-	1.00	-	-	0.039	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.003

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 28. TQFP44 (6X6 pad size) PCB soldering pad footprint



14 Order codes

Table 63. Device summary

Order code	Package	Packing
L9924LTR	TQFP44EP	Tape & Reel

Note: The device is distributed through EBV.
For orders and additional information refer to:

www.ebv.com/epona

15 Revision history

Table 64. Document revision history

Date	Revision	Changes
15-Jan-2016	1	Initial release.
10-Oct-2016	2	Updated title in cover page (added 'Automotive'); Added bullet 'AEC-Q100 qualified' in the *Features on page 1*, and car icon.
07-Feb-2017	3	Modified in *Section 4.3.5: Pin "LIN/BSS" on page 20* the paragraph below the Table 12.

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