DRV8434S Stepper Driver With Integrated Current Sense, 1/256 Microstepping, SPI Interface, Smart Tune Technology and Stall Detection

1 Features

- PWM Microstepping Stepper Motor Driver
  - SPI Interface with STEP/DIR pins
  - Up to 1/256 Microstepping Indexer
- Integrated Current Sense Functionality
  - No Sense Resistors Required
  - ±4% Full-Scale Current Accuracy
- Smart tune, slow, and mixed decay options
- 4.5 to 48-V Operating Supply Voltage Range
- Low $R_{DS(ON)}$: 330 mΩ HS + LS at 24 V, 25°C
- High Current Capacity: 2.5 A Full-Scale, 1.8 A rms
- TRQ_DAC bits to scale full-scale current
- Configurable Off-Time PWM Chopping
  - 7-µs, 16-µs, 24-µs, or 32-µs
- Supports 1.8 V, 3.3 V, 5.0 V Logic Inputs
- Daisy Chain support with SPI
- Low-Current Sleep Mode (2 µA)
- Spread spectrum clocking for low EMI
- Small Package and Footprint
- Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Charge Pump Undervoltage (CPUV)
  - Overcurrent Protection (OCP)
  - Sensorless stall detection
  - Open Load Detection (OL)
  - Overtemperature Warning (OTW)
  - Thermal Shutdown (OTSD)
  - Fault Condition Output (nFAULT)

2 Applications

- Printers and Scanners
- ATM and Money Handling Machines
- Textile Machines
- Stage Lighting Equipment
- Office and Home Automation
- Factory Automation and Robotics
- Medical Applications
- 3D Printers

3 Description

The DRV8434S is a stepper motor driver for industrial and consumer applications. The device is fully integrated with two N-channel power MOSFET H-bridge drivers, a microstepping indexer, and integrated current sensing. The DRV8434S is capable of driving up to 2.5-A full-scale output current (dependent on PCB design).

The DRV8434S uses an internal current sense architecture to eliminate the need for two external power sense resistors, saving PCB area and system cost. The device uses an internal PWM current regulation scheme selectable between smart tune, slow and mixed decay options. Smart tune automatically adjusts for optimal current regulation and reduces audible noise from the motor.

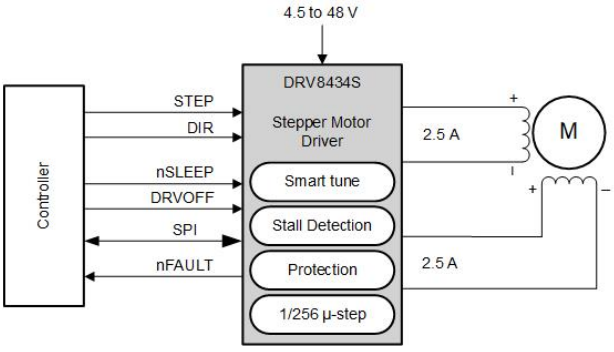
A simple SPI interface with STEP/DIR pins allows an external controller to manage the direction and step rate of the stepper motor. The device can be configured in full-step to 1/256 microstepping. With advanced stall detection algorithm, designers can detect if the motor stopped and take action as needed. The device also includes an integrated torque DAC which allows scaling the output current through SPI without needing to scale the VREF reference. Other protection features are provided for supply undervoltage, charge pump faults, overcurrent, short circuits, open load, and overtemperature. Fault conditions are indicated by the nFAULT pin.

A low-power sleep mode is provided for very low standby current using an nSLEEP pin. The device features full duplex, 4-wire synchronous SPI communication, with daisy chain support for up to 63 devices connected in series, for configurability and detailed fault reporting.

Device Information

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)
DRV8434SPWPR	HTSSOP (28)	9.7mm x 4.4mm
DRV8434SRGER	VQFN (24)	4mm x 4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial release

5 Pin Configuration and Functions

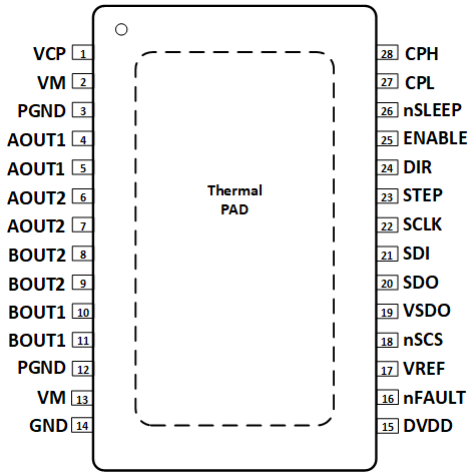


Figure 5-1. PWP PowerPAD™ Package 28-Pin HTSSOP Top View

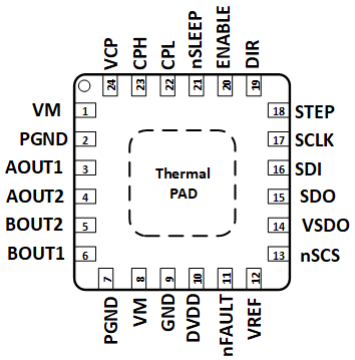


Figure 5-2. RGE Package 24-Pin VQFN with Exposed Thermal PAD Top View

5.1 Pin Functions

PIN			I/O	TYPE	DESCRIPTION
NAME	NO.				
	HTSSOP	VQFN			
AOUT1	4, 5	3	O	Output	Winding A output. Connect to stepper motor winding.
AOUT2	6, 7	4	O	Output	Winding A output. Connect to stepper motor winding.
PGND	3, 12	2, 7	—	Power	Power ground. Connect to system ground.
BOUT2	8, 9	5	O	Output	Winding B output. Connect to stepper motor winding
BOUT1	10, 11	6	O	Output	Winding B output. Connect to stepper motor winding
CPH	28	23	—	Power	Charge pump switching node. Connect a X7R, 0.022-µF, VM-rated ceramic capacitor from CPH to CPL.
CPL	27	22			
DIR	24	19	I	Input	Direction input. Logic level sets the direction of stepping; internal pulldown resistor.
ENABLE	25	20	I	Input	Logic low to disable device outputs; logic high to enable; internal pullup to DVDD.
DVDD	15	10	—	Power	Logic supply voltage. Connect a X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
GND	14	9	—	Power	Device ground. Connect to system ground.
VREF	17	12	I	Input	Current set reference input. Maximum value 3.3 V. DVDD can be used to provide VREF through a resistor divider.
nSCS	18	13	I	Input	Serial chip select. An active low on this pin enables the serial interface communications. Internal pullup to DVDD.
SCLK	22	17	I	Input	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	21	16	I	Input	Serial data input. Data is captured on the falling edge of the SCLK pin.
SDO	20	15	O	Push-Pull	Serial data output. Data is shifted out on the rising edge of the SCLK pin.
STEP	23	18	I	Input	Step input. A rising edge causes the indexer to advance one step; internal pulldown resistor.
VCP	1	24	—	Power	Charge pump output. Connect a X7R, 0.22-µF, 16-V ceramic capacitor to VM.
VM	2, 13	1, 8	—	Power	Power supply. Connect to motor supply voltage and bypass to PGND with two 0.01-µF ceramic capacitors (one for each pin) plus a bulk capacitor rated for VM.
VSDO	19	14	—	Power	Supply pin for SDO output. Connect to an external voltage depending on the desired logic level.
nFAULT	16	11	O	Open Drain	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.

PIN			I/O	TYPE	DESCRIPTION
NAME	NO.				
	HTSSOP	VQFN			
nSLEEP	26	21	I	Input	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor. An nSLEEP low pulse clears faults.
PAD	-	-	-	-	Thermal pad. Connect to system ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	50	V
Charge pump voltage (VCP, CPH)	–0.3	V_{VM} + 7	V
Charge pump negative switching pin (CPL)	–0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
SDO output reference voltage (VSDO)	–0.3	5.75	V
Control pin voltage (STEP, DIR, ENABLE, nFAULT, SDI, SDO, SCLK, nSCS)	–0.3	5.75	V
Open drain output current (nFAULT)	0	10	mA
Reference input pin voltage (VREF)	–0.3	5.75	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1	V_{VM} + 1	V
Transient 100 ns phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3	V_{VM} + 3	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	Corner pins for PWP (1, 14, 15, and 28)	±750	
			Other pins	±500	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	48	V
V_I	Logic level input voltage	0	5.5	V
V_{VREF}	VREF voltage	0.05	3.3	V
f_{STEP}	Applied STEP signal (STEP)	0	500(1)	kHz
I_{FS}	Motor full-scale current (xOUTx)	0	2.5(2)	A
I_{rms}	Motor RMS current (xOUTx)	0	1.8(2)	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load
(2) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC(1)		PWP (HTSSOP) 28 PINS	RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.7	39.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.0	28.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	16.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.2	15.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	3.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	ENABLE = 1, nSLEEP = 1, No motor load		5	6.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.8	1.2	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.2	ms
t_{EN}	Enable time	ENABLE = 0/1 to output transition			5	µs
V_{DVDD}	Internal regulator voltage	No external load, 6V < V_{VM} < 48V	4.75	5	5.25	V
		No external load, V_{VM} = 4.5V	4.2	4.35		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	6V < V_{VM} < 48V		V_{VM} + 5		V
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		360		kHz
LOGIC-LEVEL INPUTS (STEP, DIR, nSLEEP, nSCS, SCLK, SDI, ENABLE)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL1}	Input logic-low current (nSCS)	VIN = 0 V	8		12	µA
I_{IL}	Input logic-low current (other pins)	V_{IN} = 0 V	–1		1	µA
I_{IH1}	Input logic-high current (nSCS)	VIN = DVDD			500	nA
I_{IH}	Input logic-high current (other pins)	V_{IN} = 5 V			100	µA
PUSH-PULL OUTPUT (SDO)						
$R_{PD,SDO}$	Internal pull-down resistance	5mA load, with respect to GND		30	60	Ω
$R_{PU,SDO}$	Internal pull-up resistance	5mA load, with respect to VSDO		30	60	Ω
I_{SDO}	SDO Leakage Current	SDO = VSDO and 0V	-1		1	µA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic-high leakage		–1		1	µA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on resistance	T_J = 25 °C, I_O = -1 A		165	200	mΩ
		T_J = 125 °C, I_O = -1 A		250	300	mΩ
		T_J = 150 °C, I_O = -1 A		280	350	mΩ
$R_{DS(ON)}$	Low-side FET on resistance	T_J = 25 °C, I_O = 1 A		165	200	mΩ
		T_J = 125 °C, I_O = 1 A		250	300	mΩ
		T_J = 150 °C, I_O = 1 A		280	350	mΩ
t_{SR}	Output slew rate	V_{VM} = 24 V, I_O = 1 A, Between 10% and 90%		240		V/µs
PWM CURRENT CONTROL (VREF)						
K_V	Transimpedance gain	VREF = 3.3 V	1.254	1.32	1.386	V/A
I_{VREF}	VREF leakage current	VREF = 3.3 V			8.25	µA

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFF}	PWM off-time	TOFF = 00b		7		µs
		TOFF = 01b		16		
		TOFF = 10b		24		
		TOFF = 11b		32		
ΔI_{TRIP}	Current trip accuracy	0.25 A < I_O < 0.5 A	–12		12	%
		0.5 A < I_O < 1 A	–6		6	
		1 A < I_O < 2.5 A	–4		4	
$I_{O,CH}$	AOUT and BOUT current matching	I_O = 2.5 A	–2.5		2.5	%
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling, UVLO falling	4.1	4.25	4.35	V
		VM rising, UVLO rising	4.2	4.35	4.45	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{RST}	VM UVLO reset	VM falling, device reset, no SPI communications			3.9	V
V_{CPUV}	Charge pump undervoltage	VCP falling; CPUV report		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET	4			A
t_{OCP}	Overcurrent deglitch time			2		µs
t_{RETRY}	Overcurrent retry time	OCP_MODE = 1b		4		ms
t_{OL}	Open load detection time	EN_OL = 1b			50	ms
I_{OL}	Open load current threshold	EN_OL = 1b		75		mA
T_{OTW}	Overtemperature warning	Die temperature T_J	135	150	165	°C
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C
T_{HYS_OTW}	Overtemperature warning hysteresis	Die temperature T_J		20		°C

6.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{(READY)}$	SPI ready, VM > V_{RST}		1		ms
$t_{(CLK)}$	SCLK minimum period	100			ns
$t_{(CLKH)}$	SCLK minimum high time	50			ns
$t_{(CLKL)}$	SCLK minimum low time	50			ns
$t_{su(SDI)}$	SDI input setup time	20			ns
$t_{h(SDI)}$	SDI input hold time	30			ns
$t_{d(SDO)}$	SDO output delay time, SCLK high to SDO valid, C_L = 20 pF			30	ns
$t_{su(nSCS)}$	nSCS input setup time	50			ns
$t_{h(nSCS)}$	nSCS input hold time	50			ns
$t_{(HI\_nSCS)}$	nSCS minimum high time before active low			2	µs
$t_{dis(nSCS)}$	nSCS disable time, nSCS high to SDO high impedance		10		ns

6.7 Indexer Timing Requirements

Typical limits are at T_J = 25°C and V_{VM} = 24 V. Over recommended operating conditions unless otherwise noted.

NO.			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		500[1]	kHz

Typical limits are at T_J = 25°C and V_{VM} = 24 V. Over recommended operating conditions unless otherwise noted.

NO.			MIN	MAX	UNIT
2	$t_{WH(STEP)}$	Pulse duration, STEP high	970		ns
3	$t_{WL(STEP)}$	Pulse duration, STEP low	970		ns
4	$t_{SU(DIR, Mx)}$	Setup time, DIR or MODEx to STEP rising	200		ns
5	$t_{H(DIR, Mx)}$	Hold time, DIR or MODEx to STEP rising	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load.

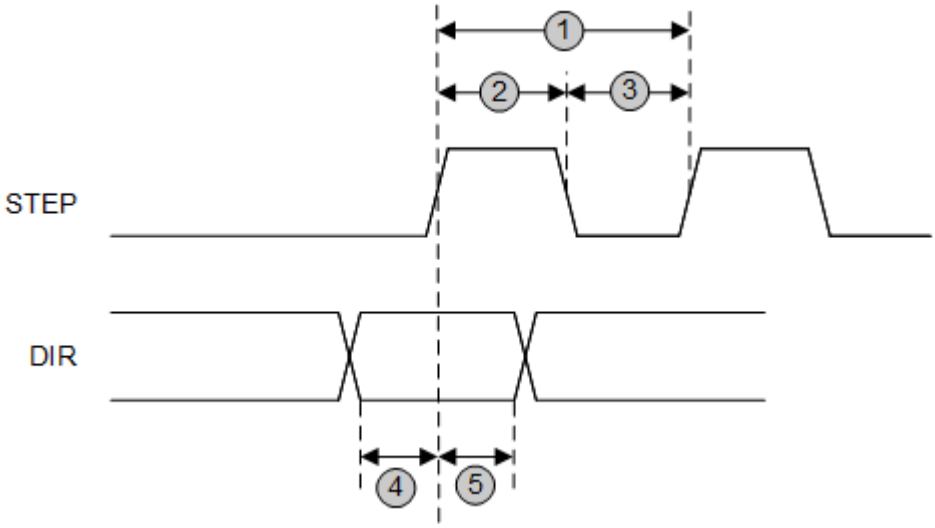


Figure 6-1. STEP and DIR Timing Diagram

6.7.1 Typical Characteristics

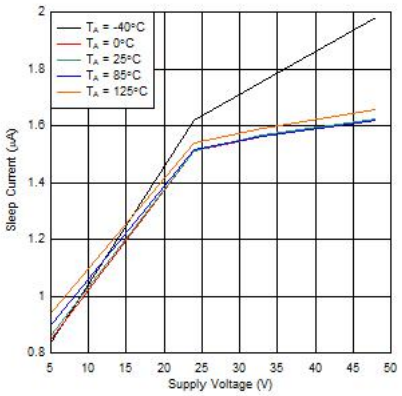


Figure 6-2. Sleep Current over Supply Voltage

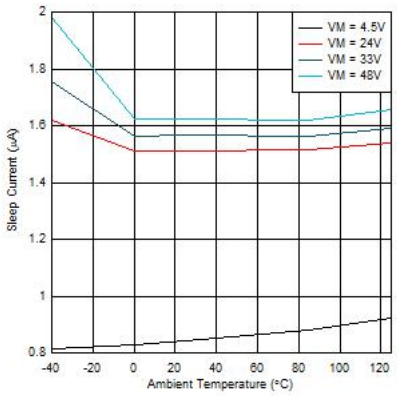


Figure 6-3. Sleep Current over Temperature

6.7.1 Typical Characteristics (continued)

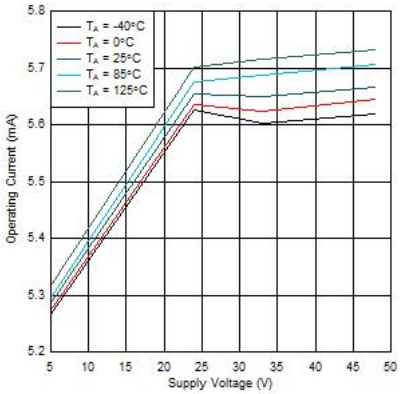


Figure 6-4. Operating Current over Supply Voltage

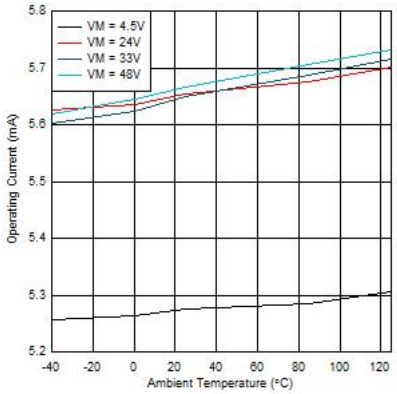


Figure 6-5. Operating Current over Temperature

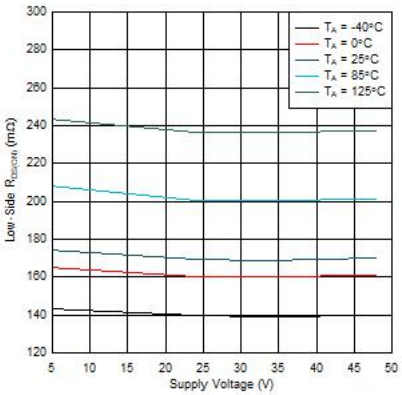


Figure 6-6. Low-Side $R_{DS(ON)}$ over Supply Voltage (MODE = 0 or 330k to GND)

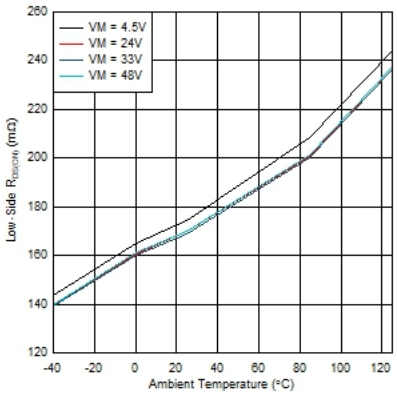


Figure 6-7. Low-Side $R_{DS(ON)}$ over Temperature (MODE = 0 or 330k to GND)

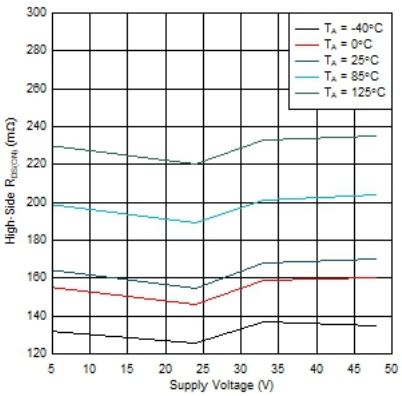


Figure 6-8. High-Side $R_{DS(ON)}$ over Supply Voltage (MODE = 0 or 330k to GND)

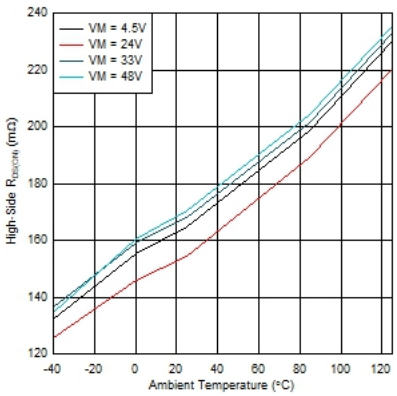


Figure 6-9. High-Side $R_{DS(ON)}$ over Temperature (MODE = 0 or 330k to GND)

7 Detailed Description

7.1 Overview

The DRV8434S is an integrated motor-driver solution for bipolar stepper motors. The device provides the maximum integration by integrating two N-channel power MOSFET H-bridges, current sense resistors and regulation circuitry, and a microstepping indexer. The DRV8434S is capable of supporting wide supply voltage of 4.5 to 48 V. The device provides an output current up to 4-A peak, 2.5-A full-scale, or 1.8-A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

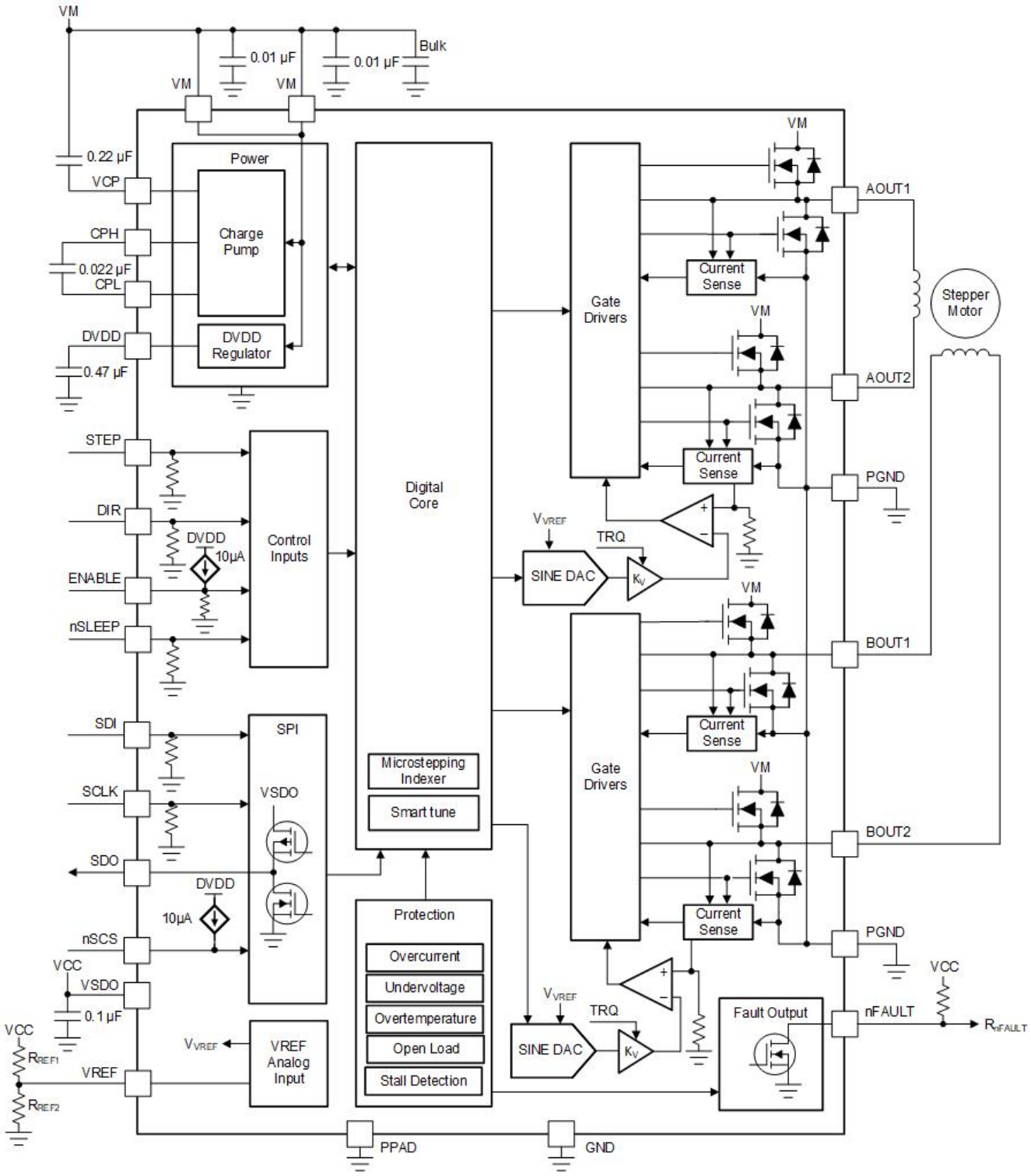
A simple STEP/DIR interface allows for an external controller to manage the direction and step rate of the stepper motor. The internal microstepping indexer can execute high-accuracy micro-stepping without requiring the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 microstepping. High microstepping contributes to significant audible noise reduction and smooth motion. In addition to a standard half stepping mode, a noncircular half stepping mode is available for increased torque output at higher motor RPM.

Stepper motor drivers need to re-circulate the winding current by implementing several types of decay modes, like slow decay, mixed decay and fast decay. The DRV8434S comes with smart tune decay modes. The smart tune is an innovative decay mechanism that automatically adjusts for optimal current regulation performance agnostic of voltage, motor speed, variation and aging effects. Smart tune Ripple Control uses a variable off-time, ripple current control scheme to minimize distortion of the motor winding current. Smart tune Dynamic Decay uses a fixed off-time, dynamic fast decay percentage scheme to minimize distortion of the motor winding current while minimizing frequency content and significantly reducing design efforts. Along with this seamless, effortless automatic smart tune, DRV8434S also provides the traditional decay modes like slow-mixed and mixed decay as well.

A torque DAC feature allows the controller to scale the output current without needing to scale the VREF voltage reference. The torque DAC is accessed using a digital input pin which allows the controller to save system power by decreasing the motor current consumption when high output torque is not required.

The device integrates a spread spectrum clocking feature for both the internal digital oscillator and internal charge pump. This feature minimizes the radiated emissions from the device. A low-power sleep mode is included which allows the system to save power when not actively driving the motor.

7.2 Functional Block Diagram



7.3 Feature Description

Table 7-1 lists the recommended external components for the DRV8434S device.

Table 7-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	Two X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	PGND	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 0.22-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.022-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47-µF to 1-µF, 6.3-V ceramic capacitor
R_{nFAULT}	VCC (1)	nFAULT	>4.7-kΩ resistor
R_{REF1}	VREF	VCC	Resistor to limit chopping current. It is recommended that the value of parallel combination of R_{REF1} and R_{REF2} should be less than 50-kΩ.
R_{REF2} (Optional)	VREF	GND	

(1) VCC is not a pin on the device, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD.

7.3.1 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, RMS, and full-scale.

7.3.1.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold I_{OCP}. The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general the minimum value of I_{OCP} specifies the peak current rating of the stepper motor driver. For the DRV8434S, the peak current rating is 4 A per bridge.

7.3.1.2 RMS Current Rating

The RMS (average) current is determined by the thermal considerations of the IC. The RMS current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The actual operating RMS current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8434S, the RMS current rating is 1.8 A per bridge.

7.3.1.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the RMS current, the full-scale current is also determined by the thermal considerations of the device. The full-scale current rating is approximately $\sqrt{2} \times I_{RMS}$ for a sinusoidal current waveform, and I_{RMS} for a square wave current waveform (full step).

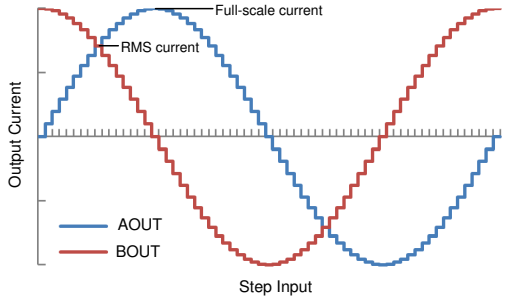


Figure 7-1. Full-Scale and RMS Current

7.3.2 PWM Motor Drivers

The DRV8434S has drivers for two full H-bridges to drive the two windings of a bipolar stepper motor. Figure 7-2 shows the block diagram of the circuitry.

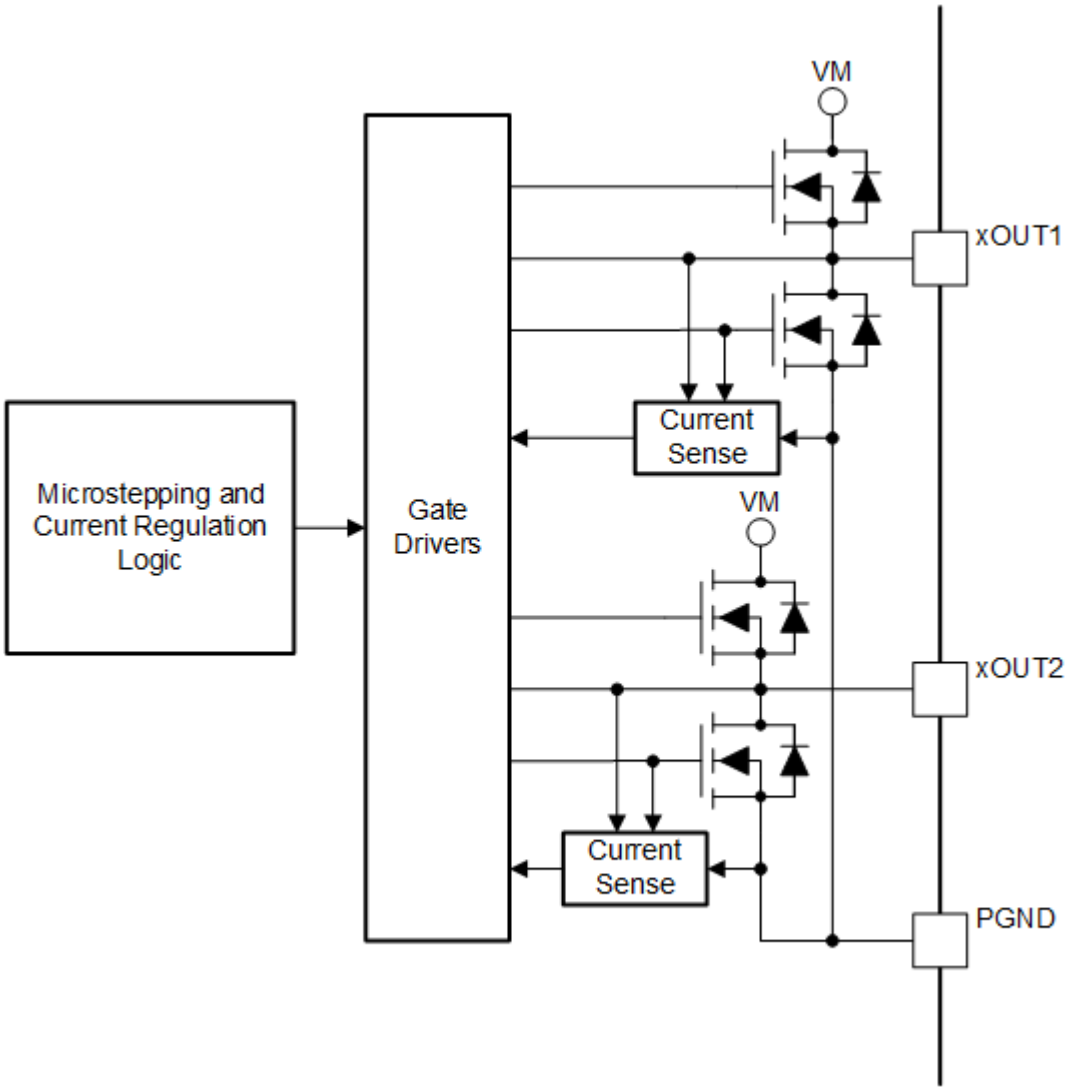


Figure 7-2. PWM Motor Driver Block Diagram

7.3.3 Microstepping Indexer

Built-in indexer logic in the device allows a number of different step modes. The MICROSTEP_MODE bits in the SPI register are used to configure the step mode as shown in Table 7-2.

Table 7-2. Microstepping Settings

MICROSTEP_MODE	STEP MODE
0000b	Full step (2-phase excitation) with 100% current
0001b	Full step (2-phase excitation) with 71% current
0010b	Non-circular 1/2 step
0011b	1/2 step
0100b	1/4 step
0101b	1/8 step

Table 7-2. Microstepping Settings (continued)

MICROSTEP_MODE	STEP MODE
0110b	1/16 step
0111b	1/32 step
1000b	1/64 step
1001b	1/128 step
1010b	1/256 step

Table 7-3 shows the relative current and step directions for full-step (71% current), 1/2 step, 1/4 step and 1/8 step operation. Higher microstepping resolutions follow the same pattern. The AOUT current is the sine of the electrical angle and the BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from the xOUT1 pin to the xOUT2 pin while driving.

At each rising edge of the STEP input the indexer advances to the next state in the table. The direction shown is with the DIR pin logic high. If the DIR pin is logic low, the sequence table is reversed.

Note

If the step mode is changed dynamically while stepping, the indexer advances to the next valid state for the new step mode setting at the rising edge of STEP.

The initial excitation state is an electrical angle of 45°, corresponding to 71% of full-scale current in both coils. This state is entered immediately after power-up, after exiting logic undervoltage lockout, or after exiting sleep mode.

Table 7-3. Relative Current and Step Directions

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	1	1		0%	100%	0.00
2				20%	98%	11.25
3	2			38%	92%	22.50
4				56%	83%	33.75
5	3	2	1	71%	71%	45.00
6				83%	56%	56.25
7	4			92%	38%	67.50
8				98%	20%	78.75
9	5	3		100%	0%	90.00
10				98%	-20%	101.25
11	6			92%	-38%	112.50
12				83%	-56%	123.75
13	7	4	2	71%	-71%	135.00
14				56%	-83%	146.25
15	8			38%	-92%	157.50
16				20%	-98%	168.75
17	9	5		0%	-100%	180.00
18				-20%	-98%	191.25
19	10			-38%	-92%	202.50
20				-56%	-83%	213.75
21	11	6	3	-71%	-71%	225.00
22				-83%	-56%	236.25
23	12			-92%	-38%	247.50
24				-98%	-20%	258.75

Table 7-3. Relative Current and Step Directions (continued)

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
25	13	7		-100%	0%	270.00
26				-98%	20%	281.25
27	14			-92%	38%	292.50
28				-83%	56%	303.75
29	15	8	4	-71%	71%	315.00
30				-56%	83%	326.25
31	16			-38%	92%	337.50
32				-20%	98%	348.75

Table 7-4 shows the full step operation with 100% full-scale current. This stepping mode consumes more power than full-step mode with 71% current, but provides a higher torque at high motor RPM.

Table 7-4. Full Step with 100% Current

FULL STEP 100%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	100	100	45
2	-100	100	135
3	-100	-100	225
4	100	–100	315

Table 7-5 shows the noncircular 1/2–step operation. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor RPM.

Table 7-5. Non-Circular 1/2-Stepping Current

NON-CIRCULAR 1/2-STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	–100	135
5	0	–100	180
6	–100	–100	225
7	–100	0	270
8	–100	100	315

7.3.4 Controlling VREF with an MCU DAC

In some cases, the full-scale output current may need to be changed between many different values, depending on motor speed and loading. The voltage of the VREF pin can be adjusted in the system to change the full-scale current.

In this mode of operation, as the DAC voltage increases, the full-scale regulation current increases as well. For proper operation, the output of the DAC must not exceed 3.3 V.

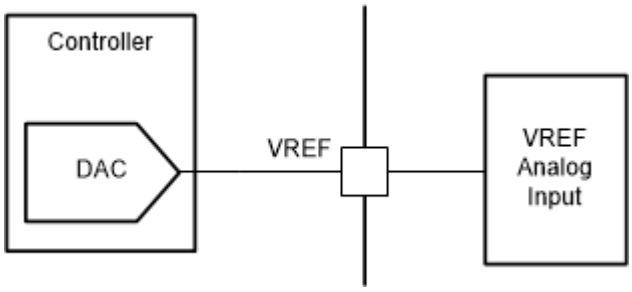


Figure 7-3. Controlling VREF with a DAC Resource

The VREF pin can also be adjusted using a PWM signal and low-pass filter.

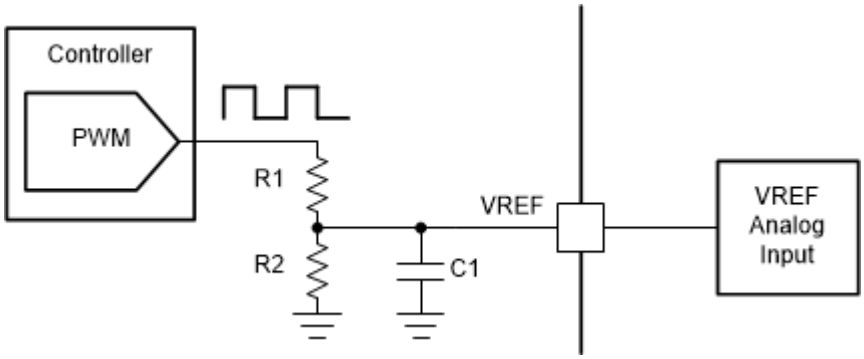


Figure 7-4. Controlling VREF With a PWM Resource

7.3.5 Current Regulation

The current through the motor windings is regulated by a PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for a period of time determined by the TOFF register setting and the selected decay mode to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

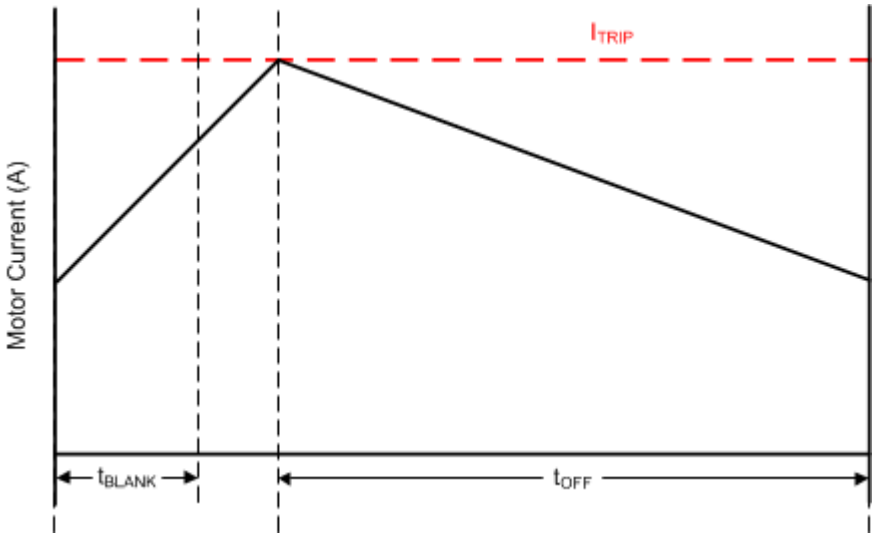


Figure 7-5. Current Chopping Waveform

The PWM regulation current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. The current sense MOSFETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the voltage at the VREF pin. In addition, the TRQ_DAC register can further scale the reference current.

Use Equation 1 to calculate the full-scale regulation current.

$$I_{FS}(A) = \frac{V_{REF}(V)}{K_V(V/A)} \times TRQ\_DAC(\%) = \frac{V_{REF}(V) \times TRQ\_DAC(\%)}{1.32(V/A)} \quad (1)$$

The TRQ_DAC is adjusted via the SPI register. Table 7-6 lists the current scalar value for different inputs.

Table 7-6. Torque DAC Settings

TRQ_DAC	CURRENT SCALAR (TRQ)
0000b	100%
0001b	93.75%
0010b	87.5%
0011b	81.25%
0100b	75%
0101b	68.75%
0110b	62.5
0111b	56.25%
1000b	50%
1001b	43.75%
1010b	37.5%
1011b	31.25%
1100b	25%

Table 7-6. Torque DAC Settings (continued)

TRQ_DAC	CURRENT SCALAR (TRQ)
1101b	18.75%
1110b	12.5%
1111b	6.25%

7.3.6 Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7-6, Item 1.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, as soon as the PWM chopping current level is reached, the H-bridge reverses state by switching on the opposite arm MOSFETs to allow the winding current to flow in the opposite direction. As the winding current approaches zero, the H-bridge is disabled to prevent further reverse current flow. Fast decay mode is shown in Figure 7-6, item 2. In slow decay mode, the winding current is re-circulated by enabling both low-side MOSFETs in the H-bridge. This is shown in Figure 7-6, Item 3.

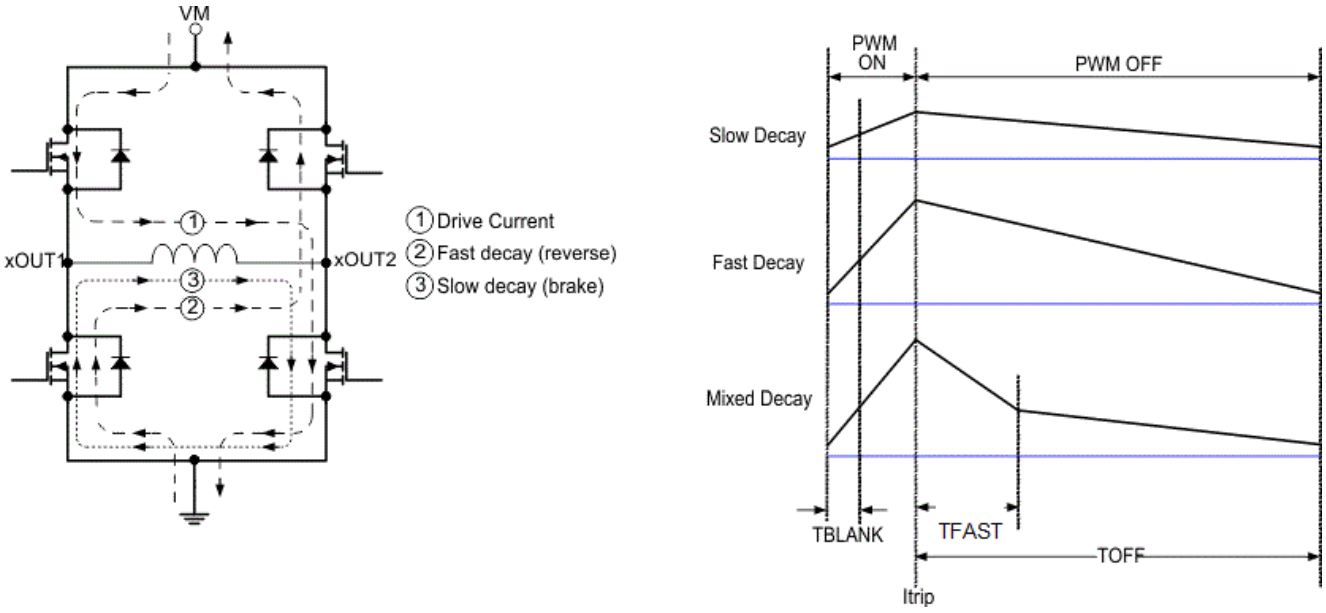


Figure 7-6. Decay Modes

The decay mode is selected by the DECAY register as shown in Table 7-7.

Table 7-7. Decay Mode Settings

DECAY	INCREASING STEPS	DECREASING STEPS
000b	Slow decay	Slow decay
001b	Slow decay	Mixed decay: 30% fast
010b	Slow decay	Mixed decay: 60% fast
011b	Slow decay	Fast decay
100b	Mixed decay: 30% fast	Mixed decay: 30% fast
101b	Mixed decay: 60% fast	Mixed decay: 60% fast
110b	Smart tune Dynamic Decay	Smart tune Dynamic Decay
111b (default)	Smart tune Ripple Control	Smart tune Ripple Control

Figure 7-7 defines increasing and decreasing current. For the slow-mixed decay mode, the decay mode is set as slow during increasing current steps and mixed decay during decreasing current steps. In full step and noncircular 1/2-step operation, the decay mode corresponding to decreasing steps is always used.

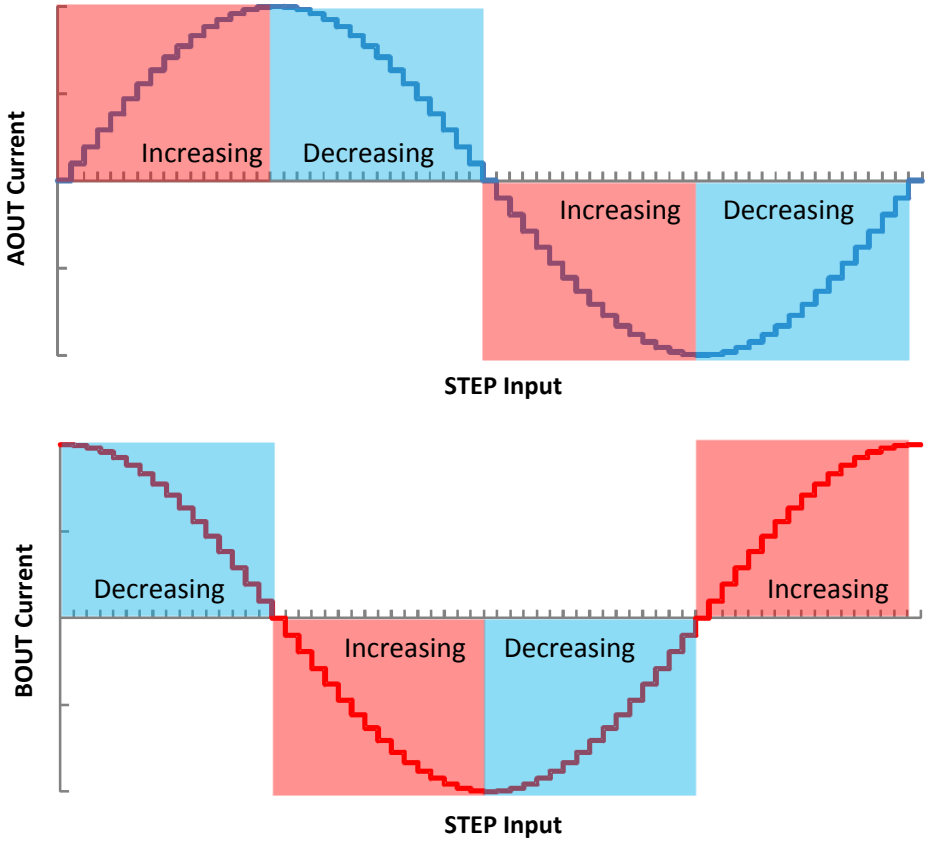


Figure 7-7. Definition of Increasing and Decreasing Steps

7.3.6.1 Slow Decay for Increasing and Decreasing Current

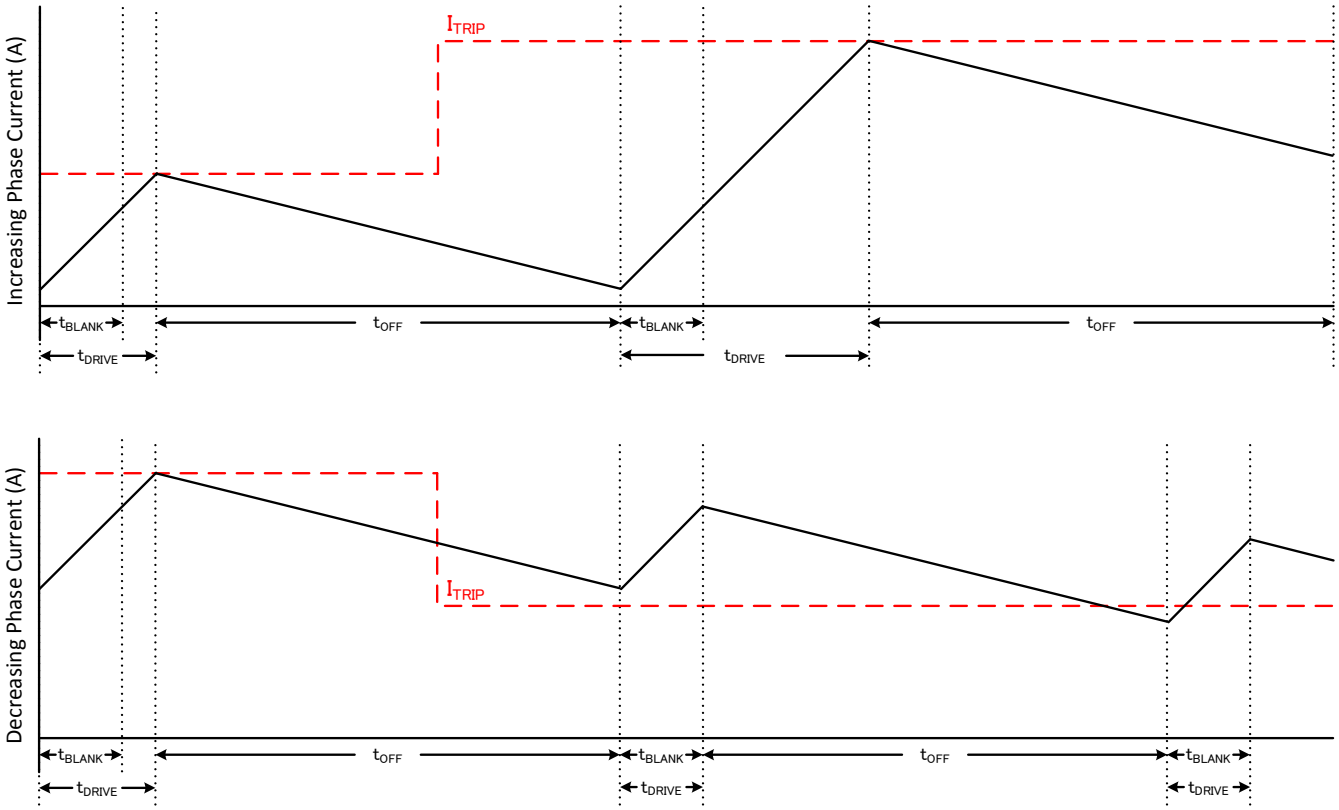


Figure 7-8. Slow/Slow Decay Mode

During slow decay, both low-side MOSFETs of the H-bridge are turned on, allowing the current to be recirculated.

Slow decay exhibits the least current ripple of the decay modes for a given t_{OFF}. However on decreasing current steps, slow decay will take a long time to settle to the new I_{TRIP} level because the current decreases very slowly. If the current at the end of the off time is above the I_{TRIP} level, slow decay will be extended for multiple off time duration, until the current at the end of the cumulative off time is below the I_{TRIP} level.

When the winding current is held static for a long time (for example when no STEP input is present) or at very low step rates, slow decay may not properly regulate the current because back-EMF will be small or absent across the motor windings. The motor current can rise rapidly, and may require an extremely long off-time to regulate the current. In some cases this could result in loss of current regulation. An aggressive decay mode is recommended in such cases.

7.3.6.2 Slow Decay for Increasing Current, Mixed Decay for Decreasing Current

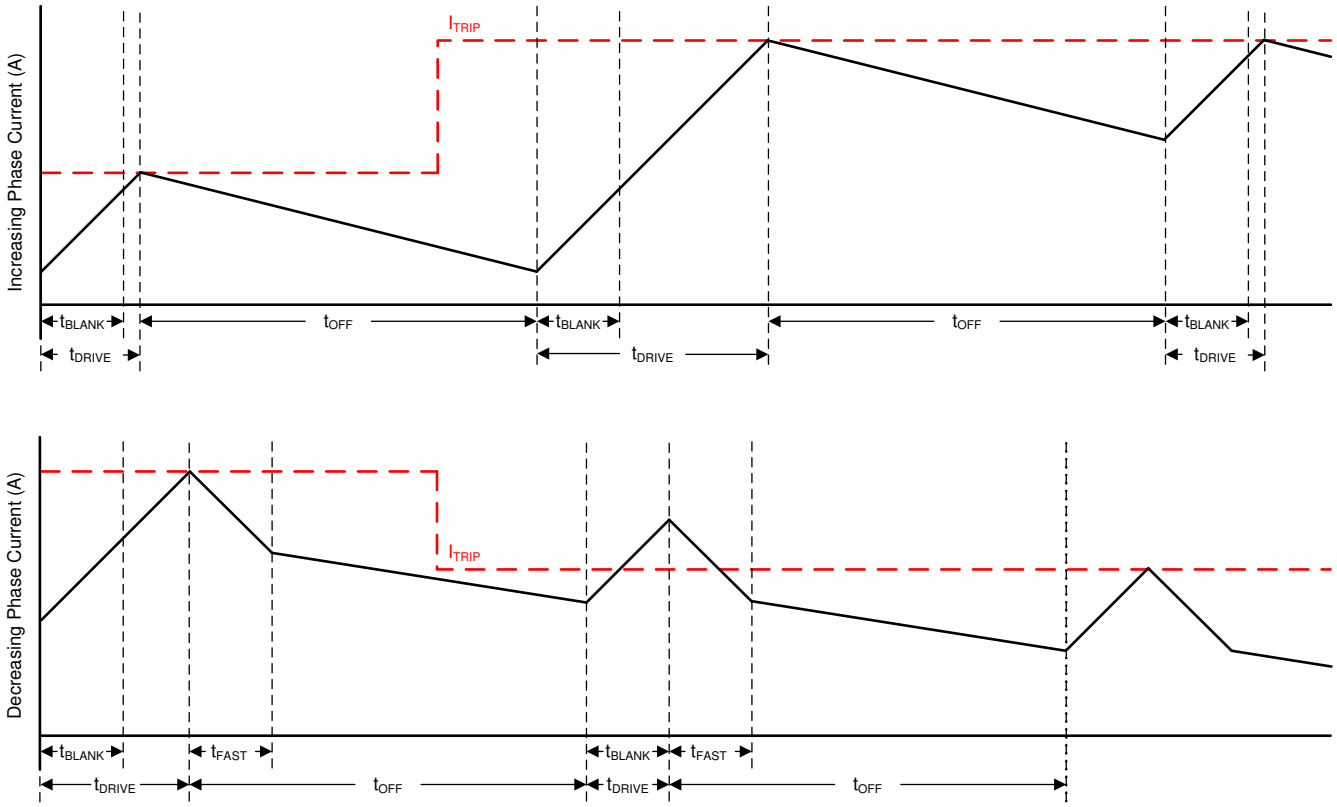


Figure 7-9. Slow-Mixed Decay Mode

Mixed decay begins as fast decay for an initial duration of the t_{OFF}, followed by slow decay for the remainder of the t_{OFF} time. Mixed decay only occurs during decreasing current. Slow decay is used for increasing current.

This decay mode exhibits the same current ripple as slow decay mode does for increasing current, because for increasing current, only slow decay is used in this mode. For decreasing current, the ripple is larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

7.3.6.3 Slow Decay for Increasing Current, Fast Decay for Decreasing current

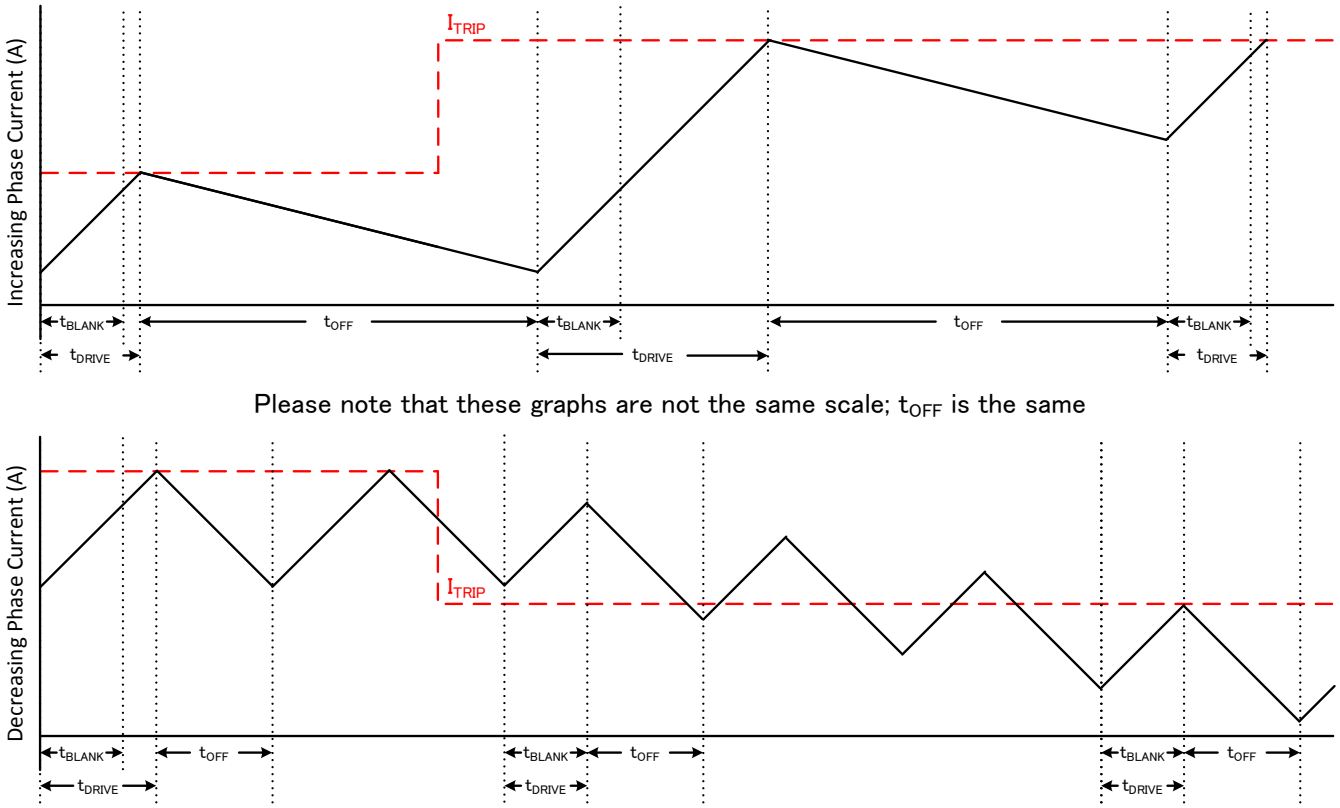


Figure 7-10. Slow/Fast Decay Mode

During fast decay, the polarity of the H-bridge is reversed. The H-bridge will be turned off as current approaches zero in order to prevent current flow in the opposite direction. In this mode, fast decay occurs only during decreasing current. Slow decay is used for increasing current.

Fast decay exhibits the highest current ripple of the decay modes for a given t_{OFF}. Transition time on decreasing current steps is much faster than slow decay since the current is allowed to decrease much faster.

7.3.6.4 Mixed Decay for Increasing and Decreasing Current

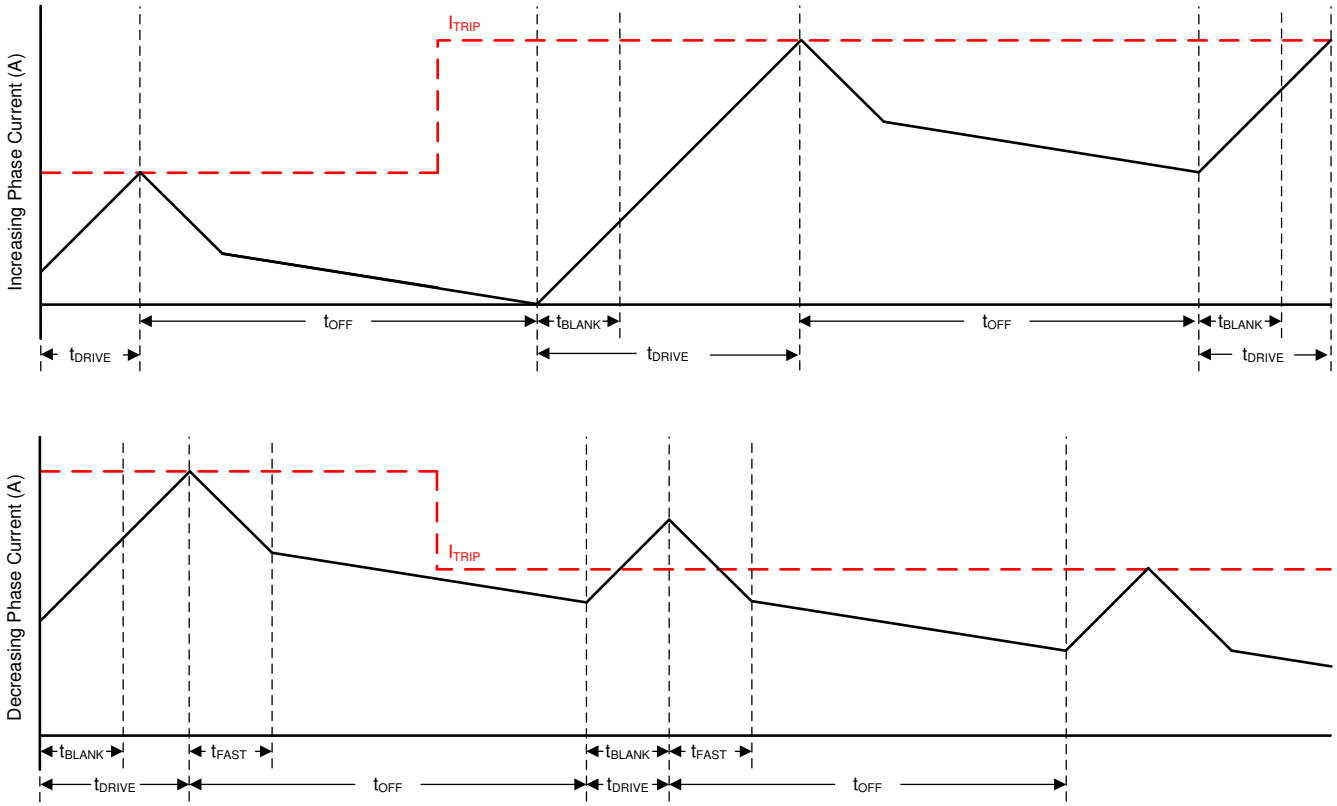


Figure 7-11. Mixed-Mixed Decay Mode

Mixed decay begins as fast decay for an initial duration of the t_{OFF} time, followed by slow decay for the remainder of t_{OFF} time. In this mode, mixed decay occurs for both increasing and decreasing current steps.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

When the winding current is held static for a long time (for example while no STEP input is present) or at very low step rates, slow decay may not properly regulate the current because back-EMF will be small or absent across the motor windings. In this case the motor current can rise rapidly and require an extremely long off-time to regulate the current. Increasing and decreasing current mixed decay mode allows the current to stay in regulation when no back-EMF is present across the motor windings.

7.3.6.5 Smart tune Dynamic Decay

The smart tune current regulation schemes are advanced current-regulation control methods compared to traditional fixed off-time current regulation schemes. Smart tune current regulation schemes help the stepper motor driver adjust the decay scheme based on factors such as:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Motor back-EMF difference on rising and falling steps
- Step transitions
- Low-current versus high-current dI/dt

The device provides two different smart tune current regulation modes, named smart tune Dynamic Decay and smart tune Ripple Control.

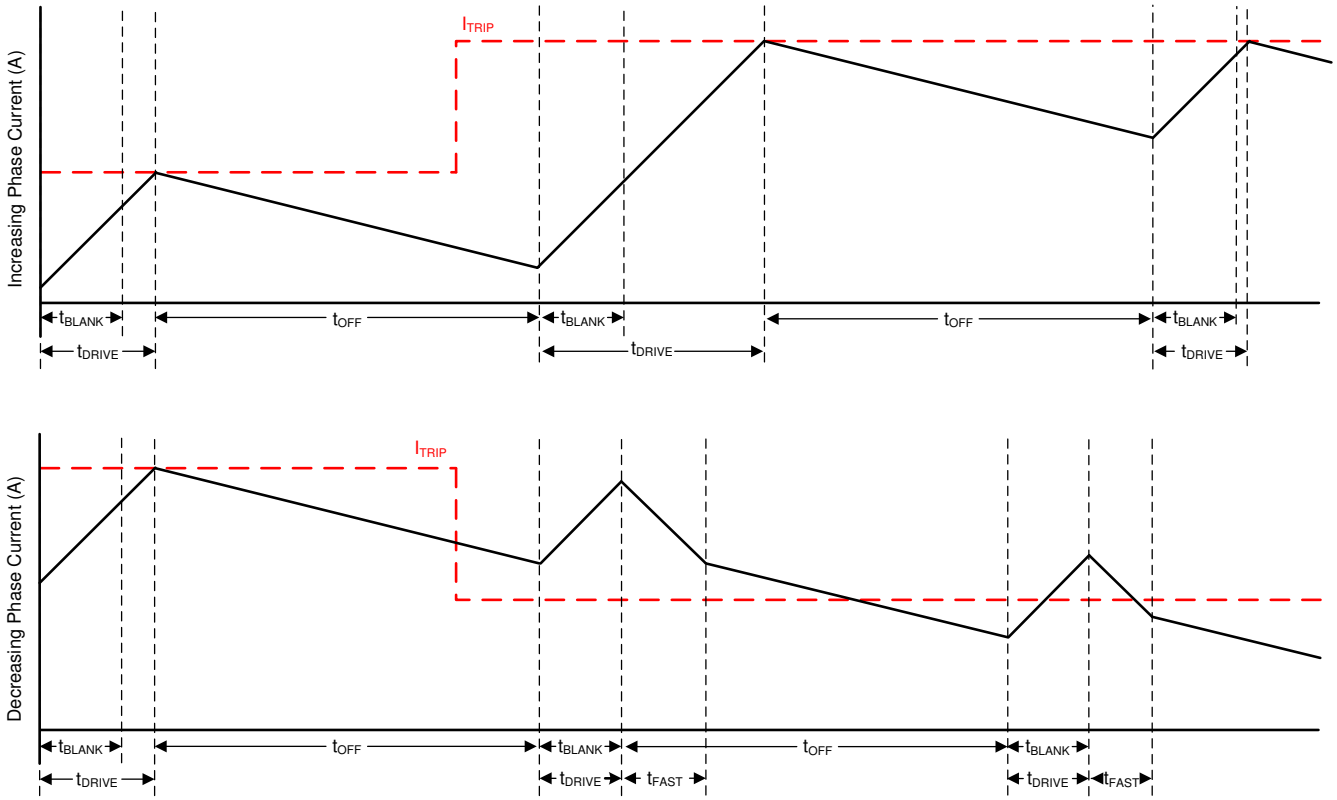


Figure 7-12. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for a motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (increases fast decay percentage) on the next cycle to prevent regulation loss. Should a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (decreases fast decay percentage) on the next cycle to operate with less ripple more efficiently. With decreasing current steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next current step quickly.

Smart tune Dynamic Decay is best suited for applications that require lowest possible current ripple, at the same time maintain a fixed frequency with the current regulation scheme.

7.3.6.6 Smart tune Ripple Control

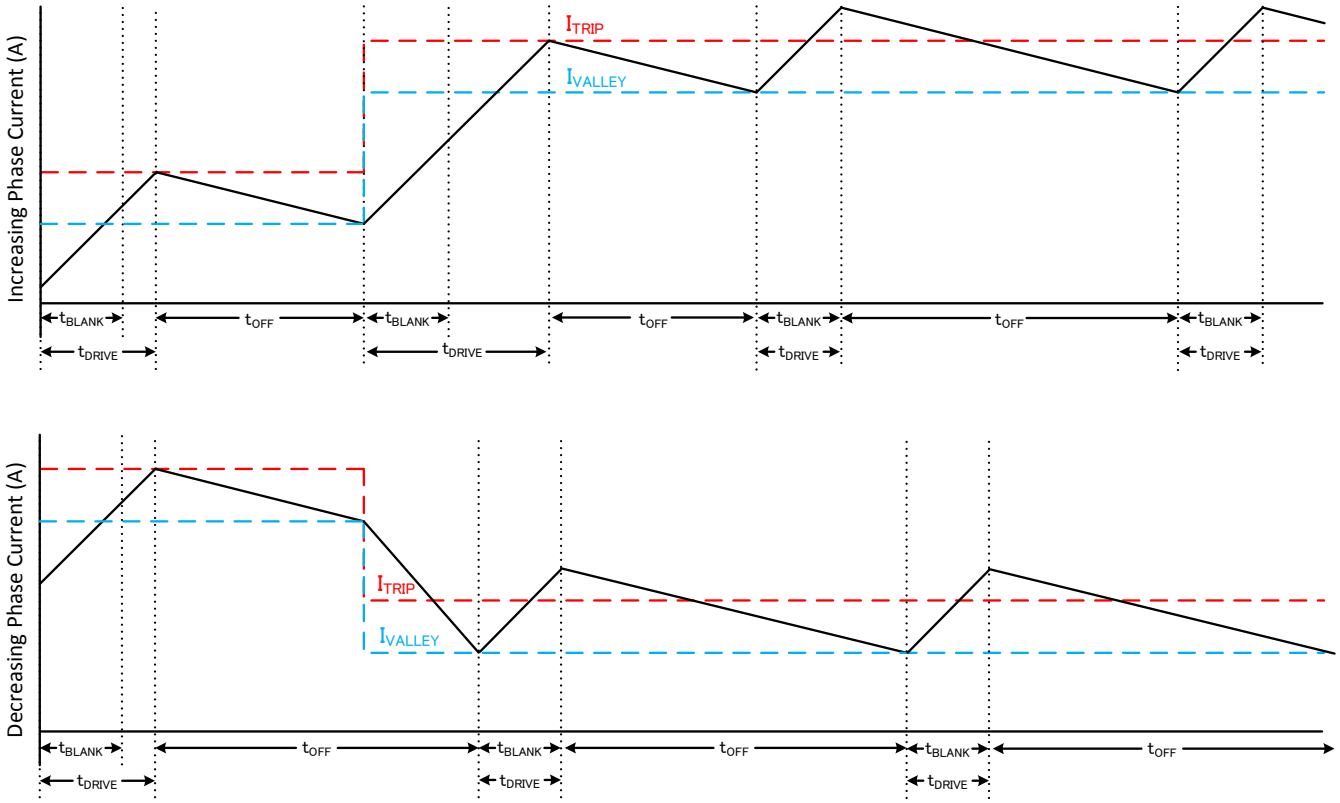


Figure 7-13. Smart tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level along with the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to slow/slow decay where both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} is variable depending on the current level and operating parameters.

The ripple current in this decay mode is programmed by the RC_RIPPLE[1:0] bits. The ripple current is dependent on the I_{TRIP} of a particular microstep level.

Table 7-8. Current Ripple Settings

RC_RIPPLE	Current Ripple at a specific microstep level
00b	19mA + 1% of I_{TRIP}
01b	19mA + 2% of I_{TRIP}
10b	19mA + 4% of I_{TRIP}
11b	19mA + 6% of I_{TRIP}

This ripple control method allows much tighter regulation of the current level increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve low current ripple with current regulation. Select a lowest possible ripple current setting that ensures the PWM frequency is above the audible range.

7.3.7 PWM OFF Time

The TOFF[1:0] bits configure the PWM OFF time for all decay modes except smart tune ripple control, as shown in Table 7-9. The OFF time settings can be changed dynamically. After a OFF time setting change, the new OFF time is applied after a 10 µs de-glitch time.

Table 7-9. OFF Time Settings

TOFF	OFF Time
00b	7 µs
01b	16 µs
10b	24 µs
11b	32 µs

7.3.8 Blanking time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM. The blanking time is approximately 1 µs.

7.3.9 Charge Pump

A charge pump is integrated to supply the high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

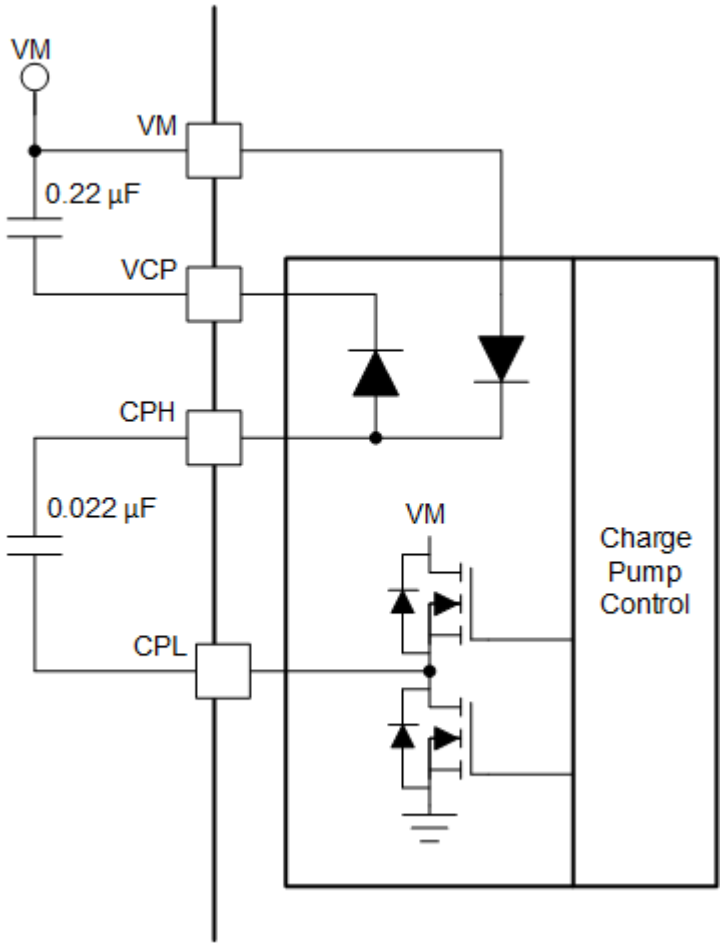


Figure 7-14. Charge Pump Block Diagram

7.3.10 Linear Voltage Regulators

A linear voltage regulator is integrated in the device for DVDD. The DVDD regulator can be used to provide VREF reference voltage. DVDD can supply a maximum of 2mA load. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 5 V. When the DVDD LDO current load exceeds 2mA, the output voltage drops significantly.

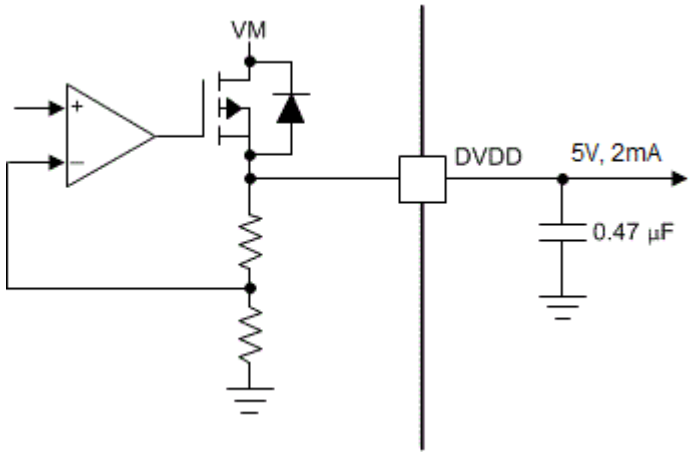


Figure 7-15. Linear Voltage Regulator Block Diagram

If logic level inputs must be tied permanently high, tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin must not be tied to DVDD, else the device will never exit sleep mode.

7.3.11 Logic Level, tri-level and quad-level Pin Diagrams

Figure 7-17 shows the input structure for STEP, DIR, nSLEEP, SDI, ENABLE and SCLK pins.

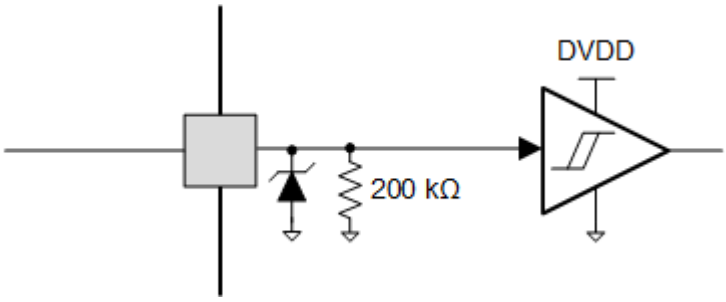


Figure 7-16. Logic-Level Input Pin Diagram

Figure 7-17 shows the input structure for the logic-level pin nSCS.

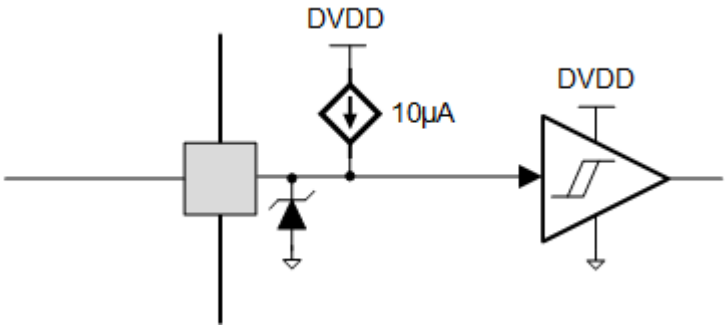


Figure 7-17. Logic-Level with Internal Pull-up Input Pin Diagram

7.3.11.1 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5-V, 3.3-V or 1.8-V supply. When a fault is detected, the nFAULT pin will be logic low. nFAULT pin will be high after power-up. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V or 1.8-V pullup, an external supply must be used.

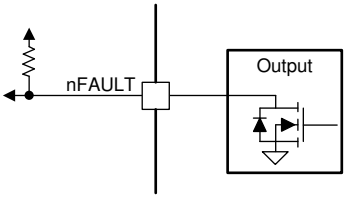


Figure 7-18. nFAULT Pin

7.3.12 Protection Circuits

The device is fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, open load, and device overtemperature events. In addition, the device is protected against stall detection in the event of overload or end-of-line movement.

7.3.12.1 VM Undervoltage Lockout (UVLO)

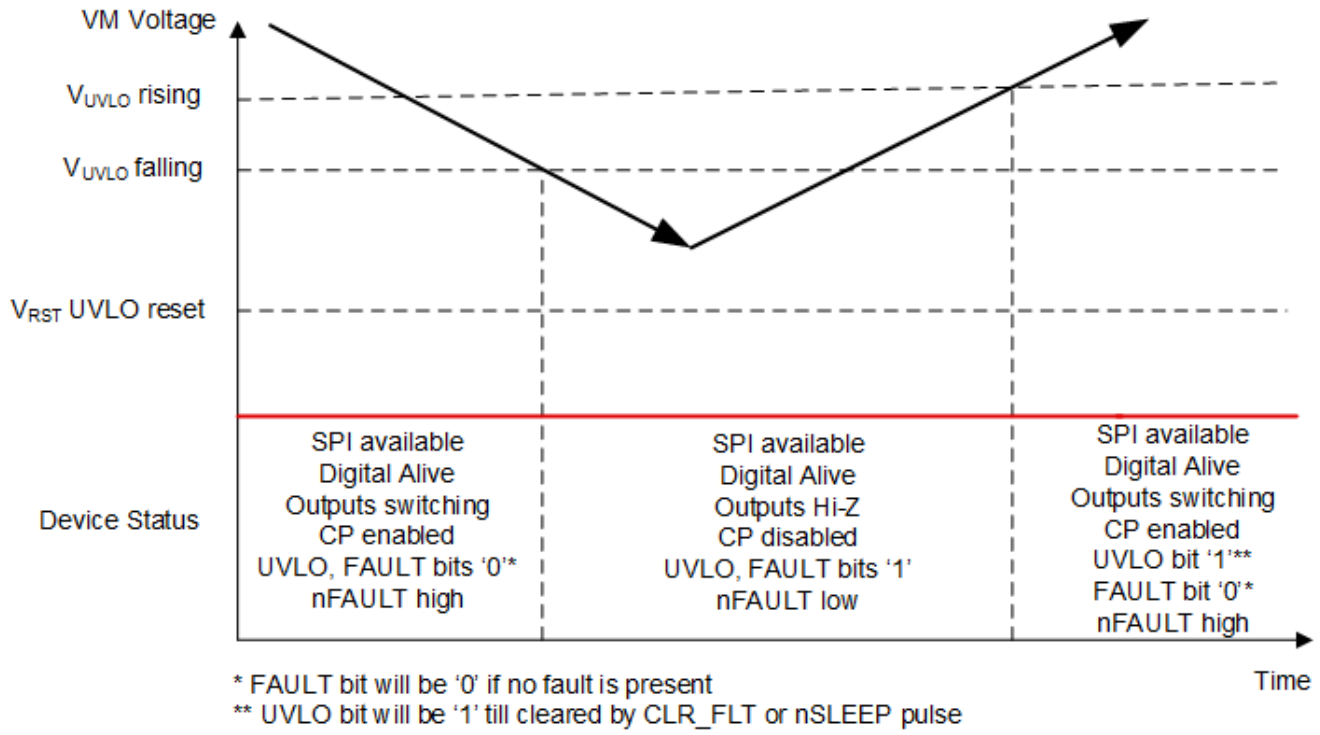


Figure 7-19. Supply Voltage Ramp Profile

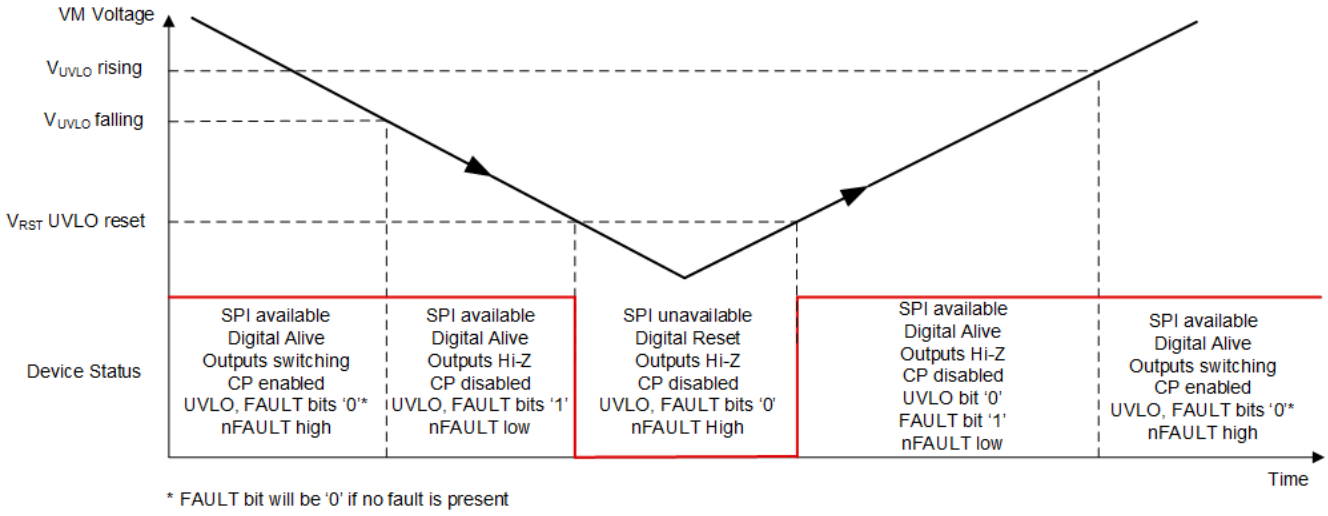


Figure 7-20. Supply Voltage Ramp Profile

If at any time the voltage on the VM pin falls below the UVLO falling threshold voltage, all the outputs are disabled (High-Z) and the charge pump (CP) is disabled. Normal operation resumes (motor driver and charge pump) when the VM voltage recovers above the UVLO rising threshold voltage.

When the voltage on the VM pin falls below the UVLO falling threshold voltage (4.25 V typical), but is above the VM UVLO reset voltage (V_{RST}, 3.9 V maximum), SPI communication is available, the digital core of the device is active, the FAULT and UVLO bits are made high in the SPI registers and the nFAULT pin is driven low, as shown in Figure 7-19. From this condition, if the VM voltage recovers above the UVLO rising threshold voltage (4.35 V

typical), nFAULT pin is released (is pulled-up to the external voltage), and the FAULT bit is reset, but the UVLO bit remains latched high until cleared through the CLR_FLT bit or an nSLEEP reset pulse.

When the voltage on the VM pin falls below the VM UVLO reset voltage (V_{RST}, 3.9 V maximum), SPI communication is unavailable, the digital core is shutdown, the FAULT and UVLO bits are low and the nFAULT pin is high. During a subsequent power-up, when the VM voltage exceeds the V_{RST} voltage, the digital core comes alive, UVLO bit stays low but the FAULT bit is made high; and the nFAULT pin is pulled low, as shown in Figure 7-20. When the VM voltage exceeds the VM UVLO rising threshold, FAULT bit is reset, UVLO bit stays low and the nFAULT pin is pulled high.

7.3.12.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. The FAULT and CPUV bits are made high in the SPI registers. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed. The CPUV bit remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse.

7.3.12.3 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, the FETs in that particular H-bridge are disabled and the nFAULT pin is driven low. The FAULT and OCP bits are latched high in the SPI registers.

For xOUTx to VM short, corresponding OCP_LSx_x bit goes high in the DIAG Status 1 register. Similarly, for xOUTx to ground short, corresponding OCP_HSx_x bit goes high. For example, for AOUT1 to VM short, OCP_LS1_A bit goes high; and for BOUT2 to ground short, the OCP_HS2_B bit goes high.

The charge pump remains active during this condition. The overcurrent protection can operate in two different modes: latched shutdown and automatic retry.

7.3.12.3.1 Latched Shutdown (OCP_MODE = 0b)

In this mode, after an OCP event, the relevant outputs are disabled and the nFAULT pin is driven low. Normal operation resumes after applying a CLR_FLT command, nSLEEP reset pulse or a power cycling. This is the default mode for an OCP event for the device.

7.3.12.3.2 Automatic Retry (OCP_MODE = 1b)

In this mode, after an OCP event, the relevant outputs are disabled and the nFAULT pin is driven low. Normal operation resumes automatically (motor-driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

7.3.12.4 Stall Detection

Stepper motors have a distinct relation between the winding current, back-EMF, and mechanical torque load of the motor, as shown in Figure 7-21. As motor load approaches the torque capability of the motor for a given winding current, the back-EMF will move in phase with the winding current. By detecting back-emf phase shift between rising and falling current quadrants of the motor current, the DRV8434S can detect a motor overload stall condition or an end-of-line travel.

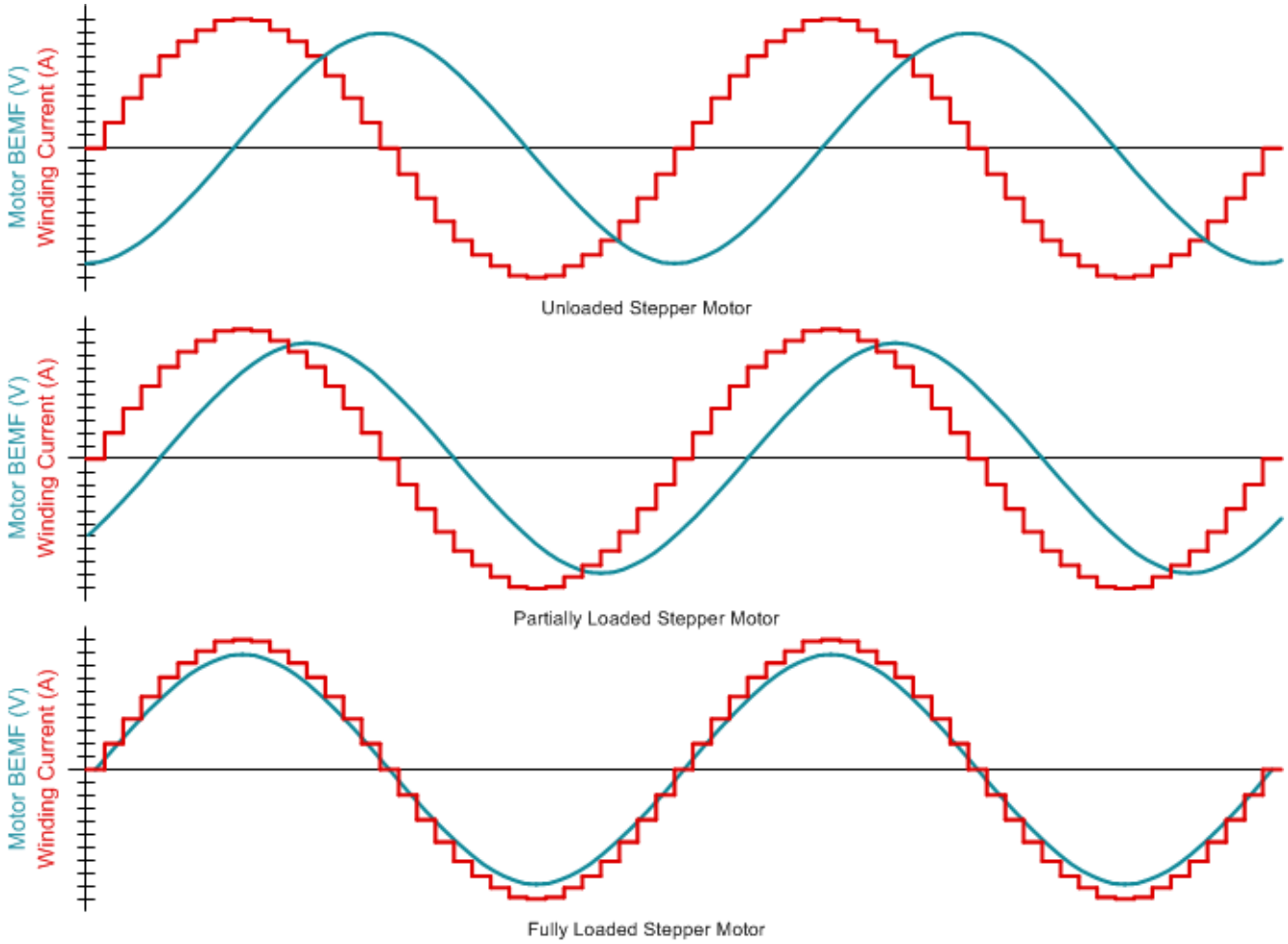


Figure 7-21. Stall Detection by Monitoring Motor Back-EMF

The Stall Detection algorithm works only when the device is programmed to operate in the smart tune Ripple Control decay mode. The EN_STL bit has to be '1' to enable stall detection. Additionally, if any fault condition exists (UVLO, OCP, OL, OTSD etc.), stall detection will be disabled.

The algorithm compares the back-EMF between the rising and falling current quadrants by monitoring PWM off time and generates a value represented by the 12-bit register TRQ_COUNT. The comparison is done in such a way that the TRQ_COUNT value is practically independent of motor current, ambient temperature and supply voltage. Full step mode of operation is supported by this algorithm.

For a lightly loaded motor, the TRQ_COUNT will be a non-zero value. As the motor approaches stall condition, TRQ_COUNT will approach zero and can be used to detect stall condition. If at anytime TRQ_COUNT falls below the stall threshold (represented by the 12-bit STALL_TH register), the device will detect a stall and the STALL, STL and FAULT bits are latched high in the SPI register. To indicate stall detection fault on the nFAULT pin, the STL_REP bit must be '1'. When the STL_REP bit is '1', the nFAULT pin will be driven low when a stall is detected.

In the stalled condition, the motor shaft does not spin. The motor starts to spin again when the stall condition is removed and the motor ramps to its target speed. The nFAULT is released and the fault registers are cleared when a clear faults command is issued either via the CLR_FLT bit or an nSLEEP reset pulse.

TRQ_COUNT is calculated as an average torque count of the most recent four electrical half-cycles of a spinning motor. The calculated value is updated in the device CTRL8 and CTRL9 registers within the next 100 ns. The registers are unchanged until the next update. Subsequent updates happen every electrical half-cycle.

High motor coil resistance can result in low TRQ_COUNT. The TRQ_SCALE bit allows scaling up low TRQ_COUNT values, for ease of further processing. If the initially calculated TRQ_COUNT value is less than 500 and the TRQ_SCALE bit is '1', then the TRQ_COUNT is multiplied by a factor of 8. If the TRQ_SCALE bit is '0', TRQ_COUNT retains the value originally calculated by the algorithm.

Stall threshold can be set in two ways – either the user can write the STALL_TH bits, or let the algorithm learn the stall threshold value using the stall learning process. The stall learning process is started by setting the STL_LRN bit to '1'. The motor is intentionally stalled briefly to allow the algorithm to learn the ideal stall threshold. At the end of a successful learning, the STALL_TH register is updated with the learnt stall threshold value. The STL_LRN_OK bit goes high after a successful learning.

A stall threshold learnt at one speed may not work well for another speed. It is recommended to re-learn the stall threshold every time the motor speed is changed considerably.

7.3.12.5 Open-Load Detection (OL)

If the winding current in any coil drops below the open load current threshold (I_{OL}) and the I_{TRIP} level set by the indexer, and if this condition persists for more than the open load detection time (t_{OL}), an open-load condition is detected. The EN_OL bit must be '1' to enable open load detection.

When an open load fault is detected, the OL and FAULT bits are latched high in the SPI register and the nFAULT pin is driven low. If the OL_A bit is high, it indicates an open load fault in winding A, between AOUT1 and AOUT2. Similarly, an open load fault between BOUT1 and BOUT2 causes the OL_B bit to go high.

When the OL_MODE bit is '1', the nFAULT line is released immediately after an open load condition is removed. When the OL_MODE bit is '0', the nFAULT line is released after an open load condition is removed and a clear faults command is issued either via the CLR_FLT bit or an nSLEEP reset pulse. The fault also clears when the device is power cycled or comes out of sleep mode.

7.3.12.6 Overtemperature Warning (OTW)

If the die temperature exceeds the trip point of the overtemperature warning (T_{OTW}), the OTW and TF bits are set in the SPI register. The device performs no additional action and continues to function. The charge pump remains active during this condition.

When the die temperature falls below the hysteresis point (T_{HYS_OTW}) of the overtemperature warning, the OTW and TF bits clear automatically.

The OTW bit can also be configured to report the fault on the nFAULT pin, as well as set the FAULT bit in the register, by setting the TW_REP bit to 1b.

7.3.12.7 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}) all MOSFETs in the H-bridge are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition. In addition, the FAULT, TF and OTS bits are latched high. This protection feature cannot be disabled. The overtemperature protection can operate in two different modes: latched shutdown and automatic recovery.

7.3.12.7.1 Latched Shutdown (OTSD_MODE = 0b)

In this mode, after a OTSD event all the outputs are disabled and the nFAULT pin is driven low. The FAULT, TF and OTS bits are latched high in the SPI register. Normal operation resumes after applying an nSLEEP reset pulse or a power cycle. This mode is the default mode for OTSD.

7.3.12.7.2 Automatic Recovery (OTSD_MODE = 1b)

In this mode, after a OTSD event all the outputs are disabled and the nFAULT pin is driven low. The FAULT, TF and OTS bits are latched high in the SPI register. Normal operation resumes (motor-driver operation and the nFAULT line released) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} - T_{HYS\_OTSD}$). The FAULT, TF and OTS bits remains latched high indicating that a thermal event occurred until a clear faults command is issued either via the CLR_FLT bit or an nSLEEP reset pulse.

Fault Condition Summary

Table 7-10. Fault Condition Summary

FAULT	CONDITION	CONFIGURATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO} (max 4.35 V)	—	nFAULT / SPI	Disabled	Disabled	Disabled	Reset (V_{VM} < 3.9 V)	Automatic: VM > V_{UVLO} (max 4.45 V)
VCP undervoltage (CPUV)	VCP < V_{CPUV} (typ VM + 2 V)	—	nFAULT / SPI	Disabled	Operating	Operating	Operating	VCP > V_{CPUV} (typ VM + 2.7 V)
Overcurrent (OCP)	I_{OUT} > I_{OCP} (min 4 A)	OCP_MODE = 0b	nFAULT / SPI	Disabled	Operating	Operating	Operating	Latched: CLR_FLT / nSLEEP
		OCP_MODE = 1b	nFAULT / SPI	Disabled	Operating	Operating	Operating	Automatic retry: t_{RETRY}
Open Load (OL)	No load detected	EN_OL = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	Report only
Stall Detection (STALL)	Stall / stuck motor	STL_REP = 0b	SPI	Operating	Operating	Operating	Operating	CLR_FLT/ nSLEEP
		STL_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	
Overtemperature Warning (OTW)	T_J > T_{OTW}	TW_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	Automatic: T_J < T_{OTW} - T_{HYS_OTW}
		TW_REP = 0b	SPI	Operating	Operating	Operating	Operating	
Thermal Shutdown (OTSD)	T_J > T_{OTSD}	OTSD_MODE = 0b	nFAULT / SPI	Disabled	Disabled	Operating	Operating	Latched: CLR_FLT / nSLEEP
		OTSD_MODE = 1b	SPI	Disabled	Disabled	Operating	Operating	Automatic: T_J < T_{OTSD} - T_{HYS_OTSD}

7.4 Device Functional Modes

7.4.1 Sleep Mode (nSLEEP = 0)

The device state is managed by the nSLEEP pin. When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled, the DVDD regulator is disabled, the charge pump is disabled, and the SPI is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.2 Disable Mode (nSLEEP = 1, ENABLE = 0)

The ENABLE pin is used to enable or disable the half bridges in the device. When the ENABLE pin is low, the output drivers are disabled in the Hi-Z state. The EN_OUT bit can also be used to disable the output drivers. When the EN_OUT bit is '0', the output drivers are disabled in the Hi-Z state.

Table 7-11. Conditions to Enable or Disable Output Drivers

nSLEEP	ENABLE	EN_OUT	H-BRIDGE
0	Don't Care	Don't Care	Disabled
1	0	0	Disabled
1	0	1	Disabled
1	1	0	Disabled
1	1	1	Enabled

7.4.3 Operating Mode (nSLEEP = 1, ENABLE = 1)

When the nSLEEP pin is high, the ENABLE pin is 1, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.4 nSLEEP Reset Pulse

In addition to the CLR_FLT bit in the SPI register, a latched fault can be cleared with an nSLEEP reset pulse. This pulse width must be greater than 20 µs and lesser than 40 µs. If nSLEEP is low for longer than 40 µs but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram (see Figure 7-22). This reset pulse resets any SPI faults and does not affect the status of the charge pump or other functional blocks.

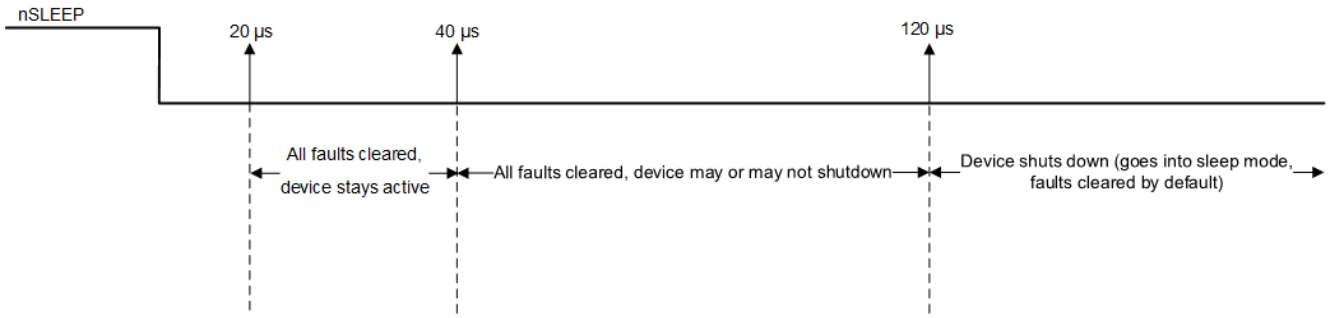


Figure 7-22. nSLEEP Reset Pulse

Functional Modes Summary

Table 7-12lists a summary of the functional modes.

Table 7-12. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	INDEXER	Logic
Sleep mode	4.5 V < VM < 48 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled	Disabled
Operating	4.5 V < VM < 48 V	nSLEEP pin = 1 ENABLE pin = 1	Operating	Operating	Operating	Operating	Operating
Disabled	4.5 V < VM < 48 V	nSLEEP pin = 1 ENABLE pin = 0	Disabled	Operating	Operating	Operating	Operating

7.5 Programming

7.5.1 Serial Peripheral Interface (SPI) Communication

The device SPI has full duplex, 4-wire synchronous communication. This section describes the SPI protocol, the command structure, and the control and status registers. The device can be connected with the MCU in the following configurations:

- One target device
- Multiple target devices in parallel connection
- Multiple target devices in series (daisy chain) connection

7.5.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit 14)
- 5 address bits, A (bits 13 through 9)
- 8 data bits, D (bits 7 through 0)

The SDO output-data word is 16 bits long and the first 8 bits make up the Status Register (S1). The Report word (R1) is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

Table 7-13. SDI Input Data Word Format

	R/W	ADDRESS					DON'T CARE	DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	W0	A4	A3	A2	A1	A0	X	D7	D6	D5	D4	D3	D2	D1	D0

Table 7-14. SDO Output Data Word Format

STATUS								REPORT							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	UVLO	CPUV	OCP	STL	TF	OL	D7	D6	D5	D4	D3	D2	D1	D0

7.5.1.2 SPI for a Single Target Device

The SPI is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in target mode. The SPI input-data (SDI) word consists of a 16-bit word, with 8 bits command and 8 bits of data. The SPI output data (SDO) word consists of 8 bits of status register with fault status indication and 8 bits of register data. Figure 7-23 shows the data sequence between the MCU and the SPI target driver.

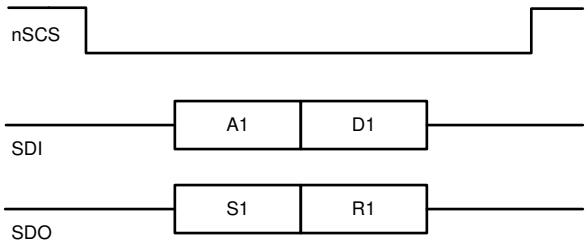


Figure 7-23. SPI Transaction Between MCU and the device

A valid frame must meet the following conditions:

- The SCLK pin must be low when the nSCS pin goes low and when the nSCS pin goes high.
- The nSCS pin should be taken high for at least 500 ns between frames.
- When the nSCS pin is asserted high, any signals at the SCLK and SDI pins are ignored, and the SDO pin is in the high-impedance state (Hi-Z).
- Full 16 SCLK cycles must occur.
- Data is captured on the falling edge of the clock and data is driven on the rising edge of the clock.
- The most-significant bit (MSB) is shifted in and out first.
- If the data word sent to SDI pin is less than 16 bits or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit command data.

7.5.1.3 SPI for Multiple Target Devices in Daisy Chain Configuration

The DRV8434S device can be connected in a daisy chain configuration to keep GPIO ports available when multiple devices are communicating to the same MCU. Figure 7-24 shows the topology when three devices are connected in series.

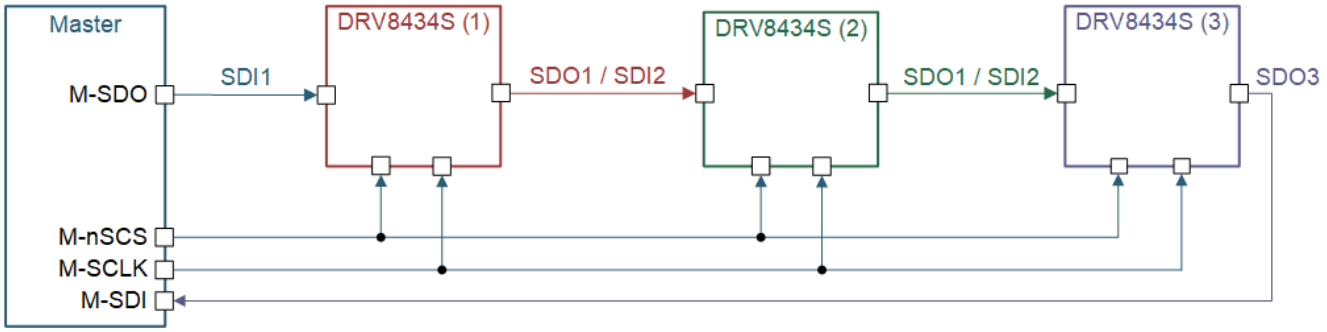


Figure 7-24. Three DRV8434S Devices Connected in Daisy Chain

The first device in the chain receives data from the MCU in the following format for 3-device configuration: 2 bytes of header (HDRx) followed by 3 bytes of address (Ax) followed by 3 bytes of data (Dx).

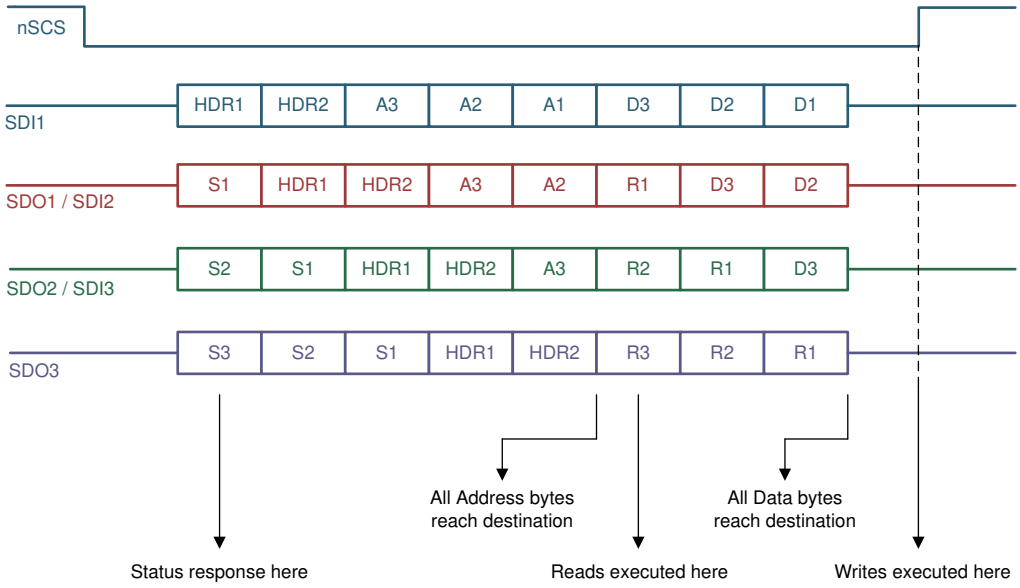


Figure 7-25. SPI Frame With Three Devices

After the data has been transmitted through the chain, the MCU receives the data string in the following format for 3-device configuration: 3 bytes of status (Sx) followed by 2 bytes of header followed by 3 bytes of report (Rx).

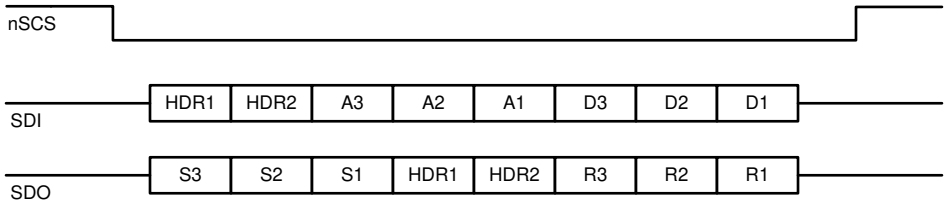


Figure 7-26. SPI Data Sequence for Three Devices

The header bytes contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. Header values N5 through N0 are 6 bits dedicated to show the number of devices in the chain. Up to 63 devices can be connected in series for each daisy chain connection.

The 5 LSBs of the HDR2 register are don't care bits that can be used by the MCU to determine integrity of the daisy chain connection. Header bytes must start with 1 and 0 for the two MSBs.

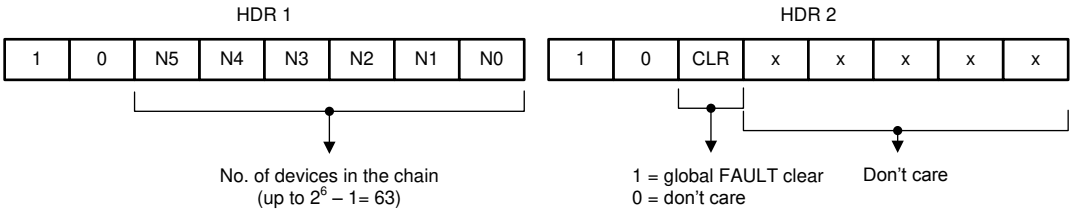


Figure 7-27. Header Bytes

The status byte provides information about the fault status register for each device in the daisy chain so that the MCU does not have to initiate a read command to read the fault status from any particular device. This keeps additional read commands for the MCU and makes the system more efficient to determine fault conditions flagged in a device. Status bytes must start with 1 and 1 for the two MSBs.

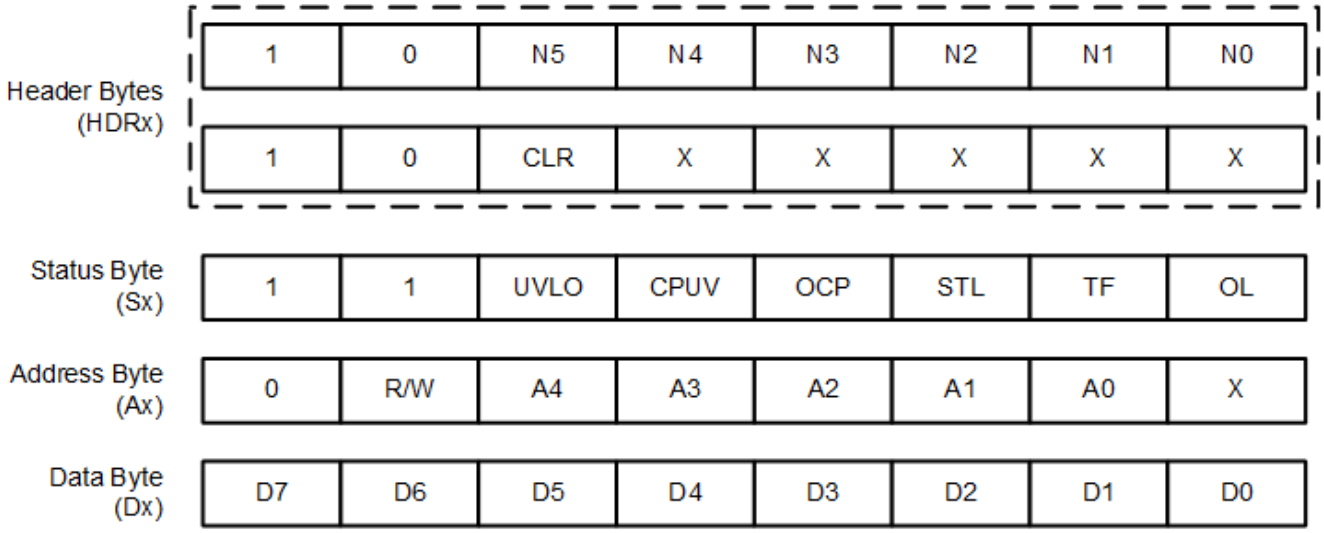


Figure 7-28. Contents of Header, Status, Address, and Data Bytes for DRV8434S

When data passes through a device, it determines the position of itself in the chain by counting the number of status bytes it receives followed by the first header byte. For example, in this 3-device configuration, device 2 in the chain receives two status bytes before receiving the HDR1 byte which is then followed by the HDR2 byte.

From the two status bytes, the data can determine that its position is second in the chain. From the HDR2 byte, the data can determine how many devices are connected in the chain. In this way, the data only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The address and data bytes remain the same with respect to a 1-device connection. The report bytes (R1 through R3), as shown in Figure 7-26, are the content of the register being accessed.

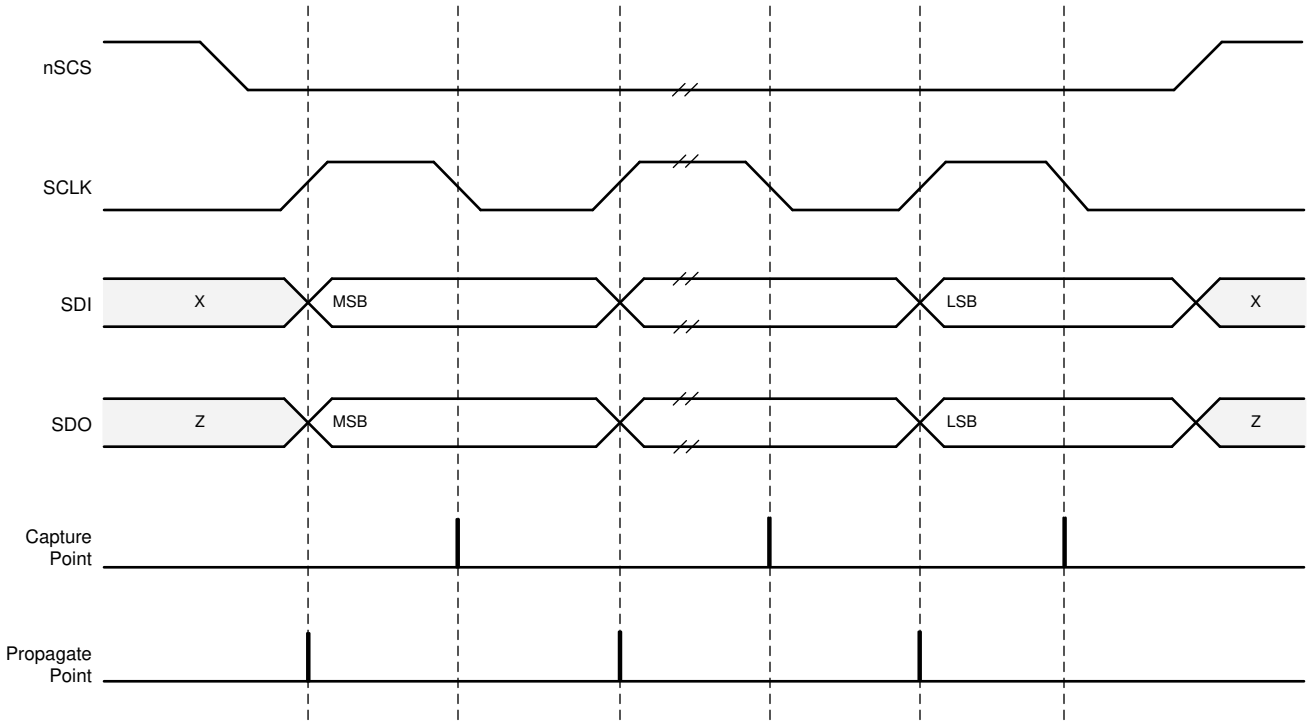


Figure 7-29. SPI Transaction

7.5.1.4 SPI for Multiple Target Devices in Parallel Configuration

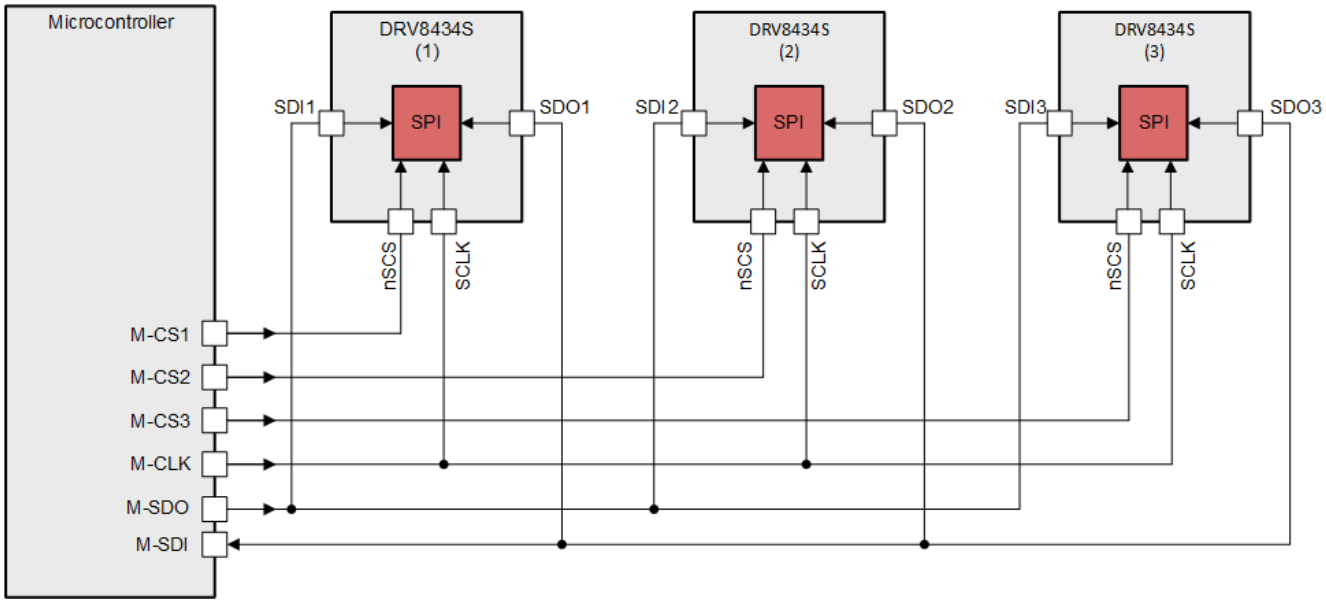


Figure 7-30. Three DRV8434S Devices Connected in Parallel Configuration

7.6 Register Maps

Table 7-15 lists the memory-mapped registers for the DRV8434S device. All register addresses not listed in Table 7-15 should be considered as reserved locations and the register contents must not be modified.

Table 7-15. Memory Map

Register Name	7	6	5	4	3	2	1	0	Access Type	Address
FAULT Status	FAULT	SPI_ERROR	UVLO	CPUV	OCP	STL	TF	OL	R	0x00
DIAG Status 1	OCP_LS2_B	OCP_HS2_B	OCP_LS1_B	OCP_HS1_B	OCP_LS2_A	OCP_HS2_A	OCP_LS1_A	OCP_HS1_A	R	0x01
DIAG Status 2	RSVD	OTW	OTS	STL_LRN_OK	STALL	RSVD	OL_B	OL_A	R	0x02
CTRL1	TRQ_DAC [3:0]				RSVD		OL_MODE	RSVD	RW	0x03
CTRL2	EN_OUT	RSVD		TOFF [1:0]		DECAY [2:0]			RW	0x04
CTRL3	DIR	STEP	SPI_DIR	SPI_STEP	MICROSTEP_MODE [3:0]				RW	0x05
CTRL4	CLR_FLT	LOCK [2:0]			EN_OL	OCP_MODE	OTSD_MODE	OTW_REP	RW	0x06
CTRL5	RSVD		STL_LRN	EN_STL	STL_REP	RSVD			RW	0x07
CTRL6	STALL_TH [7:0]								RW	0x08
CTRL7	RC_RIPPLE[1:0]		EN_SSC	TRQ_SCALE	STALL_TH[11:8]				RW	0x09
CTRL8	TRQ_COUNT [7:0]								R	0x0A
CTRL9	REV_ID[3:0]				TRQ_COUNT[11:8]				R	0x0B

Complex bit access types are encoded to fit into small table cells. Table 7-16 shows the codes that are used for access types in this section.

Table 7-16. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1 Status Registers

The status registers are used to reporting warning and fault conditions. Status registers are read-only registers

Table 7-17 lists the memory-mapped registers for the status registers. All register offset addresses not listed in Table 7-17 should be considered as reserved locations and the register contents should not be modified.

Table 7-17. Status Registers Summary Table

Address	Register Name	Section
0x00	FAULT status	Section 7.6.2
0x01	DIAG status 1	Section 7.6.3
0x02	DIAG status 2	Section 7.6.4

7.6.2 FAULT Status Register Name (address = 0x00)

FAULT status is shown in Figure 7-31 and described in Table 7-18.

Read-only

Figure 7-31. FAULT Status Register

7	6	5	4	3	2	1	0
FAULT	SPI_ERROR	UVLO	CPUV	OCP	STL	TF	OL
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-18. FAULT Status Register Field Descriptions

Bit	Field	Type	Default	Description
7	FAULT	R	0b	When nFAULT pin is at 1, FAULT bit is 0. When nFAULT pin is at 0, FAULT bit is 1.
6	SPI_ERROR	R	0b	Indicates SPI protocol errors, such as more SCLK pulses than are required or SCLK is absent even though nSCS is low. Becomes high in fault and the nFAULT pin is driven low. Normal operation resumes when the protocol error is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse.
5	UVLO	R	0b	Indicates an supply undervoltage lockout fault condition.
4	CPUV	R	0b	Indicates charge pump undervoltage fault condition.
3	OCP	R	0b	Indicates overcurrent fault condition
2	STL	R	0b	Indicates motor stall condition.
1	TF	R	0b	Logic OR of the overtemperature warning and overtemperature shutdown.
0	OL	R	0b	Indicates open-load condition.

7.6.3 DIAG Status 1 (address = 0x01)

DIAG Status 1 is shown in Figure 7-32 and described in Table 7-19.

Read-only

Figure 7-32. DIAG Status 1 Register

7	6	5	4	3	2	1	0
OCP_LS2_B	OCP_HS2_B	OCP_LS1_B	OCP_HS1_B	OCP_LS2_A	OCP_HS2_A	OCP_LS1_A	OCP_HS1_A
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-19. DIAG Status 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	OCP_LS2_B	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 2 in BOUT
6	OCP_HS2_B	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 2 in BOUT

Table 7-19. DIAG Status 1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	OCP_LS1_B	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 1 in BOUT
4	OCP_HS1_B	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 1 in BOUT
3	OCP_LS2_A	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 2 in AOUT
2	OCP_HS2_A	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 2 in AOUT
1	OCP_LS1_A	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 1 in AOUT
0	OCP_HS1_A	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 1 in AOUT

7.6.4 DIAG Status 2 (address = 0x02)

DIAG Status 2 is shown in Figure 7-33 and described in Table 7-20.

Read-only

Figure 7-33. DIAG Status 2 Register

7	6	5	4	3	2	1	0
RSVD	OTW	OTS	STL_LRN_OK	STALL	RSVD	OL_B	OL_A
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-20. DIAG Status 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R	0b	Resrved.
6	OTW	R	0b	Indicates overtemperature warning.
5	OTS	R	0b	Indicates overtemperature shutdown.
4	STL_LRN_OK	R	0b	Indicates stall detection learning is successful
3	STALL	R	0b	Indicates motor stall condition
2	RSVD	R	0b	Reserved.
1	OL_B	R	0b	Indicates open-load detection on BOUT
0	OL_A	R	0b	Indicates open-load detection on AOUT

7.6.5 Control Registers

The IC control registers are used to configure the device. Status registers are read and write capable.

Table 7-21 lists the memory-mapped registers for the control registers. All register offset addresses not listed in Table 7-21 should be considered as reserved locations and the register contents should not be modified.

Table 7-21. Control Registers Summary Table

Address	Register Name	Section
0x03	CTRL1	Section 7.6.6
0x04	CTRL2	Section 7.6.7
0x05	CTRL3	Section 7.6.8
0x06	CTRL4	Section 7.6.9
0x07	CTRL5	Section 7.6.10
0x08	CTRL6	Section 7.6.11
0x09	CTRL7	Section 7.6.12
0x0A	CTRL8	Section 7.6.13
0x0B	CTRL9	

7.6.6 CTRL1 Control Register (address = 0x03)

CTRL1 control is shown in Figure 7-34 and described in Table 7-22.

Read/Write

Figure 7-34. CTRL1 Control Register

7	6	5	4	3	2	1	0
TRQ_DAC [3:0]				RSVD		OL_MODE	RSVD
R/W-0000b				R/W-00b		R/W-0b	R/W-0b

Table 7-22. CTRL1 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	TRQ_DAC [3:0]	R/W	0000b	**0000b = 100%** 0001b = 93.75% 0010b = 87.5% 0011b = 81.25% 0100b = 75% 0101b = 68.75% 0110b = 62.5% 0111b = 56.25% 1000b = 50% 1001b = 43.75% 1010b = 37.5% 1011b = 31.25% 1100b = 25% 1101b = 18.75% 1110b = 12.5% 1111b = 6.25%
3-2	RSVD	R/W	00b	Reserved
1	OL_MODE	R/W	0b	**0b = nFAULT is released after latched OL fault is cleared using CLR_FLT bit or nSLEEP reset pulse** 1b = nFAULT is released immediately after OL fault condition is removed
0	RSVD	R/W	0b	Reserved

7.6.7 CTRL2 Control Register (address = 0x04)

CTRL2 is shown in Figure 7-35 and described in Table 7-23.

Read/Write

Figure 7-35. CTRL2 Control Register

7	6	5	4	3	2	1	0
EN_OUT	RSVD		TOFF [1:0]		DECAY [2:0]		
R/W-0b	R/W-00b		R/W-01b		R/W-111b		

Table 7-23. CTRL2 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	EN_OUT	R/W	0b	Write '0' to disable all outputs.
6-5	RSVD	R/W	00b	Reserved
4-3	TOFF [1:0]	R/W	01b	00b = 7 µs **01b = 16 µs** 10b = 24 µs 11b = 32 µs

Table 7-23. CTRL2 Control Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
2-0	DECAY [2:0]	R/W	111b	000b = Increasing SLOW, decreasing SLOW 001b = Increasing SLOW, decreasing MIXED 30% 010b = Increasing SLOW, decreasing MIXED 60% 011b = Increasing SLOW, decreasing FAST 100b = Increasing MIXED 30%, decreasing MIXED 30% 101b = Increasing MIXED 60%, decreasing MIXED 60% 110b = Smart tune Dynamic Decay **111b = Smart tune Ripple Control**

7.6.8 CTRL3 Control Register (address = 0x05)

CTRL3 is shown in Figure 7-36 and described in Table 7-24.

Read/Write

Figure 7-36. CTRL3 Control Register

7	6	5	4	3	2	1	0
DIR	STEP	SPI_DIR	SPI_STEP	MICROSTEP_MODE [3:0]			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0110b			

Table 7-24. CTRL3 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	DIR	R/W	0b	Direction input. Logic '1' sets the direction of stepping, when SPI_DIR = 1.
6	STEP	R/W	0b	Step input. Logic '1' causes the indexer to advance one step, when SPI_STEP = 1. This bit is self-clearing, automatically becomes '0' after writing '1'.
5	SPI_DIR	R/W	0b	**0b = Outputs follow input pin for DIR** 1b = Outputs follow SPI registers DIR
4	SPI_STEP	R/W	0b	**0b = Outputs follow input pin for STEP** 1b = Outputs follow SPI registers STEP
3-0	MICROSTEP_MODE [3:0]	R/W	0110b	**0000b = Full step (2-phase excitation) with 100% current** 0001b = Full step (2-phase excitation) with 71% current 0010b = Non-circular 1/2 step 0011b = 1/2 step 0100b = 1/4 step 0101b = 1/8 step 0110b = 1/16 step 0111b = 1/32 step 1000b = 1/64 step 1001b = 1/128 step 1010b = 1/256 step 1011b to 1111b = Reserved

7.6.9 CTRL4 Control Register (address = 0x06)

CTRL4 is shown in Figure 7-37 and described in Table 7-25.

Read/Write

Figure 7-37. CTRL4 Control Register

7	6	5	4	3	2	1	0
CLR_FLT	LOCK [2:0]			EN_OL	OCP_MODE	OTSD_MODE	OTW_REP
R/W-0b	R/W-011b			R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-25. CTRL4 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	CLR_FLT	R/W	0b	Write '1' to this bit to clear all latched fault bits. This bit automatically resets after being written.
6-4	LOCK [2:0]	R/W	011b	Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x06h bit 7 (CLR_FLT). Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
3	EN_OL	R/W	0b	Write '1' to enable open load detection
2	OCP_MODE	R/W	0b	**0b = Overcurrent condition causes a latched fault** 1b = Overcurrent condition causes an automatic retrying fault
1	OTSD_MODE	R/W	0b	**0b = Overtemperature condition will cause latched fault** 1b = Overtemperature condition will cause automatic recovery fault
0	TW_REP	R/W	0b	**0b = Overtemperature or undertemperature warning is not reported on the nFAULT line** 1b = Overtemperature or undertemperature warning is reported on the nFAULT line

7.6.10 CTRL5 Control Register (address = 0x07)

CTRL5 control is shown in Figure 7-38 and described in Table 7-26.

Read/Write

Figure 7-38. CTRL5 Control Register

7	6	5	4	3	2	1	0
RSVD		STL_LRN	EN_STL	STL_REP	RSVD		
R/W-00b		R/W-0b	R/W-0b	R/W-1b	R/W-000b		

Table 7-26. CTRL5 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RSVD	R/W	00b	Reserved. Should always be '00'.
5	STL_LRN	R/W	0b	Write '1' to learn stall count for stall detection. This bit automatically returns to '0' when the stall learning process is complete.
4	EN_STL	R/W	0b	**0b = Stall detection is disabled** 1b = Stall detection is enabled
3	STL_REP	R/W	1b	0b = Stall detection is not reported on nFAULT **1b = Stall detection is reported on nFAULT**
2-0	RSVD	R/W	000b	Reserved. Should always be '000'.

7.6.11 CTRL6 Control Register (address = 0x08)

CTRL6 is shown in Figure 7-39 and described in Table 7-27.

Read/Write

Figure 7-39. CTRL6 Control Register

7	6	5	4	3	2	1	0
STALL_TH [7:0]							
R/W-00000011b							

Table 7-27. CTRL6 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	STALL_TH [7:0]	R/W	00000011b	Lower 8-bits of stall threshold. 000000000000b = 0 count XXXXXXXXXXXXb = 1 to 4094 counts 111111111111b = 4095 counts

7.6.12 CTRL7 Control Register (address = 0x09)

CTRL7 is shown in Figure 7-40 and described in Table 7-28.

Read-only

Figure 7-40. CTRL7 Control Register

7	6	5	4	3	2	1	0
RC_RIPPLE[1:0]		EN_SSC	TRQ_SCALE	STALL_TH[11:8]			
R/W-00b		R/W-1b	R/W-0b	R/W-0000b			

Table 7-28. CTRL7 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RC_RIPPLE[1:0]	R/W	00b	**00b = 1% ripple** 01b = 2% ripple 10b = 4% ripple 11b = 6% ripple
5	EN_SSC	R/W	1b	**1b = spread-spectrum enabled** 0b = spread-spectrum disabled
4	TRQ_SCALE	R/W	0b	**0b = No torque count scaling is applied** 1b = Torque count is scaled up by a factor of 8
3-0	STALL_TH	R/W	0000b	Upper 4-bits of stall threshold.

7.6.13 CTRL8 Control Register (address = 0x0A)

CTRL8 is shown in Figure 7-41 and described in Table 7-29.

Read-only

Figure 7-41. CTRL8 Control Register

7	6	5	4	3	2	1	0
TRQ_COUNT[7:0]							
R-11111111b							

Table 7-29. CTRL8 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	TRQ_COUNT	R	11111111b	Lower 8-bits of TRQ_COUNT. 000000000000b = 0 count XXXXXXXXXXXXb = 1 to 4094 counts 111111111111b = 4095 counts

7.6.14 CTRL9 Control Register (address = 0x0B)

CTRL9 is shown in Figure 7-42 and described in Table 7-30.

Read-only

Figure 7-42. CTRL9 Control Register

7	6	5	4	3	2	1	0

Figure 7-42. CTRL9 Control Register (continued)

REV_ID[3:0]	TRQ_COUNT[11:8]
R-0000b	R-1111b

Table 7-30. CTRL9 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	REV_ID	R	0000b	Silicon Revision Identification. 0000b indicates Production Revision.
3-0	TRQ_COUNT	R	1111b	Upper 4-bits of TRQ_COUNT.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8434S is used in bipolar stepper control.

8.2 Typical Application

The following design procedure can be used to configure the DRV8434S.

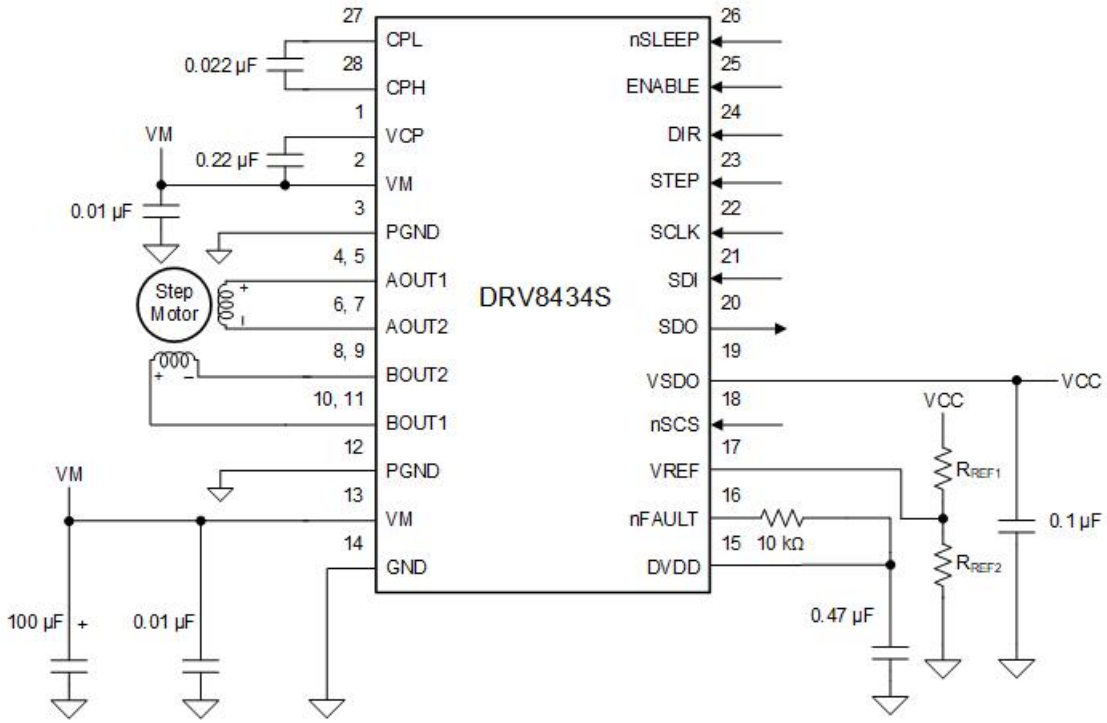


Figure 8-1. Typical Application Schematic (HTSSOP package)

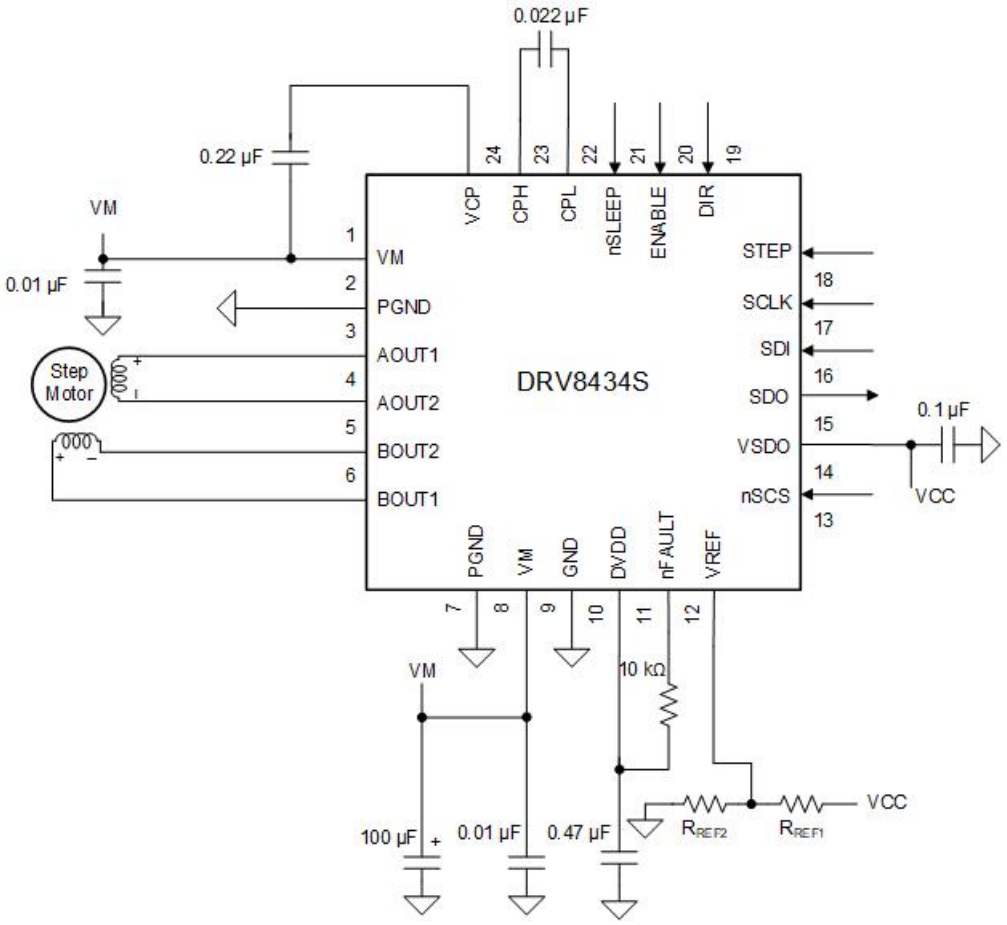


Figure 8-2. Typical Application Schematic (VQFN package)

8.2.1 Design Requirements

Table 8-1 lists the design input parameters for system design.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	0.9 Ω/phase
Motor winding inductance	L_L	1.4 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	1/8 step
Target motor speed	v	18.75 rpm
Target full-scale current	I_{FS}	2 A

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8434S requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin. If the target motor speed is too high, the motor does not spin. Make sure that the motor can support the target speed. Use Equation 2 to calculate f_{step} for a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step})

$$f_{step}\ (\text{steps / s}) = \frac{\text{v (rpm)} \times 360\ (^\circ / \text{rot})}{\theta_{step}\ (^\circ / \text{step}) \times n_m\ (\text{steps / microstep}) \times 60\ (\text{s / min})} \quad (2)$$

The value of θ_{step} can be found in the stepper motor data sheet, or written on the motor. For example, the motor in this application is required to rotate at 1.8°/step for a target of 18.75 rpm at 1/8 microstep mode. Using Equation 2, f_{step} can be calculated as 500 Hz.

The microstepping level is set by the MICROSTEP_MODE bits. Higher microstepping results in a smoother motor motion and less audible noise, but requires a higher f_{step} to achieve the same motor speed.

8.2.2.2 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the VREF voltage and the TRQ_DAC setting, as shown in Equation 3.

The maximum allowable voltage on the VREF pin is 3.3 V. DVDD can be used to provide VREF through aresistor divider.

During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step.

$$I_{FS}(A) = \frac{V_{REF}(V)}{K_V(V/A)} \times \text{TRQ\_DAC}(\%) = \frac{V_{REF}(V) \times \text{TRQ\_DAC}(\%)}{1.32(V/A)} \quad (3)$$

8.2.2.3 Decay Mode

The DRV8434A operates with smart tune ripple control decay mode. When a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8434A places the winding in slow decay.

8.2.2.4 Application Curves

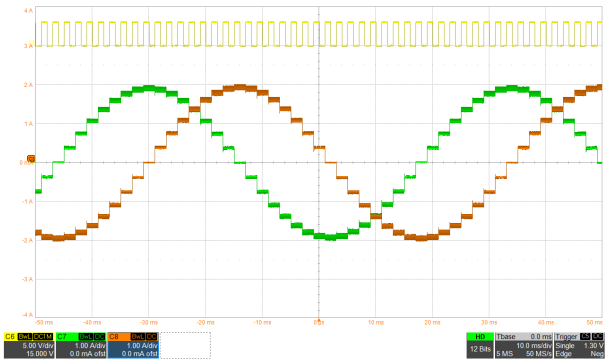


Figure 8-3. 1/8 Microstepping With smart tune Ripple Control Decay

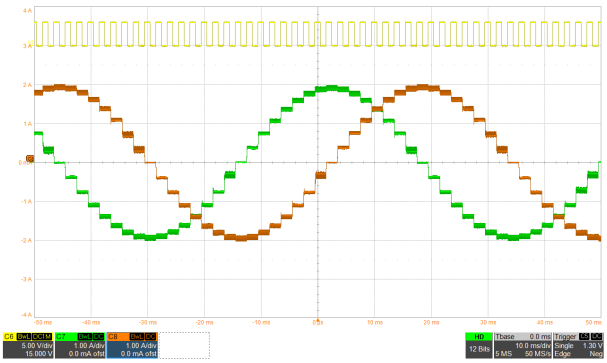


Figure 8-4. 1/8 Microstepping With smart tune Dynamic Decay

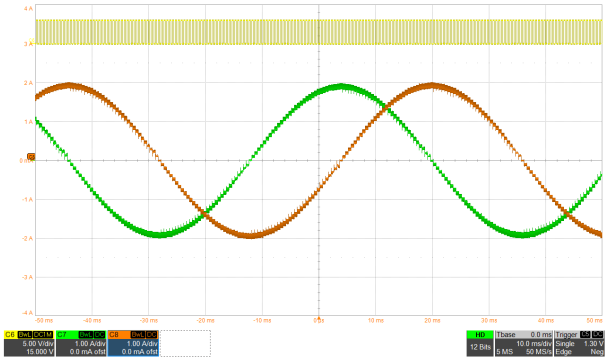


Figure 8-5. 1/32 Microstepping With smart tune Ripple Control Decay

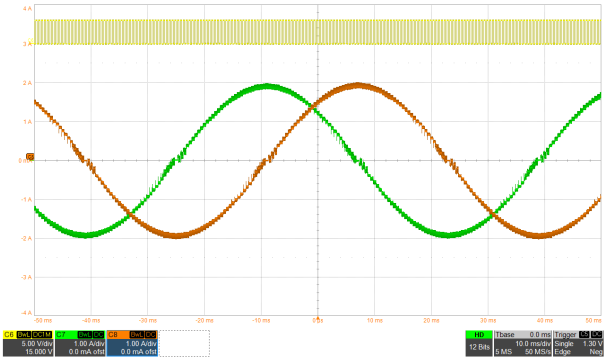


Figure 8-6. 1/32 Microstepping With smart tune Dynamic Decay

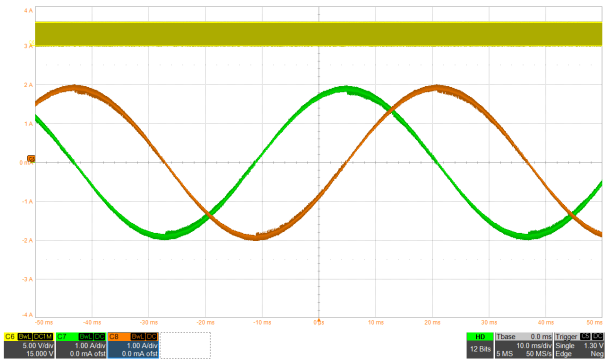


Figure 8-7. 1/256 Microstepping With smart tune Ripple Control Decay

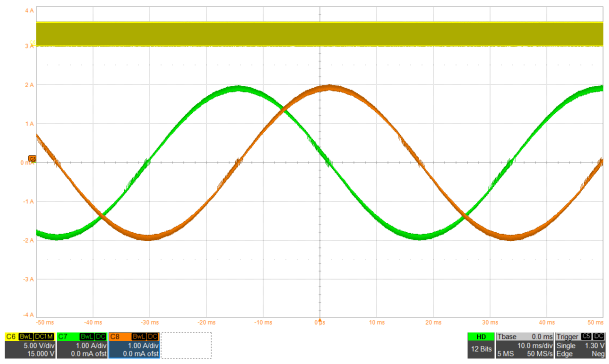


Figure 8-8. 1/256 Microstepping With smart tune Dynamic Decay

8.2.2.5 Thermal Application

This section presents the power dissipation calculation and junction temperature estimation of the device.

8.2.2.5.1 Power Dissipation

The total power dissipation constitutes of three main components - conduction loss (P_{COND}), switching loss (P_{SW}) and power loss due to quiescent current consumption (P_Q).

8.2.2.5.2 Conduction Loss

The current path for a motor connected in full-bridge is through the high-side FET of one half-bridge and low-side FET of the other half-bridge. The conduction loss (P_{COND}) depends on the motor rms current (I_{RMS}) and high-side ($R_{DS(ONH)}$) and low-side ($R_{DS(ONL)}$) on-state resistances as shown in Equation 4.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) \quad (4)$$

The conduction loss for the typical application shown in Table 8-1 is calculated in Equation 5.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) = 2 \times (2\text{-A} / \sqrt{2})^2 \times (0.165\text{-}\Omega + 0.165\text{-}\Omega) = 1.32\text{-W} \quad (5)$$

Note

This power calculation is highly dependent on the device temperature which significantly effects the high-side and low-side on-resistance of the FETs. For more accurate calculation, consider the dependency of on-resistance of FETs with device temperature.

8.2.2.5.3 Switching Loss

The power loss due to the PWM switching frequency depends on the slew rate (t_{SR}), supply voltage, motor RMS current and the PWM switching frequency. The switching losses in each H-bridge during rise-time and fall-time are calculated as shown in Equation 6 and Equation 7.

$$P_{SW\_RISE} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RISE\_PWM} \times f_{PWM} \quad (6)$$

$$P_{SW\_FALL} = 0.5 \times V_{VM} \times I_{RMS} \times t_{FALL\_PWM} \times f_{PWM} \quad (7)$$

Both t_{RISE_PWM} and t_{FALL_PWM} can be approximated as V_{VM}/ t_{SR}. After substituting the values of various parameters, and assuming 30-kHz PWM frequency, the switching losses in each H-bridge are calculated as shown below -

$$P_{SW\_RISE} = 0.5 \times 24\text{-V} \times (2\text{-A} / \sqrt{2}) \times (24\text{-V} / 240\ \text{V/µs}) \times 30\text{-kHz} = 0.05\text{-W} \quad (8)$$

$$P_{SW\_FALL} = 0.5 \times 24\text{-V} \times (1\text{-A} / \sqrt{2}) \times (24\text{-V} / 240\ \text{V/µs}) \times 30\text{-kHz} = 0.05\text{-W} \quad (9)$$

The total switching loss for the stepper motor driver (P_{SW}) is calculated as twice the sum of rise-time (P_{SW_RISE}) switching loss and fall-time (P_{SW_FALL}) switching loss as shown below -

$$P_{SW} = 2 \times (P_{SW\_RISE} + P_{SW\_FALL}) = 2 \times (0.05\text{-W} + 0.05\text{-W}) = 0.2\text{-W} \quad (10)$$

Note

The rise-time (t_{RISE}) and the fall-time (t_{FALL}) are calculated based on typical values of the slew rate (t_{SR}). This parameter is expected to change based on the supply-voltage, temperature and device to device variation.

The switching loss is directly proportional to the PWM switching frequency. The PWM frequency in an application will depend on the supply voltage, inductance of the motor coil, back emf voltage and OFF time or the ripple current (for smart tune ripple control decay mode).

8.2.2.5.4 Power Dissipation Due to Quiescent Current

The power dissipation due to the quiescent current consumed by the power supply is calculated as shown below -

$$P_Q = V_{VM} \times I_{VM} \quad (11)$$

Substituting the values, quiescent power loss can be calculated as shown below -

$$P_Q = 24\text{-V} \times 5\text{-mA} = 0.12\text{-W} \quad (12)$$

Note

The quiescent power loss is calculated using the typical operating supply current (I_{VM}) which is dependent on supply-voltage, temperature and device to device variation.

8.2.2.5.5 Total Power Dissipation

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss as shown in Equation 13.

$$P_{TOT} = P_{COND} + P_{SW} + P_Q = 1.32\text{-W} + 0.2\text{-W} + 0.12\text{-W} = 1.64\text{-W} \quad (13)$$

8.2.2.5.6 Device Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as -

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 29.7 °C/W for the HTSSOP package and 39 °C/W for the VQFN package.

Assuming 25°C ambient temperature, the junction temperature for the HTSSOP package is calculated as shown below -

$$T_J = 25°C + (1.64\text{-W} \times 29.7°C/W) = 73.71°C \quad (14)$$

The junction temperature for the VQFN package is calculated as shown below -

$$T_J = 25°C + (1.64\text{-W} \times 39°C/W) = 88.96\ °C \quad (15)$$

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply (VM) range from 4.5 V to 48 V. A 0.01-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the device as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

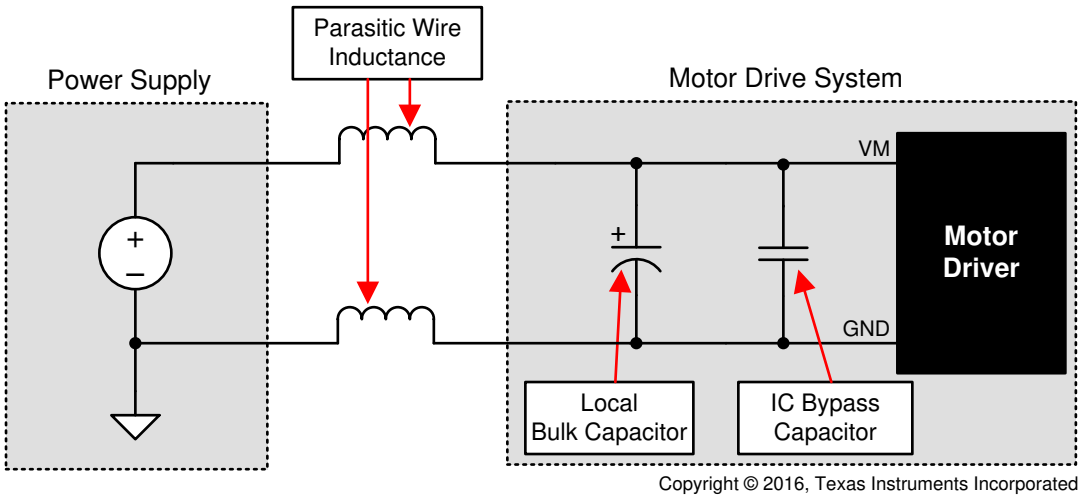


Figure 9-1. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to PGND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device PGND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.022 µF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 0.47 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.

10.1.1 Layout Example

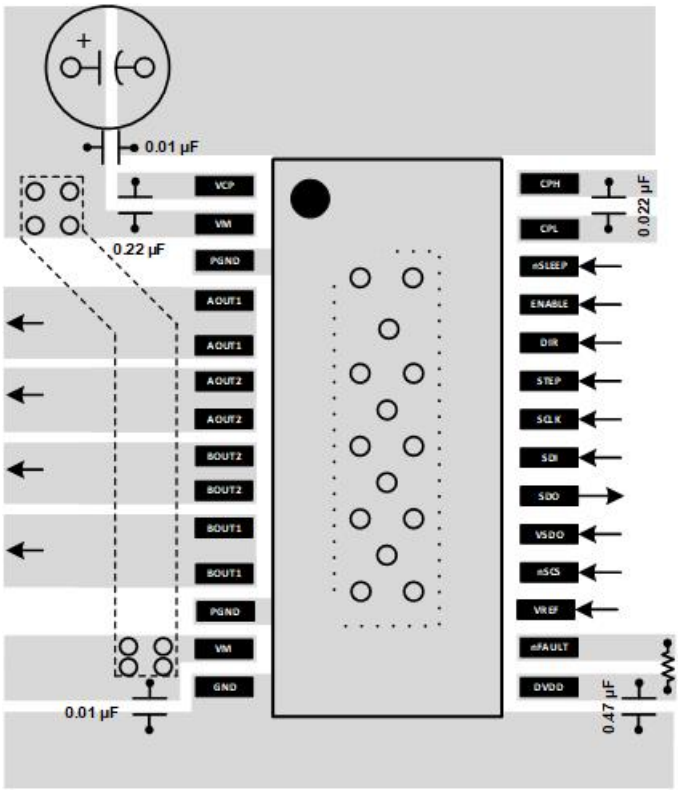


Figure 10-1. HTSSOP Layout Example

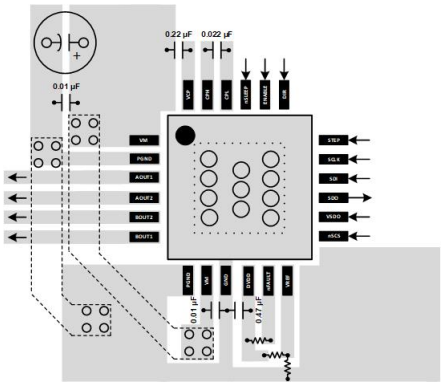


Figure 10-2. QFN Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

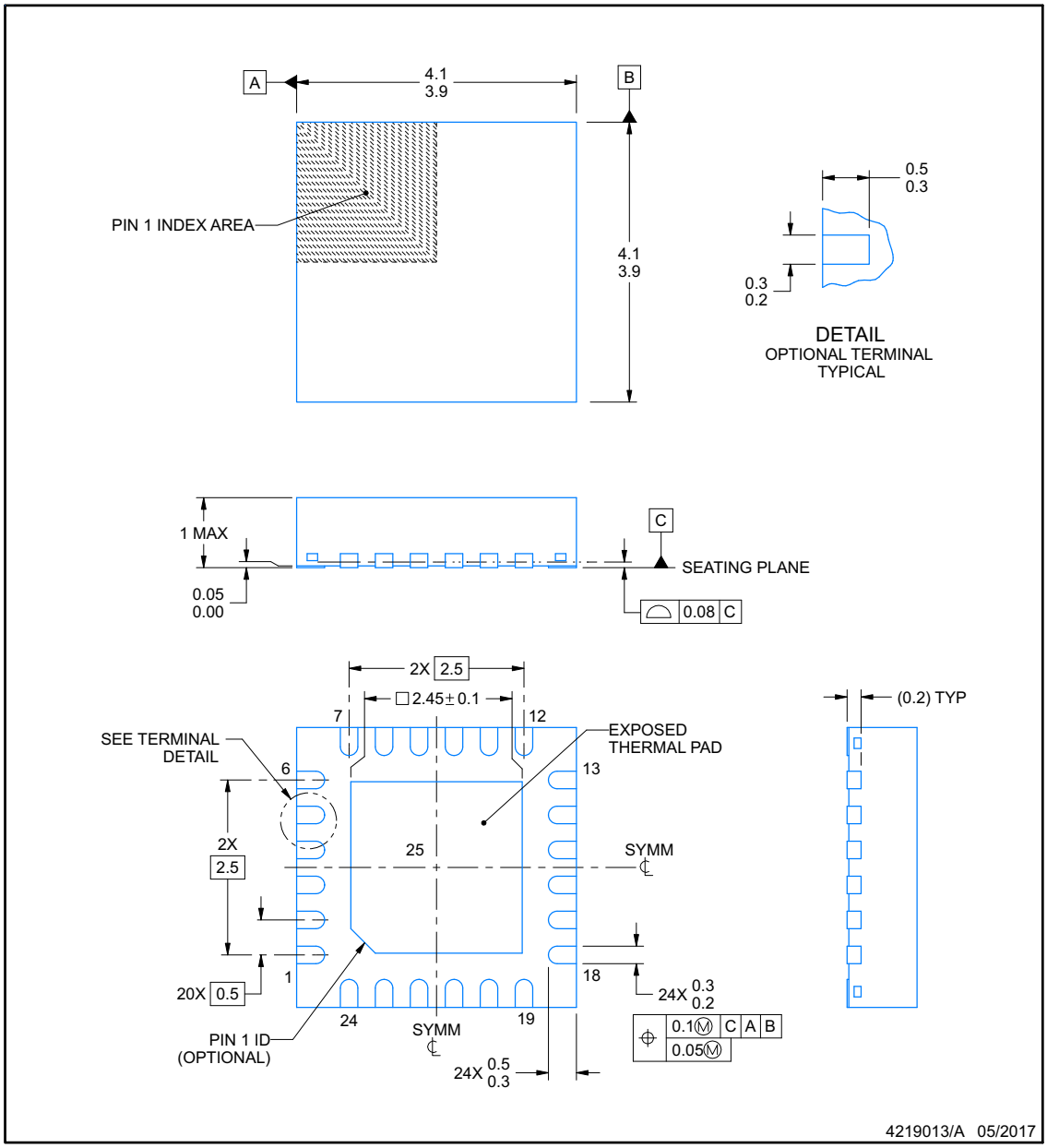
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

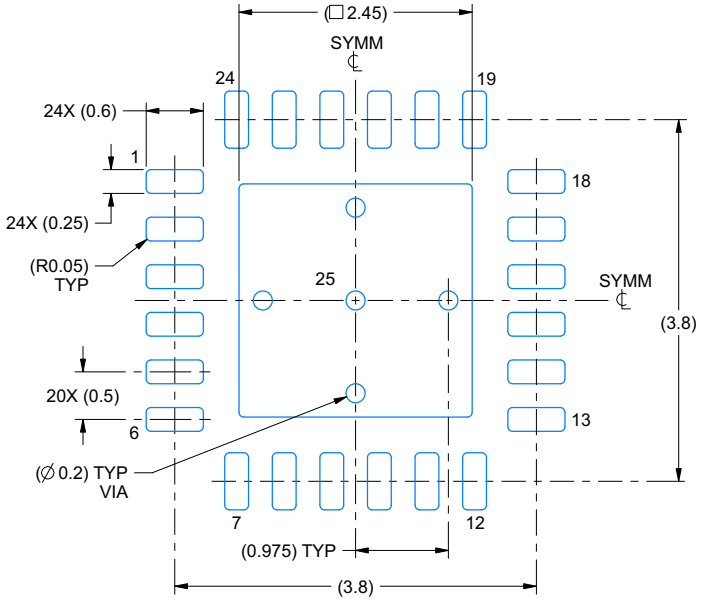
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

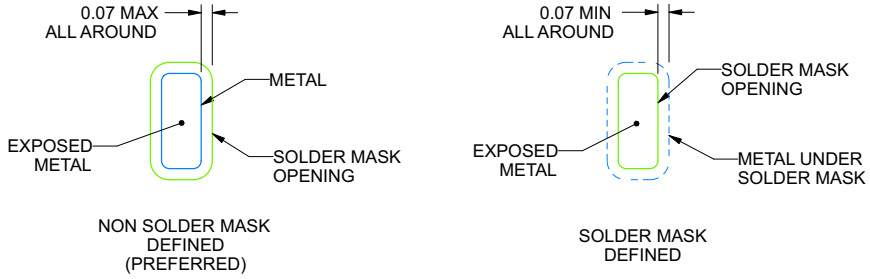
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

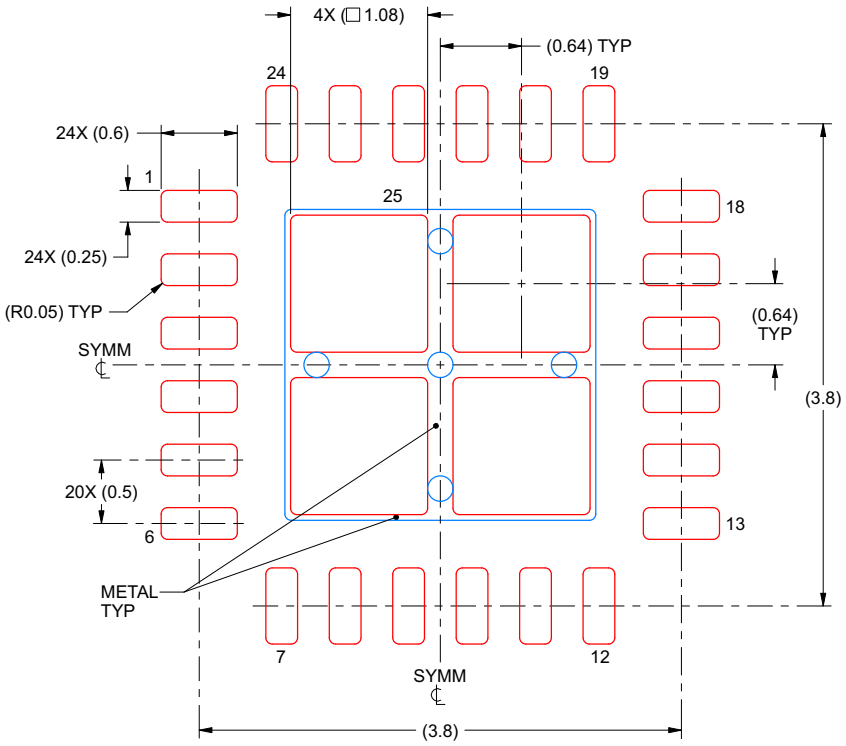
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

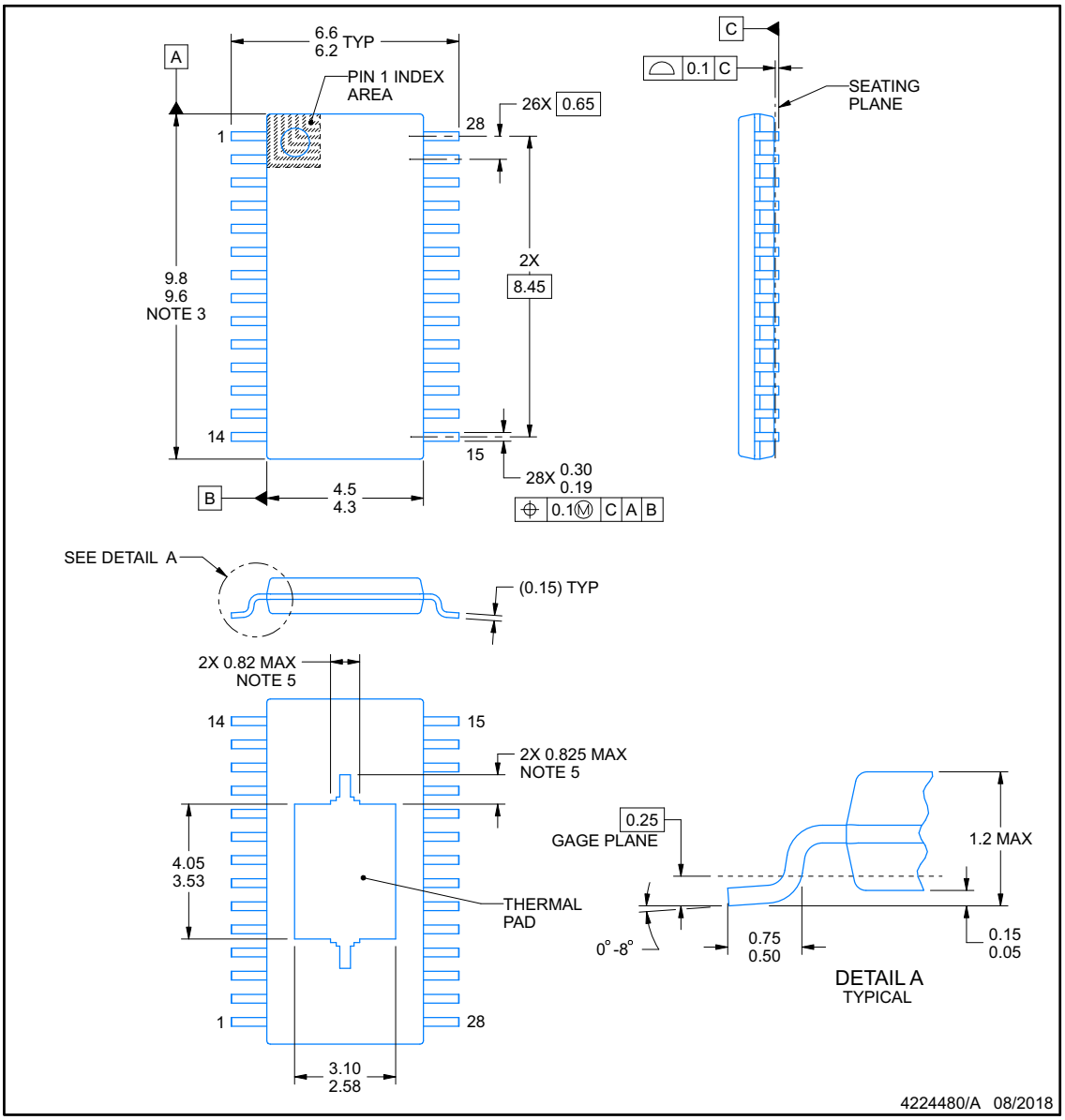
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

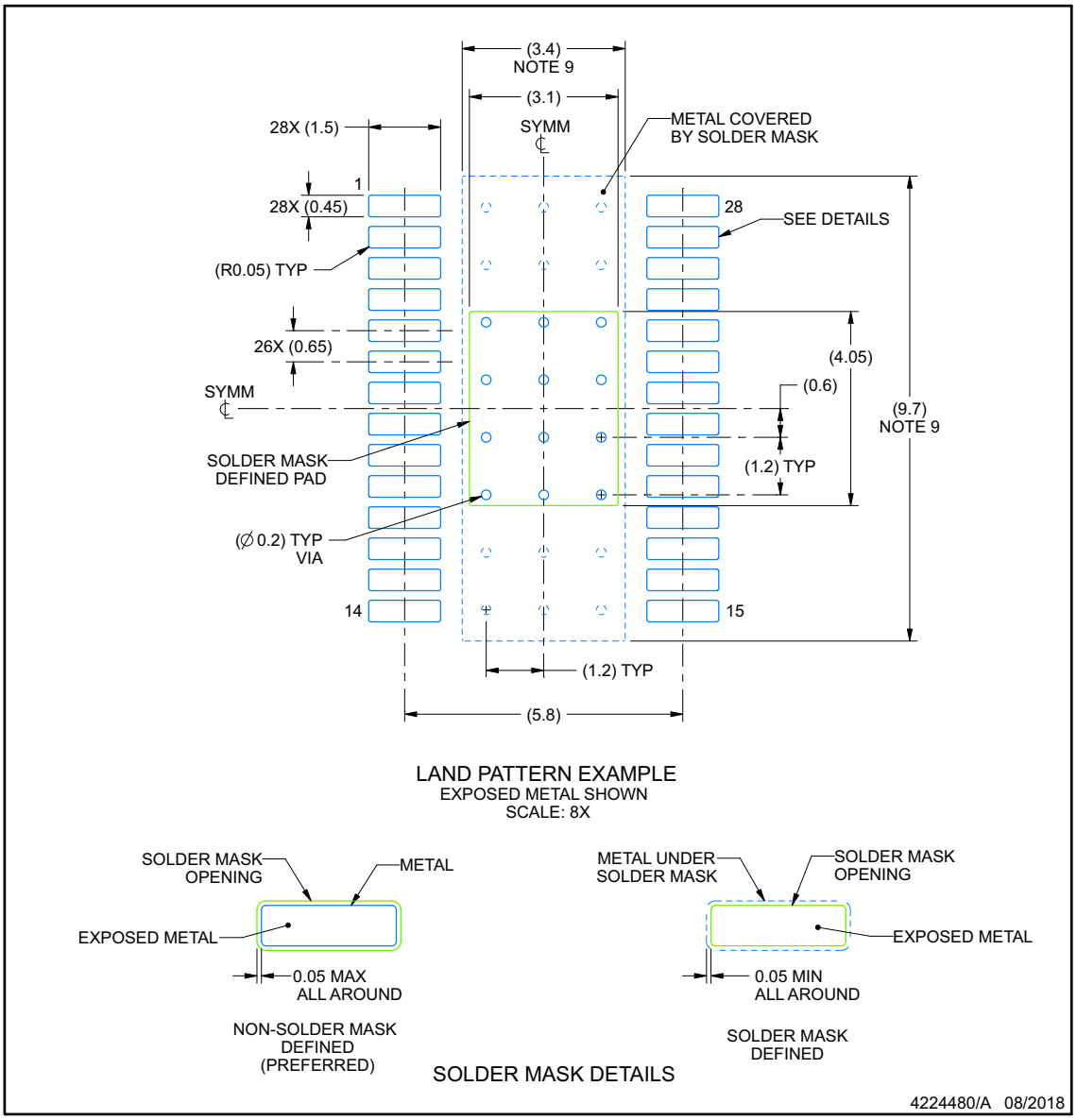
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

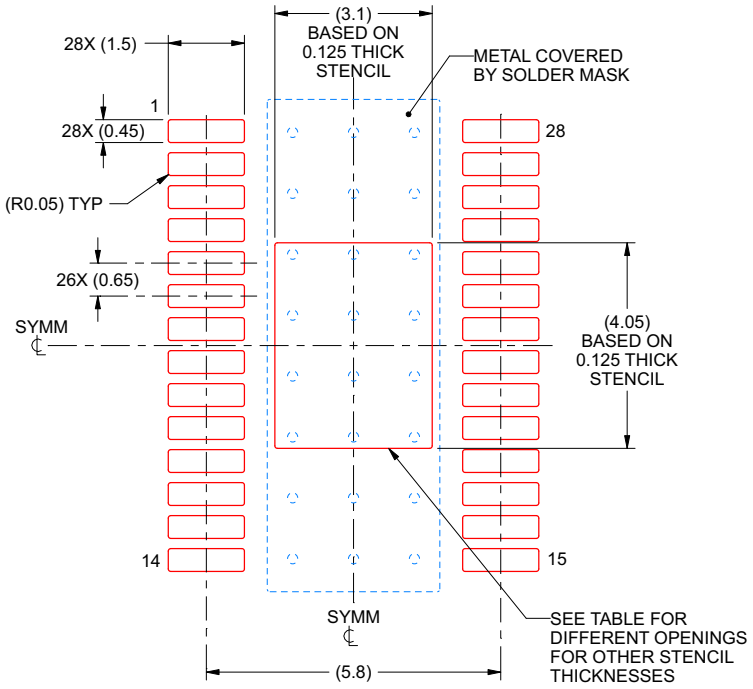
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 4.53
0.125	3.10 X 4.05 (SHOWN)
0.15	2.83 X 3.70
0.175	2.62 X 3.42

4224480/A 08/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8434SPWPR	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8434S	Samples
DRV8434SRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV 8434S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

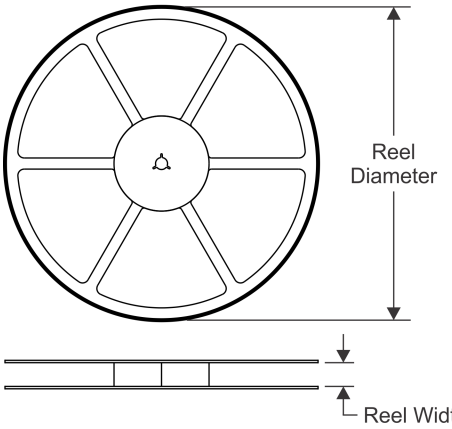
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

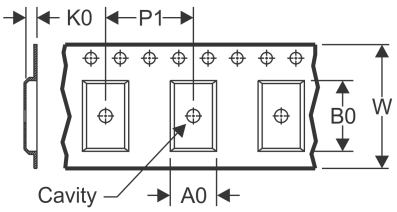
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

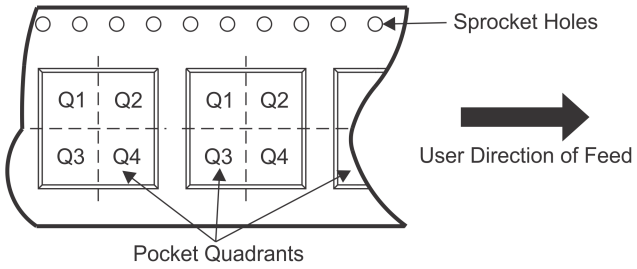


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

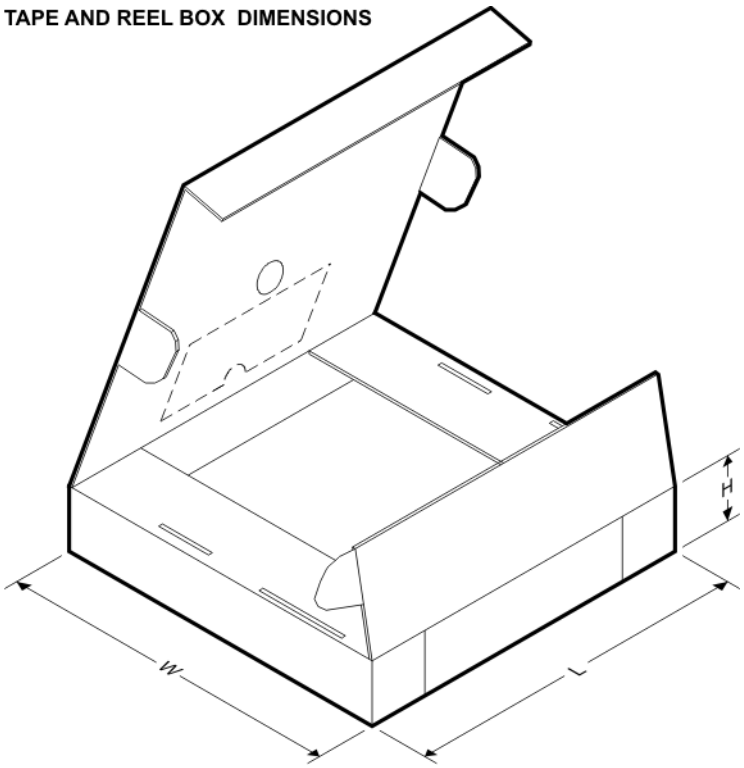
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8434SPWPR	HTSSOP	PWP	28	2500	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
DRV8434SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8434SPWPR	HTSSOP	PWP	28	2500	853.0	449.0	35.0
DRV8434SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

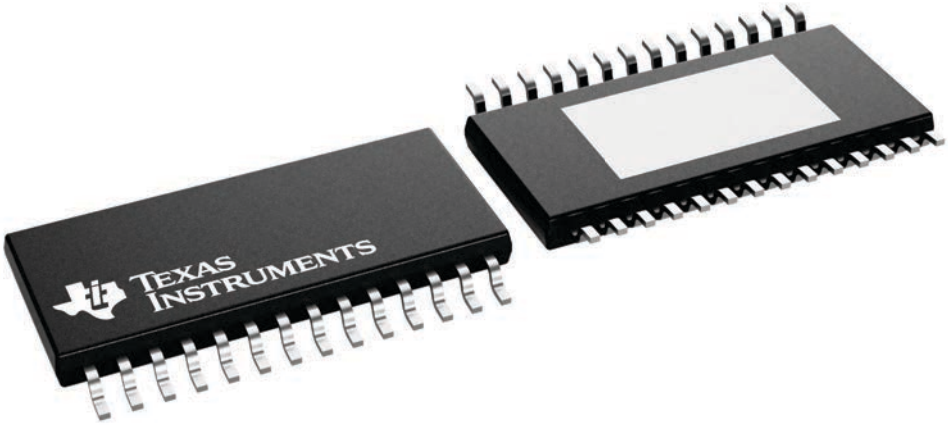
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

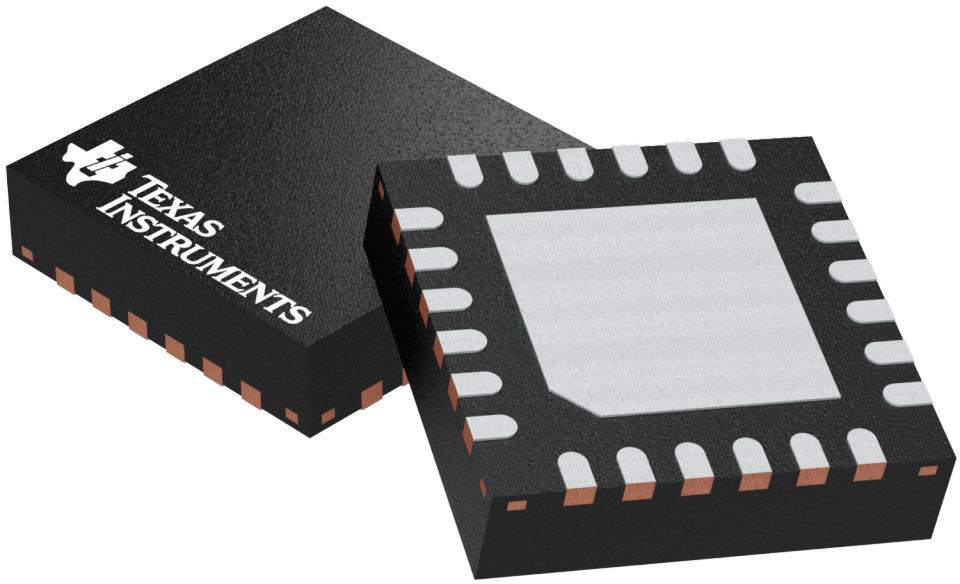


4224765/B

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

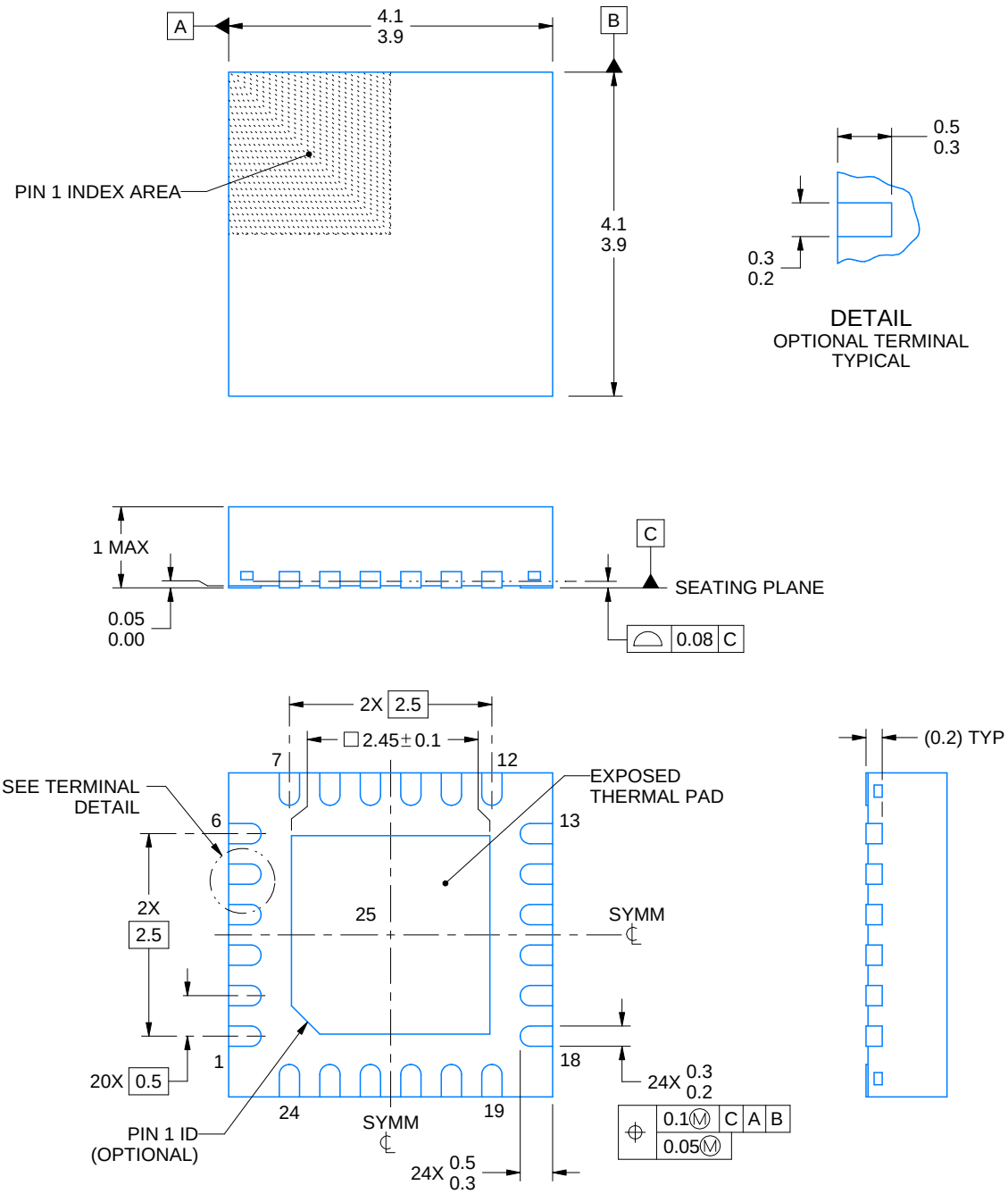
4204104/H

PACKAGE OUTLINE

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

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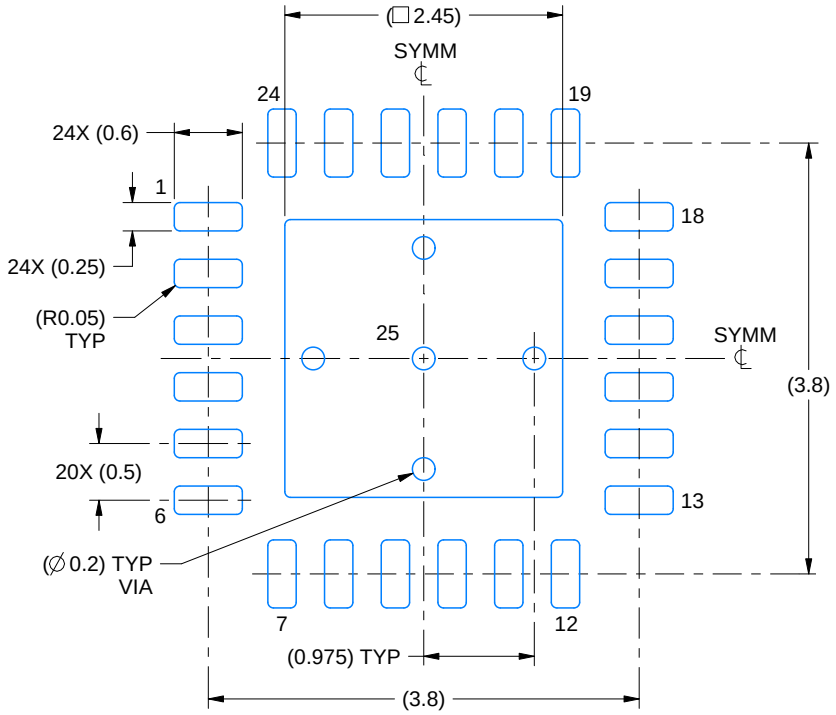
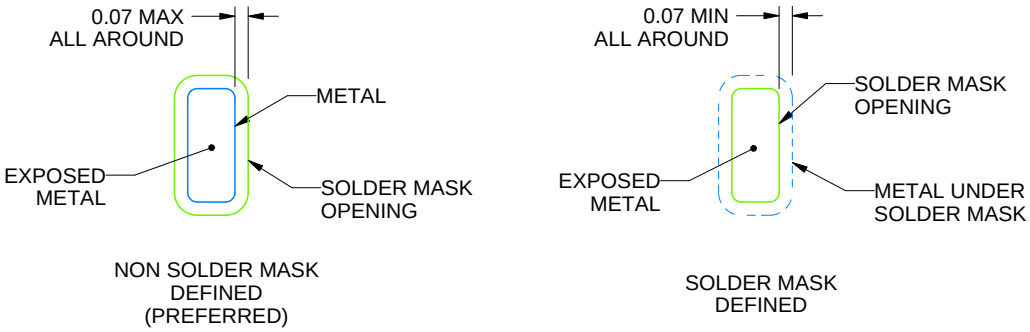
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

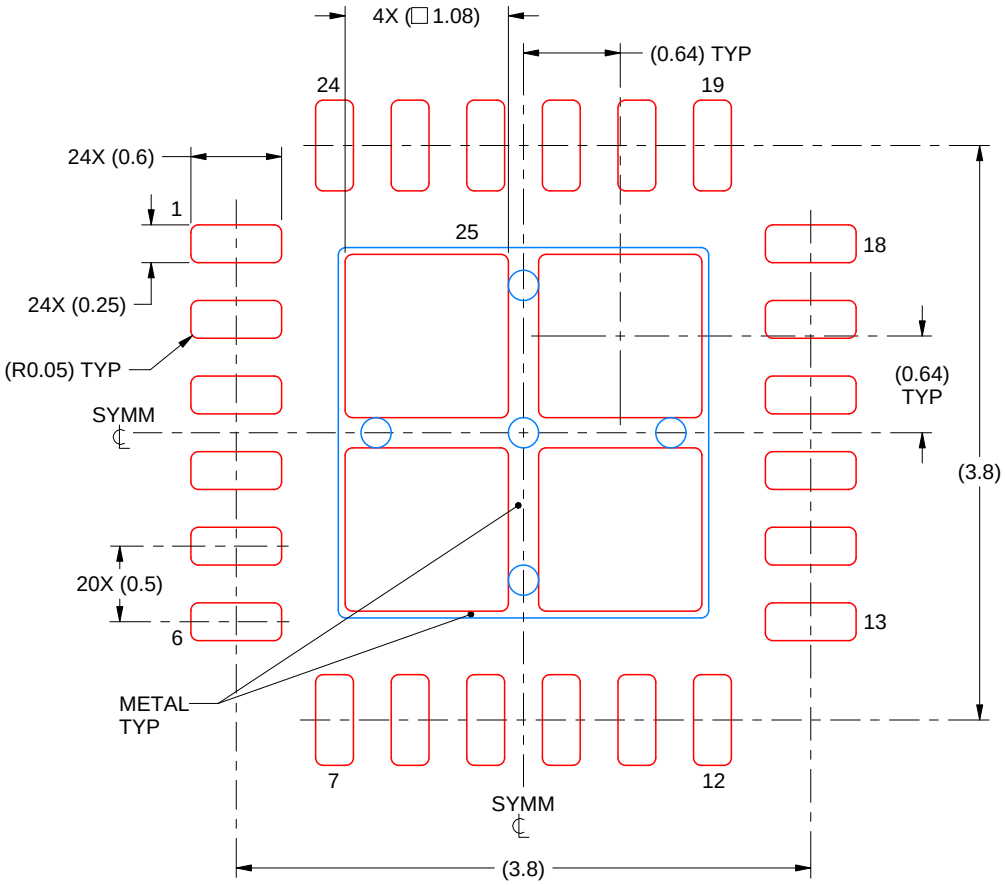


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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