三相脉宽调制 (PWM) 电机驱动器

查询样品: DRV8332-HT

特性

- 具有低 R_{DS}（导通）金属氧化物半导体场效应晶体管 (MOSFET)（T_J= 25°C 时为 80mΩ）的高效功率驱动器（高达 97%）
- 运行电源电压高达 50V（绝对最大值 70V）
- 高达 5A 持续相电流（峰值 7A）
- 三相半桥独立控制
- PWM 运行频率高达 500kHz
- 片内集成欠压、过温、过载和短路保护功能
- 可编程逐周期电流限制保护
- 针对每个半桥的独立电源和接地引脚
- 智能栅极驱动和交叉导电预防
- 无需外部缓冲器或肖特基二极管

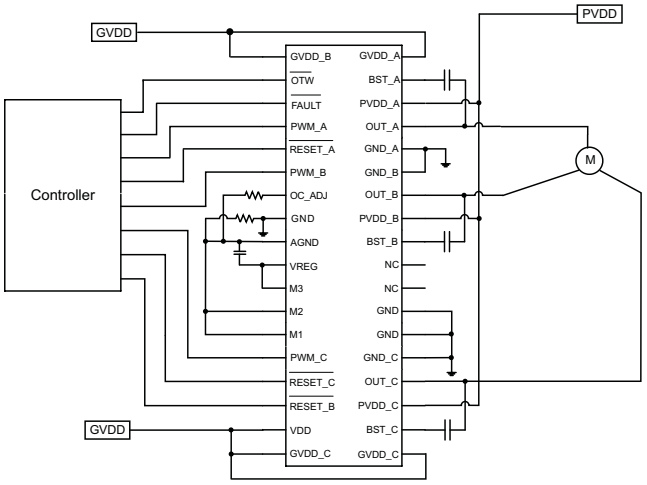
应用范围

- 无刷直流 (BLDC) 电机
- 三相永磁同步电机
- 逆变器
- 半桥驱动器
- 机器人控制系统

支持极端温度环境下的应用

- 受控基线
- 同一组装和测试场所
- 同一制造场所
- 支持极端（-55°C 至 175°C）温度范围 (1)
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性
- 德州仪器 (TI) 高温产品利用高度优化的硅（芯片）解决方案，此解决方案对设计和制造工艺进行了提升以在拓展的温度范围内大幅提高性能。 在最大额定温度下，器件可连续正常运行 1000 小时。

简化的应用示意图



(1) 可定制工作温度范围

说明

DRV8332 是一款具有先进保护系统的高性能、集成三相电机驱动器。

由于功率 MOSFET 的低 R_{DS}（导通）和智能栅极驱动器设计，这个电机驱动器的效率可高达 97%，可实现更小电源和散热片的使用，是高能效应用的理想选择。

说明（继续）

DRV8332 需要两个电源，一个为 12V，用于 GVDD 和 VDD，另外一个可高达 50V，用于 PVDD。 DRV8332 在高达500kHz PWM开关频率运行时仍可保持高精度和高效率。 它还具有一个创新保护系统，此系统可在很宽故障条件下保护器件不受损伤。 这些保护是短路保护、过流保护、欠压保护和两级过热保护。 DRV8332 有一个限流电路，此电路可在诸如电机启动等负载瞬态期间防止器件过流关断。 一个可编程过流检测器可实现可调电流限值和保护级别以满足不同的电机需要。

DRV8332 具有用于每个半桥的独特独立电源和接地引脚，这样可通过外部检测电阻来提供电流测量，并且支持具有不同电源电压需求的半桥驱动器。

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 175°C	DDV	DRV8332HDDV	DRV8332H

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted (1)

	VALUE
VDD to GND	–0.3 V to 13.2 V
GVDD_X to GND	–0.3 V to 13.2 V
PVDD_X to GND_X (2)	–0.3 V to 70 V
OUT_X to GND_X (2)	–0.3 V to 70 V
BST_X to GND_X (2)	–0.3 V to 80 V
Maximum bootstrap in rush current, IBST_In	0.4 A
Transient peak output current (per pin), pulse width limited by internal over-current protection circuit.	16 A
Transient peak output current for latch shut down (per pin)	20 A
VREG to AGND	–0.3 V to 4.2 V
GND_X to GND	–0.3 V to 0.3 V
GND to AGND	–0.3 V to 0.3 V
PWM_X, $\overline{\text{RESET\_X}}$ to GND	–0.3 V to 4.2 V
OC_ADJ, M1, M2, M3 to AGND	–0.3 V to 4.2 V
$\overline{\text{FAULT}}$, $\overline{\text{OTW}}$ to GND	–0.3 V to 7 V
Maximum continuous sink current ($\overline{\text{FAULT}}$, $\overline{\text{OTW}}$)	9 mA
Maximum operating junction temperature range, T_J	-55°C to 185°C
Storage temperature, T_{STG}	–55°C to 175°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represent the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
PVDD_X	Half bridge X (A, B, or C) DC supply voltage	0	50	52.5	V
GVDD_X	Supply for logic regulators and gate-drive circuitry	10.8	12	13.2	V
VDD	Digital regulator supply voltage	10.8	12	13.2	V
I_{O_PULSE}	Pulsed peak current per output pin (could be limited by thermal)			7	A
I_O	Continuous current per output pin (DRV8332)			5	A
F_{SW}	PWM switching frequency			380	kHz
R_{OCP_CBC}	OC programming resistor range in cycle-by-cycle current limit modes	30		200	kΩ
C_{BST}	Bootstrap capacitor range	33		220	nF
T_{ON_MIN}	Minimum PWM pulse duration, low side		50		nS
T_J	Operating junction temperature	-55		175	°C

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8332-HT DDV 44 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	42.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	0.2	
θ_{JB}	Junction-to-board thermal resistance(4)	17.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	17.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告（文献号：ZHCA543）。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的规定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然对流条件下的结至环境热阻抗。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结至电路板的热阻。
(5) 结至顶部的特征参数，(ψ_{JT})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(6) 结至电路板的特征参数，(ψ_{JB})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到了内容接近的说明。

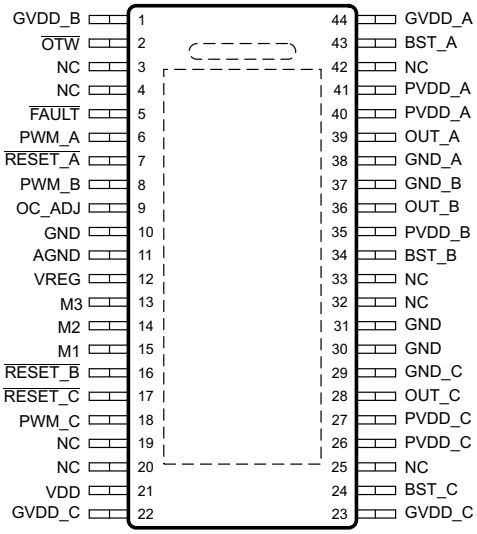
MODE SELECTION PINS

MODE PINS			OUTPUT CONFIGURATION	DESCRIPTION
M3	M2	M1		
1	0	0	1 3PH or 3 HB	Three-phase or three half bridges with cycle-by-cycle current limit
1	0	1	1 3PH or 3 HB	Three-phase or three half bridges with OC latching shutdown (no cycle-by-cycle current limit)
0	x	x	Reserved	
1	1	x	Reserved	

DEVICE INFORMATION

Pin Assignment

DDV PACKAGE
(TOP VIEW)



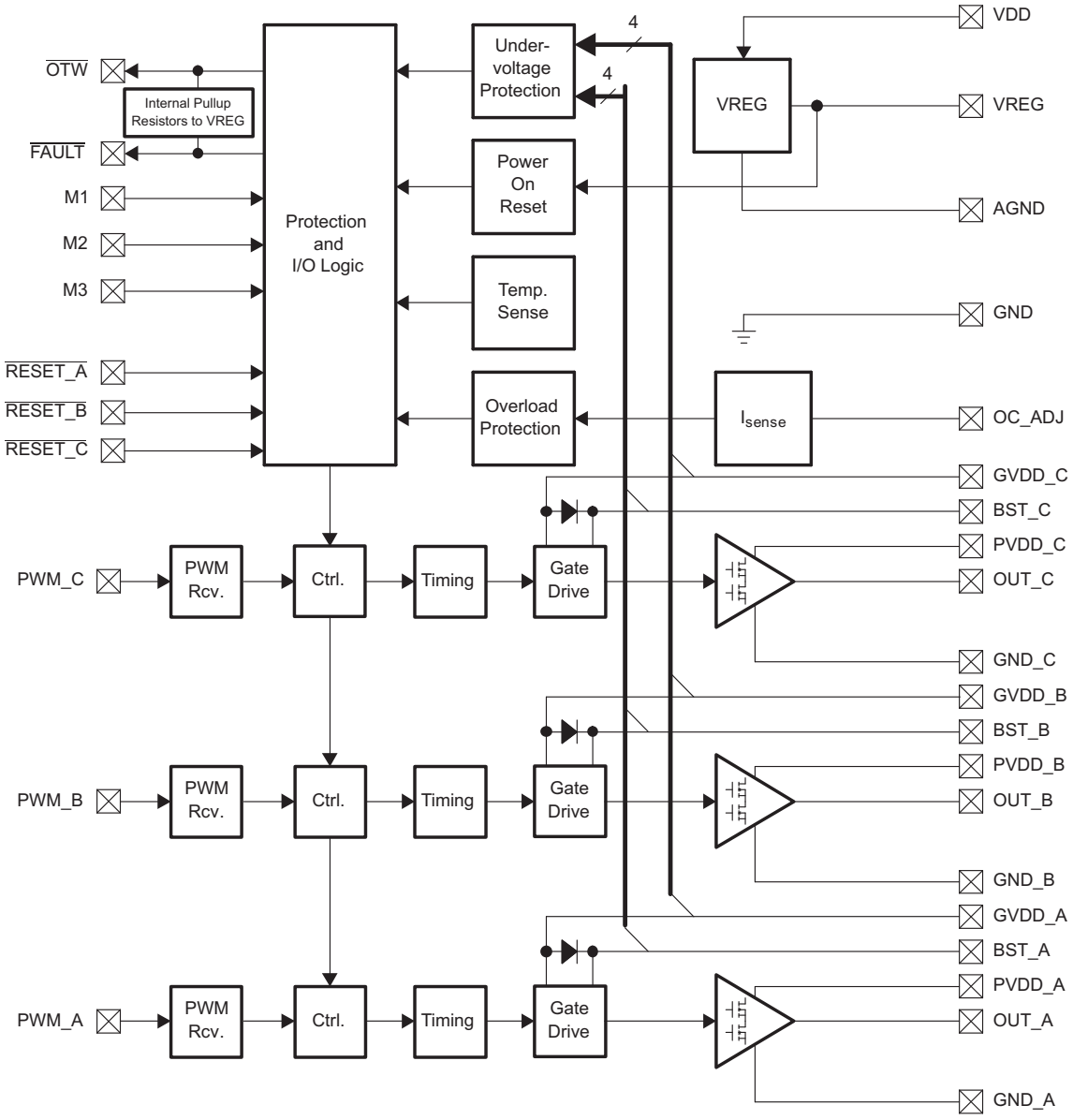
Pin Functions

NAME	PIN	FUNCTION (1)	DESCRIPTION
AGND	11	P	Analog ground
BST_A	43	P	High side bootstrap supply (BST), external capacitor to OUT_A required
BST_B	34	P	High side bootstrap supply (BST), external capacitor to OUT_B required
BST_C	24	P	High side bootstrap supply (BST), external capacitor to OUT_C required
GND	10, 30, 31	P	Ground
GND_A	38	P	Power ground for half-bridge A requires close decoupling capacitor to ground
GND_B	37	P	Power ground for half-bridge B requires close decoupling capacitor to ground
GND_C	29	P	Power ground for half-bridge C requires close decoupling capacitor to ground
GVDD_A	44	P	Gate-drive voltage supply
GVDD_B	2	P	Gate-drive voltage supply
GVDD_C	22, 23	P	Gate-drive voltage supply
M1	15	I	Mode selection pin
M2	14	I	Mode selection pin
M3	13	I	Reserved mode selection pin, AGND connection is recommended
NC	3,4,19,20,25,32, 33, 42	-	No connection pin. Ground connection is recommended
OC_ADJ	9	O	Analog overcurrent programming pin, requires resistor to AGND
$\overline{\text{OTW}}$	2	O	Overtemperature warning signal, open-drain, active-low. An internal pull-up resistor to VREG (3.3 V) is provided on output. Level compliance for 5-V logic can be obtained by adding external pull-up resistor to 5 V
OUT_A	39	O	Output, half-bridge A
OUT_B	36	O	Output, half-bridge B
OUT_C	28	O	Output, half-bridge C
PVDD_A	40, 41	P	Power supply input for half-bridge A requires close decoupling capacitor to ground.
PVDD_B	35	P	Power supply input for half-bridge B requires close decoupling capacitor to gound.
PVDD_C	26, 27	P	Power supply input for half-bridge C requires close decoupling capacitor to ground.
PWM_A	6	I	Input signal for half-bridge A

(1) I = input, O = output, P = power, T = thermal

NAME	PIN	FUNCTION (1)	DESCRIPTION
PWM_B	8	I	Input signal for half-bridge B
PWM_C	18	I	Input signal for half-bridge C
$\overline{\text{RESET\_A}}$	7	I	Reset signal for half-bridge A, active-low
$\overline{\text{RESET\_B}}$	16	I	Reset signal for half-bridge B, active-low
$\overline{\text{RESET\_C}}$	17	I	Reset signal for half-bridge C, active-low
$\overline{\text{FAULT}}$	5	O	Fault signal, open-drain, active-low. An internal pull-up resistor to VREG (3.3 V) is provided on output. Level compliance for 5-V logic can be obtained by adding external pull-up resistor to 5 V
VDD	21	P	Power supply for digital voltage regulator requires capacitor to ground for decoupling.
VREG	12	P	Digital regulator supply filter pin requires 0.1-µF capacitor to AGND.

SYSTEM BLOCK DIAGRAM

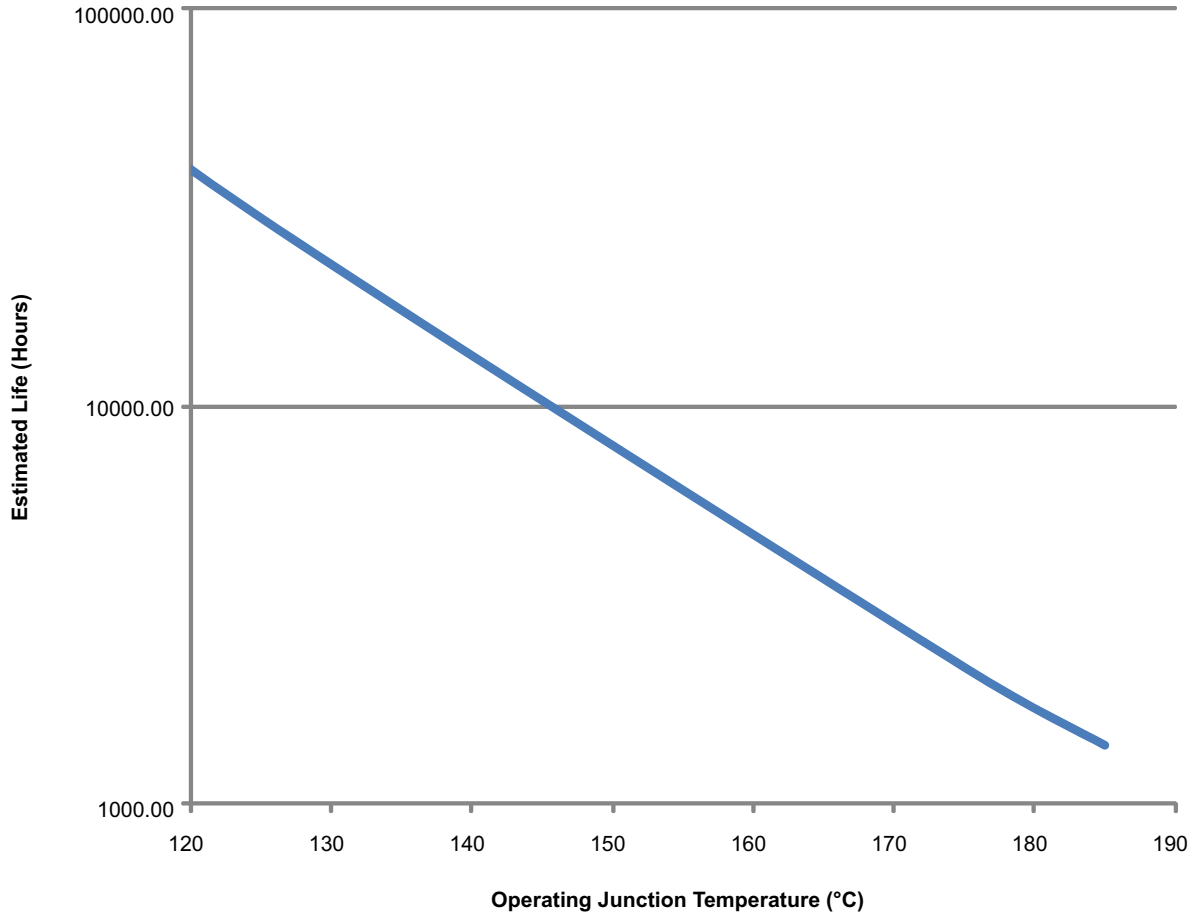


ELECTRICAL CHARACTERISTICS

T_J = -55°C to 175°C, PVDD = 50 V, GVDD = VDD = 12 V, f_{SW} = 380 kHz, unless otherwise noted. All performance is in accordance with recommended operating conditions unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal Voltage Regulator and Current Consumption						
V_{REG}	Voltage regulator, only used as a reference node	VDD = 12 V	2.85	3.3	3.75	V
I_{VDD}	VDD supply current	Idle, reset mode		9	15	mA
		Operating, 50% duty cycle		10.5		
I_{GVDD_X}	Gate supply current per half-bridge	Reset mode		1.7	2.5	mA
		Operating, 50% duty cycle		8		
I_{PVDD_X}	Half-bridge X (A, B, or C) idle current	Reset mode		0.7	1	mA
Output Stage						
$R_{DS(on)}$	MOSFET drain-to-source resistance, low side (LS)	T_J = 25°C, GVDD = 12 V		260		mΩ
	MOSFET drain-to-source resistance, high side (HS)	T_J = 25°C, GVDD = 12 V		260		mΩ
V_F	Diode forward voltage drop	T_J = 25°C - 125°C, I_O = 5 A		1		V
t_R	Output rise time	Resistive load, I_O = 5 A		14		nS
t_F	Output fall time	Resistive load, I_O = 5 A		14		nS
t_{PD_ON}	Propagation delay when FET is on	Resistive load, I_O = 5 A		38		nS
t_{PD_OFF}	Propagation delay when FET is off	Resistive load, I_O = 5 A		38		nS
t_{DT}	Dead time between HS and LS FETs	Resistive load, I_O = 5 A		5.5		nS
I/O Protection						
$V_{uvp,G}$	Gate supply voltage GVDD_X undervoltage protection threshold			8.5		V
$V_{uvp,hyst}$ (1)	Hysteresis for gate supply undervoltage event			0.3		V
I_{OC}	Overcurrent limit protection	Resistor—programmable, nominal, R_{OCP} = 36 kΩ		7.4		A
I_{OCT}	Overcurrent response time	Time from application of short condition to Hi-Z of affected FET(s)		250		ns
Static Digital Specifications						
V_{IH}	High-level input voltage	PWM_A, PWM_B, PWM_C, M1, M2, M3	2		3.6	V
V_{IH}	High-level input voltage	$\overline{\text{RESET\_A}}$, $\overline{\text{RESET\_B}}$, $\overline{\text{RESET\_C}}$	2		3.6	V
V_{IL}	Low-level input voltage	PWM_A, PWM_B, PWM_C, M1, M2, M3, $\overline{\text{RESET\_A}}$, $\overline{\text{RESET\_B}}$, $\overline{\text{RESET\_C}}$			0.8	V
I_{lkg}	Input leakage current		-100		100	µA
OTW / FAULT						
R_{INT_PU}	Internal pullup resistance, $\overline{\text{OTW}}$ to VREG, $\overline{\text{FAULT}}$ to VREG		20	26	35	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor only	1.95	3.3	3.65	V
V_{OL}	Low-level output voltage	I_O = 4 mA		0.2	0.4	V

(1) Specified by design



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 1. Electromigration Fail Mode Derating Chart

TYPICAL CHARACTERISTICS

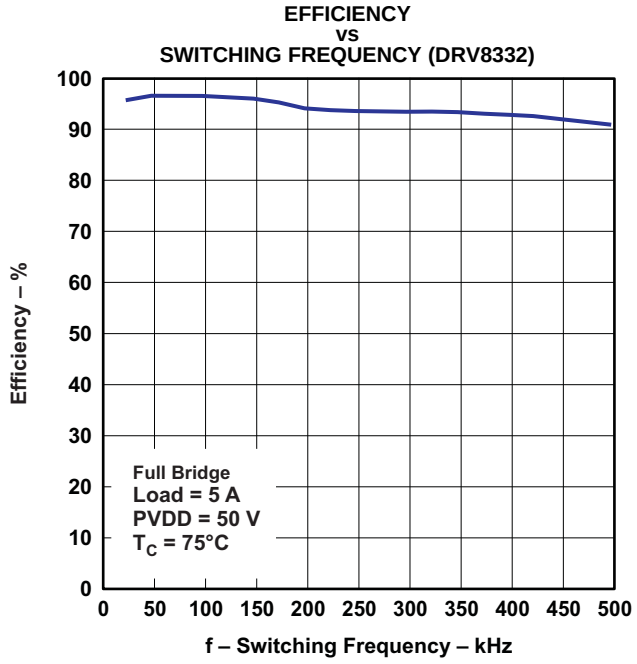


Figure 2.

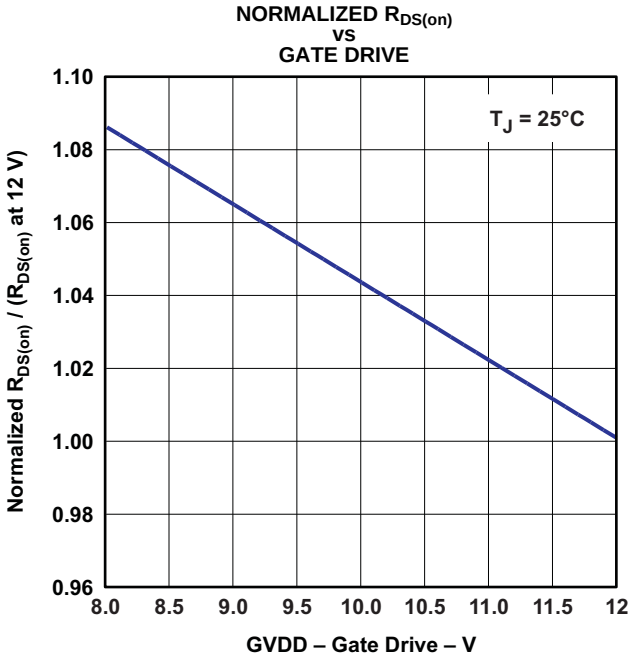


Figure 3.

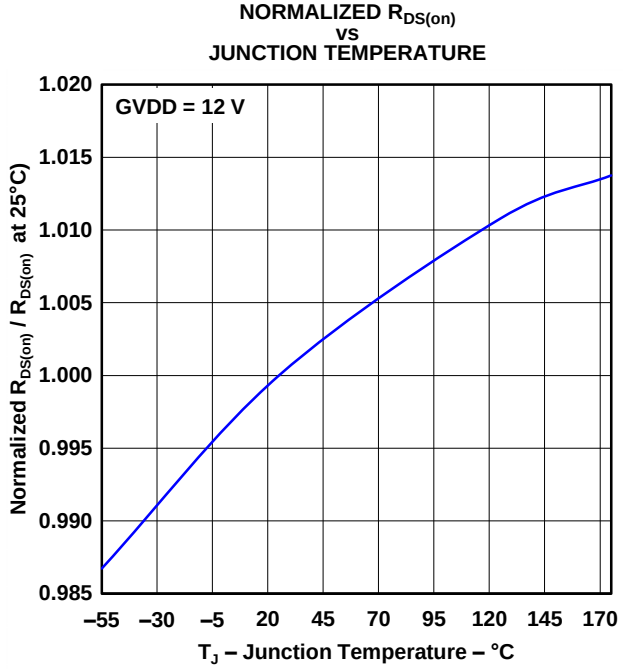


Figure 4.

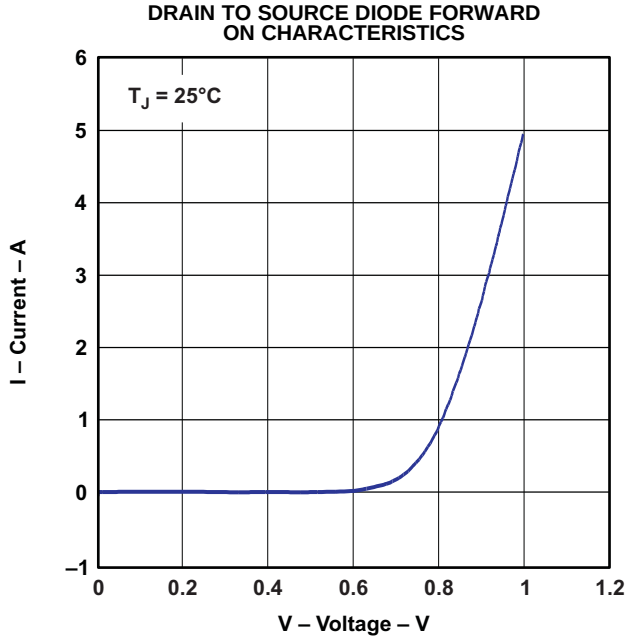


Figure 5.

TYPICAL CHARACTERISTICS (continued)

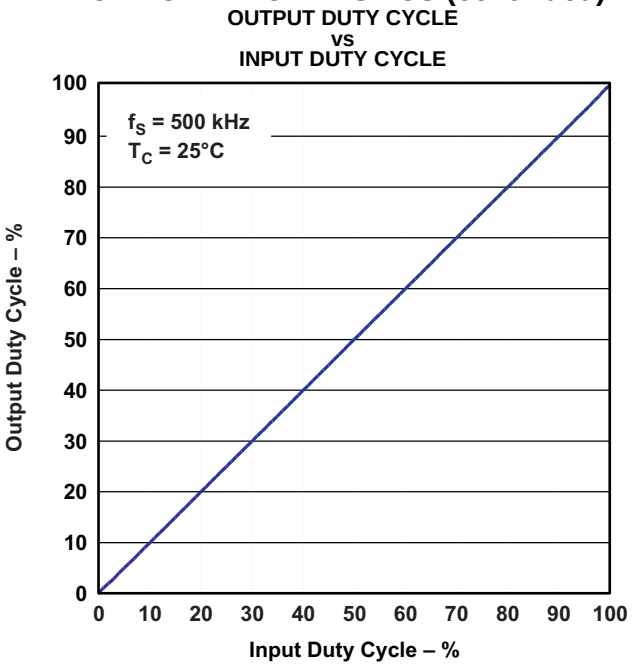


Figure 6.

THEORY OF OPERATION

POWER SUPPLIES

To facilitate system design, the DRV8332 needs only a 12-V supply in addition to H-Bridge power supply (PVDD). An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, the high-side gate drive requiring a floating voltage supply, which is accommodated by built-in bootstrap circuitry requiring external bootstrap capacitor.

To provide symmetrical electrical characteristics, the PWM signal path, including gate drive and output stage, is designed as identical, independent half-bridges. For this reason, each half-bridge has a separate gate drive supply (GVDD_X), a bootstrap pin (BST_X), and a power-stage supply pin (PVDD_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Special attention should be paid to place all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. Furthermore, decoupling capacitors need a short ground path back to the device.

For a properly functioning bootstrap circuit, a small ceramic capacitor (an X5R or better) must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 10 kHz to 500 kHz, the use of 100-nF ceramic capacitors (X5R or better), size 0603 or 0805, is recommended for the bootstrap supply. These 100-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET fully turned on during the remaining part of the PWM cycle. In an application running at a switching frequency lower than 10 kHz, the bootstrap capacitor might need to be increased in value.

Special attention should be paid to the power-stage power supply; this includes component selection, and routing. As indicated, each half-bridge has independent power-stage supply pin (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a ceramic capacitor (X5R or better) placed as close as possible to each supply pin.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 50-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the DRV8332 are fully protected against erroneous power-stage turn-on due to parasitic gate charging. Thus, voltage-supply ramp rates (dv/dt) are non-critical within the specified voltage range (see the *Recommended Operating Conditions* section of this data sheet).

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up

The DRV8332 does not require a power-up sequence. The outputs of the H-bridges remain in a high impedance state until the gate-drive supply voltage GVDD_X and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, holding RESET_A, RESET_B, and RESET_C in a low state while powering up the device is recommended. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

Powering Down

The DRV8332 does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the UVP voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is a good practice to hold RESET_A, RESET_B and RESET_C low during power down to prevent any unknown state during this transition.

ERROR REPORTING

The $\overline{\text{FAULT}}$ and $\overline{\text{OTW}}$ pins are both active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown, such as overtemperatue shut down, overcurrent shut-down, or undervoltage protection, is signaled by the $\overline{\text{FAULT}}$ pin going low. Likewise, $\overline{\text{OTW}}$ goes low when the device junction temperature exceeds 125°C (see Table 1).

Table 1. Protection Mode Signal Descriptions

$\overline{\text{FAULT}}$	$\overline{\text{OTW}}$	DESCRIPTION
0	0	Overtemperature warning and (overtemperature shut down or overcurrent shut down or undervoltage protection) occurred
0	1	Overcurrent shut-down or GVDD undervoltage protection occurred
1	0	Overtemperature warning
1	1	Device under normal operation

TI recommends monitoring the $\overline{\text{OTW}}$ signal using the system microcontroller and responding to an $\overline{\text{OTW}}$ signal by reducing the load current to prevent further heating of the device resulting in device overtemperature shutdown (OTSD).

To reduce external component count, an internal pullup resistor to internal VREG (3.3 V) is provided on both $\overline{\text{FAULT}}$ and $\overline{\text{OTW}}$ outputs. Level compliance for 5-V logic can be obtained by adding external pull-up resistors to 5 V (see the *Electrical Characteristics* section of this data sheet for further specifications).

DEVICE PROTECTION SYSTEM

The DRV8332 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overcurrent, overtemperature, and undervoltage. The DRV8332 responds to a fault by immediately setting the half bridge outputs in a high-impedance (Hi-Z) state and asserting the $\overline{\text{FAULT}}$ pin low. In situations other than overcurrent or overtemperature, the device automatically recovers when the fault condition has been removed or the gate supply voltage has increased. For highest possible reliability, reset the device externally no sooner than 1 second after the shutdown when recovering from an overcurrent shut down (OCSD) or OTSD fault.

Bootstrap Capacitor Under Voltage Protection

When the device runs at a low switching frequency (e.g. less than 10 kHz with a 100-nF bootstrap capacitor), the bootstrap capacitor voltage might not be able to maintain a proper voltage level for the high-side gate driver. A bootstrap capacitor undervoltage protection circuit (BST_UVP) will prevent potential failure of the high-side MOSFET. When the voltage on the bootstrap capacitors is less than the required value for safe operation, the DRV8332 will initiate bootstrap capacitor recharge sequences (turn off high side FET for a short period) until the bootstrap capacitors are properly charged for safe operation. This function may also be activated when PWM duty cycle is too high (e.g. less than 20 ns off time at 10 kHz). Note that bootstrap capacitor might not be able to be charged if no load or extremely light load is presented at output during BST_UVP operation, so it is recommended to turn on the low side FET for at least 50 ns for each PWM cycle to avoid BST_UVP operation if possible.

For all applications, it is recommended to add 26-Ω resistor between the GVDD power supply and GVDD_X pins to limit the inrush current on the internal bootstrap diodes.

Overcurrent (OC) Protection

The DRV8332 has independent, fast-reacting current detectors with programmable trip threshold (OC threshold) on all high-side and low-side power-stage FETs. There are two settings for OC protection through mode selection pins: cycle-by-cycle (CBC) current limiting mode and OC latching (OCL) shut down mode.

In CBC current limiting mode, the detector outputs are monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current from further increasing, i.e., it performs a CBC current-limiting function rather than prematurely shutting down the device. This feature could effectively limit the inrush current during motor start-up or transient without damaging the device. During short to power and short to ground conditions, the current limit circuitry might not be able to control the current to a proper level, a second protection system triggers a latching shutdown, resulting in the related half bridge being set in the high-impedance (Hi-Z) state. Current limiting and overcurrent protection are independent for half-bridges A, B, and C, respectively.

Figure 7 illustrates cycle-by-cycle operation with high side OC event and Figure 8 shows cycle-by-cycle operation with low side OC. Dashed lines are the operation waveforms when no CBC event is triggered and solide lines show the waveforms when CBC event is triggered. In CBC current limiting mode, when low side FET OC is detected, devcie will turn off the affected low side FET and keep the high side FET at the same half brdige off until next PWM cycle; when high side FET OC is detected, devcie will turn off the affected high side FET and turn on the low side FET at the half brdige until next PWM cycle.

In OC latching shut down mode, the CBC current limit and error recovery circuitries are disabled and an overcurrent condition will cause the device to shutdown immediately. After shutdown, RESET_A, RESET_B, and / or RESET_C must be asserted to restore normal operation after the overcurrent condition is removed.

For added flexibility, the OC threshold is programmable using a single external resistor connected between the OC_ADJ pin and AGND pin. See Table 2 for information on the correlation between programming-resistor value and the OC threshold.

Table 2. Programming-Resistor Values and OC Threshold

OC-ADJUST RESISTOR VALUES (kΩ)	MAXIMUM CURRENT BEFORE OC OCCURS (A)
30	8.8
36	7.4
39	6.9
43	6.3
47	5.8
56	4.9
68	4.1
82	3.4
100	2.8
120	2.4
150	1.9
200	1.4

It should be noted that a properly functioning overcurrent detector assumes the presence of a proper inductor or power ferrite bead at the power-stage output. Short-circuit protection is not guaranteed with direct short at the output pins of the power stage.

Overtemperature Protection

The DRV8332 has a two-level temperature-protection system that asserts an active-low warning signal (OTW) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and FAULT being asserted low. OTSD is latched in this case and RESET_A, RESET_B, and RESET_C must be asserted low to clear the latch.

Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the DRV8332 fully protect the device in any power-up / down and brownout situation. While powering up, the POR circuit resets the overcurrent circuit and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach 9.8 V (typical). Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and FAULT being asserted low. The device automatically resumes operation when all supply voltage on the bootstrap capacitors have increased above the UVP threshold.

DEVICE RESET

Three reset pins are provided for independent control of half-bridges A, B, and C. When RESET_X is asserted low, two power-stage FETs in half-bridges X are forced into a high-impedance (Hi-Z) state.

A rising-edge transition on reset input allows the device to resume operation after a shut-down fault. E.g., when half-bridge X has OC shutdown, a low to high transition of RESET_X pin will clear the fault and FAULT pin. When an OTSD occurs, all three RESET_A, RESET_B, and RESET_C need to have a low to high transition to clear the fault and reset FAULT signal.

DIFFERENT OPERATIONAL MODES

The DRV8332 supports two different modes of operation:

1. Three-phase (3PH) or three half bridges (HB) with CBC current limit
2. Three-phase or three half bridges with OC latching shutdown (no CBC current limit)

Because each half bridge has independent supply and ground pins, a shunt sensing resistor can be inserted between PVDD to PVDD_X or GND_X to GND (ground plane). A high side shunt resistor between PVDD and PVDD_X is recommended for differential current sensing because a high bias voltage on the low side sensing could affect device operation. If low side sensing has to be used, a shunt resistor value of 10 mΩ or less or sense voltage 100 mV or less is recommended.

and Figure 9 show the three-phase application examples, and Figure 10 shows how to connect to DRV8332 with some simple logic to accommodate conventional 6 PWM inputs control.

We recommend using complementary control scheme for switching phases to prevent circulated energy flowing inside the phases and to make current limiting feature active all the time. Complementary control scheme also forces the current flowing through sense resistors all the time to have a better current sensing and control of the system.

Figure 11 shows six steps trapezoidal scheme with hall sensor control and Figure 12 shows six steps trapezoidal scheme with sensorless control. The hall sensor sequence in real application might be different than the one we showed in Figure 11 depending on the motor used. Please check motor manufacture datasheet for the right sequence in applications. In six step trapezoidal complementary control scheme, a half bridge with larger than 50% duty cycle will have a positive current and a half bridge with less than 50% duty cycle will have a negative current. For normal operation, changing PWM duty cycle from 50% to 100% will adjust the current from 0 to maximum value with six steps control. It is recommanded to apply a minimum 50ns to 100 nS PWM pulse at each switching cycle at lower side to properly charge the bootstrap cap. The impact of minimum pulse at low side FET is pretty small, e.g., the maximum duty cycle is 99.9% with 100ns minimum pulse on low side. RESET_Xpin can be used to get channel X into high impedance mode. If you prefer PWM switching one channel but hold low side FET of the other channel on (and third channel in Hi-Z) for 2-quadrant mode, OT latching shutdown mode is recommended to prevent the channel with low side FET on stuck in Hi-Z during OC event in CBC mode.

The DRV8332 can also be used for sinusoidal waveform control and field oriented control. Please check TI website MCU motor control library for control algorithms.

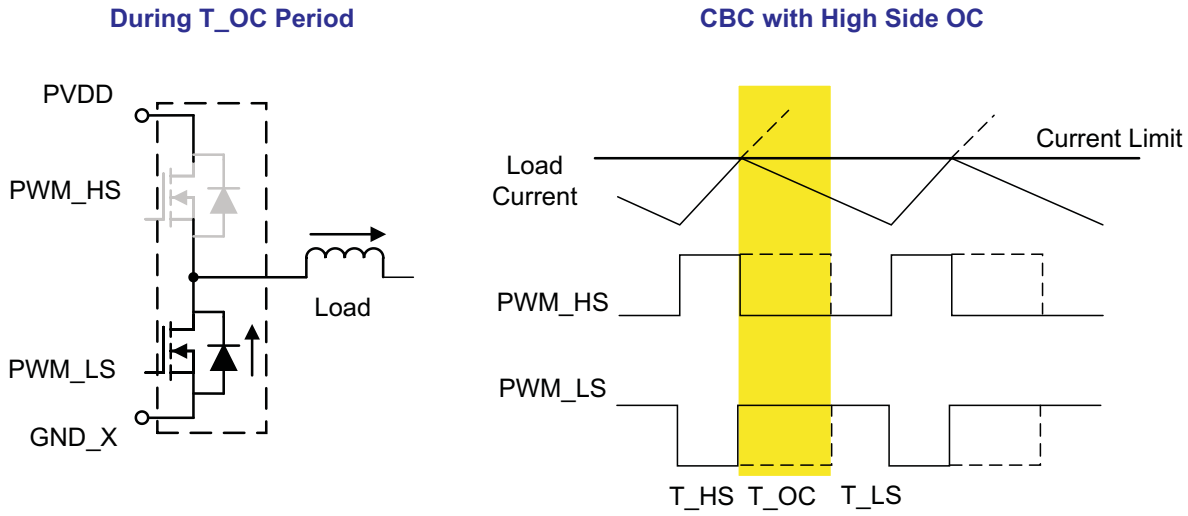


Figure 7. Cycle-by-Cycle Operation with High Side OC (dashed line: normal operation; solid line: CBC event)

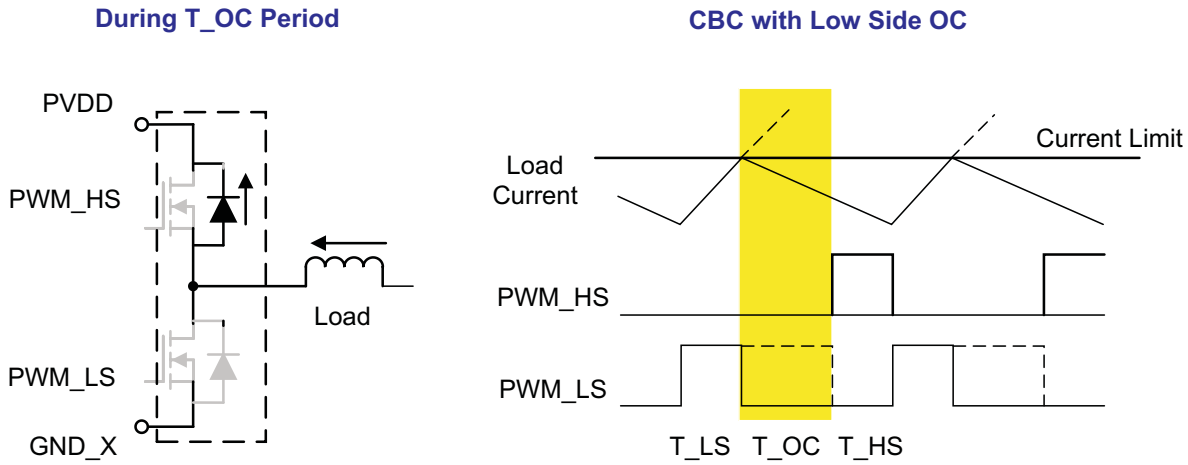


Figure 8. Cycle-by-Cycle Operation with Low Side OC (dashed line: normal operation; solid line: CBC event)

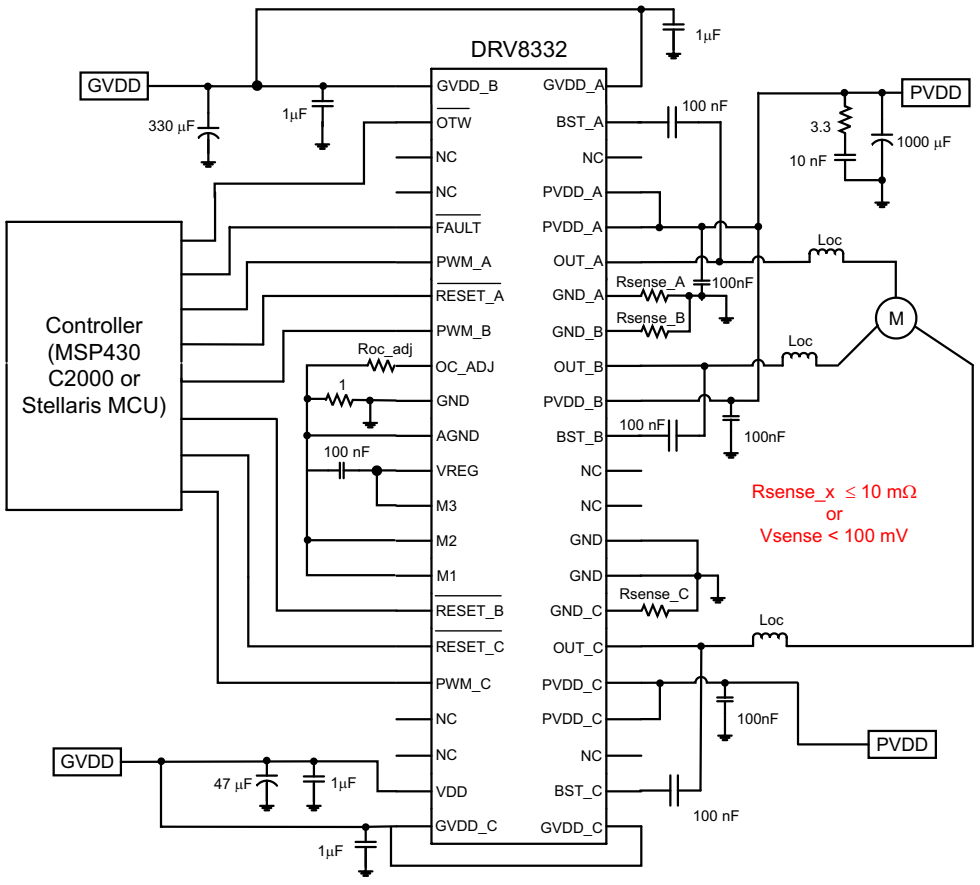


Figure 9. DRV8332 Application Diagram for Three-Phase Operation

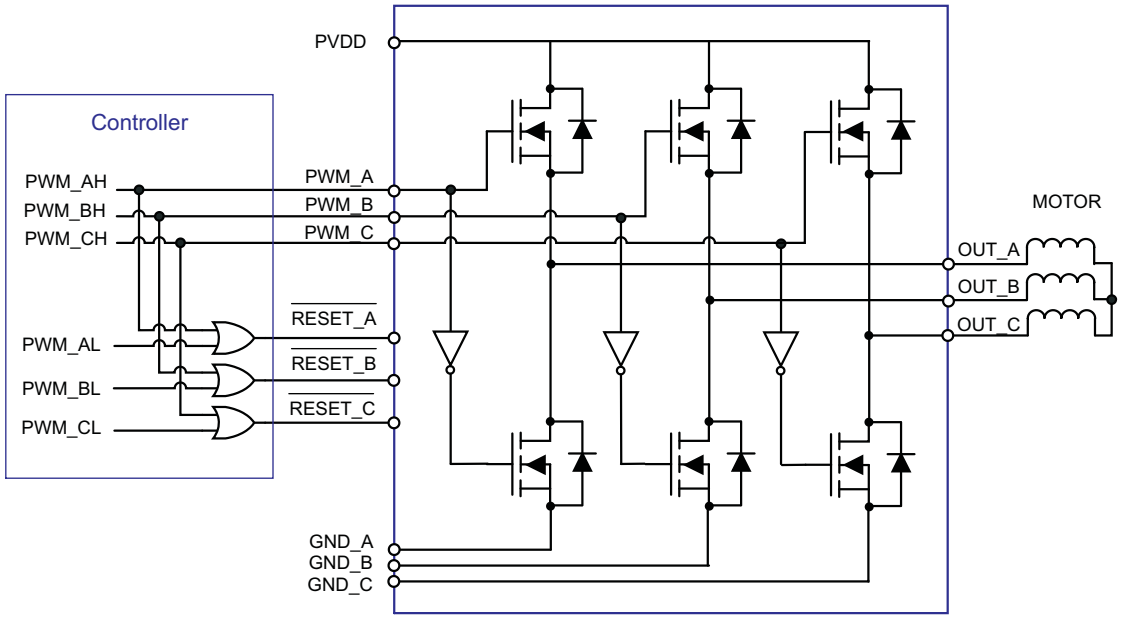


Figure 10. Control Signal Logic with Conventional 6 PWM Input Scheme

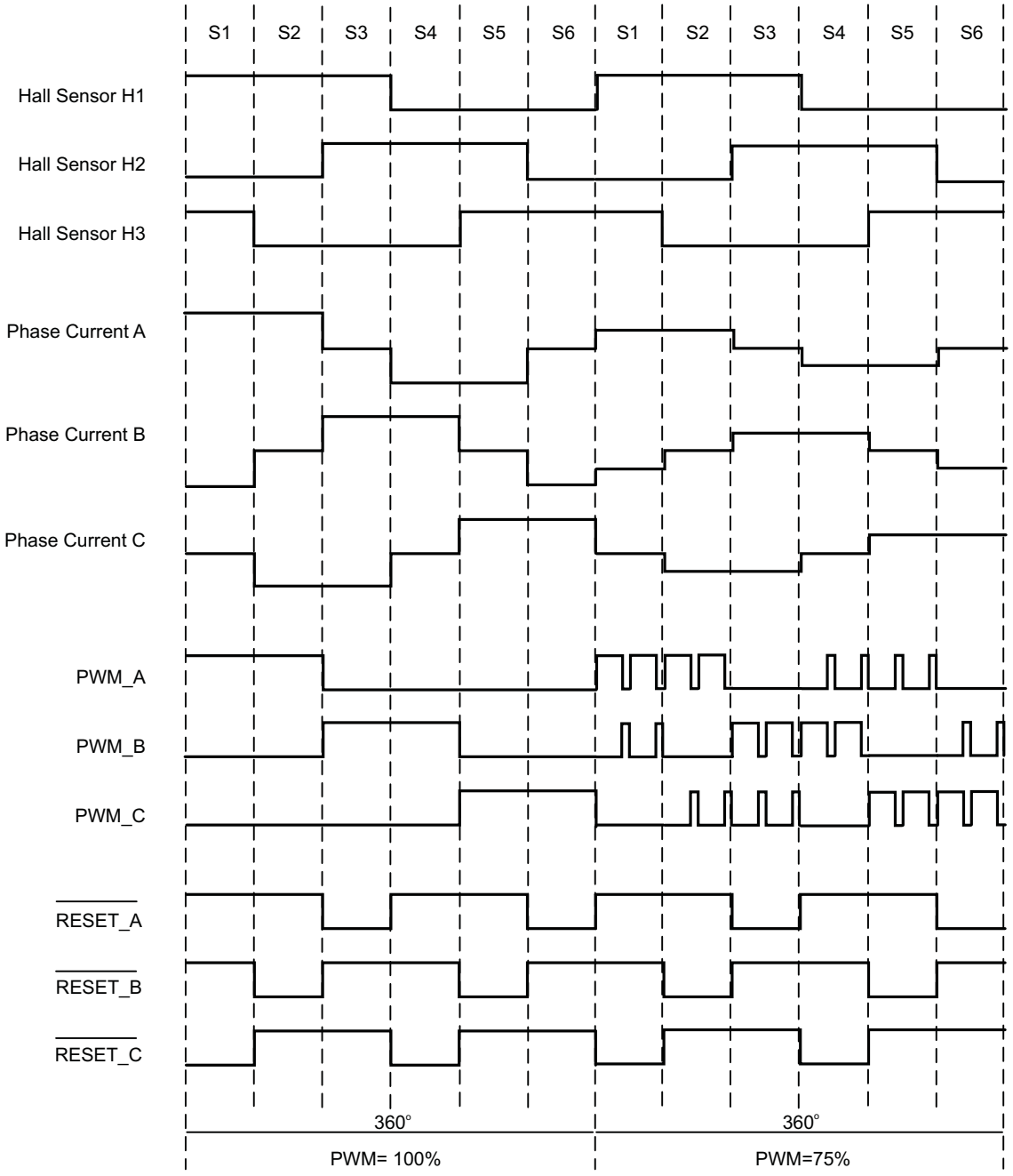


Figure 11. Hall Sensor Control with 6 Steps Trapezoidal Scheme

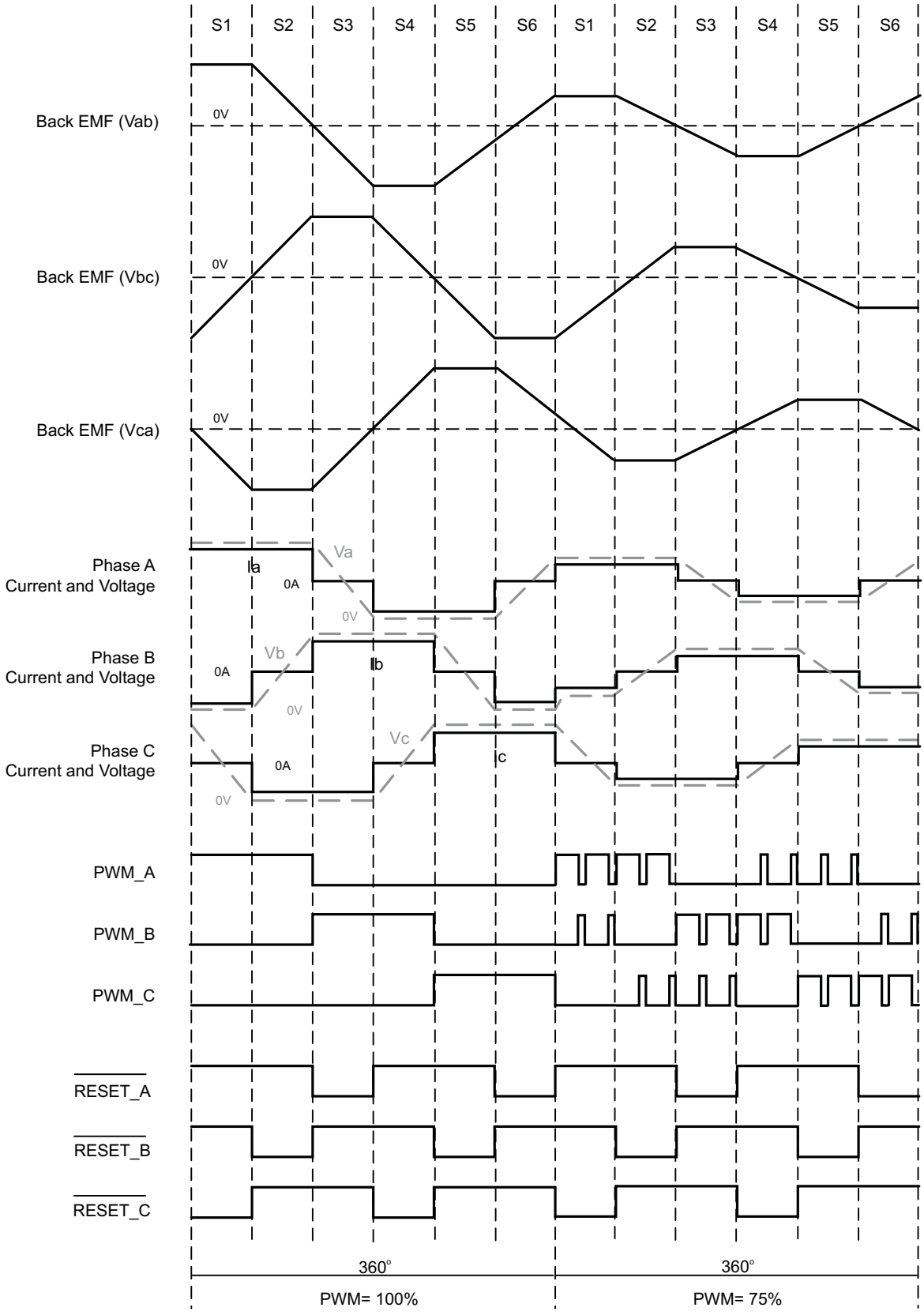


Figure 12. Sensorless Control with 6 Steps Trapezoidal Scheme

APPLICATION INFORMATION

SYSTEM DESIGN RECOMMENDATIONS

Voltage of Decoupling Capacitor

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. The high frequency decoupling capacitor should use ceramic capacitor with X5R or better rating. For a 50-V application, a minimum voltage rating of 63 V is recommended.

Current Requirement of 12V Power Supply

The DRV8332 requires a 12V power supply for GVDD and VDD pins. The total supply current is pretty low at room temp (less than 50mA), but the current could increase significantly when the device temperature goes too high (e.g. above 125°C), especially at heave load conditions due to substrate current collection by 12V guard rings. So it is recommended to design the 12V power supply with current capability at least 5-10% of your load current and no less than 100mA to assure the device performance across all temperature range.

VREG Pin

The VREG pin is used for internal logic and should not be used as a voltage source for external circuitries. The capacitor on VREG pin should be connected to AGND.

VDD Pin

The transient current in VDD pin could be significantly higher than average current through VDD pin. A low resistive path to GVDD should be used. A 22-µF to 47-µF capacitor should be placed on VDD pin beside the 100-nF to 1-µF decoupling capacitor to provide a constant voltage during transient.

OTW Pin

$\overline{\text{OTW}}$ reporting indicates the device approaching high junction temperature. This signal can be used with MCU to decrease system power when $\overline{\text{OTW}}$ is low in order to prevent OT shut down at a higher temperature.

No external pull up resistor or 3.3V power supply is needed for 3.3V logic. The $\overline{\text{OTW}}$ pin has an internal pullup resistor connecting to an internal 3.3V to reduce external component count. For 5V logic, an external pull up resistor to 5V is needed.

FAULT Pin

The $\overline{\text{FAULT}}$ pin reports any fault condition resulting in device shut down. No external pull up resistor or 3.3V power supply is needed for 3.3V logic. The $\overline{\text{FAULT}}$ pin has an internal pullup resistor connecting to an internal 3.3V to reduce external component count. For 5V logic, an external pull upresistor to 5V is needed.

OC_ADJ Pin

For accurate control of the oevercurrent protection, the OC_ADJ pin has to be connected to AGND through an OC adjust resistor.

PWM_X and RESET_X Pins

It is recommanded to connect these pins to either AGND or GND when they are not used, and these pins only support 3.3V logic.

Mode Select Pins

Mode select pins (M1, M2, and M3) should be connected to either VREG (for logic high) or AGND for logic low. It is not recommended to connect mode pins to board ground if 1-Ω resistor is used between AGND and GND.

Output Inductor Selection

For normal operation, inductance in motor (assume larger than 10 µH) is sufficient to provide low di/dt output (e.g. for EMI) and proper protection during overload condition (CBC current limiting feature). So no additional output inductors are needed during normal operation.

However during a short condition, the motor (or other load) could be shorted, so the load inductance might not present in the system anymore; the current in short condition can reach such a high level that may exceed the abs max current rating due to extremely low impendence in the short circuit path and high di/dt before oc detection circuit kicks in. So a ferrite bead or inductor is recommended to utilize the short circuit protection feature in DRV8332. With an external inductor or ferrite bead, the current will rise at a much slower rate and reach a lower current level before oc protection starts. The device will then either operate CBC current limit or OC shut down automatically (when current is well above the current limit threshold) to protect the system.

For a system that has limited space, a power ferrite bead can be used instead of an inductor. The current rating of ferrite bead has to be higher than the RMS current of the system at normal operation. A ferrite bead designed for very high frequency is NOT recommended. A minimum impedance of 10 Ω or higher is recommended at 10 MHz or lower frequency to effectively limit the current rising rate during short circuit condition.

The TDK MPZ2012S300A and MPZ2012S101A (with size of 0805 inch type) have been tested in our system to meet short circuit conditions in the DRV8332. But other ferrite beads that have similar frequency characteristics can be used as well.

For higher power applications, such as in the DRV8332, there might be limited options to select suitable ferrite bead with high current rating. If an adequate ferrite bead cannot be found, an inductor can be used.

The inductance can be calculated as:

$$Loc\_\min = \frac{PVDD \cdot Toc\_delay}{Ipeak - Iave} \quad (1)$$

Where Toc_delay = 250 nS, Ipeak = 15 A (below abs max rating).

Because an inductor usually saturates pretty quickly after reaching its current rating, it is recommended to use an inductor with a doubled value or an inductor with a current rating well above the operating condition.

THERMAL INFORMATION

The thermally enhanced package provided with the DRV8332 is designed to interface directly to heat sink using a thermal interface compound in between, (e.g., Ceramique from Arctic Silver, TIMTronics 413, etc.). The heat sink then absorbs heat from the ICs and couples it to the local air.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this example the power pad or heat slug)
- Thermal grease thermal resistance
- Heat sink thermal resistance

The thermal grease thermal resistance can be calculated from the exposed power pad or heat slug area and the thermal grease manufacturer's area thermal resistance (expressed in °C-in ^{2}/W or °C-mm^2/W). The approximate exposed heat slug size is as follows:

- DRV8332, 44-pin DDV …… 0.055 in^2 (35.6 mm ^{2})

The thermal resistance of a thermal pad is considered higher than a thin thermal grease layer and is not recommended. Thermal tape has an even higher thermal resistance and should not be used at all. Heat sink thermal resistance is predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured.

Thus the system $R_{\theta JA}$ = $R_{\theta JC}$ + thermal grease resistance + heat sink resistance.

See the TI application report, *IC Package Thermal Metrics* (SPRA953A), for more thermal information.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8332HDDV	ACTIVE	HTSSOP	DDV	44	35	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 175	DRV8332H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

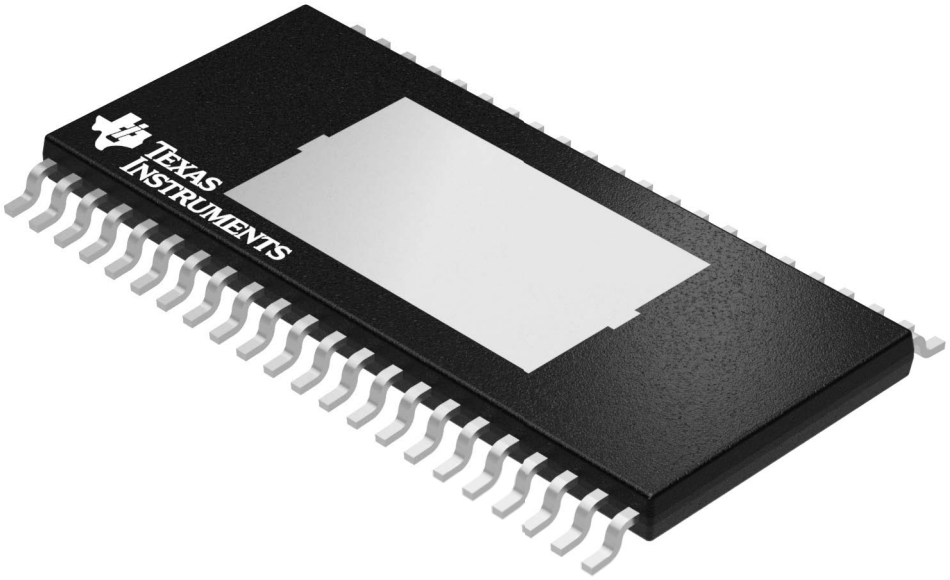
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

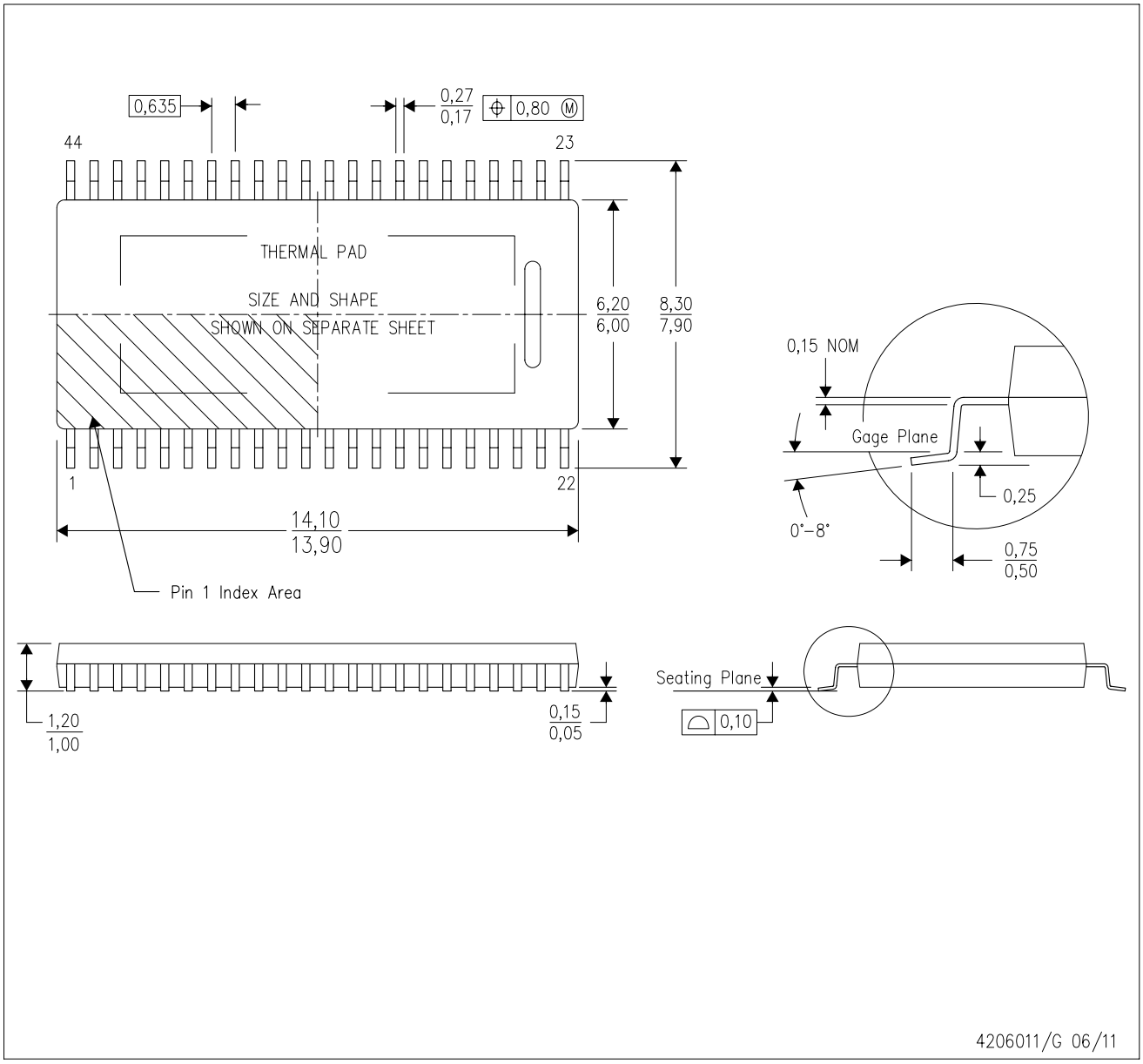
DDV 44 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDV (R–PDSO–G44) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.

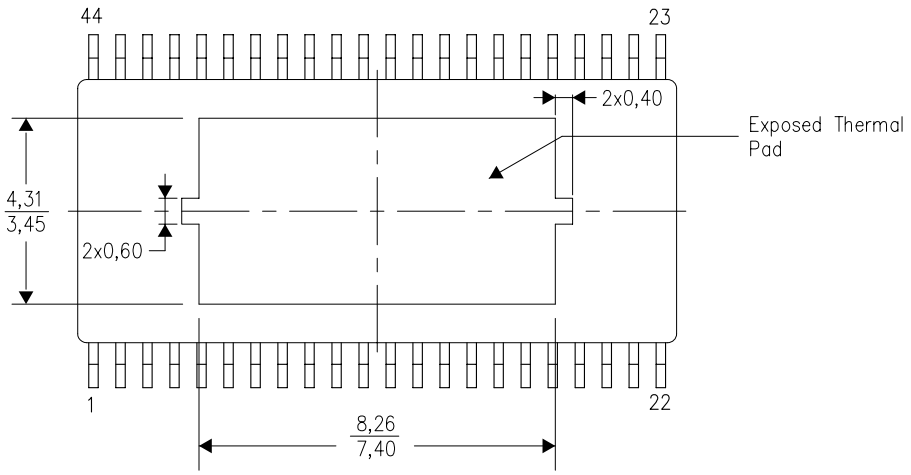
DDV (R–PDSO–G44) PowerPAD ™SMALL OUTLINE PACKAGE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206975–4/D 07/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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