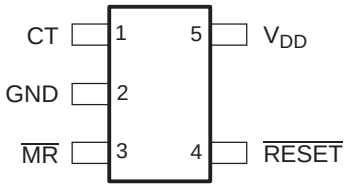
NANOPOWER SUPERVISORY CIRCUITS

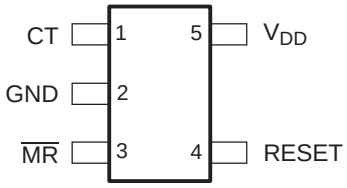
FEATURES

- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Supply Current of 220 nA (Typ)**
- **Precision Supply Voltage Supervision Range: 1.8 V, 2.5 V, 3 V, 3.3 V**
- **Power-On Reset Generator With Selectable Delay Time of 10 ms or 200 ms**
- **Push/Pull $\overline{\text{RESET}}$ Output (TPS3836), RESET Output (TPS3837), or Open-Drain RESET Output (TPS3838)**
- **Manual Reset**
- **5-Pin SOT-23 Package**

TPS3836, TPS3838
DBV PACKAGE
(TOP VIEW)



TPS3837
DBV PACKAGE
(TOP VIEW)



SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

APPLICATIONS

- **Applications Using Automotive Low-Power DSPs, Microcontrollers, or Microprocessors**
- **Battery-Powered Equipment**
- **Intelligent Instruments**
- **Wireless Communication Systems**
- **Automotive Systems**

(1) Custom temperature ranges available

DESCRIPTION

The TPS3836, TPS3837, TPS3838 families of supervisory circuits provide circuit initialization and timing supervision, primarily for digital signal processing (DSP) and processor-based systems.

During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{DD} has risen above V_{IT}.

When CT is connected to GND, a fixed delay time of typical 10 ms is asserted. When connected to V_{DD}, the delay time is typically 200 ms.

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When the supply voltage drops below V_{IT}, the output becomes active (low) again.

All the devices of this family have a fixed-sense V_{IT} set by an internal voltage divider.

The TPS3836 has an active-low push-pull $\overline{\text{RESET}}$ output. The TPS3837 has active-high push-pull RESET, and the TPS3838 integrates an active-low open-drain $\overline{\text{RESET}}$ output.

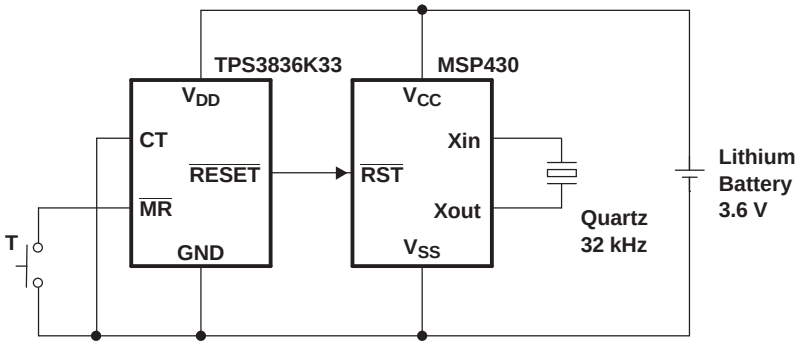

Figure 1. Typical Operating Circuit

The product spectrum is designed for supply voltages of 1.8 V, 2.5 V, 3 V, and 3.3 V. The circuits are available in a 5-pin SOT-23 package. The TPS3836, TPS3837, and TPS3838 families are characterized for operation over a temperature range of –55°C to 125°C.

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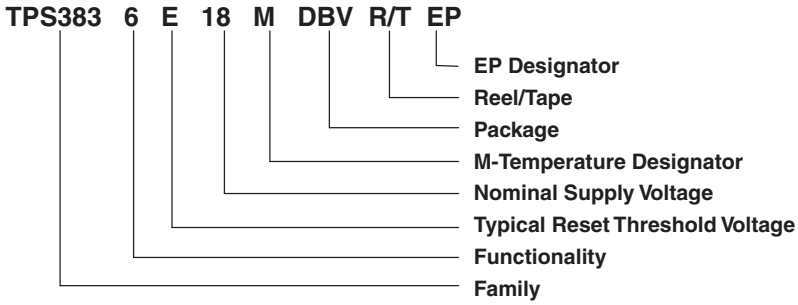
ORDERING INFORMATION

T_A	ORDERABLE PART NUMBER(1)	THRESHOLD VOLTAGE	SYMBOL
–55°C to 125°C	TPS3836J25MDBVTEP	2.25 V	PKRM
	TPS3836L30MDBVREP	2.64 V	BTX
	TPS3837K33MDBVREP	2.93 V	PKZM

(1) DBVR indicates reel of 3000 parts, DBVT indicates tape of 250 parts.

ORDERING INFORMATION



FUNCTION TABLE

$\overline{MR}$	$V_{DD} > V_{IT}$	$\overline{RESET}$ (1)	RESET(2)
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

(1) TPS3836 and TPS3838
(2) TPS3837

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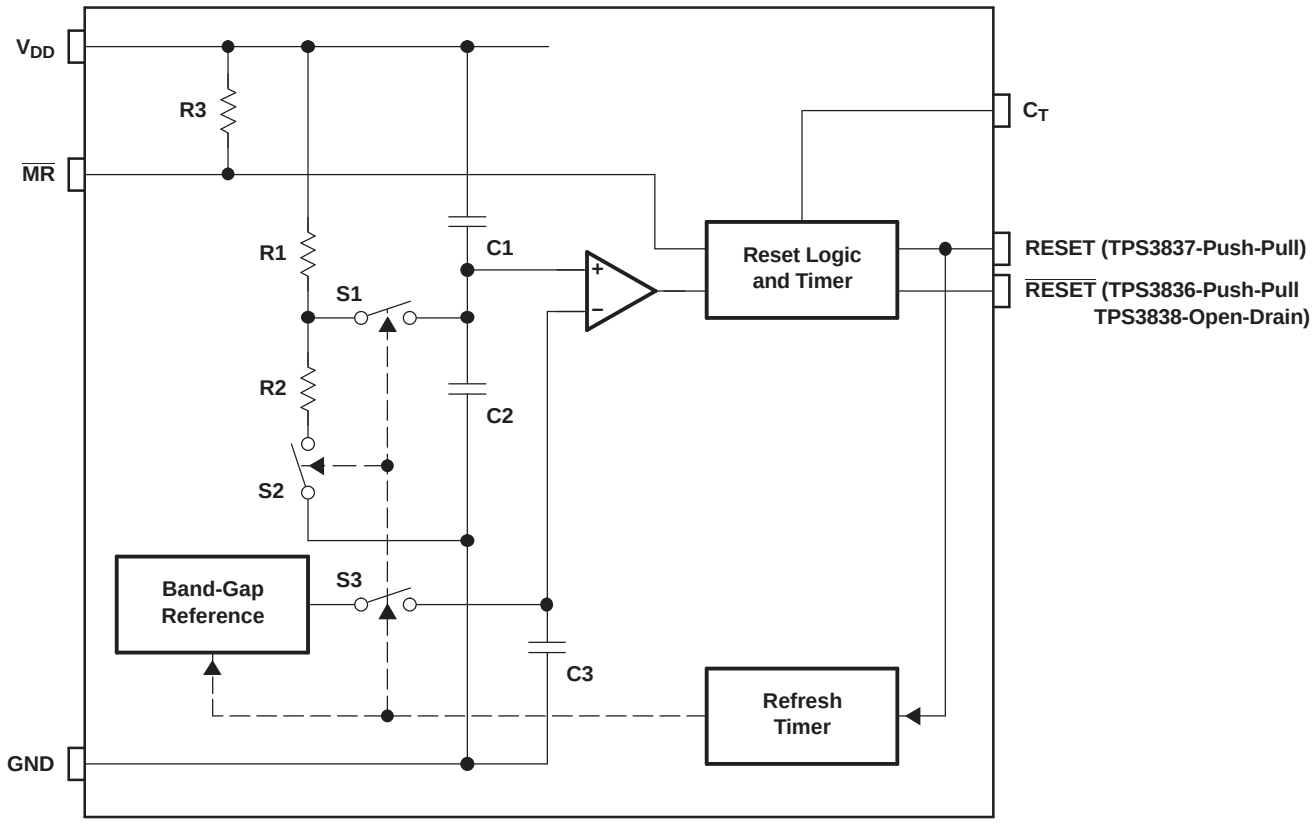
FUNCTIONAL BLOCK DIAGRAM



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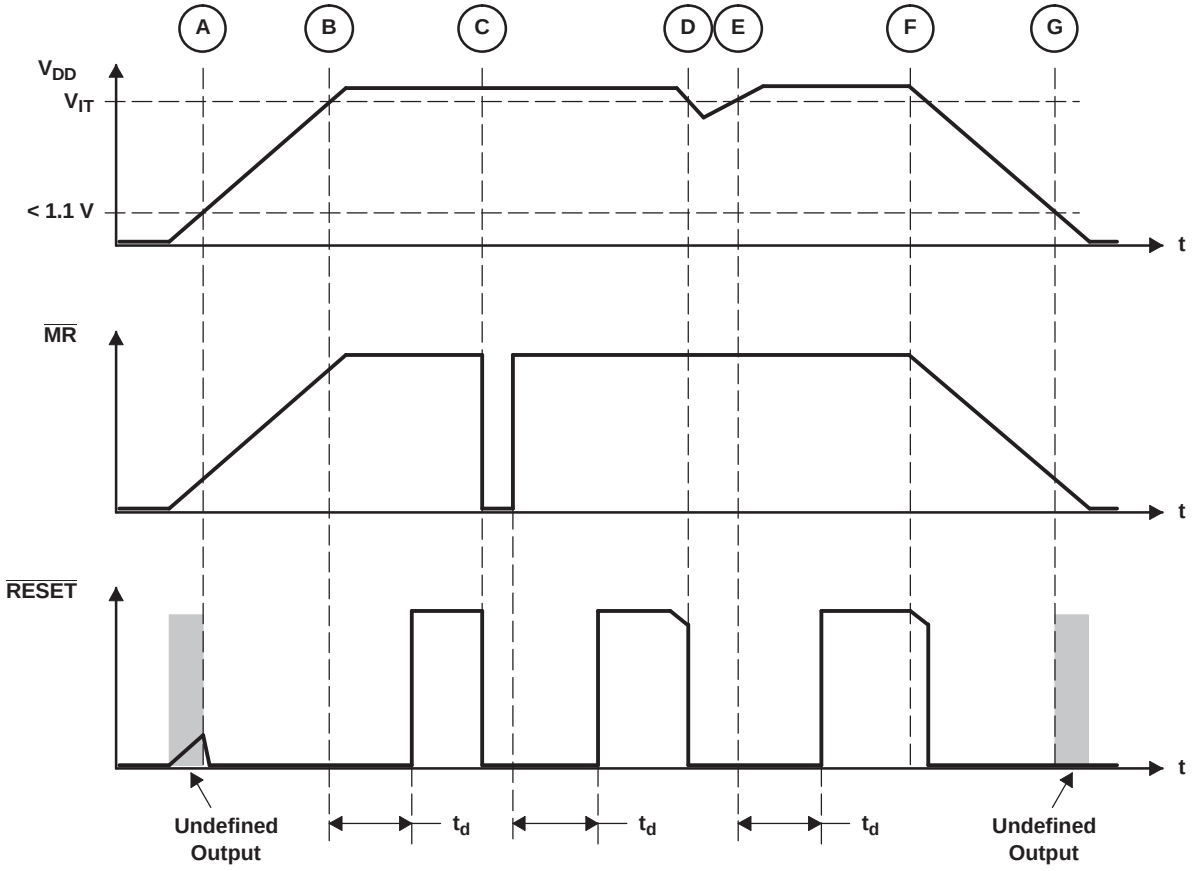
TIMING DIAGRAM



Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

V_{DD}	Supply voltage(2)	7 V
	All other pins(2)	–0.3 V to 7 V
I_{OL}	Maximum low output current	5 mA
I_{OH}	Maximum high output current	–5 mA
I_{IK}	Input clamp current ($V_I < 0$ or $V_I > V_{DD}$)	±10 mA
I_{OK}	Output clamp current ($V_O < 0$ or $V_O > V_{DD}$)	±10 mA
T_A	Operating free-air temperature range	–55°C to 125°C
T_{stg}	Storage temperature range	–65°C to 150°C
T_J	Maximum junction temperature	150°C
	Soldering temperature	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, the device must not be continuously operated at 7 V for more than t = 1000 h.

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Thermal Resistance Table

RESISTANCE	HIGH	LOW
θ_{JC} (°C/W)	130.9	148.1
θ_{JA} (°C/W)	205.6	347

Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	1.6	6	V
V_I	Input voltage	0	V_{DD} + 0.3	V
V_{IH}	High-level input voltage	0.7 × V_{DD}		V
V_{IL}	Low-level input voltage		0.3 × V_{DD}	V
$\Delta t/\Delta v$	Input transition rise and fall rate at $\overline{MR}$		100	ns/V
T_A	Operating free-air temperature	–55	125	°C

Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RESET}$ (TPS3836)	V_{DD} = 3.3 V, I_{OH} = –2 mA		0.8 × V_{DD}			V
			V_{DD} = 6 V, I_{OH} = –3 mA					
		RESET (TPS3837)	V_{DD} = 2 V, I_{OH} = –1 mA					
			V_{DD} = 3.3 V, I_{OH} = –2 mA					
V_{OL}	Low-level output voltage	$\overline{RESET}$ (TPS3836/8)	V_{DD} = 2 V, I_{OL} = 1 mA				0.4	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA					
		RESET (TPS3837)	V_{DD} = 3.3 V, I_{OL} = 2 mA					
			V_{DD} = 6 V, I_{OL} = 3 mA					
	Power-up reset voltage(1)	TPS3836/8	V_{DD} ≥ 1.1 V, I_{OL} = 50 µA				0.2	V
		TPS3837	V_{DD} ≥ 1.1 V, I_{OH} = –50 µA	T_A = 25°C	0.8 × V_{DD}			
				T_A = Full range	0.6 × V_{DD}			
V_{IT}	Negative-going input threshold voltage(2)	TPS383xE18			1.64	1.71	1.73	V
		TPS383xJ25			2.16	2.25	2.31	
		TPS383xH30			2.7	2.79	2.85	
		TPS383xL30			2.54	2.64	2.71	
		TPS383xK33	T_A = 25°C		2.82	2.93	3.1	
			T_A = Full range		2.72	2.93	3.2	
V_{hys}	Hysteresis at V_{DD} input		1.7 V < V_{IT} < 2.5 V			30		mV
			2.5 V < V_{IT} < 3.5 V			40		
			3.5 V < V_{IT} < 5 V			50		
I_{IH}	High-level input current	$\overline{MR}$ (3)	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6 V	T_A = 25°C	–30	–60	–90	µA
				T_A = Full range	–20	–60	–120	
		CT	CT = V_{DD} = 6 V		–25		25	nA
I_{IL}	Low-level input current	$\overline{MR}$ (3)	$\overline{MR}$ = 0 V, V_{DD} = 6 V	T_A = 25°C	–130	–200	–340	µA
				T_A = Full range	–90	–200	–350	
		CT	CT = 0 V, V_{DD} = 6 V		–25		25	nA
I_{OH}	High-level output current	TPS3838	V_{DD} = V_{IT} + 0.2 V, V_{OH} = V_{DD}				25	nA

(1) The lowest voltage at which $\overline{RESET}$ output becomes active, t_r, V_{DD} ≥ 15 µs/V
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminal.
(3) If manual reset is unused, $\overline{MR}$ should be connected to V_{DD} to minimize current consumption.

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Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Supply current	$V_{DD} > V_{IT}$, $V_{DD} < 3$ V	T_A = 25°C		220	500	nA
			T_A = Full range			600	
		$V_{DD} > V_{IT}$, $V_{DD} > 3$ V	T_A = 25°C		250	550	
			T_A = Full range			650	
		$V_{DD} < V_{IT}$	T_A = 25°C		10	25	µA
			T_A = Full range			30	
	Internal pullup resistor at $\overline{MR}$				33		kΩ
C_I	Input capacitance at $\overline{MR}$, CT	V_I = 0 V to V_{DD}			5		pF

Timing Requirements

R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
t_w	Pulse width	At V_{DD}	$V_{IH} = V_{IT} + 0.2$ V, $V_{IL} = V_{IT} - 0.2$ V	6	µs
		At $\overline{MR}$	$V_{DD} \geq V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	1	µs

Switching Characteristics

R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{DD} \geq V_{IT} + 0.2$ V, $\overline{MR} = 0.7 \times V_{DD}$, See timing diagram	CT = GND	5	10	15	ms
				CT = V_{DD}		200		
t_{PHL}	Propagation (delay) time, high- to low-level output	V_{DD} to $\overline{RESET}$ delay (TPS3836, TPS3838)	$V_{IL} = V_{IT} - 0.2$ V, $V_{IH} = V_{IT} + 0.2$ V			10		µs
			V_{IL} = 1.6 V			50		
t_{PLH}	Propagation (delay) time, low- to high-level output	V_{DD} to RESET delay (TPS3837)	$V_{IL} = V_{IT} - 0.2$ V, $V_{IH} = V_{IT} + 0.2$ V			10		µs
			V_{IL} = 1.6 V			50		
t_{PHL}	Propagation (delay) time, high- to low-level output	$\overline{MR}$ to RESET delay (TPS3836, TPS3838)	$V_{DD} \geq V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$			0.3		µs
t_{PLH}	Propagation (delay) time, low- to high-level output	$\overline{MR}$ to RESET delay (TPS3837)	$V_{DD} \geq V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$			0.3		µs

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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{DD}	Supply current	vs Supply voltage	2
I_{MR}	Manual reset current	vs Manual reset voltage	3
V_{OL}	Low-level output voltage	vs Low-level output current	4
V_{OH}	High-level output voltage	vs High-level output current	5
	Normalized reset threshold voltage	vs Free-air temperature	6
	Minimum pulse duration at V_{DD}	vs V_{DD} threshold overdrive	7

SUPPLY CURRENT vs SUPPLY VOLTAGE

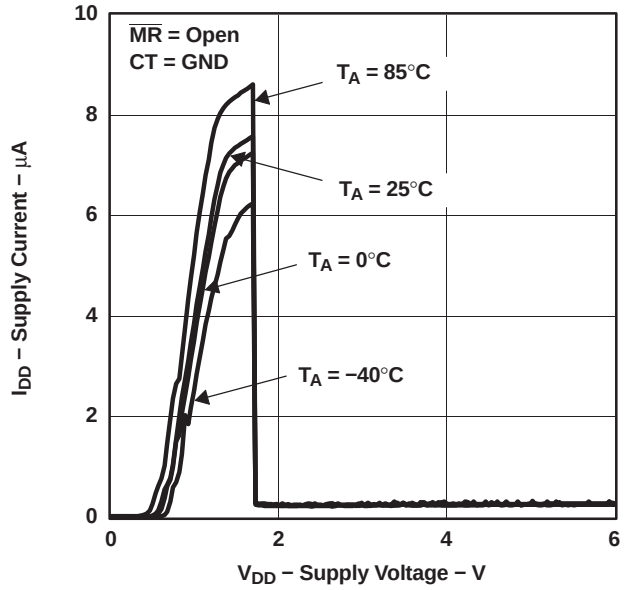

Figure 2.

MANUAL RESET CURRENT vs MANUAL RESET VOLTAGE

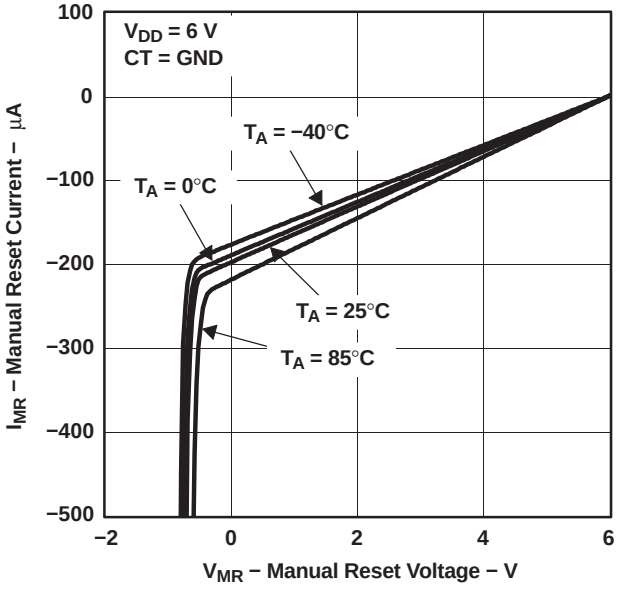

Figure 3.

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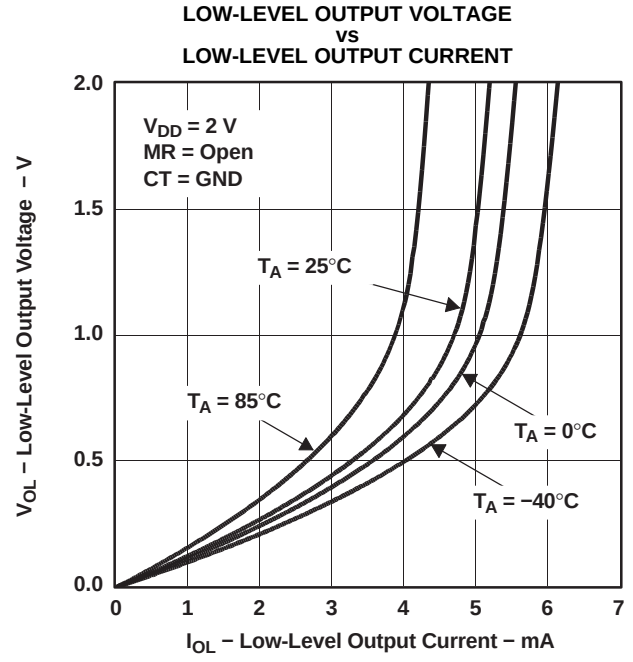

Figure 4.

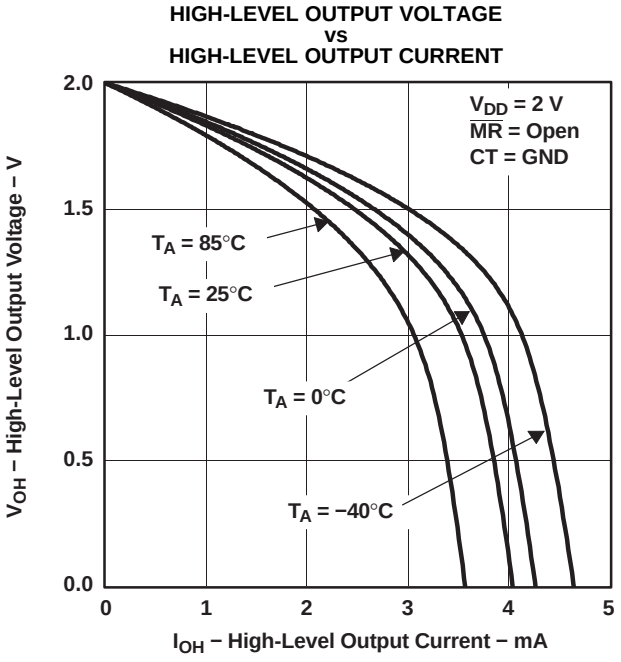

Figure 5.

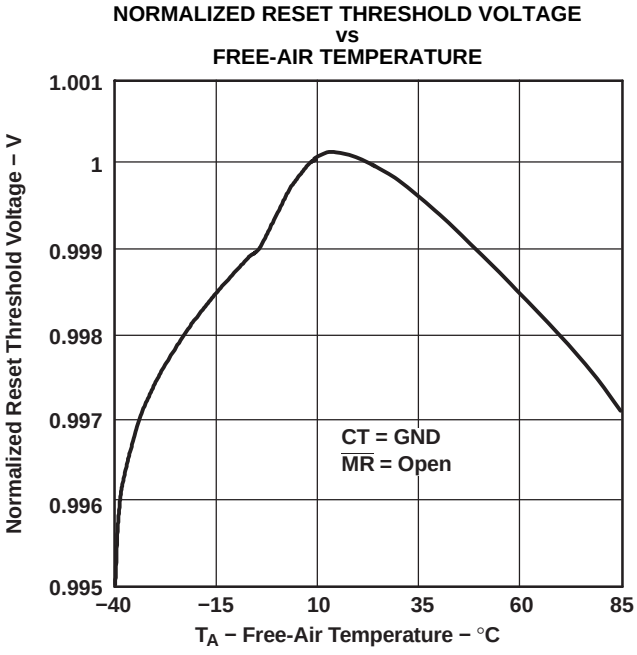

Figure 6.

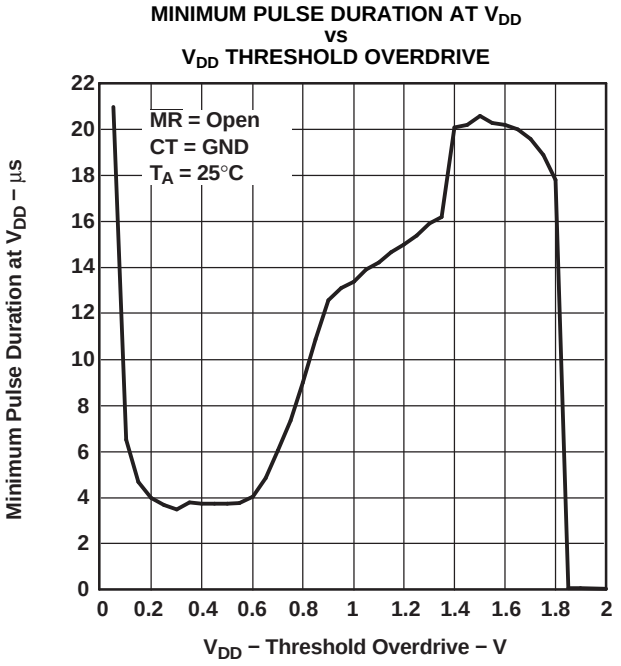

Figure 7.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3836J25MDBVTEP	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKRM	Samples
TPS3836L30MDBVREP	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BTX	Samples
TPS3837K33MDBVREP	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKZM	Samples
TPS3837K33QDBVREP	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PLSQ	Samples
V62/06637-09XE	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PLSQ	Samples
V62/06637-15XE	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKRM	Samples
V62/06637-17XE	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BTX	Samples
V62/06637-22XE	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PKZM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS3836-EP :

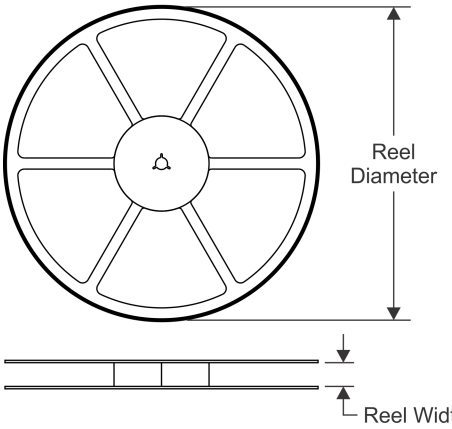
- Catalog: TPS3836
- Automotive: TPS3836-Q1

NOTE: Qualified Version Definitions:

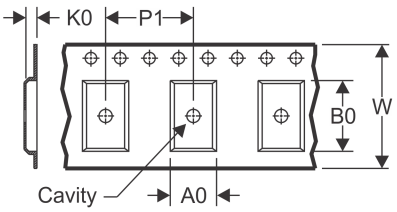
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

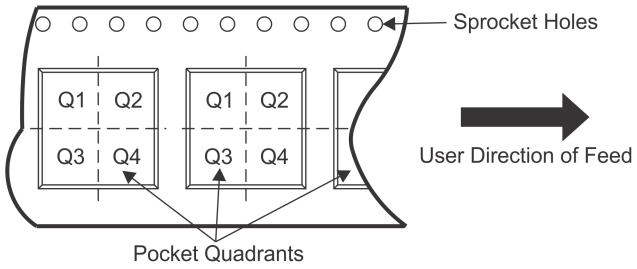


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

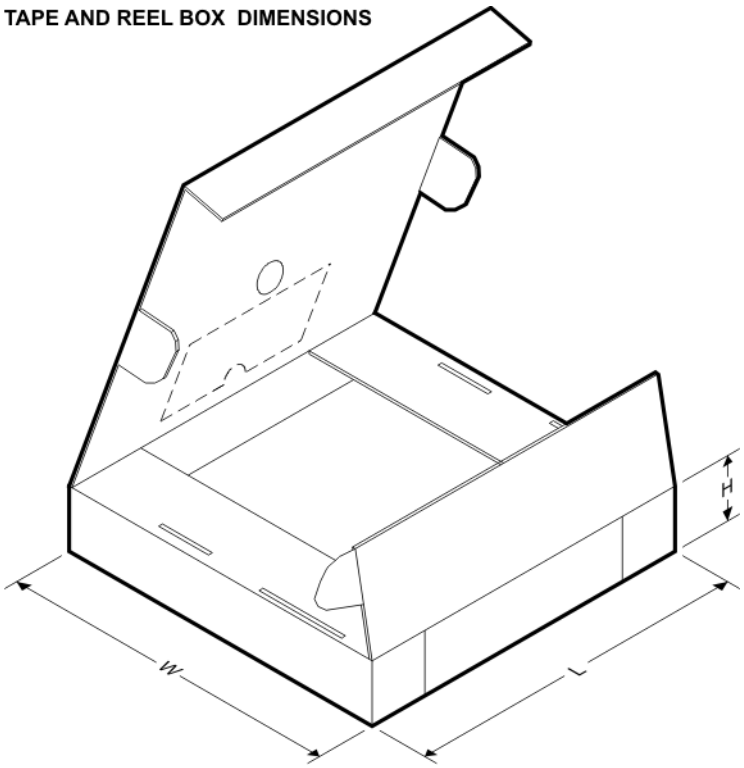
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3836J25MDBVTEP	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3836L30MDBVREP	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3837K33MDBVREP	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3837K33QDBVREP	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

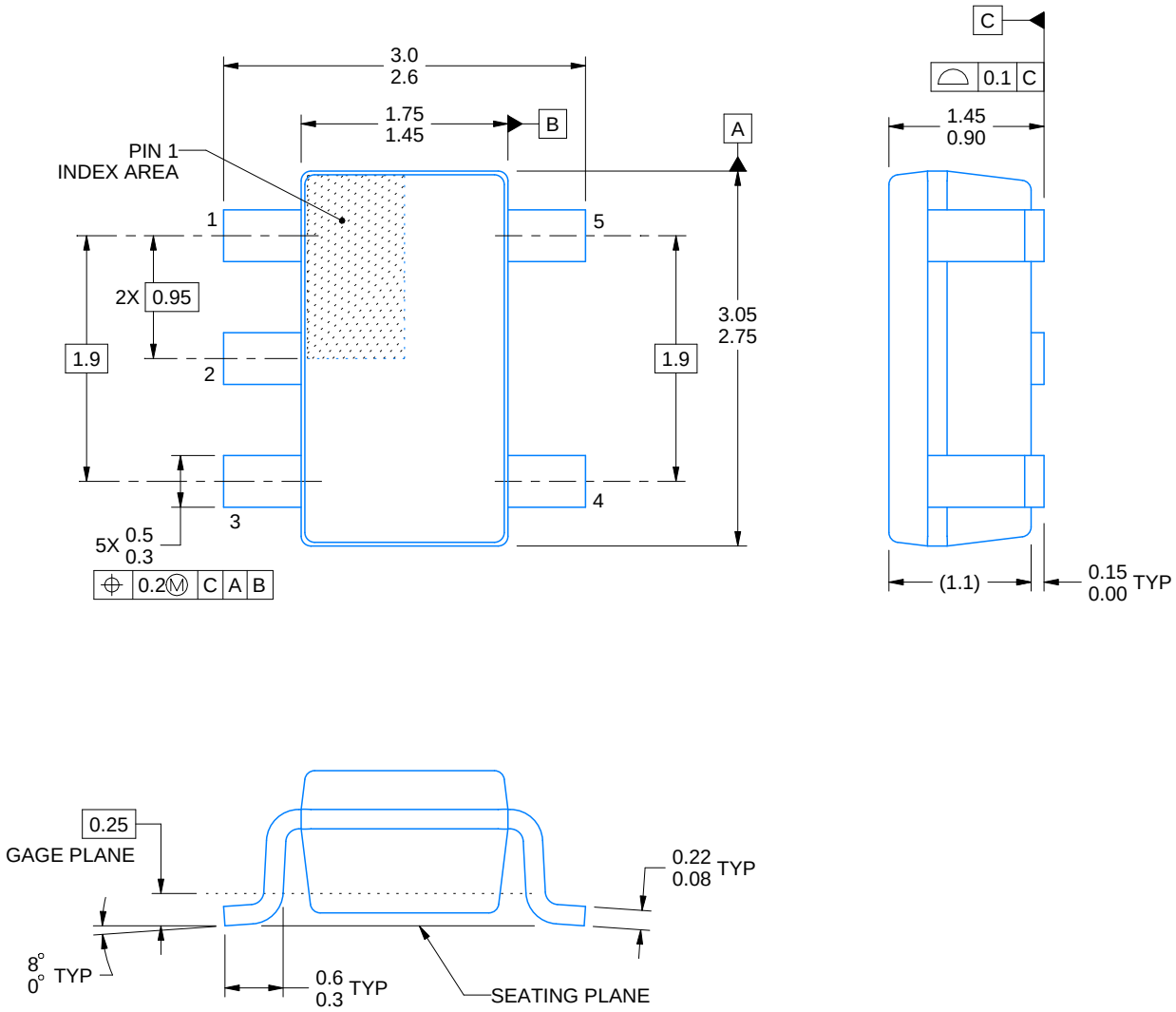
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3836J25MDBVTEP	SOT-23	DBV	5	250	182.0	182.0	20.0
TPS3836L30MDBVREP	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3837K33MDBVREP	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3837K33QDBVREP	SOT-23	DBV	5	3000	182.0	182.0	20.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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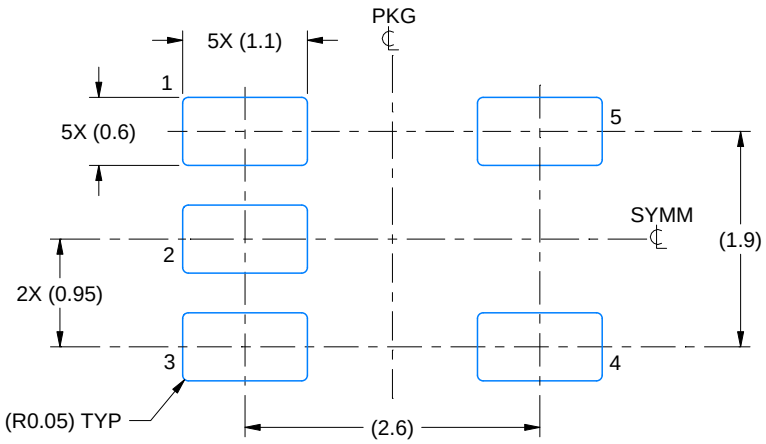
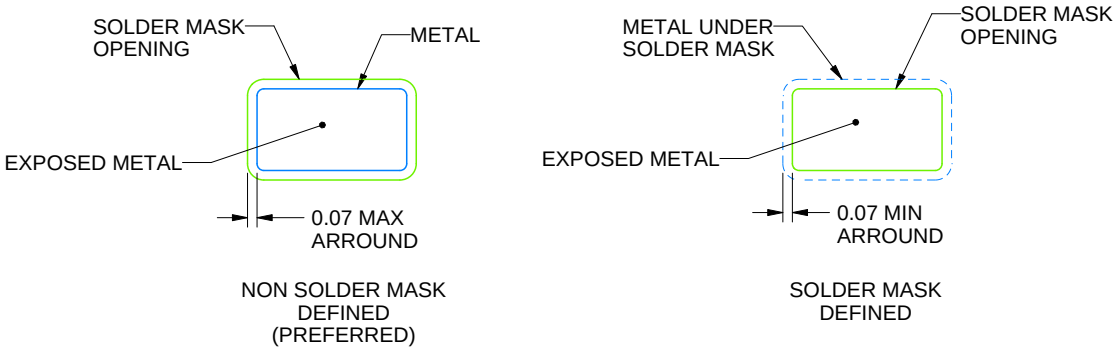
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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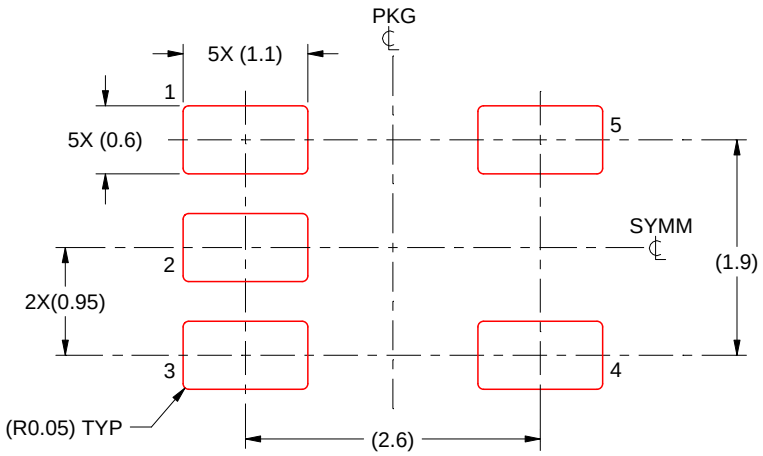
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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