TPS3700-Q1 窗口比较器，用于过压和欠压检测

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件充电器件模型 (CDM) ESD 分类等级 C6
- 宽电源电压范围：1.8 至 18V
- 可调节阀值：低至 400mV
- 针对过压和欠压检测的开漏输出
- 低静态电流：5.5μA（典型值）
- 高阀值精度：
  - 过温时为 1%
  - 0.25%（典型值）
- 内部滞后：5.5mV（典型值）
- 采用一个薄型小外形尺寸晶体管 (ThinSOT)23-6 封装

2 应用范围

- 汽车安全应用
- 车身电子装置
- 信息娱乐
- 电池电量低检测
- 电源排序
- 工业控制系统
- 现场可编程门阵列 (FPGA) 和特定用途集成电路 (ASIC) 应用
- 微控制器和数字信号处理器 (DSP) 应用

3 说明

TPS3700-Q1 宽电源电压窗口比较器在 1.8V 至 18V 的电压范围内运行。 此器件具有两个带有内部 400mV 基准的高精度比较器和两个用于过压和欠压检测的额定值为 18V 的开漏输出。 TPS3700-Q1 器件可被用作一个窗口比较器或者两个独立电压监视器；使用外部电阻器可对监视电压进行设定。

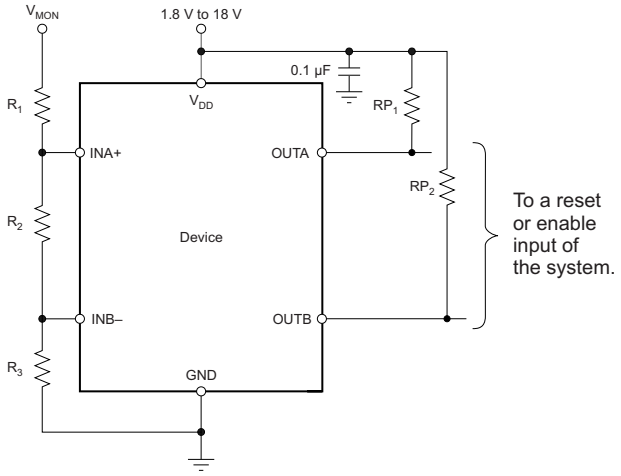
当 INA+ 端子上的电压下降至低于 (V_{IT+} - V_{hys}) 时，OUTA 端子被驱动至低电平，而当电压返回到各自阀值 (V_{IT+}) 之上时，OUTA 端子变为高电平。 当 INB- 端子上的电压上升至高于 V_{IT+}时，OUTB 端子被驱动至低电平，而当电压下降至低于各自的阀值 (V_{IT+} - V_{hys}) 时，OUTB 端子变为高电平。 TPS3700-Q1 器件中的两个比较器包括用于滤波的内置滞后来抑制短时毛刺脉冲，从而确保无故障触发的稳定输出运行。

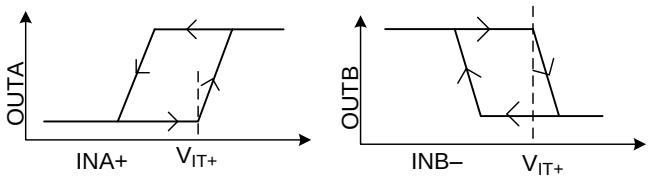
TPS3700-Q1 器件采用
薄型小外形尺寸晶体管 (ThinSOT)23-6 封装，并且额定结温温度范围介于 -40°C 至 125°C 之间。

器件信息

订货编号	封装	封装尺寸
TPS3700QDDCRQ1	SOT23 (6)	2.90mm x 1.60mm

4 简化电路原理图





目录

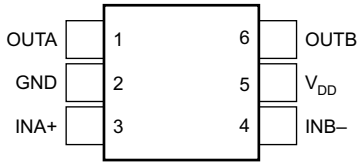
5 修订历史记录

Changes from Original (March 2014) to Revision A **Page**

- 已更改 器件状态从 *产品预览* 更改为 *生产数据*。 1

6 Terminal Configuration and Functions

6-Terminal SOT23
DDC Package
(Top View)



Terminal Functions

TERMINAL		DESCRIPTION
NAME	NUMBER	
GND	2	Ground
INA+	3	This terminal is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage ($V_{IT+} – V_{hys}$), the OUTA terminal is driven low.
INB–	4	This terminal is connected to the voltage that is monitored with the use of an external resistor divider. When the voltage at this terminal exceeds the threshold voltage (V_{IT+}), the OUTB terminal is driven low.
OUTA	1	This terminal is the INA+ comparator open-drain output. The OUTA terminal is driven low when the voltage at this comparator is below ($V_{IT+} – V_{hys}$). The output goes high when the sense voltage returns above the respective threshold (V_{IT+}).
OUTB	6	This terminal is the INB– comparator open-drain output. The OUTB terminal is driven low when the voltage at this comparator exceeds V_{IT+}. The output goes high when the sense voltage returns below the respective threshold ($V_{IT+} – V_{hys}$).
V_{DD}	5	This terminal is the supply voltage input. Connect a 1.8-V to 18-V supply to the V_{DD} terminal to power the device. Placing a 0.1-µF ceramic capacitor close to this terminal is good analog design practice.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	V_{DD}	–0.3	20	V
	OUTA, OUTB	–0.3	20	V
	INA+, INB–	–0.3	7	V
Current	Output terminal current		40	mA
Operating junction temperature, T_J		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–65	150	°C
V_{ESD}(1)	Human body model (HBM) ESD stress voltage(2)		2.5	kV
	Charge device model (CDM) ESD stress voltage(3)		1	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		1.8	18	V
V_I	Input voltage	INA+, INB–	0	6	V
V_O	Output voltage	OUTA, OUTB	0	18	V

7.4 Thermal Information

THERMAL METRIC(1)		DDC (6 TERMINALS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	54.3	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	52.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to 125°C, and 1.8 V < V_{DD} < 18 V, unless otherwise noted.
Typical values are at T_J = 25°C and V_{DD} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		1.8		18	V
$V_{(POR)}$	Power-on reset voltage(1)	V_{OL}max = 0.2 V, $I_{(OUTA/B)}$ = 15 µA			0.8	V
V_{IT+}	Positive-going input threshold voltage	V_{DD} = 1.8 V	396	400	404	mV
		V_{DD} = 18 V	396	400	404	mV
$V_{IT–}$	Negative-going input threshold voltage	V_{DD} = 1.8 V	387	394.5	400	mV
		V_{DD} = 18 V	387	394.5	400	mV
V_{hys}	Hysteresis voltage (hys = V_{IT+} – $V_{IT–}$)			5.5	12	mV
$I_{(INA+)}$ $I_{(INB–)}$	Input current (at the INA+ or INB– terminal)	V_{DD} = 1.8 V and 18 V, V_I = 6.5 V	–25	1	25	nA
		V_{DD} = 1.8 V and 18 V, V_I = 0.1 V	–15	1	15	nA
V_{OL}	Low-level output voltage	V_{DD} = 1.3 V, I_O = 0.4 mA			250	mV
		V_{DD} = 1.8 V, I_O = 3 mA			250	mV
		V_{DD} = 5 V, I_O = 5 mA			250	mV
$I_{lkg(OD)}$	Open-drain output leakage-current	V_{DD} = 1.8 V and 18 V, V_O = V_{DD}			300	nA
		V_{DD} = 1.8 V, V_O = 18 V			300	nA
I_{DD}	Supply current	V_{DD} = 1.8 V, no load		5.5	11	µA
		V_{DD} = 5 V		6	13	µA
		V_{DD} = 12 V		6	13	µA
		V_{DD} = 18 V		7	13	µA
	Startup delay(2)			150		µs
UVLO	Undervoltage lockout(3)	V_{DD} falling	1.3		1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)}$ > 15 µs/V. Below $V_{(POR)}$, the output cannot be determined.
(2) During power on, V_{DD} must exceed 1.8 V for at least 150 µs before the output is in a correct state.
(3) When V_{DD} falls below UVLO, OUTA is driven low and OUTB goes to high impedance. The outputs cannot be determined below $V_{(POR)}$.

7.6 Timing Requirements

Over operating temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
t_{PHL}	High-to-low propagation delay(1)	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400 mV See Figure 1		18		µs
t_{PLH}	Low-to-high propagation delay(1)	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400 mV See Figure 1		29		µs

(1) High-to-low and low-to-high refers to the transition at the input terminals (INA+ and INB–).

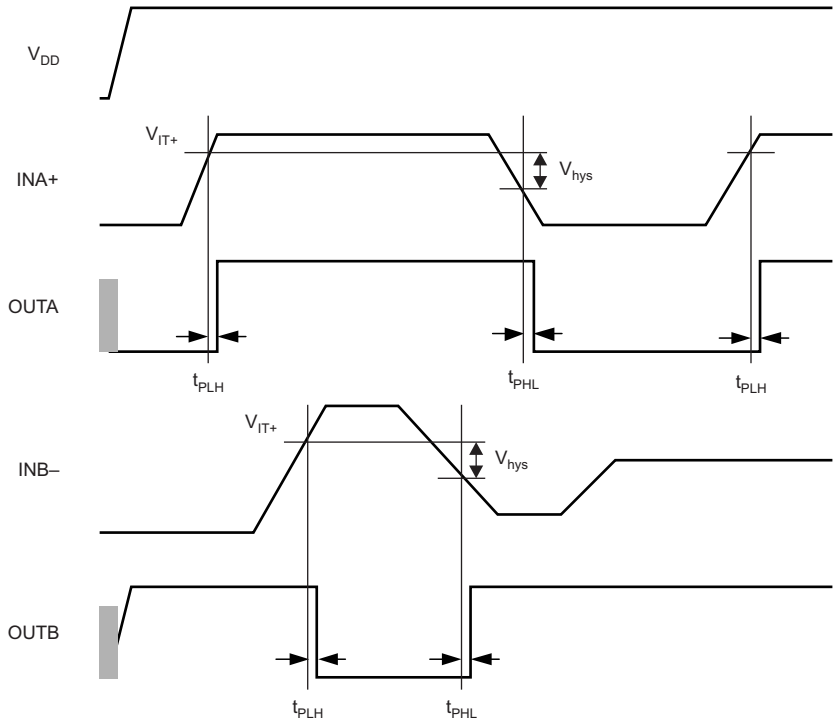


Figure 1. Timing Diagram

7.7 Switching Characteristics

Over operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_O = (0.1 to 0.9) × V_{DD}		2.2		µs
t_f	Output fall time	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_O = (0.1 to 0.9) × V_{DD}		0.22		µs

7.8 Typical Characteristics

At T_J = 25°C and V_{DD} = 5 V, unless otherwise noted.

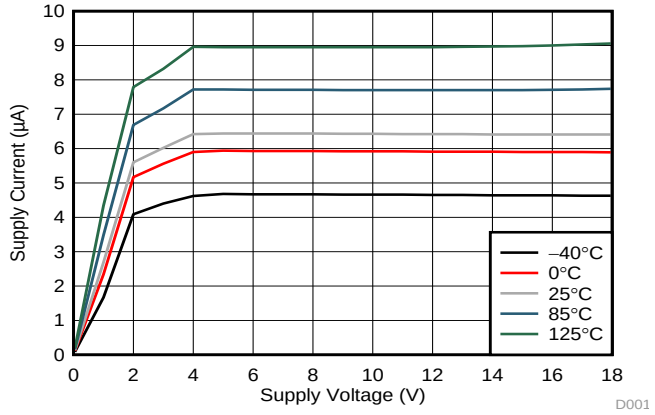


Figure 2. Supply Current (I_{DD}) vs Supply Voltage (V_{DD})

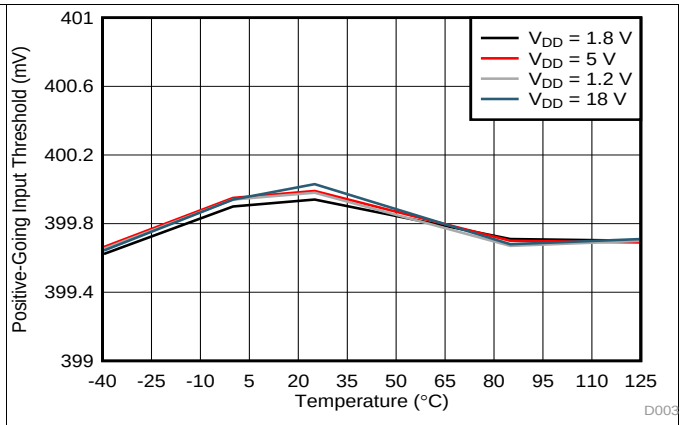


Figure 3. Rising Input Threshold Voltage (V_{IT+}) vs Temperature

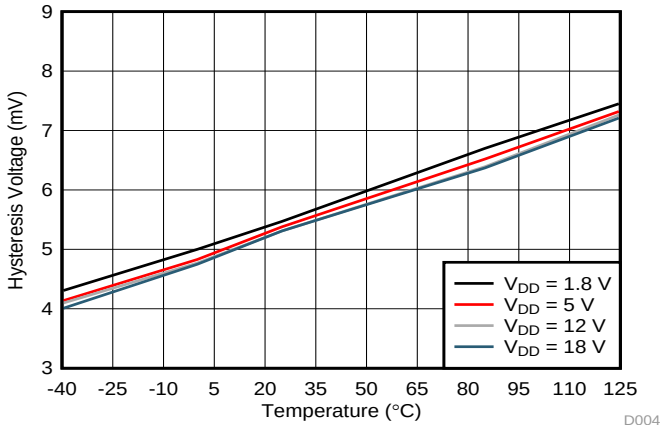


Figure 4. Hysteresis (V_{hys}) vs Temperature

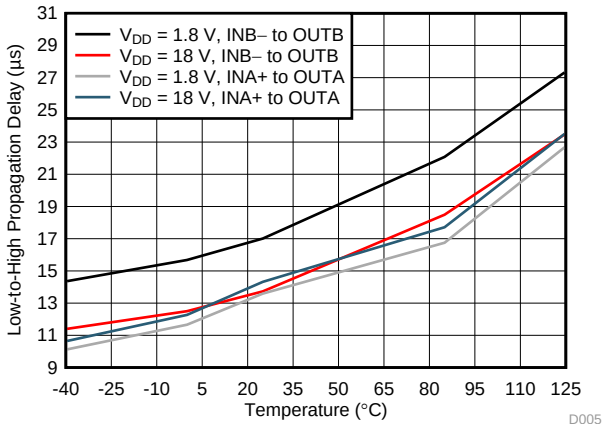


Figure 5. Propagation Delay vs Temperature (High-to-Low Transition at the Inputs)

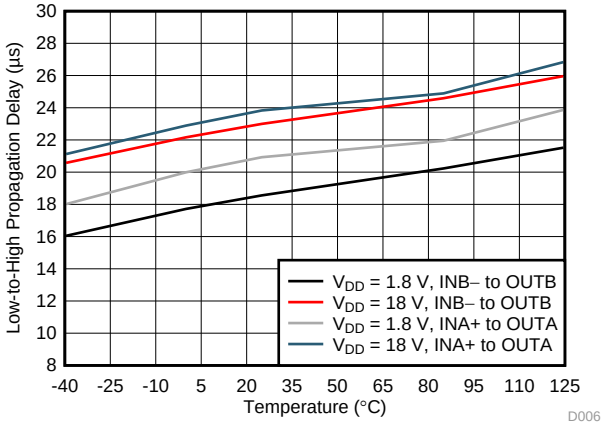
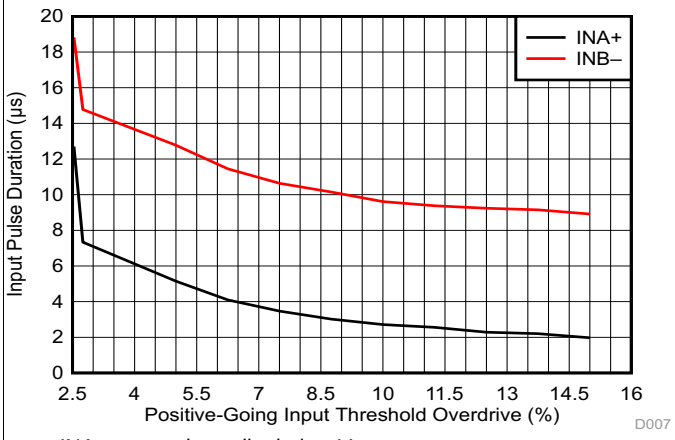


Figure 6. Propagation Delay vs Temperature (Low-to-High Transition at the Inputs)



INA+ = negative spike below $V_{IT–}$
INB– = positive spike above V_{IT+}

Figure 7. Minimum Pulse Width vs Threshold Overdrive Voltage

Typical Characteristics (continued)

At T_J = 25°C and V_{DD} = 5 V, unless otherwise noted.

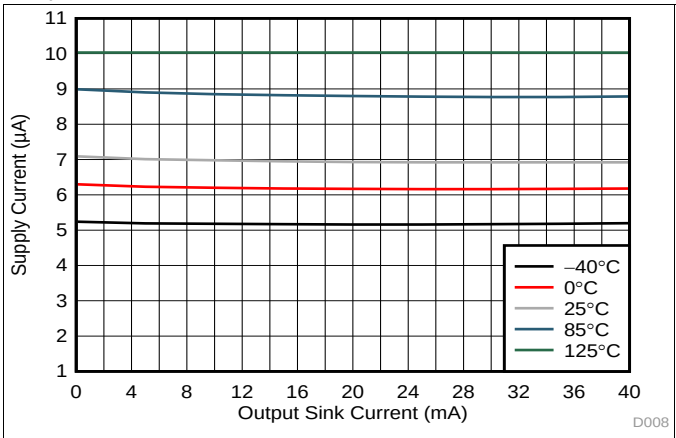


Figure 8. Supply Current (I_{DD}) vs Output Sink Current

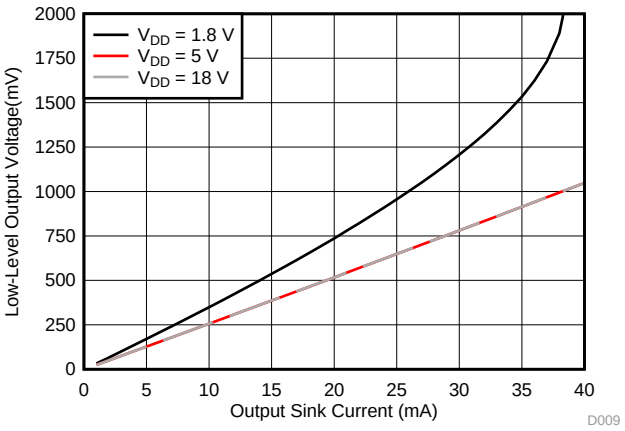


Figure 9. Output Voltage Low (V_{OL}) vs Output Sink Current (–40°C)

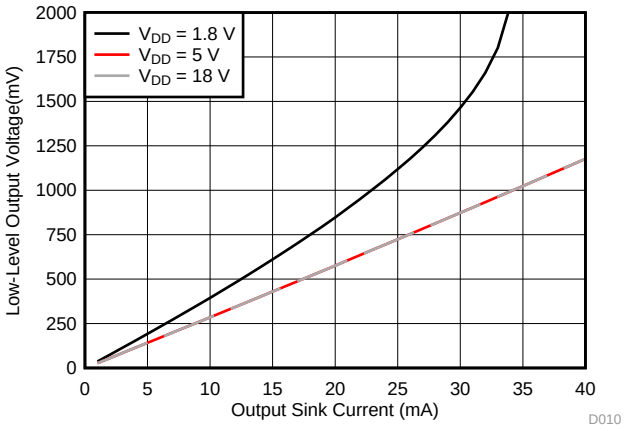


Figure 10. Output Voltage Low (V_{OL}) vs Output Sink Current (0°C)

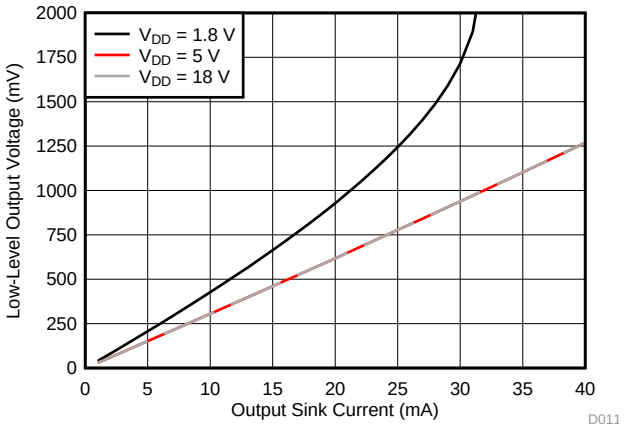


Figure 11. Output Voltage Low (V_{OL}) vs Output Sink Current (25°C)

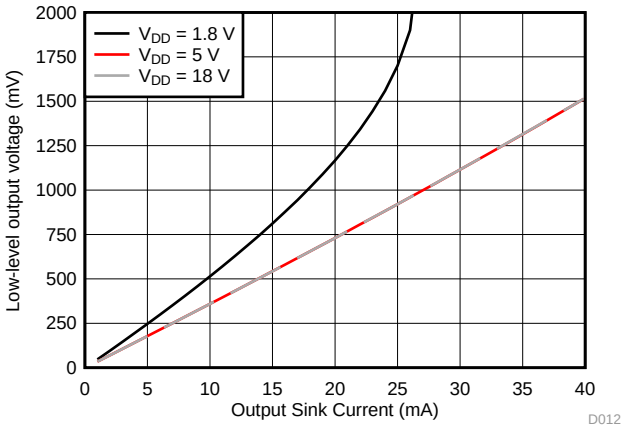


Figure 12. Output Voltage Low (V_{OL}) vs Output Sink Current (85°C)

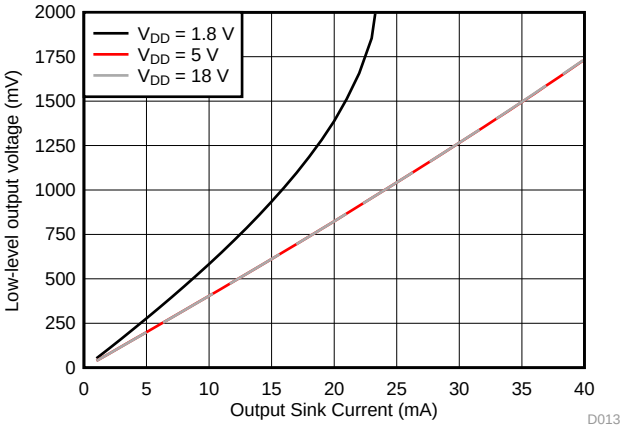


Figure 13. Output Voltage Low (V_{OL}) vs Output Sink Current (125°C)

8 Detailed Description

8.1 Overview

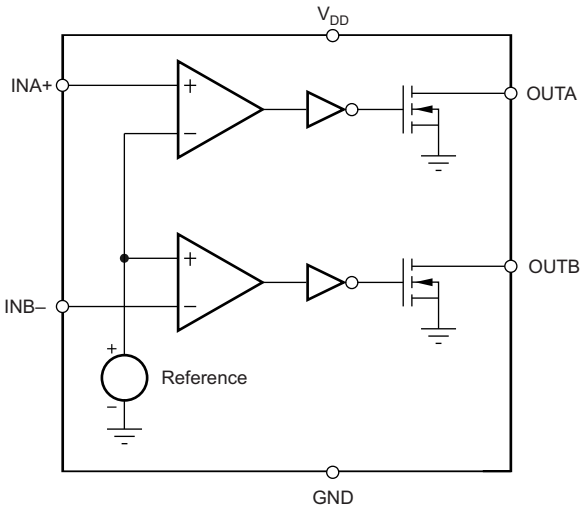
The TPS3700-Q1 device combines two comparators for overvoltage and undervoltage detection. The TPS3700-Q1 device is a wide-supply voltage range (1.8 to 18 V) device with a high-accuracy rising input threshold of 400 mV (1% over temperature) and built-in hysteresis. The outputs are also rated to 18 V and can sink up to 40 mA.

The TPS3700-Q1 device is designed to assert the output signals, as shown in Table 1. Each input terminal can be set to monitor any voltage above 0.4 V using an external resistor divider network. With the use of two input terminals of different polarities, the TPS3700-Q1 device forms a window comparator. Broad voltage thresholds can be supported that allow the device to be used in a wide array of applications.

Table 1. TPS3700-Q1 Truth Table

CONDITION	OUTPUT	STATUS
INA+ > V_{IT+}	OUTA high	Output A not asserted
INA+ < V_{IT-}	OUTA low	Output A asserted
INB– > V_{IT+}	OUTB low	Output B asserted
INB– < V_{IT-}	OUTB high	Output B not asserted

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Inputs (INA+, INB–)

The TPS3700-Q1 device combines two comparators. Each comparator has one external input (inverting and noninverting); the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to the reference voltage (400 mV). Both comparators also have a built-in falling hysteresis that makes the device less sensitive to supply rail noise and ensures stable operation.

The comparator inputs can swing from ground to 6.5 V, regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for extremely noisy applications in order to reduce sensitivity to transients and layout parasitics.

For comparator A, the corresponding output (OUTA) is driven to logic low when the input INA+ voltage drops below (V_{IT+} – V_{hys}). When the voltage exceeds V_{IT+}, the output (OUTA) goes to a high-impedance state; see Figure 1.

Feature Description (continued)

For comparator B, the corresponding output (OUTB) is driven to logic low when the voltage at input INB– exceeds V_{IT+}. When the voltage drops below $V_{IT+} – V_{hys}$ the output (OUTB) goes to a high-impedance state; see Figure 1. Together, these comparators form a window-detection function as discussed in the *Window Comparator* section.

8.3.2 Outputs (OUTA, OUTB)

In a typical TPS3700-Q1 application, the outputs are connected to a reset or enable input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]) or the outputs are connected to the enable input of a voltage regulator (such as a DC-DC or low-dropout regulator [LDO]).

The TPS3700-Q1 device provides two open-drain outputs (OUTA and OUTB). Pullup resistors must be used to hold these lines high when the output goes to high impedance (not asserted). By connecting pullup resistors to the proper voltage rails, the outputs can be connected to other devices at the correct interface-voltage levels. The TPS3700-Q1 outputs can be pulled up to 18 V, independent of the device supply voltage. To ensure proper voltage levels, some thought should be given while choosing the pullup resistor values. The pullup resistor value is determined by V_{OL}, sink-current capability, and output-leakage current ($I_{lkg(OD)}$). These values are specified in the Electrical Characteristics table. By using wired-AND logic, OUTA and OUTB can merge into one logic signal.

Table 1 and the *Inputs (INA+, INB–)* section describe how the outputs are asserted or de-asserted. See Figure 1 for a timing diagram that describes the relationship between threshold voltages and the respective output.

8.3.3 Window Comparator

The inverting and noninverting configuration of the comparators forms a window-comparator detection circuit using a resistor divider network, as shown in Figure 14 and Figure 15. The input terminals can monitor any system voltage above 400 mV with the use of a resistor divider network. The INA+ and INB– terminals monitor for undervoltage and overvoltage conditions, respectively.

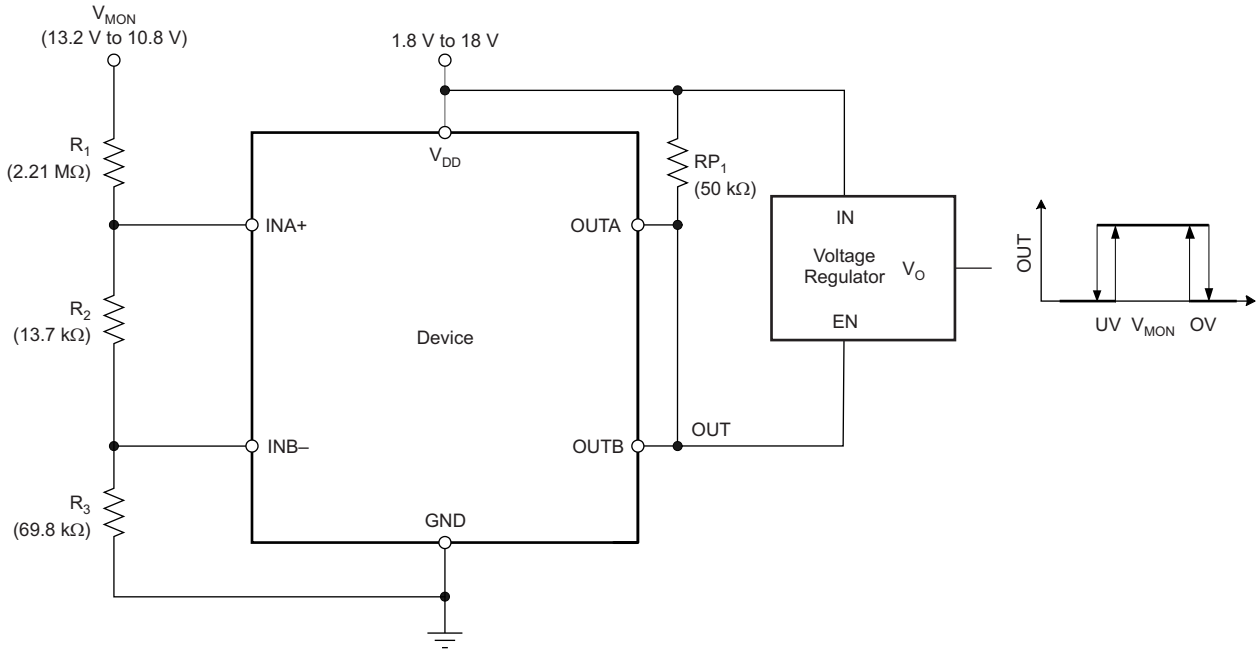


Figure 14. Window Comparator Block Diagram

Feature Description (continued)

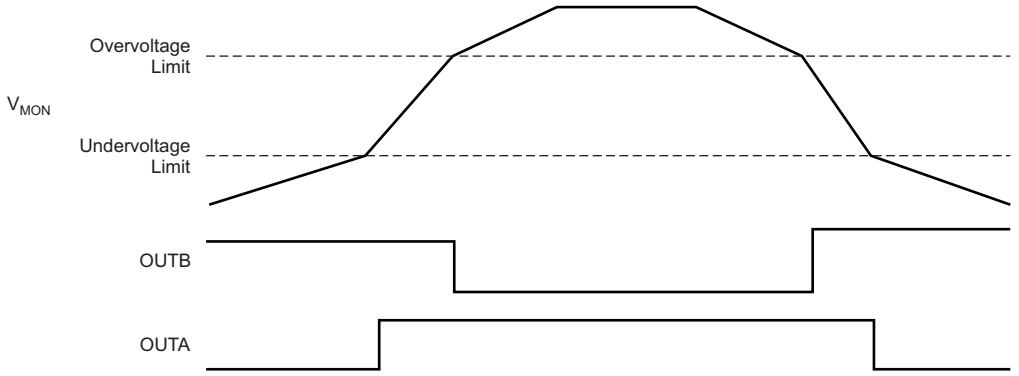


Figure 15. Window Comparator Timing Diagram

8.3.4 Immunity to Input Terminal Voltage Transients

The TPS3700-Q1 device is relatively immune to short voltage transient spikes on the input terminals. Sensitivity to transients is dependent on both transient duration and amplitude; see the *Minimum Pulse Width vs Threshold Overdrive Voltage* curve (Figure 7) in the Typical Characteristics section.

8.4 Device Functional Modes

The TPS3700-Q1 has a single functional mode, which is on when V_{DD} is greater than 1.8 V.

9 Application and Implementation

9.1 Application Information

The TPS3700-Q1 device is a wide-supply voltage window comparator that operates over a V_{DD} range of 1.8-V to 18-V. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for overvoltage and undervoltage detection. The device can be used either as a window comparator or as two independent voltage monitors. The monitored voltages are set with the use of external resistors.

9.1.1 V_{PULLUP} to a Voltage Other Than V_{DD}

The outputs are often tied to V_{DD} through a resistor. However some applications may require the outputs to be pulled up to a higher or lower voltage than V_{DD} in order to correctly interface with the reset and enable the terminal of other devices.

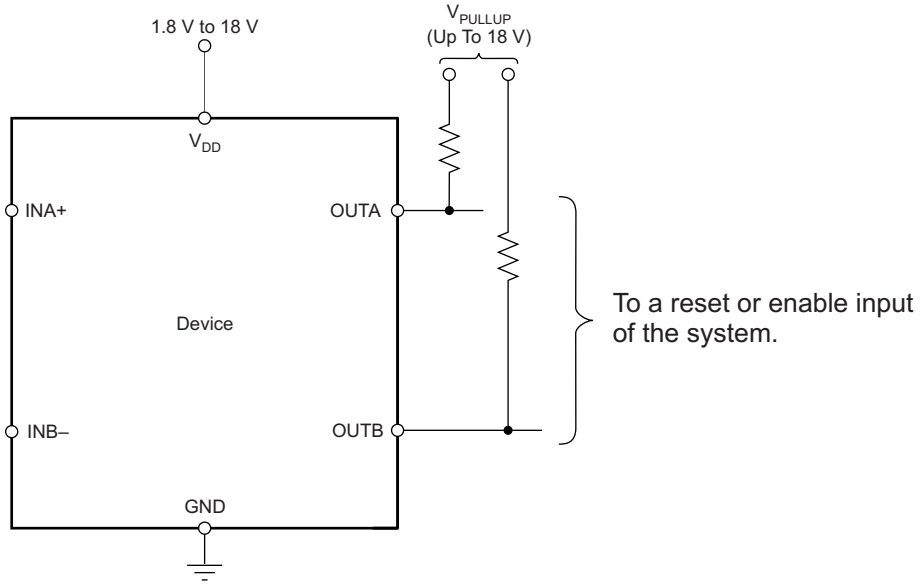


Figure 16. Interfacing to Voltages Other Than V_{DD}

Application Information (continued)

9.1.2 Monitoring V_{DD}

Many applications monitor the same rail that is powering V_{DD}. In these applications the resistor divider is simply connected to the V_{DD} rail.

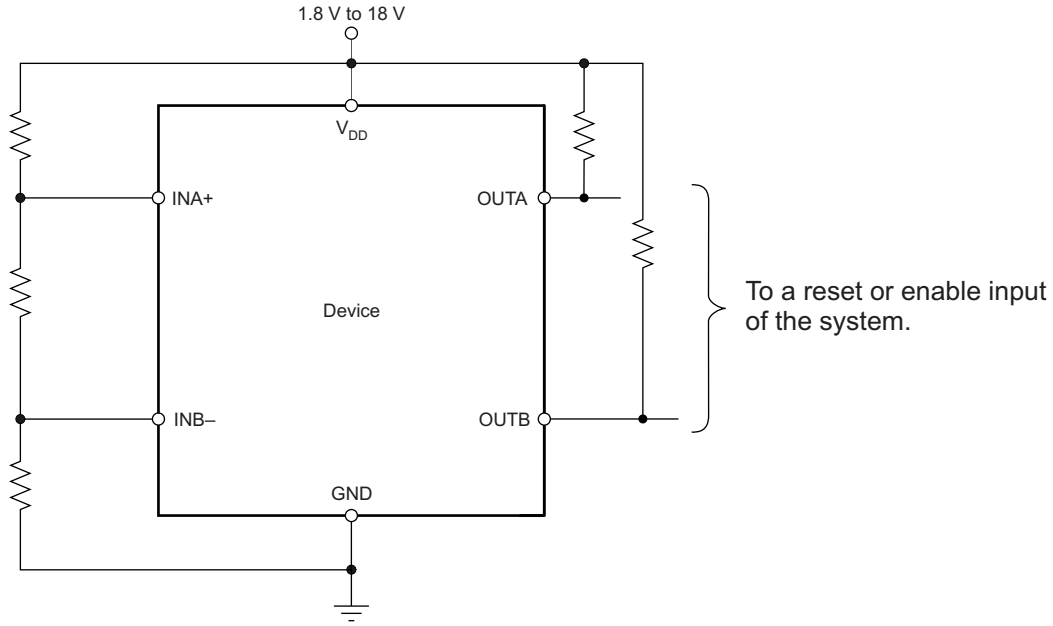
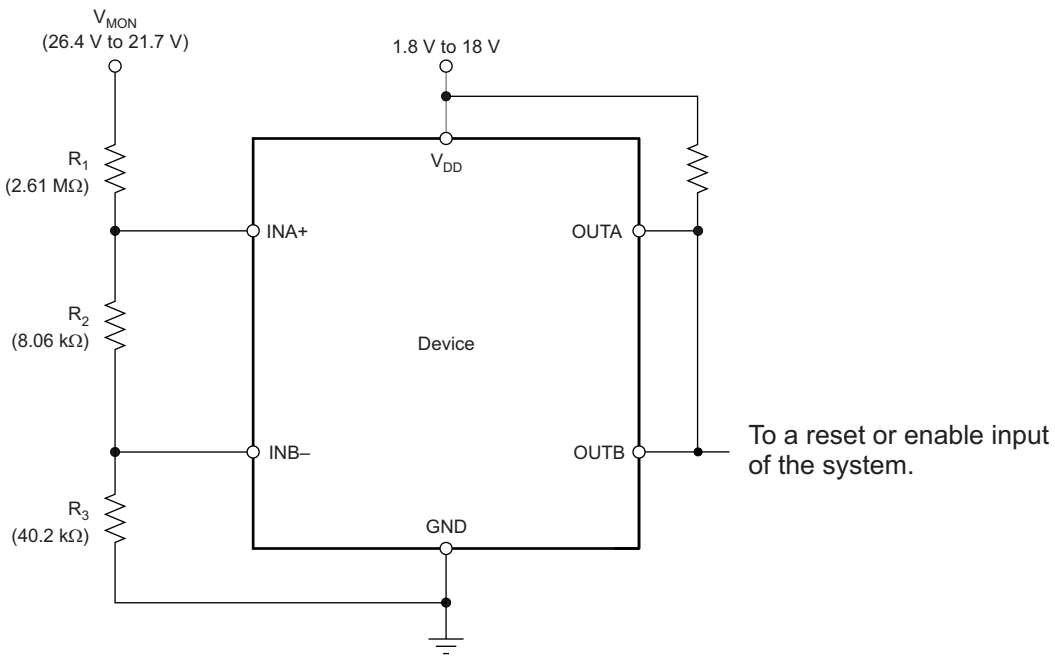


Figure 17. Monitoring the Same Voltage as V_{DD}

9.1.3 Monitoring a Voltage Other Than V_{DD}

Some applications monitor rails other than the one that is powering V_{DD}. In these types of applications the resistor divider used to set the desired thresholds in connected to the rail that is being monitored.



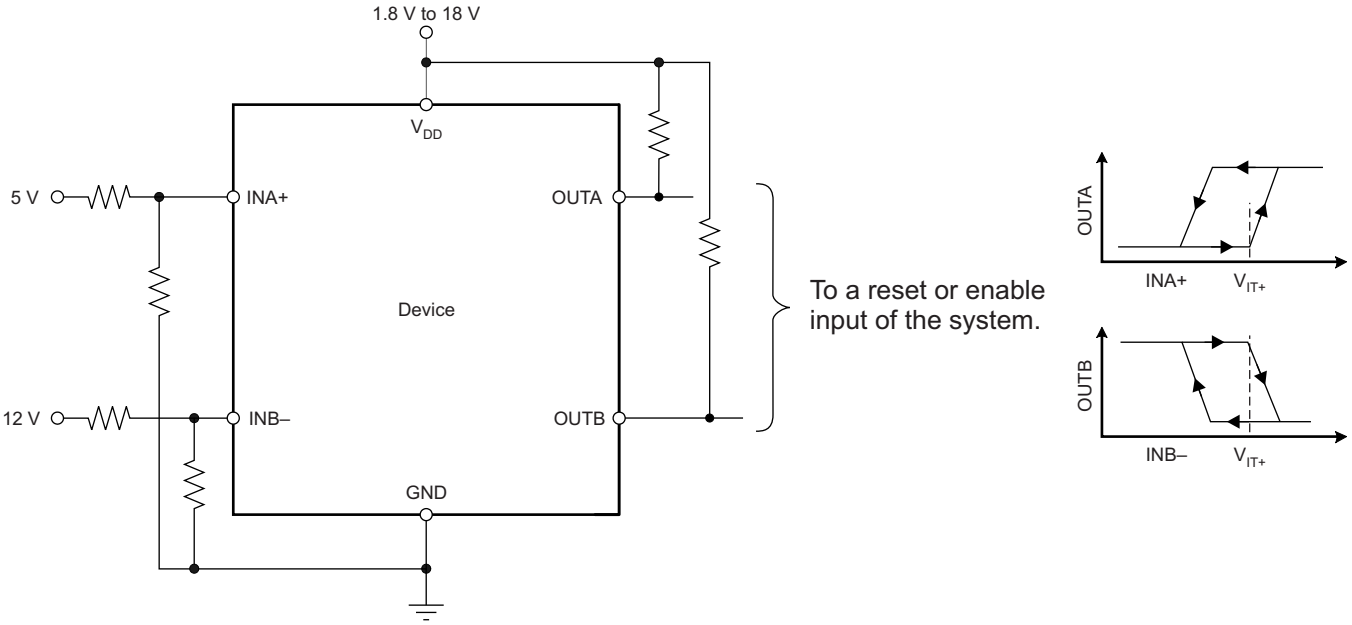
NOTE: The inputs can monitor a voltage higher than V_{DD}max with the use of an external resistor divider network.

Figure 18. Monitoring a Voltage Other Than V_{DD}

Application Information (continued)

9.1.4 Monitoring Overvoltage and Undervoltage for Separate Rails

Some applications may want to monitor for overvoltage conditions on one rail while also monitoring for undervoltage conditions on a different rail. In those applications two independent resistor dividers will need to be used.



NOTE: In this case, OUTA is driven low when an undervoltage condition is detected at the 5-V rail and OUTB is driven low when an overvoltage condition is detected at the 12-V rail.

Figure 19. Monitoring Overvoltage for One Rail and Undervoltage for a Different Rail

9.2 Typical Application

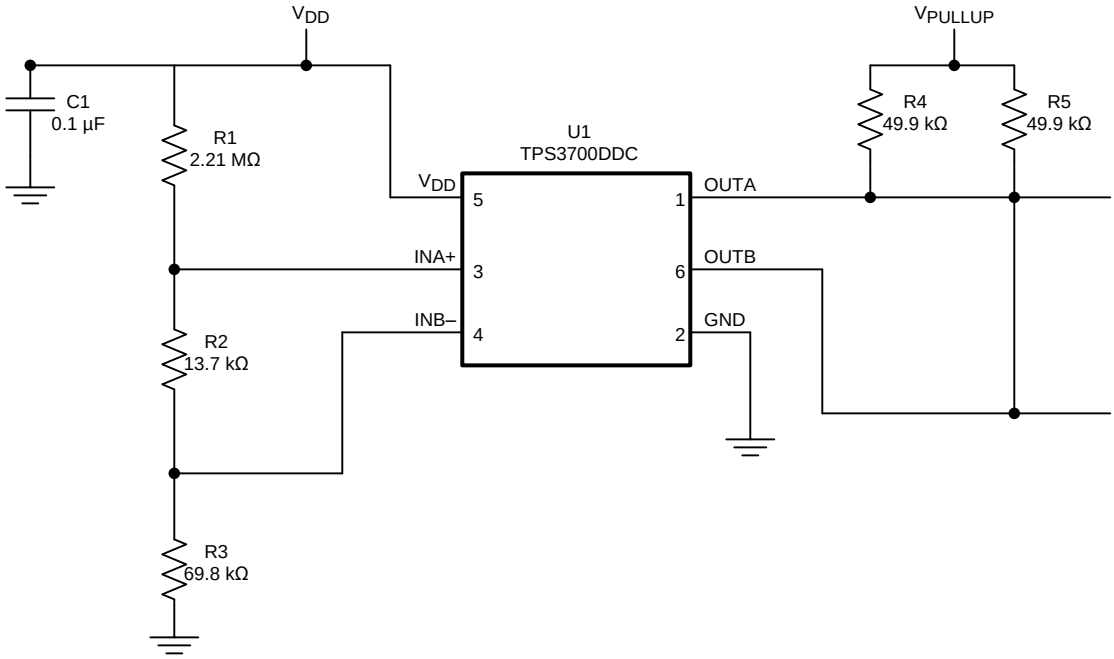


Figure 20. Typical Application Schematic

9.2.1 Design Requirements

9.2.1.1 Input Supply Capacitor

Although an input capacitor is not required for stability, connecting a 0.1-µF low equivalent series resistance (ESR) capacitor across the V_{DD} terminal and GND terminal is good analog design practice. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

9.2.1.2 Input Capacitors

Although not required in most cases, for extremely noisy applications, placing a 1-nF to 10-nF bypass capacitor from the comparator inputs (INA+, INB–) to the GND terminal is good analog design practice. This capacitor placement reduces device sensitivity to transients.

9.2.2 Detailed Design Procedure

Use Equation 1 through Equation 4 to calculate the resistor divider values and target threshold voltage.

$$R_T = R_1 + R_2 + R_3 \quad (1)$$

Select a value for R_T such that the current through the divider is approximately 100-times higher than the input current at the INA+ and INB– terminals. The resistors can have high values to minimize current consumption as a result of low-input bias current without adding significant error to the resistive divider. See the application note *Optimizing Resistor Dividers at a Comparator Input* (SLVA450) for details on sizing input resistors.

Use Equation 2 to calculate the value of R_3.

$$R_3 = \frac{R_T}{V_{MON(OV)}} \times V_{IT+} \quad (2)$$

where

- $V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected

Typical Application (continued)

Use Equation 3 or Equation 4 to calculate the value of R_2.

$$R_2 = \left(\frac{R_T}{V_{MON}\,(\text{no UV})} \times V_{IT+} \right) - R_3 \quad (3)$$

where

- $V_{MON(\text{no UV})}$ is the target voltage at which an undervoltage condition is removed as V_{MON} rises

$$R_2 = \left(\frac{R_T}{V_{MON(UV)}} \times (V_{IT+} - V_{hys}) \right) - R_3 \quad (4)$$

where:

$V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected

9.2.3 Application Curves

T_J = 25°C

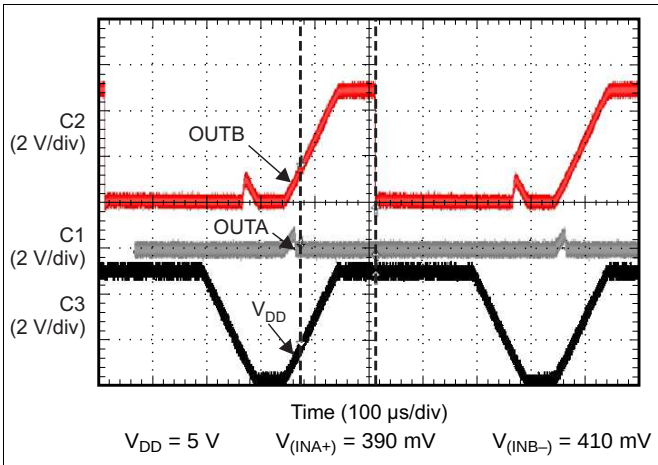


Figure 21. Startup Delay (Outputs Pulled Up to V_{DD})

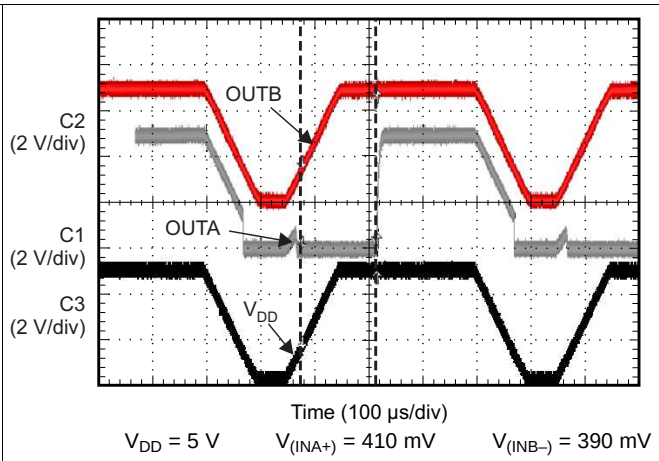


Figure 22. Startup Delay (Outputs Pulled Up to V_{DD})

10 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 1.8 V and 18 V.

11 Layout

11.1 Layout Guidelines

Placing a 0.1-µF capacitor close to the V_{DD} terminal to reduce the input impedance to the device is good analog design practice. The pullup resistors can be separated if separate logic functions are needed (see Figure 23) or both resistors can be tied to a single pullup resistor if a logical AND function is desired.

11.2 Layout Example

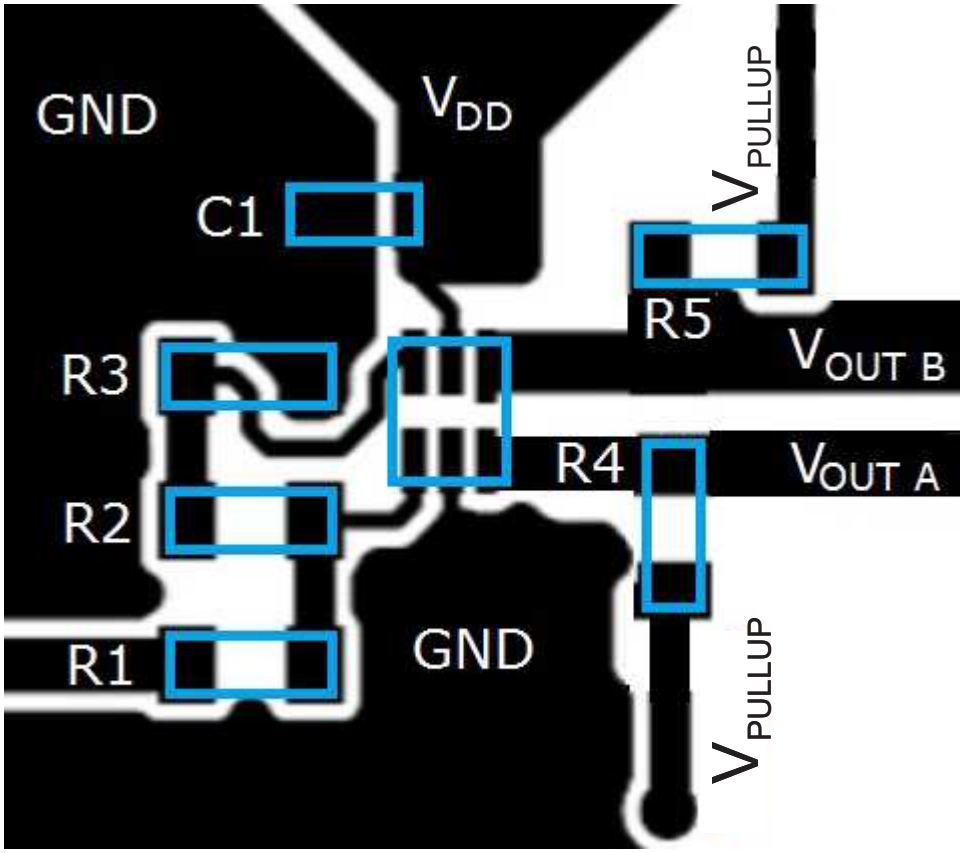


Figure 23. TPS3700-Q1 Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- *将 TPS3700 用作一个负电压轨过压和欠压检测器*，SLVA600
- *优化比较器输入上的电阻分压器*，SLVA450
- *TPS3700EVM-114 评估模块*，SLVU683

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 机械封装和可订购信息

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3700QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PD7Q	Samples
TPS3700QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	5O	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

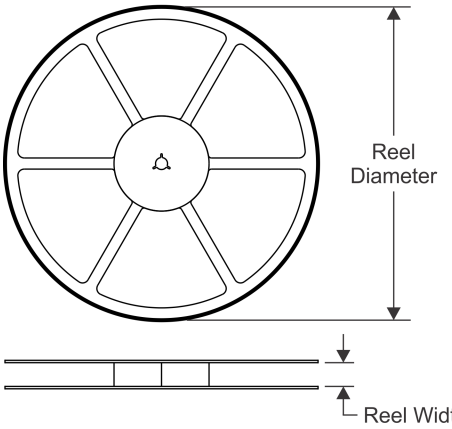
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

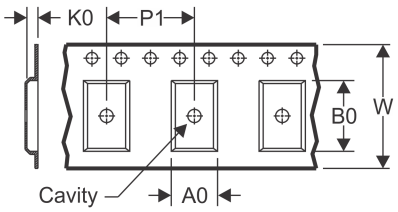
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

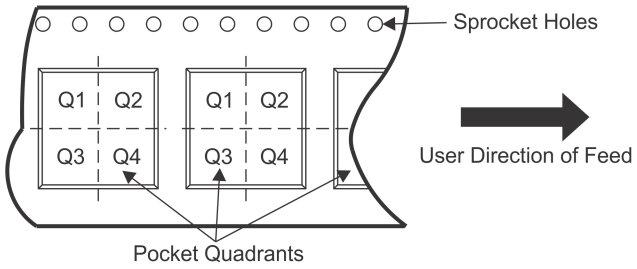


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

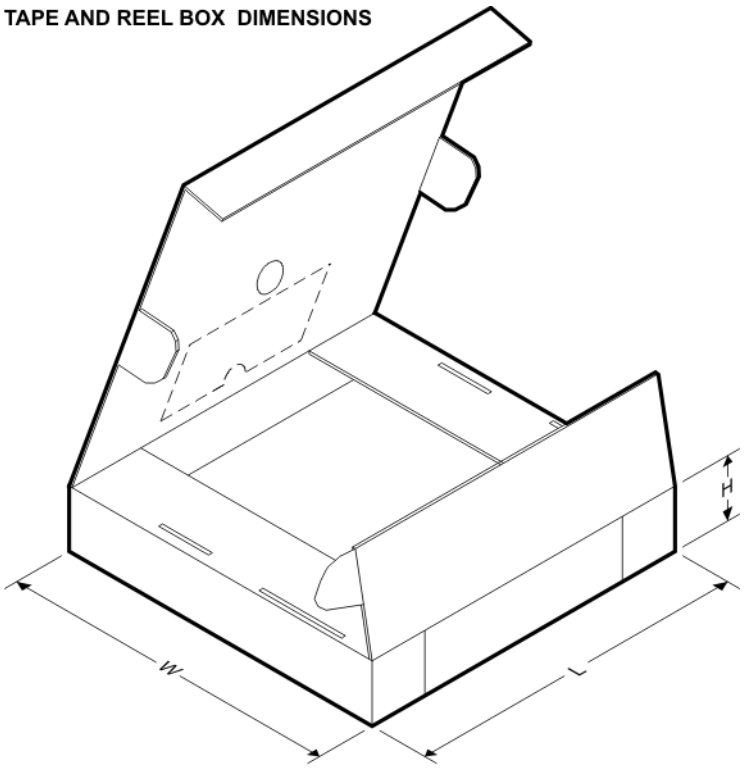
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3700QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3700QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

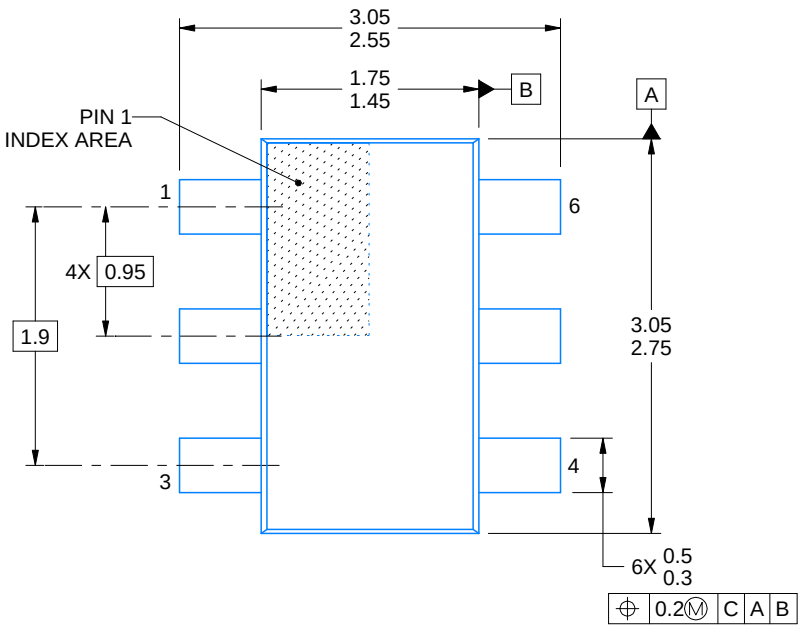
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3700QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3700QDSERQ1	WSON	DSE	6	3000	213.0	191.0	35.0

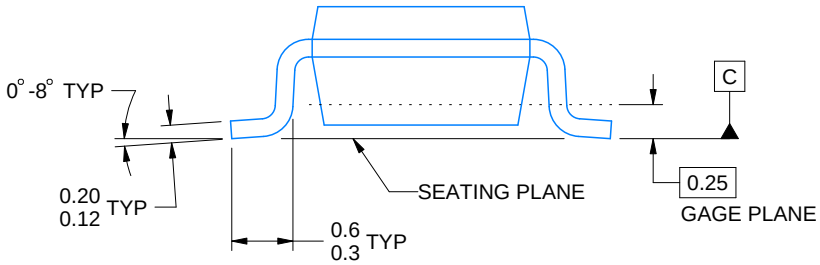
PACKAGE OUTLINE

DDC0006A

SOT - 1.1 max height

SOT

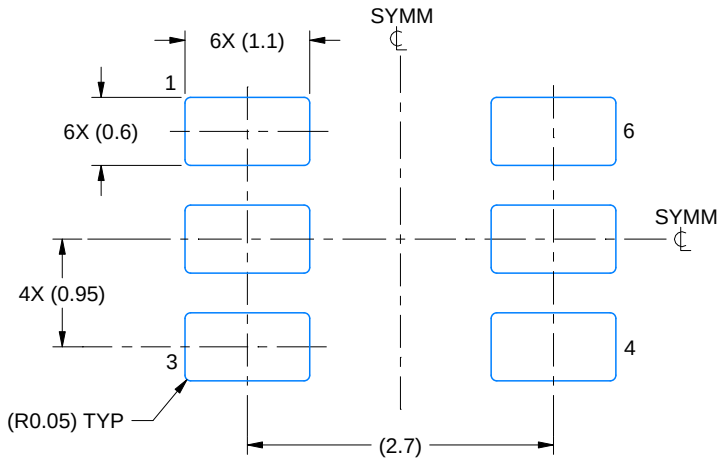




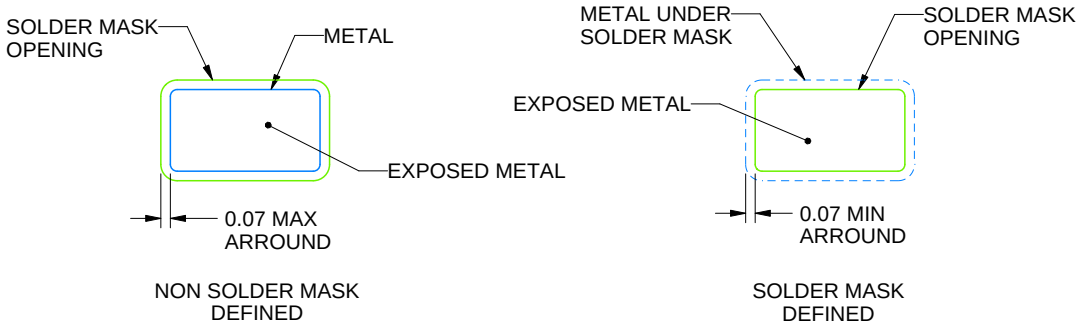
4214841/B 11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

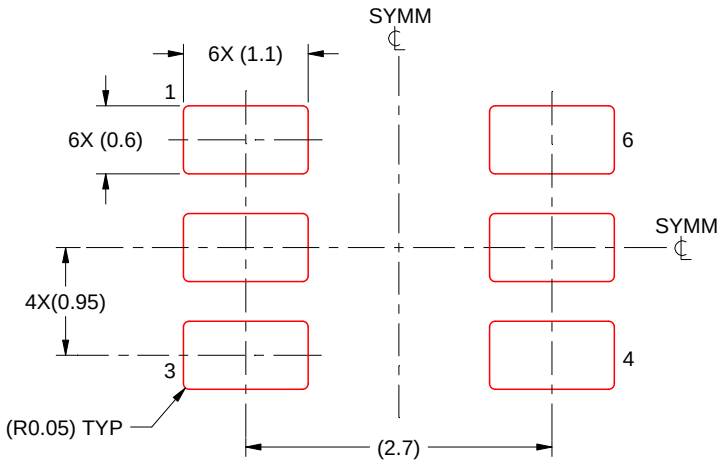


SOLDERMASK DETAILS

4214841/B 11/2020

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



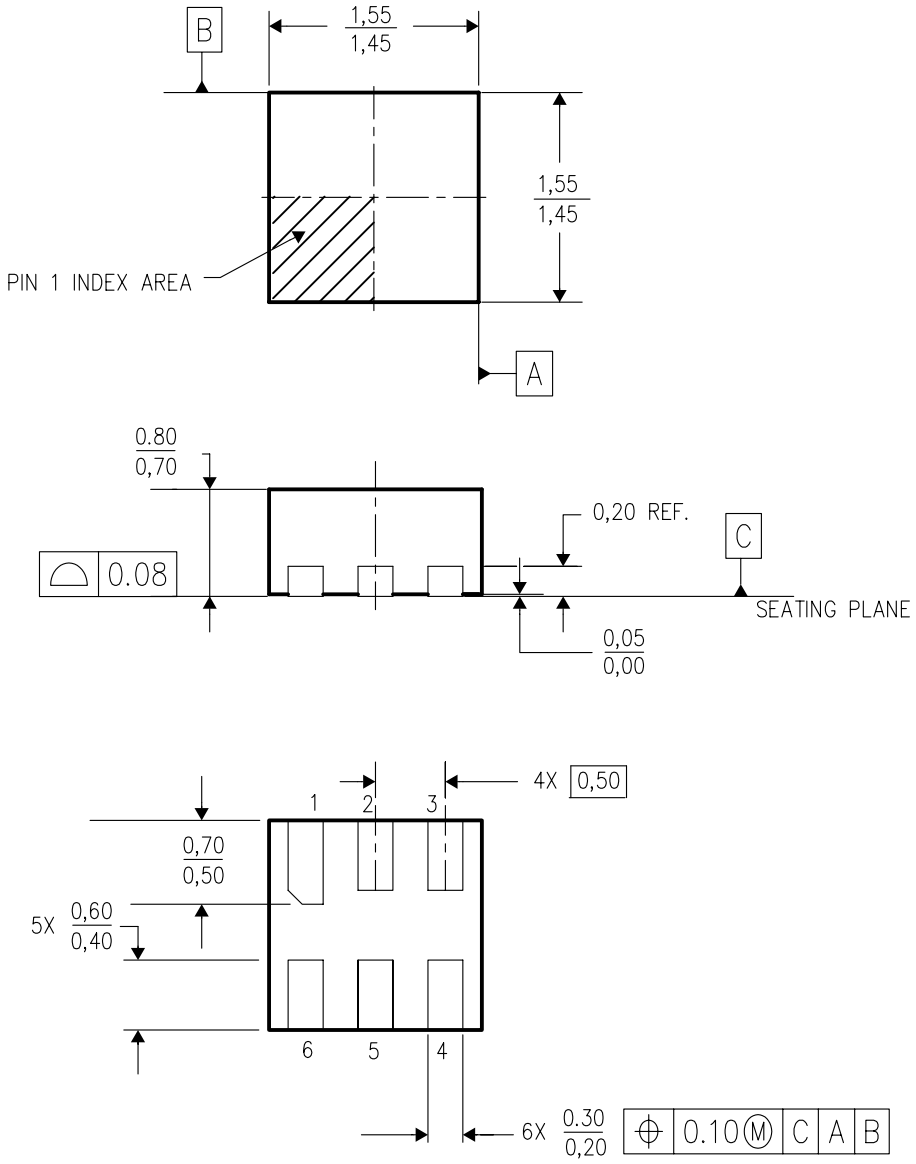
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/B 11/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



4207810/A 03/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

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