TEXAS INSTRUMENTS

TPS3851

ZHCSFP1 –NOVEMBER 2016

# TPS3851 集成有看门狗定时器的高精度电压监控器

1 特性

- 0.8% 电压阈值精度
- 高精度欠压监控：
  - 支持 1.8V 到 5.0V 共模电压
  - 支持 4% 和 7% 欠压阈值
  - 0.5% 迟滞
- 经过出厂编程的高精度看门狗和复位定时器：
  - ±15% 精度 WDT 和 RST 延迟
- 看门狗禁用功能
- 用户可编程的看门狗超时
- 输入电压范围 (V_{DD})：1.6V 至 6.5V
- 低静态电流：I_{DD} = 10µA（典型值）
- 漏极开路输出
- 手动复位输入 ($\overline{MR}$)
- 采用 3mm x 3mm、8 引脚晶圆级超小外形无引线 (VSON) 封装
- 工作结温范围：
  -40°C 至 +125°C

2 应用

- 安全型 应用
- 远程信息处理控制单元
- 现场可编程门阵列 (FPGA) 和专用集成电路 (ASIC)
- 微控制器和数字信号处理器 (DSP)

全集成微控制器监控电路

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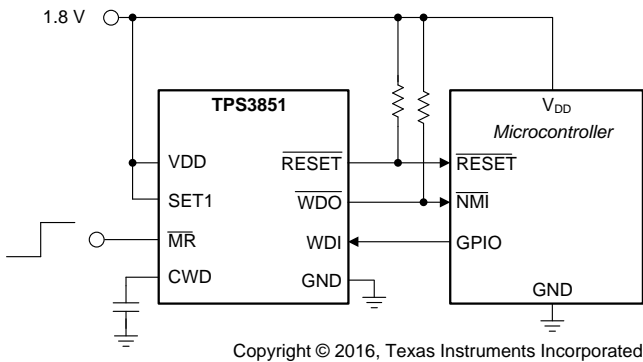
3 说明

TPS3851 完美结合了高精度电压监控器和可编程看门狗定时器。TPS3851 比较器的欠压阈值 (V_{ITN}) 精度达 0.8%（−40°C 至 +125°C 范围内）。TPS3851 还包含与欠压阈值相关的高精度迟滞，因此成为了紧容差系统的理想之选。监视器 $\overline{RESET}$ 延迟 的 精度达 15%，支持高精度延迟定时。
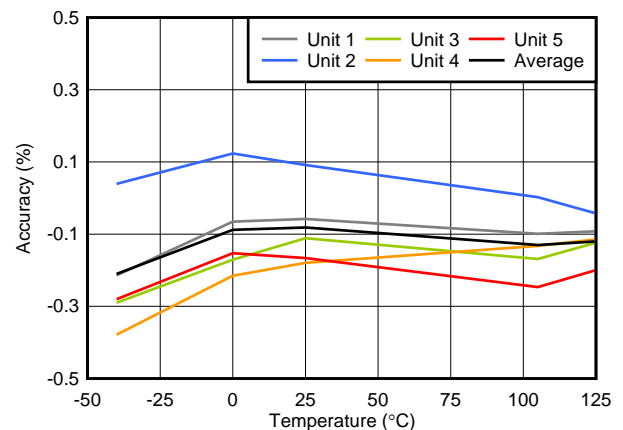
TPS3851 包含一个可编程的看门狗定时器，适用于多种 应用。专用的看门狗输出 ($\overline{WDO}$) 可提高分辨率，从而帮助确定出现故障情况的原因。看门狗超时可通过外部电容编程，也可以采用工厂编程的默认延迟设置。可通过逻辑引脚禁用看门狗，避免在开发过程中出现意外的看门狗超时。

TPS3851 采用小型 3.00mm × 3.00mm 8 引脚 VSON 封装。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
TPS3851	VSON (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

欠压阈值 (V_{ITN}) 精度与温度间的关系

English Data Sheet: SBVS300

目录

4 修订历史记录

日期	修订版本	注释
2016 年 11 月	*	最初发布版本。

5 Pin Configuration and Functions

**DRB Package: TPS3851
3-mm × 3-mm VSON-8
Top View**

Not to scale
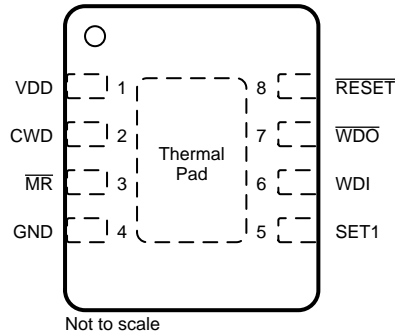
Pin Functions

NAME	NO.	I/O	DESCRIPTION
CWD	2	I	Programmable watchdog timeout input. The watchdog timeout is set by connecting a capacitor between this pin and ground. Connecting via a 10-kΩ resistor to V_{DD} or leaving unconnected further enables the selection of the preset watchdog timeouts; see the *CWD Functionality* section. The TPS3851 determines the watchdog timeout using either Equation 1 or Equation 2 with standard or extended timing, respectively.
GND	4	—	Ground pin
$\overline{MR}$	3	I	Manual reset pin. A logical low on this pin issues a $\overline{RESET}$. This pin is internally pulled up to V_{DD}. $\overline{RESET}$ remains low for a fixed reset delay (t_{RST}) time after $\overline{MR}$ is deasserted (high).
$\overline{RESET}$	8	O	Reset output. Connect $\overline{RESET}$ using a 1-kΩ to 100-kΩ resistor to the correct pullup voltage rail (V_{PU}). $\overline{RESET}$ goes low when V_{DD} goes below the undervoltage threshold (V_{ITN}). When V_{DD} is within the normal operating range, the $\overline{RESET}$ timeout-counter starts. At completion, $\overline{RESET}$ goes high. During startup, the state of $\overline{RESET}$ is undefined below the specified power-on-reset (POR) voltage (V_{POR}). Above POR, $\overline{RESET}$ goes low and remains low until the monitored voltage is within the correct operating range (above $V_{ITN}+V_{HYST}$) and the $\overline{RESET}$ timeout is complete.
SET1	5	I	Logic input. Grounding the SET1 pin disables the watchdog timer. SET1 and CWD select the watchdog timeouts; see the *SET1* section.
VDD	1	I	Supply voltage pin. For noisy systems, connecting a 0.1-μF bypass capacitor is recommended.
WDI	6	I	Watchdog input. A falling edge must occur at WDI before the timeout (t_{WD}) expires. When the watchdog is not in use, the SET1 pin can be used to disable the watchdog. WDI is ignored when $\overline{RESET}$ or $\overline{WDO}$ are low (asserted) and when the watchdog is disabled. If the watchdog is disabled, WDI cannot be left unconnected and must be driven to either VDD or GND.
$\overline{WDO}$	7	O	Watchdog output. Connect $\overline{WDO}$ with a 1-kΩ to 100-kΩ resistor to the correct pullup voltage rail (V_{PU}). $\overline{WDO}$ goes low (asserts) when a watchdog timeout occurs. $\overline{WDO}$ only asserts when $\overline{RESET}$ is high. When a watchdog timeout occurs, $\overline{WDO}$ goes low (asserts) for the set $\overline{RESET}$ timeout delay (t_{RST}). When $\overline{RESET}$ goes low, $\overline{WDO}$ is in a high-impedance state.
Thermal pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage range	VDD	−0.3	7	V
Output voltage range	$\overline{\text{RESET}}$, $\overline{\text{WDO}}$	−0.3	7	V
Voltage ranges	SET1, WDI, $\overline{\text{MR}}$	−0.3	7	V
	CWD	−0.3	V_{DD} + 0.3[2]	
Output pin current	$\overline{\text{RESET}}$, $\overline{\text{WDO}}$		±20	mA
Input current (all pins)			±20	mA
Continuous total power dissipation		See *Thermal Information*		
Temperature	Operating junction, T_J[3]	−40	150	°C
	Operating free-air, T_A[3]	−40	150	
	Storage, T_{stg}	−65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{DD} + 0.3 V or 7.0 V, whichever is smaller.
(3) Assume that $T_J = T_A$ as a result of the low dissipated power in this device.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{DD}	Supply pin voltage	1.6		6.5	V
V_{SET1}	SET1 pin voltage	0		6.5	V
C_{CWD}	Watchdog timing capacitor	0.1[1][2]		1000[1][2]	nF
CWD	Pullup resistor to VDD	9	10	11	kΩ
R_{PU}	Pullup resistor, $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$	1	10	100	kΩ
$I_{\overline{\text{RESET}}}$	$\overline{\text{RESET}}$ pin current			10	mA
$I_{\overline{\text{WDO}}}$	Watchdog output current			10	mA
T_J	Junction temperature	−40		125	°C

(1) Using standard timing with a C_{CWD} capacitor of 0.1 nF or 1000 nF gives a $t_{WD(typ)}$ of 0.704 ms or 3.23 seconds, respectively.
(2) Using extended timing with a C_{CWD} capacitor of 0.1 nF or 1000 nF gives a $t_{WD(typ)}$ of 62.74 ms or 77.45 seconds, respectively.

6.4 Thermal Information

THERMAL METRIC[1]		TPS3851 DRB (VSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at $V_{ITN} + V_{HYST} \leq V_{DD} \leq 6.5$ V over the operating temperature range of –40°C ≤ T_A, T_J ≤ 125°C (unless otherwise noted); the open-drain pullup resistors are 10 kΩ for each output; typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL CHARACTERISTICS						
V_{DD}[1][2][3]	Supply voltage		1.6		6.5	V
I_{DD}	Supply current			10	19	µA
RESET FUNCTION						
V_{POR}[2]	Power-on reset voltage	$I_{\overline{RESET}}$ = 15 µA, $V_{OL(MAX)}$ = 0.25 V			0.8	V
V_{UVLO}[1]	Undervoltage lockout voltage			1.35		V
V_{ITN}	Undervoltage threshold accuracy, entering $\overline{RESET}$	V_{DD} falling	V_{ITN} – 0.8%		V_{ITN} + 0.8%	
V_{HYST}	Hysteresis voltage	V_{DD} rising	0.2%	0.5%	0.8%	
$I_{\overline{MR}}$	$\overline{MR}$ pin internal pullup current	$V_{\overline{MR}}$ = 0 V	500	620	700	nA
WATCHDOG FUNCTION						
I_{CWD}	CWD pin charge current	CWD = 0.5 V	337	375	413	nA
V_{CWD}	CWD pin threshold voltage		1.192	1.21	1.228	V
V_{OL}	$\overline{RESET}$, $\overline{WDO}$ output low	VDD = 5 V, I_{SINK} = 3 mA			0.4	V
I_D	$\overline{RESET}$, $\overline{WDO}$ output leakage current, open-drain	VDD = V_{ITN} + V_{HYST}, $V_{\overline{RESET}}$ = $V_{\overline{WDO}}$ = 6.5 V			1	µA
V_{IL}	Low-level input voltage ($\overline{MR}$, SET1)				0.25	V
V_{IH}	High-level input voltage ($\overline{MR}$, SET1)		0.8			V
$V_{IL(WDI)}$	Low-level input voltage (WDI)				0.3 × V_{DD}	V
$V_{IH(WDI)}$	High-level input voltage (WDI)		0.8 × V_{DD}			V

(1) When V_{DD} falls below V_{UVLO}, $\overline{RESET}$ is driven low.
(2) When V_{DD} falls below V_{POR}, $\overline{RESET}$ and $\overline{WDO}$ are undefined.
(3) During power-on, V_{DD} must be a minimum 1.6 V for at least 300 µs before $\overline{RESET}$ correlates with V_{DD}.
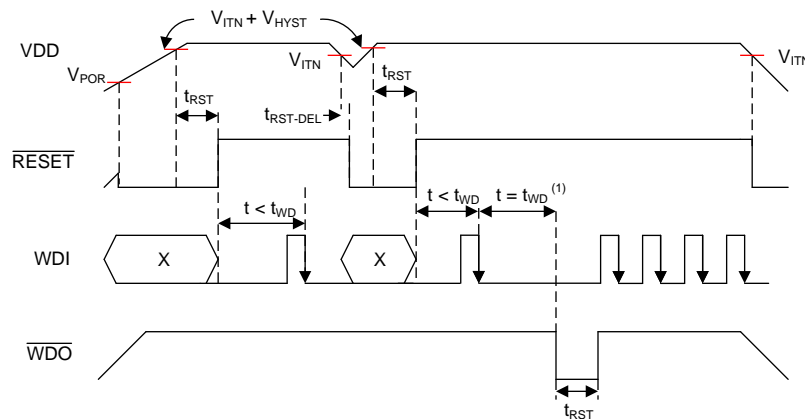
6.6 Timing Requirements

at $V_{ITN} + V_{HYST} \leq V_{DD} \leq 6.5$ V over the operating temperature range of –40°C ≤ T_A, T_J ≤ 125°C (unless otherwise noted); the open-drain pullup resistors are 10 kΩ for each output; typical values are at T_J = 25°C

			MIN	NOM	MAX	UNIT
GENERAL						
t_{INIT}	CWD pin evaluation period			381		µs
	Minimum $\overline{MR}$, SET1 pin pulse duration			1		µs
	Startup delay[1]			300		µs
RESET FUNCTION						
t_{RST}	Reset timeout period		170	200	230	ms
$t_{RST-DEL}$	V_{DD} to $\overline{RESET}$ delay	$V_{DD} = V_{ITN} + V_{HYST} + 2.5\%$		35		µs
		$V_{DD} = V_{ITN} - 2.5\%$		17		
t_{MR-DEL}	$\overline{MR}$ to $\overline{RESET}$ delay			200		ns
WATCHDOG FUNCTION						
t_{WD}	Watchdog timeout[2]	CWD = NC, SET1 = 0[3]	Watchdog disabled			
		CWD = NC, SET1 = 1[3]	1360	1600	1840	ms
		CWD = 10 kΩ to VDD, SET1 = 0[3]	Watchdog disabled			
		CWD = 10 kΩ to VDD, SET1 = 1[3]	170	200	230	ms
$t_{WD-setup}$	Setup time required for device to respond to changes on WDI after being enabled			150		µs
	Minimum WDI pulse duration			50		ns
t_{WD-del}	WDI to $\overline{WDO}$ delay			50		ns

(1) During power-on, V_{DD} must be a minimum 1.6 V for at least 300 µs before $\overline{RESET}$ correlates with V_{DD}.
(2) The fixed watchdog timing covers both standard and extended versions.
(3) SET1 = 0 means $V_{SET1} < V_{IL}$; SET1 = 1 means $V_{SET1} > V_{IH}$.

(1) See 图 2 for WDI timing requirements.
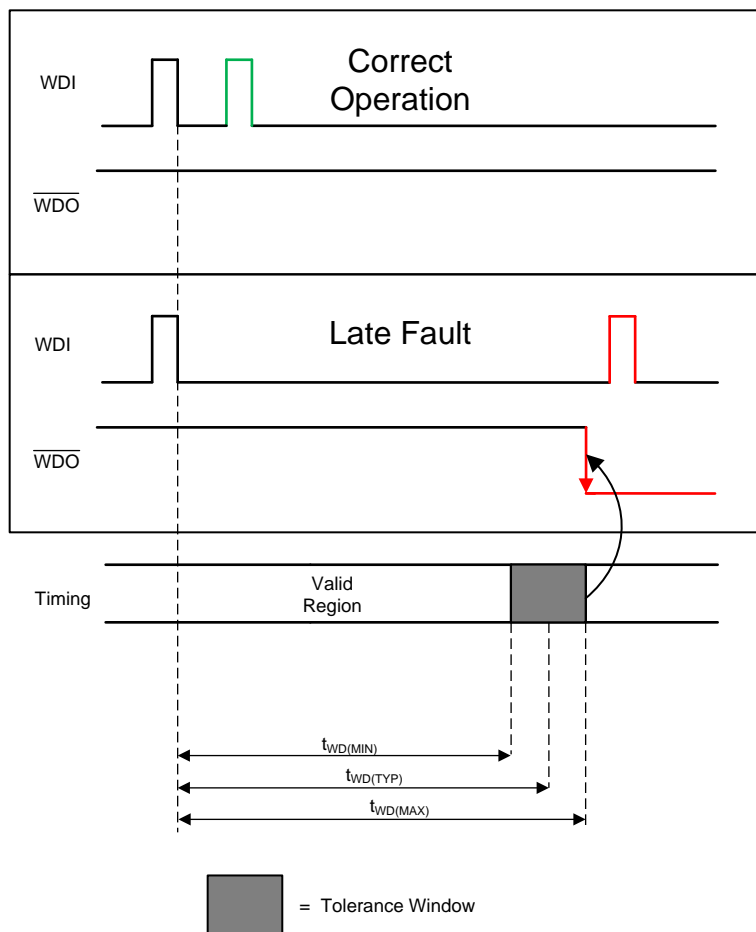
图 1. Timing Diagram

图 **2. Watchdog Timing Diagram**

6.7 Typical Characteristics

all typical characteristics curves are taken at 25°C with 1.6 V ≤ VDD ≤ 6.5 V (unless other wise noted)

图 3. Supply Current vs V_{DD}
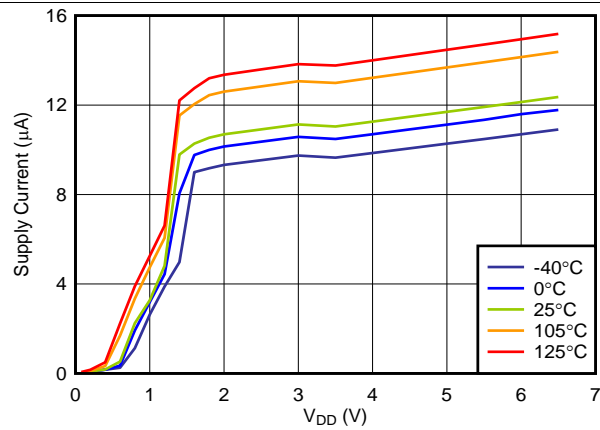

VDD = 1.6 V

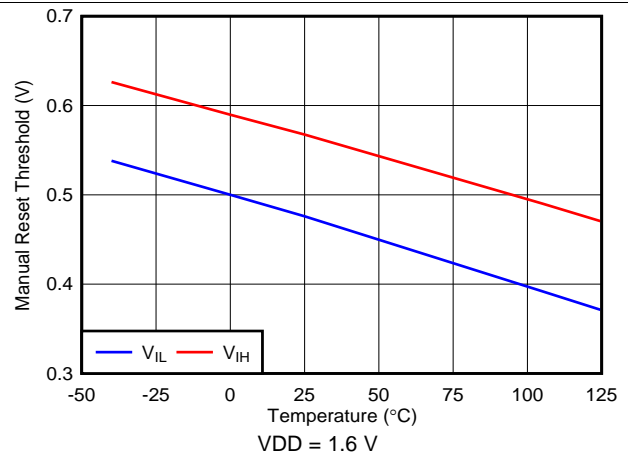**图 4. $\overline{MR}$ Threshold vs Temperature**
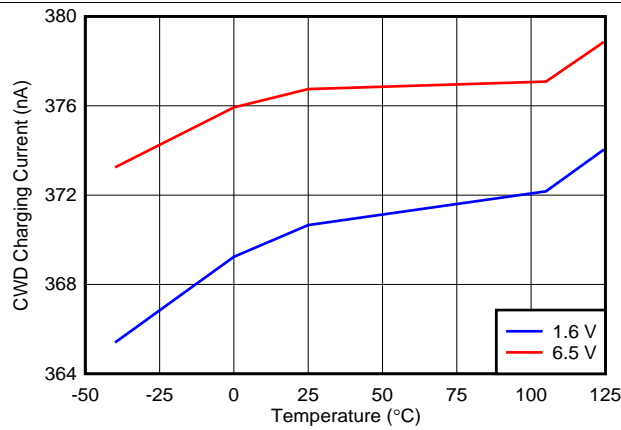
图 5. CWD Charging Current vs Temperature

TPS3851G18, V_{ITN} = 1.728 V

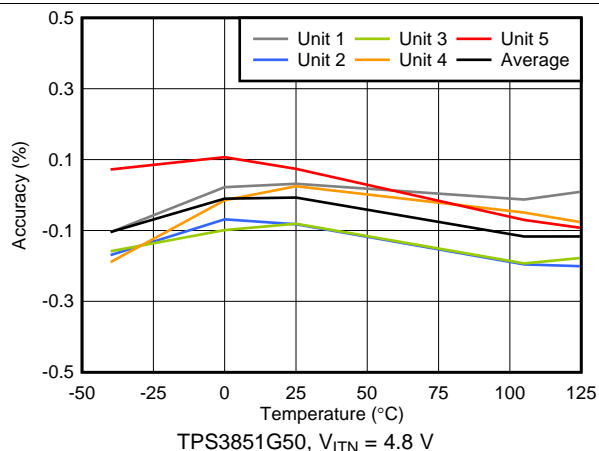**图 6. V_{ITN} + V_{HYST} Accuracy vs Temperature**

TPS3851G18, V_{ITN} = 1.728 V
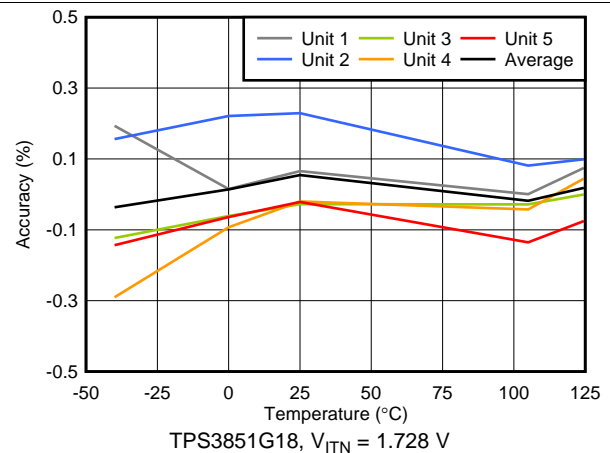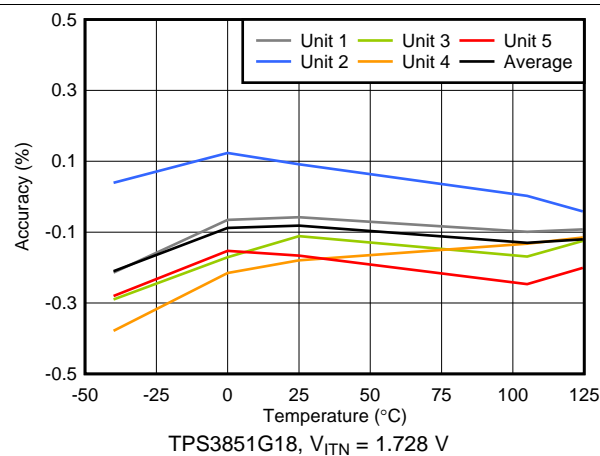
图 7. V_{ITN} Accuracy vs Temperature

TPS3851G50, V_{ITN} = 4.8 V
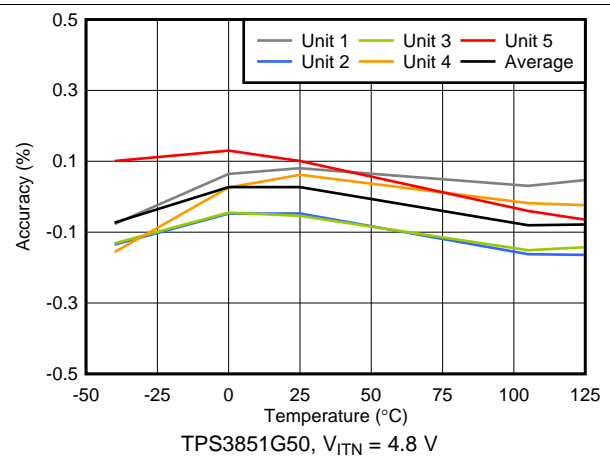
图 8. V_{ITN} + V_{HYST} Accuracy vs Temperature

Typical Characteristics (接下页)

all typical characteristics curves are taken at 25°C with 1.6 V ≤ VDD ≤ 6.5 V (unless other wise noted)

TPS3851G50, V_{ITN} = 4.8 V

图 9. V_{ITN} Accuracy vs Temperature

Includes G and H versions; 1.8-V, 2.5-V, 3.0-V, 3.3-V, and 5-V thresholds; total units = 36,627
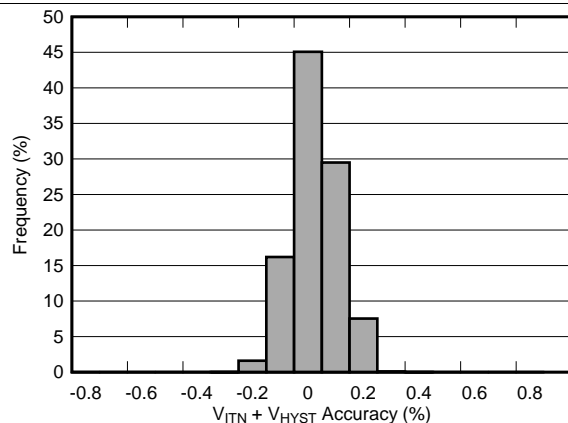
图 10. V_{ITN} + V_{HYST} Accuracy Histogram

Includes G and H versions; 1.8-V, 2.5-V, 3.0-V, 3.3-V, and 5-V thresholds; total units = 36,627
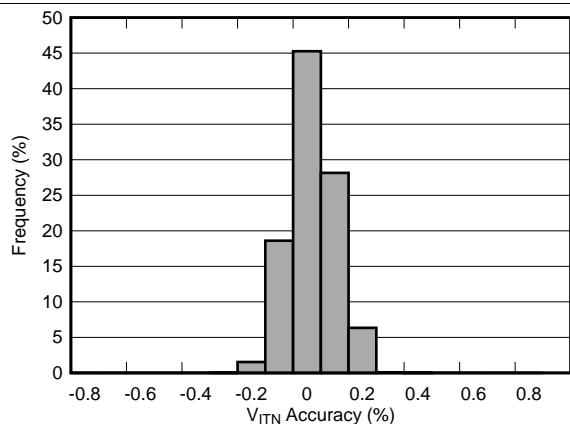
图 11. V_{ITN} Accuracy Histogram

Includes G and H versions; 1.8-V, 2.5-V, 3.0-V, 3.3-V, and 5-V thresholds; total units = 36,627
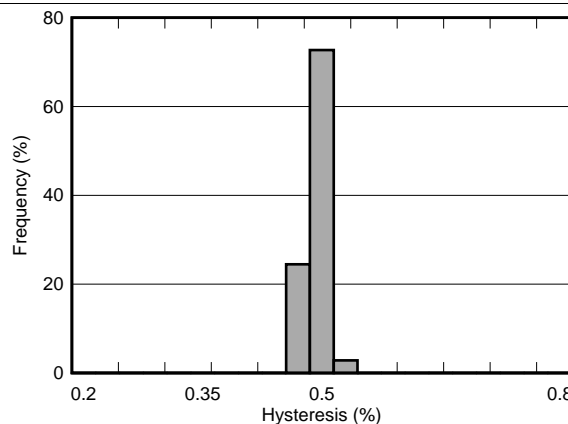
图 12. Hysteresis Histogram

VDD = 1.6 V

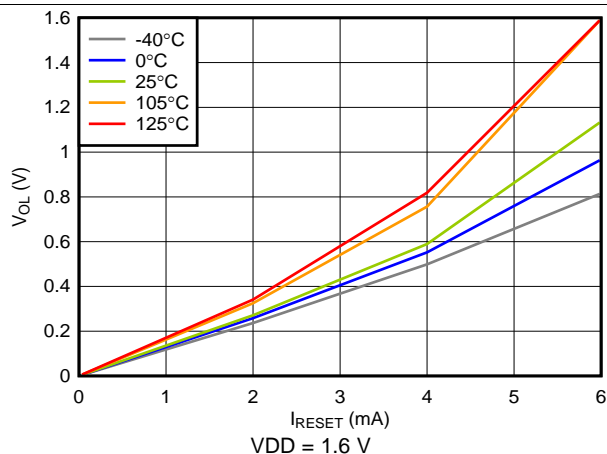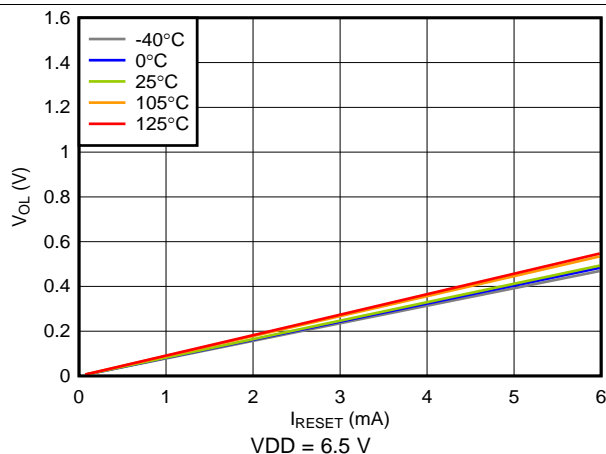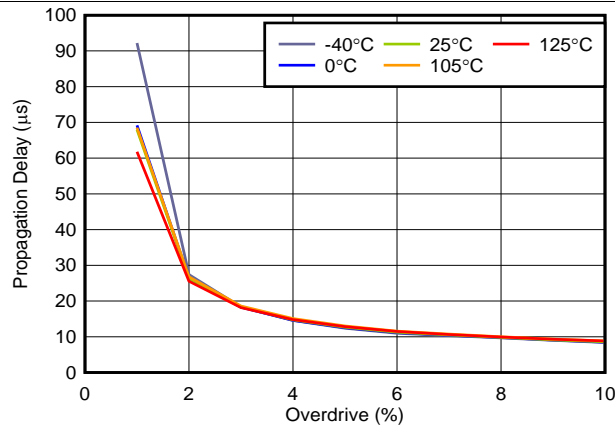**图 13. Low-Level $\overline{RESET}$ Voltage vs $\overline{RESET}$ Current**

VDD = 6.5 V

图 14. Low-Level $\overline{RESET}$ Voltage vs $\overline{RESET}$ Current

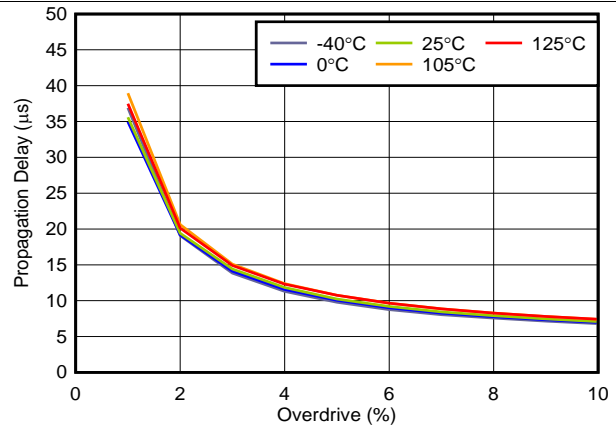## Typical Characteristics (接下页)

all typical characteristics curves are taken at 25°C with 1.6 V ≤ VDD ≤ 6.5 V (unless other wise noted)
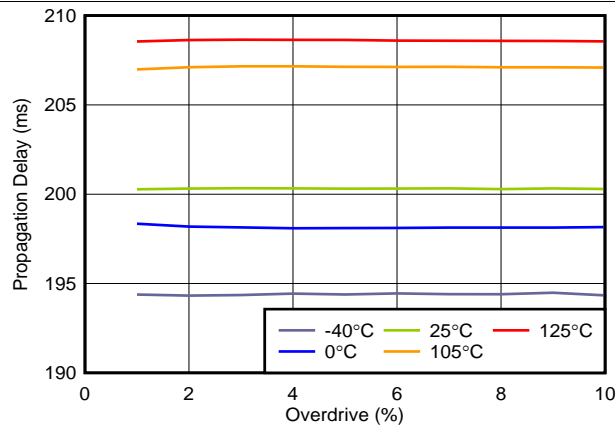

TPS3851G18 entering undervoltage
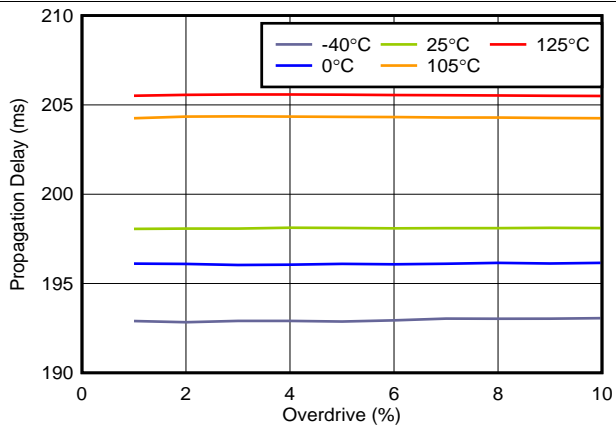
图 15. Propagation Delay vs Overdrive

TPS3851G50 entering undervoltage

图 16. Propagation Delay vs Overdrive

TPS3851G18 exiting undervoltage

图 17. Propagation Delay (t_{RST}) vs Overdrive

TPS3851G50 exiting undervoltage

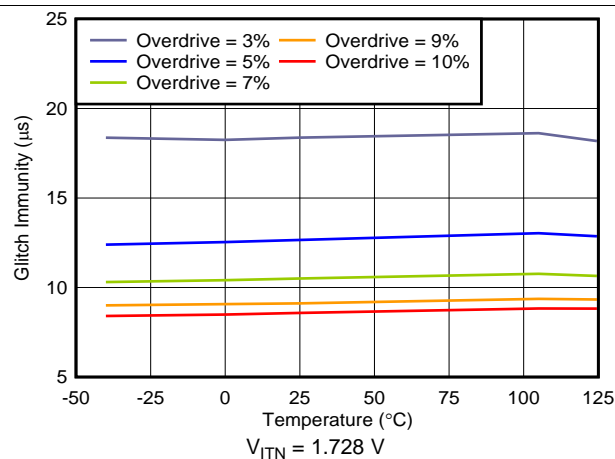图 18. Propagation Delay (t_{RST}) vs Overdrive

V_{ITN} = 1.728 V

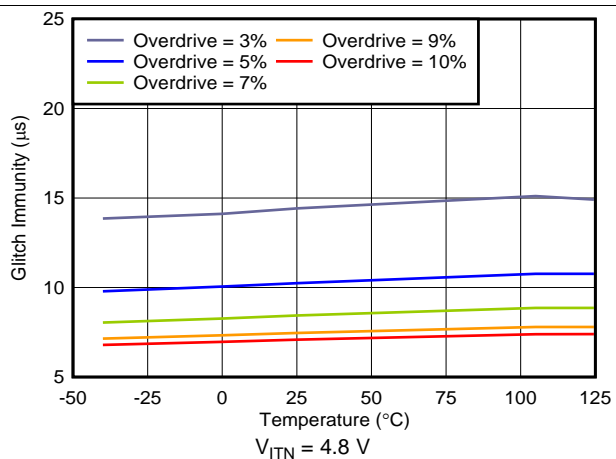图 19. High-to-Low Glitch Immunity vs Temperature

V_{ITN} = 4.8 V

图 20. High-to-Low Glitch Immunity vs Temperature

7 Detailed Description

7.1 Overview

The TPS3851 is a high-accuracy voltage supervisor with an integrated watchdog timer. This device includes a precision undervoltage supervisor with a threshold that achieves 0.8% accuracy over the specified temperature range of –40°C to +125°C. In addition, the TPS3851 includes accurate hysteresis on the threshold, making the device ideal for use with tight tolerance systems where voltage supervisors must ensure a $\overline{\text{RESET}}$ before the minimum supply tolerance of the microprocessor or system-on-a-chip (SoC) is reached. There are two options for the watchdog timing standard and extended timing. To get standard timing use the TPS3851Xyy(y)S, for extended timing use the TPS3851Xyy(y)E.

7.2 Functional Block Diagram

(1)   Note: $R_1 + R_2 = 4.5\ \text{M}\Omega$.

11
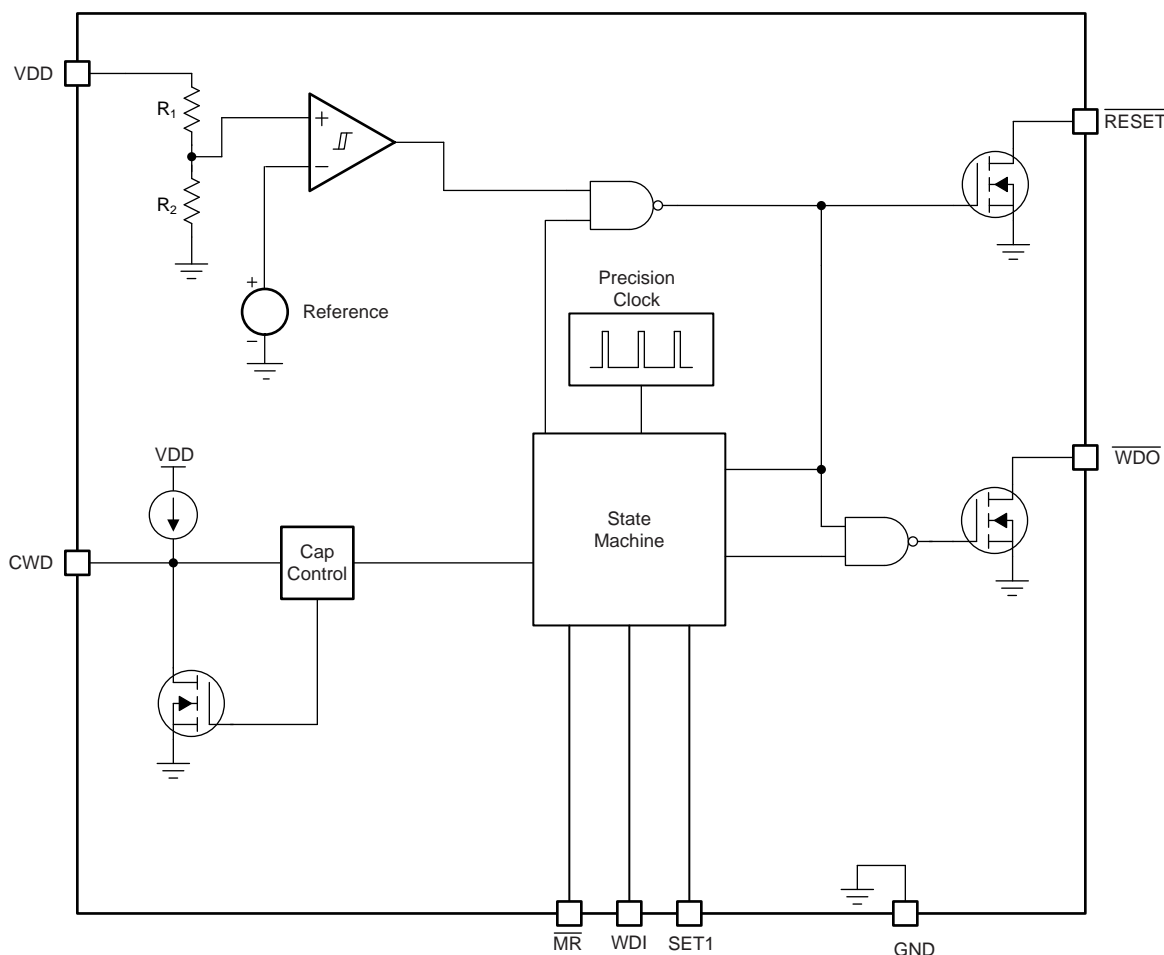
Functional Block Diagram (接下页)

7.2.1 Feature Description

7.2.1.1 $\overline{RESET}$

Connect $\overline{RESET}$ to V_{PU} through a 1-kΩ to 100-kΩ pullup resistor. $\overline{RESET}$ remains high (deasserted) when V_{DD} is greater than the negative threshold voltage (V_{ITN}). If V_{DD} falls below the negative threshold (V_{ITN}), then $\overline{RESET}$ is asserted, driving the $\overline{RESET}$ pin to low impedance. When V_{DD} rises above V_{ITN} + V_{HYST}, a delay circuit is enabled that holds $\overline{RESET}$ low for a specified reset delay period (t_{RST}). When the reset delay has elapsed, the $\overline{RESET}$ pin goes to a high-impedance state and uses a pullup resistor to hold $\overline{RESET}$ high. The pullup resistor must be connected to the proper voltage rail to allow other devices to be connected at the correct interface voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by output logic low voltage (V_{OL}), capacitive loading, leakage current (I_D), and the current through the $\overline{RESET}$ pin $I_{\overline{RESET}}$.

7.2.1.2 Manual Reset $\overline{MR}$

The manual reset ($\overline{MR}$) input allows a processor or other logic circuits to initiate a reset. A logic low on $\overline{MR}$ causes $\overline{RESET}$ to assert. After $\overline{MR}$ returns to a logic high and V_{DD} is above V_{ITN} + V_{HYST}, $\overline{RESET}$ is deasserted after the reset delay time (t_{RST}). If $\overline{MR}$ is not controlled externally, then $\overline{MR}$ can either be connected to V_{DD} or left floating because the $\overline{MR}$ pin is internally pulled up.

7.2.1.3 UV Fault Detection

The TPS3851 features undervoltage detection for common rails between 1.8 V and 5 V. The voltage is monitored on the input rail of the device. If V_{DD} drops below V_{ITN}, then $\overline{RESET}$ is asserted (driven low). When V_{DD} is above V_{ITN} + V_{HYST}, $\overline{RESET}$ deasserts after t_{RST}, as shown in 图 21. The internal comparator has built-in hysteresis that provides some noise immunity and ensures stable operation. Although not required in most cases, for noisy applications, good analog design practice is to place a 1-nF to 100-nF bypass capacitor close to the VDD pin to reduce sensitivity to transient voltages on the monitored signal.
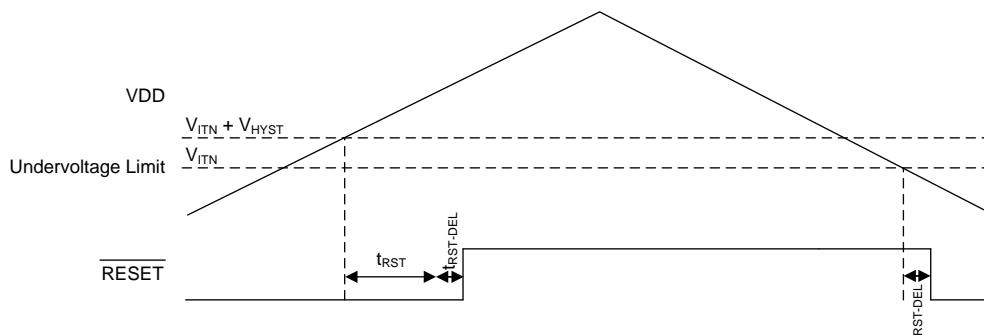

图 21. Undervoltage Detection

7.2.1.4 Watchdog Mode

This section provides information for the watchdog mode of operation.

7.2.1.4.1 CWD

The CWD pin provides the user the functionality of both high-precision, factory-programmed watchdog timing options and user-programmable watchdog timing. The TPS3851 features three options for setting the watchdog timer: connecting a capacitor to the CWD pin, connecting a pullup resistor to VDD, and leaving the CWD pin unconnected. The configuration of the CWD pin is evaluated by the device every time V_{DD} enters the valid region (V_{ITN} + V_{HYST} < V_{DD}). The pin evaluation is controlled by an internal state machine that determines which option is connected to the CWD pin. The sequence of events typically takes 381 μs (t_{INIT}) to determine if the CWD pin is left unconnected, pulled-up through a resistor, or connected to a capacitor. If the CWD pin is being pulled up to VDD, a 10-kΩ resistor is required.

Functional Block Diagram (接下页)

7.2.1.4.2 Watchdog Input WDI

WDI is the watchdog timer input that controls the $\overline{\text{WDO}}$ output. The WDI input is triggered by the falling edge of the input signal. To ensure proper functionality of the watchdog timer, always issue the WDI pulse before $t_{WD(min)}$. If the pulse is issued in this region, then $\overline{\text{WDO}}$ remains unasserted. Otherwise, the device asserts $\overline{\text{WDO}}$, putting the $\overline{\text{WDO}}$ pin into a low-impedance state.

The watchdog input (WDI) is a digital pin. In order to ensure there is no increase in I_{DD}, drive the WDI pin to either VDD or GND at all times. Putting the pin to an intermediate voltage can cause an increase in supply current (I_{DD}) because of the architecture of the digital logic gates. When $\overline{\text{RESET}}$ is asserted, the watchdog is disabled and all signals input to WDI are ignored. When $\overline{\text{RESET}}$ is no longer asserted, the device resumes normal operation and no longer ignores the signal on WDI. If the watchdog is disabled, drive the WDI pin to either VDD or GND. 图 22 shows the valid region for a WDI pulse to be issued to prevent $\overline{\text{WDO}}$ from being triggered and pulled low.
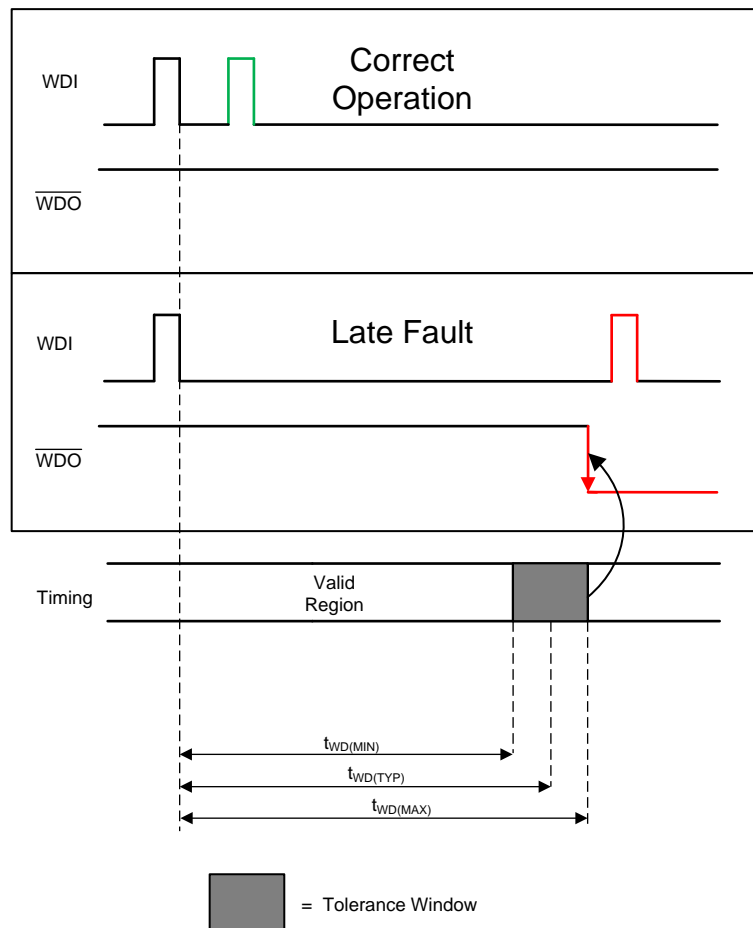

图 22. Watchdog Timing Diagram

7.2.1.4.3 Watchdog Output $\overline{\text{WDO}}$

The TPS3851 features a watchdog timer with an independent watchdog output ($\overline{\text{WDO}}$). The independent watchdog output provides the flexibility to flag a fault in the watchdog timing without performing an entire system reset. When $\overline{\text{RESET}}$ is not asserted (high), the $\overline{\text{WDO}}$ signal maintains normal operation. When asserted, $\overline{\text{WDO}}$ remains low for t_{RST}. When the $\overline{\text{RESET}}$ signal is asserted (low), the $\overline{\text{WDO}}$ pin goes to a high-impedance state. When $\overline{\text{RESET}}$ is unasserted, the watchdog timer resumes normal operation.

Functional Block Diagram (接下页)

7.2.1.4.4 SET1

The SET1 pin can enable and disable the watchdog timer. If SET1 is set to GND, the watchdog timer is disabled and WDI is ignored. If the watchdog timer is disabled, drive the WDI pin to either GND or VDD to ensure that there is no increase in I_{DD}. When SET1 is logic high, the watchdog operates normally. The SET1 pin can be changed dynamically; however, if the watchdog is going from disabled to enabled there is a 150-µs setup time where the watchdog does not respond to changes on WDI, as shown in 图 23.
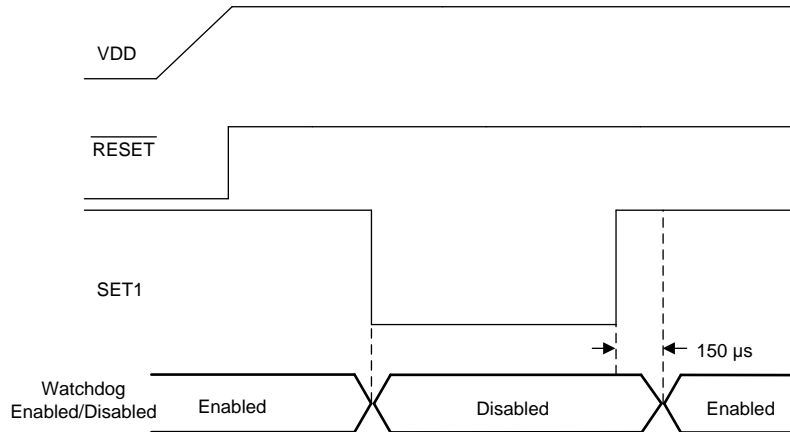

图 23. Enabling and Disabling the Watchdog

7.3 Device Functional Modes

表 1 summarises the functional modes of the TPS3851.

表 1. Device Functional Modes

V_{DD}	WDI	$\overline{WDO}$	$\overline{RESET}$
$V_{DD} < V_{POR}$	---	---	Undefined
$V_{POR} \leq V_{DD} < V_{DD(min)}$	Ignored	High	Low
$V_{DD(min)} \leq V_{DD} \leq V_{ITN} + V_{HYST}$[1]	Ignored	High	Low
$V_{DD} > V_{ITN}$[2]	$t_{PULSE} < t_{WD(min)}$[3]	High	High
$V_{DD} > V_{ITN}$[2]	$t_{PULSE} > t_{WD(min)}$[3]	Low	High

(1) Only valid before V_{DD} has gone above $V_{ITN} + V_{HYST}$.
(2) Only valid after V_{DD} has gone above $V_{ITN} + V_{HYST}$.
(3) Where t_{pulse} is the time between the falling edges on WDI.

7.3.1 V_{DD} is Below V_{POR} ($V_{DD} < V_{POR}$)

When V_{DD} is less than V_{POR}, $\overline{RESET}$ is undefined and can be either high or low. The state of $\overline{RESET}$ largely depends on the load that the $\overline{RESET}$ pin is experiencing.

7.3.2 Above Power-On-Reset, But Less Than $V_{DD(min)}$ ($V_{POR} \leq V_{DD} < V_{DD(min)}$)

When the voltage on V_{DD} is less than $V_{DD(min)}$, and greater than or equal to V_{POR}, the $\overline{RESET}$ signal is asserted (logic low). When $\overline{RESET}$ is asserted, the watchdog output $\overline{WDO}$ is in a high-impedance state regardless of the WDI signal that is input to the device.

7.3.3 Normal Operation ($V_{DD} \geq V_{DD(min)}$)

When V_{DD} is greater than or equal to $V_{DD(min)}$, the $\overline{RESET}$ signal is determined by V_{DD}. When $\overline{RESET}$ is asserted, $\overline{WDO}$ goes to a high-impedance state. WDO is then pulled high through the pullup resistor.

8 Application and Implementation

> 注
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

8.1.1 CWD Functionality

The TPS3851 features three options for setting the watchdog timer: connecting a capacitor to the CWD pin, connecting a pullup resistor to VDD, and leaving the CWD pin unconnected. 图 24 shows a schematic drawing of all three options. If this pin is connected to VDD through a 10-kΩ pullup resistor or left unconnected (high impedance), then the factory-programmed watchdog timeouts are enabled; see the *Factory-Programmed Timing Options* section. Otherwise, the watchdog timeout can be adjusted by placing a capacitor from the CWD pin to ground.
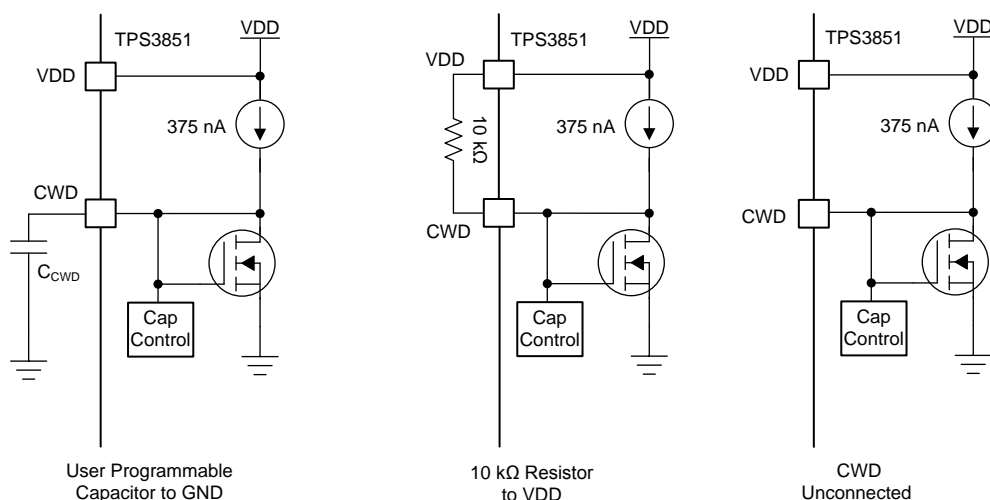

图 24. CWD Charging Circuit

8.1.1.1 Factory-Programmed Timing Options

If using the factory-programmed timing options (listed in 表 2), the CWD pin must either be unconnected or pulled up to VDD through a 10-kΩ pullup resistor. Using these options enables high-precision, 15% accurate watchdog timing.

表 2. Factory Programmed Watchdog Timing

INPUT		STANDARD AND EXTENDED TIMING WDT (t_{WD})			UNIT
CWD	**SET1**	**MIN**	**TYP**	**MAX**	
NC	0	Watchdog disabled			
NC	1	1360	1600	1840	ms
10 kΩ to VDD	0	Watchdog disabled			
10 kΩ to VDD	1	170	200	230	ms

Application Information (接下页)

8.1.1.2 Adjustable Capacitor Timing

Adjustable capacitor timing is achievable by connecting a capacitor to the CWD pin. If a capacitor is connected to CWD, then a 375-nA, constant-current source charges C_{CWD} until V_{CWD} = 1.21 V. 表 3 shows how to calculate t_{WD} using 公式 1 and 公式 2 and the SET1 pin. The TPS3851 determines the watchdog timeout with the formulas given in 公式 1 and 公式 2, where C_{CWD} is in nanofarads and t_{WD} is in milliseconds.

$$t_{WD(standard)} \text{ (ms)} = 3.23 \times C_{CWD} \text{ (nF)} + 0.381 \text{ (ms)} \tag{1}$$

$$t_{WD(extended)} \text{(ms)} = 77.4 \times C_{CWD} \text{(nF)} + 55 \text{ (ms)} \tag{2}$$

The TPS3851 is designed and tested using C_{CWD} capacitors between 100 pF and 1 μF. Note that 公式 1 and 公式 2 are for ideal capacitors, capacitor tolerances vary the actual device timing. For the most accurate timing, use ceramic capacitors with COG dielectric material. If a C_{CWD} capacitor is used, 公式 1 can be used to set t_{WD} for standard timing. Use 公式 2 to calculate t_{WD} for extended timing. 表 4 shows the minimum and maximum calculated t_{WD} values using an ideal capacitor for both the standard and extended timing.

表 3. Programmable CWD Timing

INPUT		STANDARD TIMING WDT (t_{WD})			EXTENDED TIMING WDT (t_{WD})			UNIT
CWD	SET1	MIN	TYP	MAX	MIN	TYP	MAX	
C_{CWD}	0	Watchdog disabled			Watchdog disabled			
C_{CWD}	1	$t_{WD(std)}$ × 0.85	$t_{WD(std)}$[1]	$t_{WD(std)}$ × 1.15	$t_{WD(ext)}$ × 0.85	$t_{WD(ext)}$[2]	$t_{WD(ext)}$ × 1.15	ms

(1) Calculated from 公式 1 using an ideal capacitor.
(2) Calculated from 公式 2 using an ideal capacitor.

表 4. t_{WD} Values for Common Ideal Capacitor Values

C_{CWD}	STANDARD TIMING WDT (t_{WD})			EXTENDED TIMING WDT (t_{WD})			UNIT
	MIN[1]	TYP	MAX[1]	MIN[1]	TYP	MAX[1]	
100 pF	0.598	0.704	0.809	53.33	62.74	72.15	ms
1 nF	3.069	3.611	4.153	112.5	132.4	152.3	ms
10 nF	27.78	32.68	37.58	704.7	829	953.4	ms
100 nF	274.9	323.4	371.9	6626	7795	8964	ms
1 μF	2746	3230	3715	65837	77455	89073	ms

(1) The minimum and maximum values are calculated using an ideal capacitor.

8.1.2 Overdrive Voltage

Forcing a $\overline{\text{RESET}}$ is dependent on two conditions: the amplitude V_{DD} is beyond the trip point (ΔV_1 and ΔV_2), and the length of time that the voltage is beyond the trip point (t_1 and t_2). If the voltage is just under the trip point for a long period of time, $\overline{\text{RESET}}$ asserts and the output is pulled low. However, if V_{DD} is just under the trip point for a few nanoseconds, $\overline{\text{RESET}}$ does not assert and the output remains high. The length of time required for $\overline{\text{RESET}}$ to assert can be changed by increasing the amount V_{DD} goes under the trip point. If V_{DD} is under the trip point by 10%, the amount of time required for the comparator to respond is much faster and causes $\overline{\text{RESET}}$ to assert much quicker than when barely under the trip point voltage. 公式 3 shows how to calculate the percentage overdrive.

$$\text{Overdrive} = |(V_{DD} / V_{ITX} - 1) \times 100\% | \tag{3}$$

In 公式 3, V_{ITX} corresponds to the threshold trip point. If V_{DD} is exceeding the positive threshold, $V_{ITN} + V_{HYST}$ is used. V_{ITN} is used when V_{DD} is falling below the negative threshold. In 图 25, t_1 and t_2 correspond to the amount of time that V_{DD} is over the threshold; the propagation delay versus overdrive for V_{ITN} and $V_{ITN} + V_{HYST}$ is illustrated in 图 16 and 图 18, respectively.

The TPS3851 is relatively immune to short positive and negative transients on VDD because of the overdrive voltage curve.
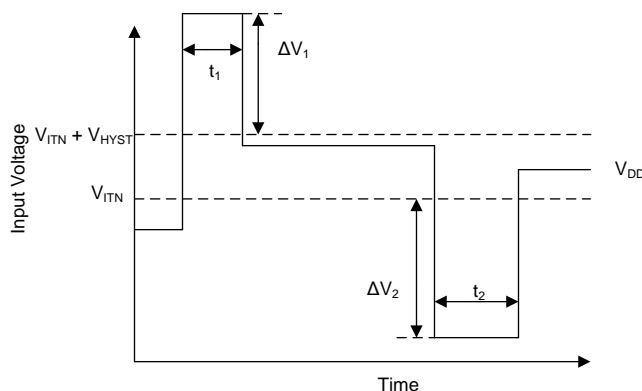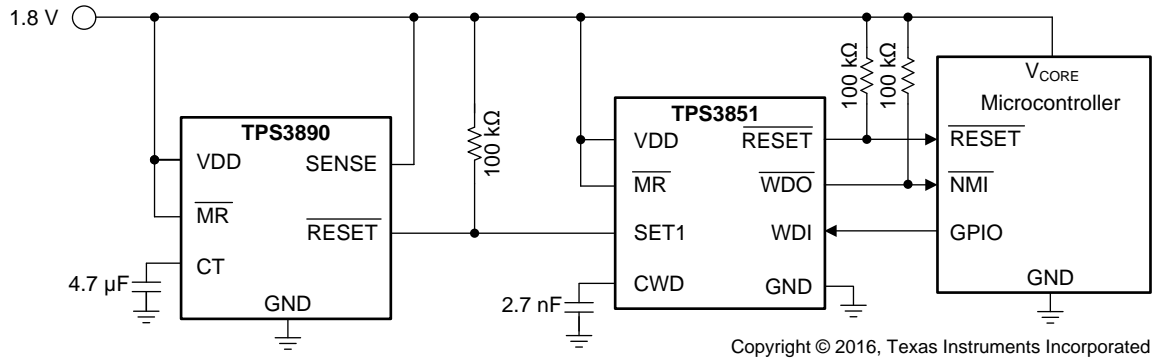

图 25. Overdrive Voltage

8.2 Typical Application

图 26. **Monitoring the Supply Voltage and Watchdog Supervision of a Microcontroller**

8.2.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Watchdog disable for initialization period	Watchdog must remain disabled for 5 seconds until logic enables the watchdog timer	5.02 seconds (typ)
Output logic voltage	1.8-V CMOS	1.8V CMOS
Monitored rail	1.8 V with a 5% threshold	Worst-case V_{ITN} = 1.714 V – 4.7%
Watchdog timeout	10 ms typical	$t_{WD(min)}$ = 7.3 ms, $t_{WD(TYP)}$ = 9.1 ms, $t_{WD(max)}$ = 11 ms
Maximum device current consumption	50 µA	37 µA when $\overline{RESET}$ or $\overline{WDO}$ is asserted[1]

(1)   Only includes the TPS3851G18S current consumption.

8.2.2 Detailed Design Procedure

8.2.2.1 Monitoring the 1.8-V Rail

The undervoltage comparator allows for precise voltage supervision of common rails between 1.8 V and 5.0 V. This application calls for very tight monitoring of the rail with only 5% of variation allowed on the rail. To ensure this requirement is met, the TPS3851G18S was chosen for its –4% threshold. To calculate the worst-case for V_{ITN}, the accuracy must also be taken into account. The worst-case for V_{ITN} can be calculated by 公式 4:

$$V_{ITN(Worst\ Case)} = V_{ITN(typ)} \text{ x } 0.992 = 1.8 \text{ x } 0.96 \text{ x } 0.992 = 1.714 \text{ V} \tag{4}$$

8.2.2.2 Calculating $\overline{RESET}$ and $\overline{WDO}$ Pullup Resistor

The TPS3851 uses an open-drain configuration for the $\overline{RESET}$ circuit, as shown in 图 27. When the FET is off, the resistor pulls the drain of the transistor to VDD and when the FET is turned on, the FET attempts to pull the drain to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that V_{OL} is below the maximum value. To choose the proper pullup resistor, there are three key specifications to keep in mind: the pullup voltage (V_{PU}), the recommended maximum $\overline{RESET}$ pin current ($I_{\overline{RESET}}$), and V_{OL}. The maximum V_{OL} is 0.4 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.4 V with $I_{\overline{RESET}}$ kept below 10 mA. For this example, with a V_{PU} of 1.8 V, a resistor must be chosen to keep $I_{\overline{RESET}}$ below 50 μA because this value is the maximum consumption current allowed. To ensure this specification is met, a pullup resistor value of 100 kΩ was selected, which sinks a maximum of 18 μA when $\overline{RESET}$ or $\overline{WDO}$ is asserted. As illustrated in 图 13, the $\overline{RESET}$ current is at 18 μA and the low-level output voltage is approximately zero.
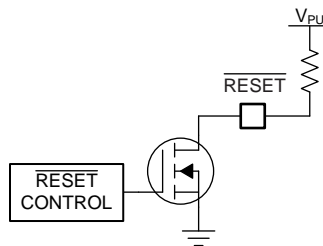

图 27. $\overline{RESET}$ Open-Drain Configuration

8.2.2.3 Setting the Watchdog

As illustrated in 图 24 there are three options for setting the watchdog timer. The design specifications in this application require the programmable timing option (external capacitor connected to CWD). When a capacitor is connected to the CWD pin, the watchdog timer is governed by 公式 1 for the standard timing version. Note that only the standard version is capable of meeting this timing requirement. 公式 1 is only valid for ideal capacitors, any temperature or voltage derating must be accounted for separately.

$$C_{CWD} \text{ (nF)} = (t_{WD}\text{(ms)} - 0.0381) / 3.23 = (10 - 0.381) / 3.23 = 2.97 \text{ nF} \tag{5}$$

The nearest standard capacitor value to 2.9 nF is 2.7 nF. Selecting 2.7 nF for the C_{CWD} capacitor gives the following minimum timing parameters:

$$t_{WD(MIN)} = 0.85 \times t_{WD(TYP)} = 0.85 \times (3.23 \times 2.7 + 0.381) = 7.73 \text{ ms} \tag{6}$$

$$t_{WD(MAX)} = 1.15 \times t_{WD(TYP)} = 1.15 \times (3.23 \times 2.7 + 0.381) = 10.46 \text{ ms} \tag{7}$$

Capacitor tolerance also influences $t_{WD(MIN)}$ and $t_{WD(MAX)}$. Select a ceramic COG dielectric capacitor for high accuracy. For 2.7 nF, COG capacitors are readily available with 5% tolerances. This selection results in a 5% decrease in $t_{WD(MIN)}$ and a 5% increase in $t_{WD(MAX)}$, giving 7.34 ms and 11 ms, respectively. To ensure proper functionality, a falling edge must be issued before $t_{WD(min)}$. 图 29 illustrates that a WDI signal with a period of 5 ms keeps $\overline{WDO}$ from asserting.

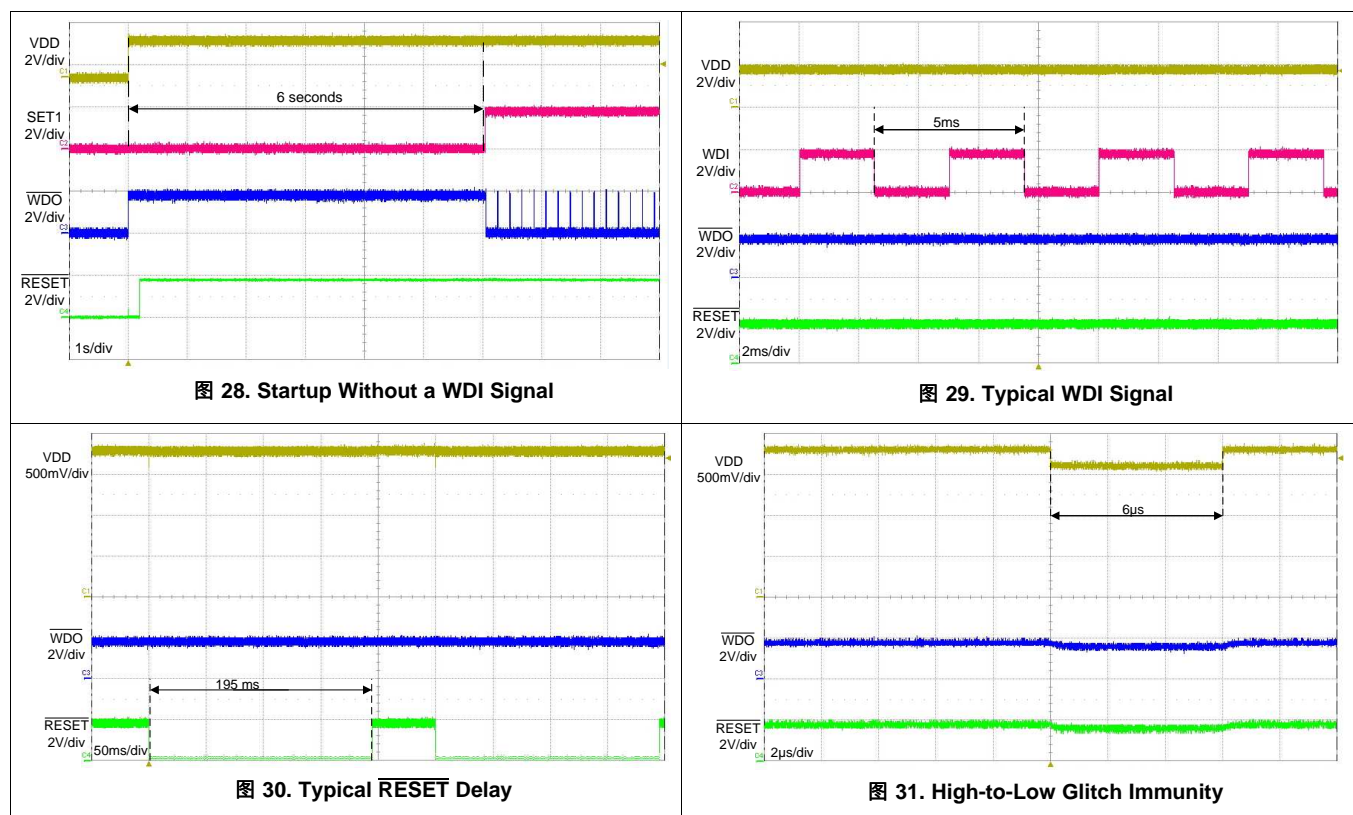### 8.2.2.4 *Watchdog Disabled During Initialization Period*

The watchdog is often needed to be disabled during startup to allow for an initialization period. When the initialization period is over, the watchdog timer is turned back on to allow the microcontroller to be monitored by the TPS3851. To achieve this setup, SET1 must start at GND. In this design, SET1 is controlled by a TPS3890 supervisor. In this application, the TPS3890 was chosen to monitor VDD as well, which means that the $\overline{\text{RESET}}$ on the TPS3890 stays low until V_{DD} rises above V_{ITN}. When VDD comes up, the delay time can be adjusted through the CT capacitor on the TPS3890. With this approach, the $\overline{\text{RESET}}$ delay can be adjusted from a minimum of 25 µs to a maximum of 30 seconds. For this design, a typical delay of 5 seconds is needed before the watchdog timer is enabled. The CT capacitor calculation (see the TPS3890 data sheet) yields an ideal capacitance of 4.67 µF, giving a closest standard ceramic capacitor value of 4.7 µF. When connecting a 4.7-µF capacitor from CT to GND, the typical delay time is 5 seconds. 图 28 shows that when the watchdog is disabled, the $\overline{\text{WDO}}$ output remains high. However when SET1 goes high and there is no WDI signal, $\overline{\text{WDO}}$ begins to assert. See the TPS3890 data sheet for detailed information on the TPS3890.

8.2.3 Glitch Immunity

图 31 shows the high-to-low glitch immunity for the TPS3851G18S with a 7% overdrive with V_{DD} starting at 1.8 V. This curve shows that V_{DD} can go below the threshold for at least 6 µs before $\overline{\text{RESET}}$ asserts.

8.2.4 Application Curves

Unless otherwise stated, application curves were taken at T_A = 25°C.

图 28. Startup Without a WDI Signal

图 29. Typical WDI Signal

图 30. Typical $\overline{\text{RESET}}$ Delay

图 31. High-to-Low Glitch Immunity

9 Power Supply Recommendations

This device is designed to operate from an input supply with a voltage range between 1.6 V and 6.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin.

10 Layout

10.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-µF ceramic capacitor as near as possible to the VDD pin.
- If a C_{CWD} capacitor or pullup resistor is used, place these components as close as possible to the CWD pin. If the CWD pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin.
- Place the pullup resistors on $\overline{RESET}$ and $\overline{WDO}$ as close to the pin as possible.
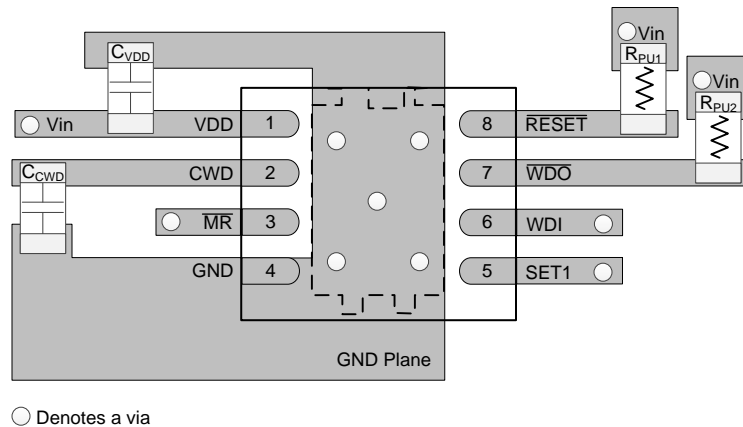
10.2 Layout Example

○ Denotes a via

图 32. TPS3851 Recommended Layout

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

表 **5.** 器件命名规则

说明	命名规则	值
TPS3851 （具有看门狗的高精度监控器）	—	—
X （标称阈值，受监视电压标称值的百分比）	G	V_{ITN} = –4%
	H	V_{ITN} = -7%
yy(y) （受监视电压标称值选项）	18	1.8V
	25	2.5V
	30	3.0V
	33	3.3V
	50	5.0V
z （看门狗超时周期标称值）	S	t_{WD} (ms) = 3.23 x C_{WD} (nF) + 0.381 (ms)
	E	t_{WD} (ms) = 77.4 x C_{WD} (nF) + 55.2 (ms)

11.2 文档支持

11.2.1 相关文档

相关文档如下：
- 《*TPS3890 延迟可编程的低静态电流、1% 精密监控器*》（文献编号：SLVSD65）
- 《*TPS3851EVM-780 评估模块*》（文献编号：SBVU033）

11.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

TPS3851

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

产品		应用	
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3851G18EDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851DD	Samples
TPS3851G18EDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851DD	Samples
TPS3851G18SDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851DC	Samples
TPS3851G18SDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851DC	Samples
TPS3851G25EDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851ED	Samples
TPS3851G25EDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851ED	Samples
TPS3851G30EDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851FD	Samples
TPS3851G30EDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851FD	Samples
TPS3851G33EDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851GD	Samples
TPS3851G33EDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851GD	Samples
TPS3851G33SDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851GC	Samples
TPS3851G33SDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851GC	Samples
TPS3851G50EDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851HD	Samples
TPS3851G50EDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851HD	Samples
TPS3851G50SDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851HC	Samples
TPS3851G50SDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851HC	Samples
TPS3851H18EDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851LD	Samples
TPS3851H18EDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851LD	Samples
TPS3851H25EDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851MD	Samples
TPS3851H25EDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851MD	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3851H30EDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851ND	Samples
TPS3851H30EDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851ND	Samples
TPS3851H33EDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851PD	Samples
TPS3851H33EDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851PD	Samples
TPS3851H50EDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851RD	Samples
TPS3851H50EDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	851RD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

Images above are just a representation of the package family, actual package may vary.
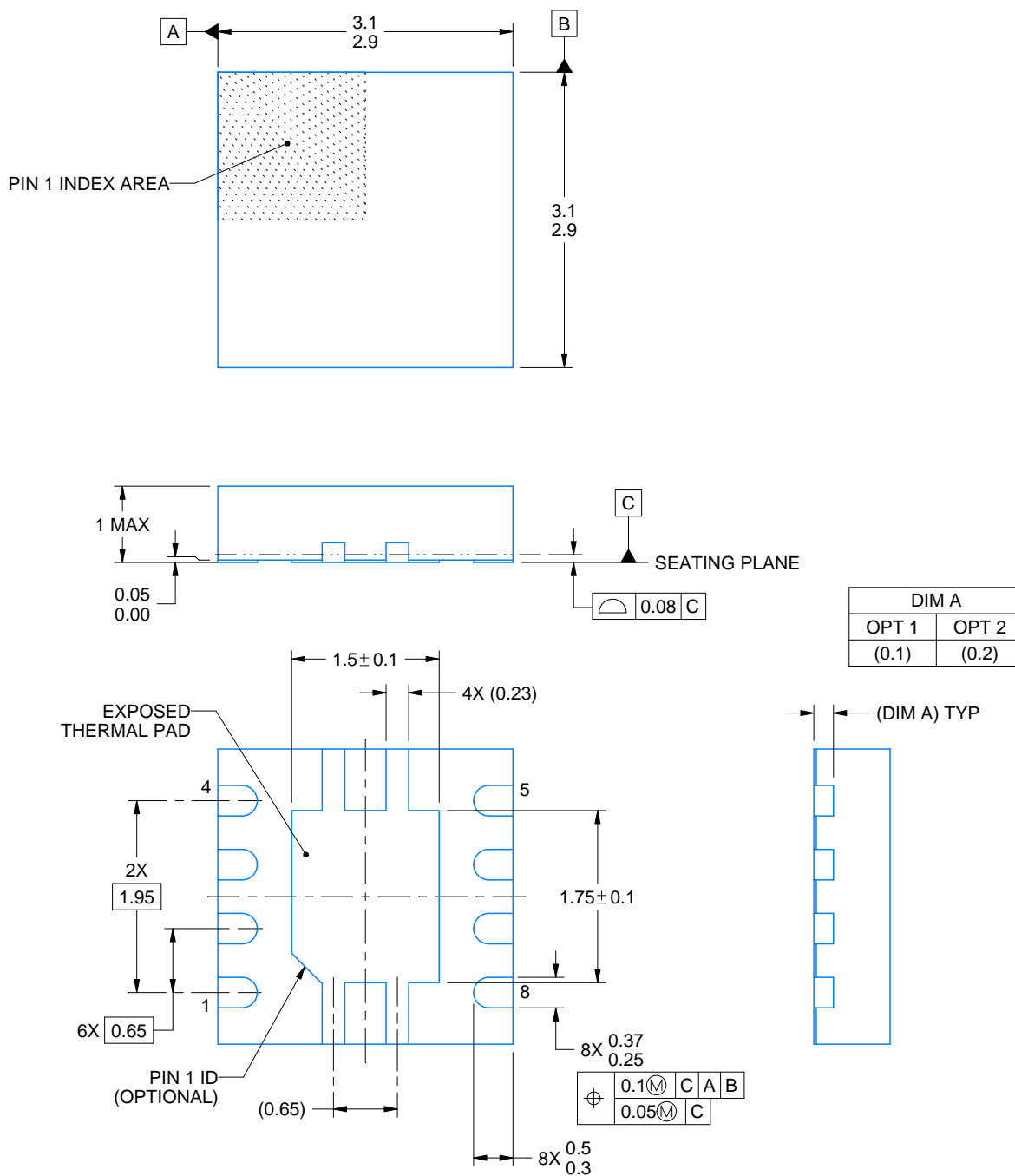Refer to the product data sheet for package details.

4203482/L

A | 3.1 / 2.9 | B

PIN 1 INDEX AREA

3.1 / 2.9

1 MAX

0.05 / 0.00

C

SEATING PLANE

⌒ 0.08 C

DIM A	
OPT 1	OPT 2
(0.1)	(0.2)

1.5 ± 0.1

4X (0.23)

EXPOSED THERMAL PAD

4

5

2X 1.95

1.75 ± 0.1

1

8

6X 0.65

8X 0.37 / 0.25

PIN 1 ID (OPTIONAL)

(0.65)

(DIM A) TYP

⊕ | 0.1 Ⓜ | C | A | B
0.05 Ⓜ | C

8X 0.5 / 0.3

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
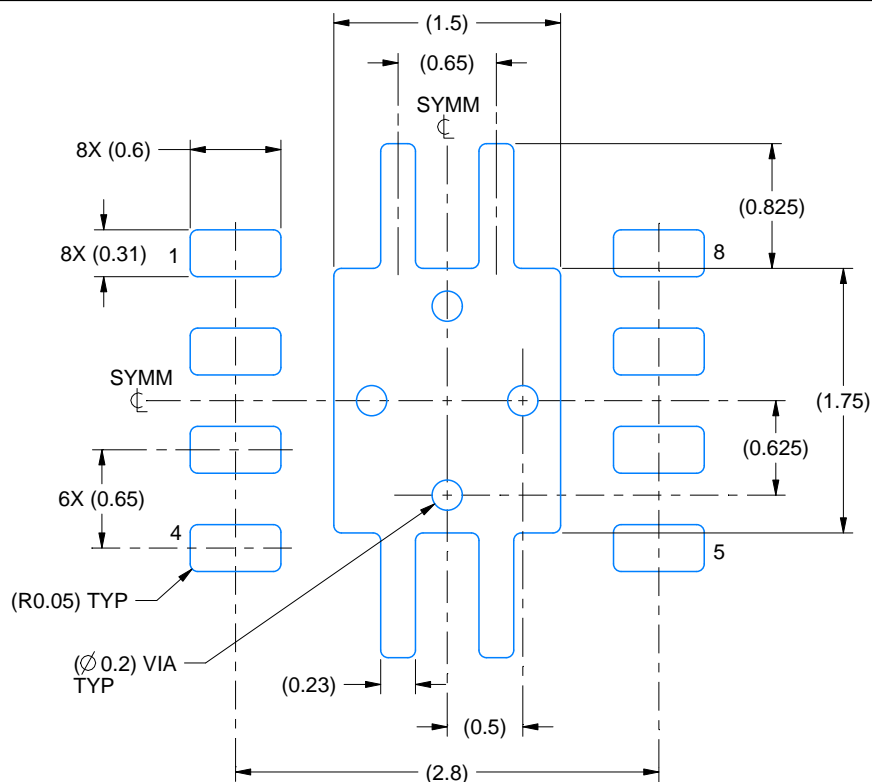
LAND PATTERN EXAMPLE
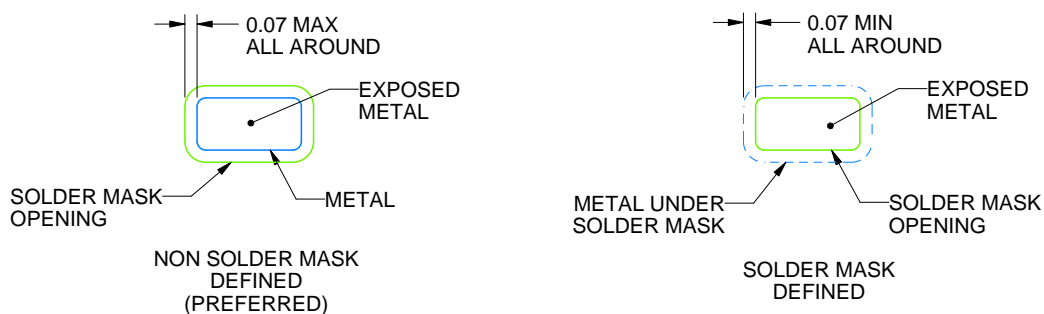EXPOSED METAL SHOWN
SCALE:20X

0.07 MAX
ALL AROUND

EXPOSED
METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

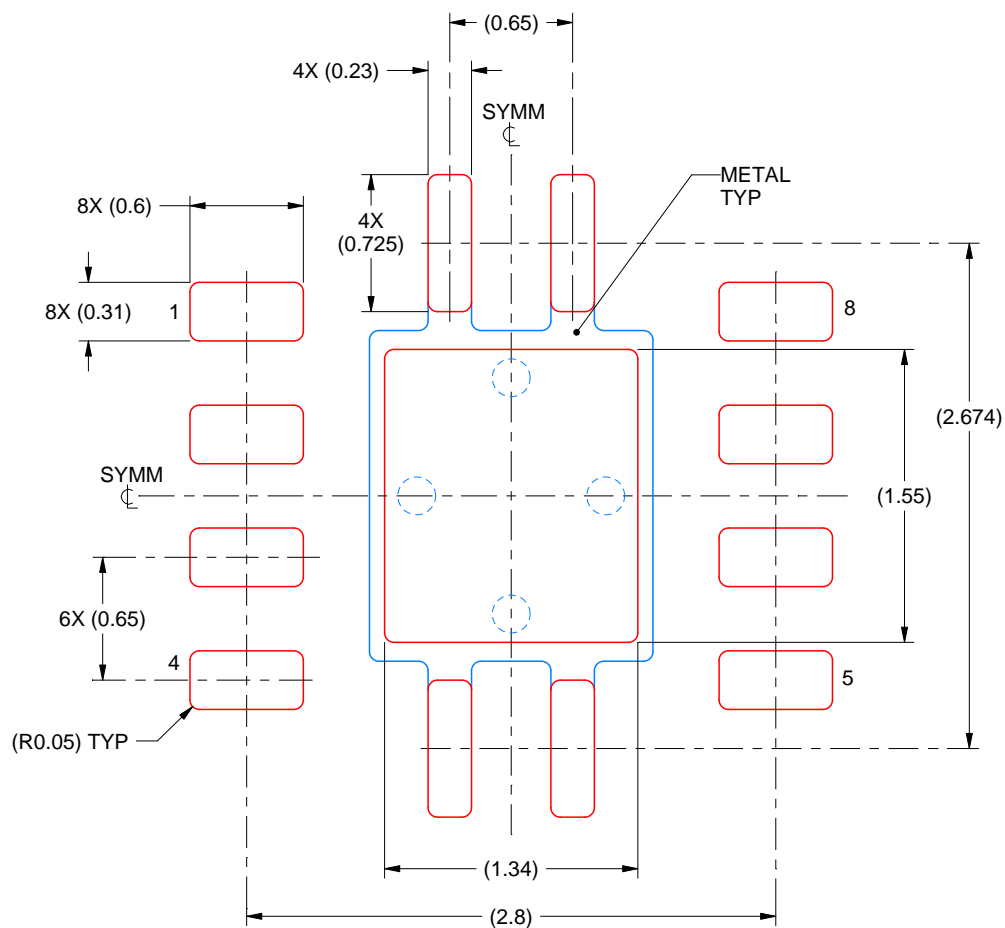SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

SYMM

(0.65)

4X (0.23)

4X
(0.725)

METAL
TYP

8X (0.6)

8X (0.31)   1

8

SYMM

(2.674)

(1.55)

6X (0.65)

4

5

(R0.05) TYP

(1.34)

(2.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.