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TEXAS INSTRUMENTS

TL7700-SEP
ZHCSJJ4 – MARCH 2019

采用增强型航天塑料的 **TL7700-SEP** 耐辐射电源电压监控器

1 特性

- VID V62/19602
- 耐辐射
  - 单粒子锁定 (SEL) 在 125°C 下的抗扰度可达 $43MeV\text{-}cm^2/mg$
  - 每个晶圆批次的 RLAT 总电离剂量 (TID) 高达 20krad(Si)
- 增强型航天塑料
  - 受控基线
  - 金线
  - NiPdAu 铅涂层
  - 一个组装和测试基地
  - 一个制造基地
  - 支持军用（–55°C 至 125°C）温度范围
  - 延长了产品生命周期
  - 延长了产品变更通知
  - 产品可追溯性
  - 采用增强型模塑化合物实现低释气
- 可通过两个外部电阻器来调节检测电压
- 1.0% 检测电压容差 (25°C)
- 可调节检测电压的迟滞
- 宽工作电源电压范围：
  1.8V 至 40V
- 低功耗：
  I_{CC} = 0.6mA（典型值），V_{CC} = 40V

2 应用

- 支持近地球轨道空间 应用
- 适用于卫星的电源监控器
- 监控 DPS、MCU、FPGA 和 ASIC

3 说明

TL7700-SEP 是一款专为用作微型计算机和微处理器系统中的复位控制器而设计的双极集成电路。使用两个外部电阻器可将检测电压设置为大于 0.5V 的任何值。

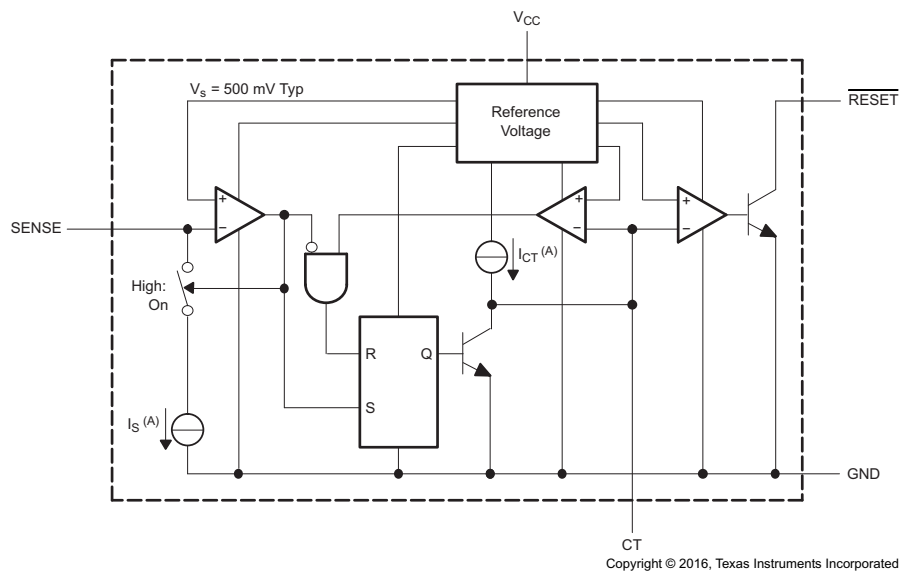电路功能非常稳定，电源电压范围为 1.8V 至 40V。由于具有最小电源电流，因此该产品可用于交流线路供电型应用、便携式电池供电型应用和汽车 应用。TL7700-SEP 器件的设计工作温度范围是 –55°C 至 125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
V62/19602	TSSOP (8)	3.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

功能方框图

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目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 3 月	*	初始发行版。

5 Pin Configuration and Functions

**PW Package
8-Pin TSSOP
Top View**

```
      CT [ 1    8 ] RESET
   SENSE [ 2    7 ] NC
      NC [ 3    6 ] NC
     GND [ 4    5 ] VCC
```
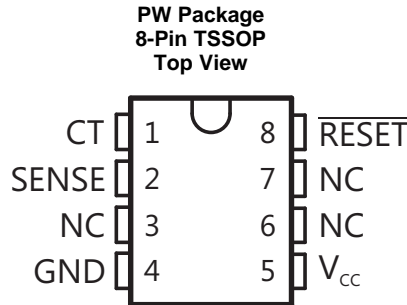
NC – No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CT	1	I/O	Timing capacitor connection. This terminal sets the RESET output pulse duration (t_{po}). It is connected internally to a 15-µA constant-current source. There is a limit on the switching speed of internal elements; even if CT is set to 0, response speeds remain at approximately 5 to 10 µs. If CT is open, the device can be used as an adjustable-threshold noninverting comparator. If CT is low, the internal output-stage comparator is active, and the RESET output transistor is on. An external voltage must not be applied to this terminal due to the internal structure of the device. Therefore, drive the device using an open-collector transistor, FET, or 3-state buffer (in the low-level or high-impedance state).
GND	4	—	Ground Keep this terminal as low impedance as possible to reduce circuit noise.
NC	3, 6, 7	—	No internal connection
RESET	8	O	Reset output This terminal can be connected directly to a system that resets in the active-low state. A pullup resistor usually is required because the output is an npn open-collector transistor. An additional transistor should be connected when the active-high reset or higher output current is required.
SENSE	2	I	Voltage sense This terminal has a threshold level of 500 mV. The sense voltage and hysteresis can be set at the same time when the two voltage-dividing resistors are connected. The reference voltage is temperature compensated to inhibit temperature drift in the threshold voltage within the operating temperature range.
VCC	5	—	Power supply This terminal is used in an operating-voltage range of 1.8 V to 40 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage[2]		41	V
V_s	SENSE input voltage	−0.3	41	V
V_{OH}	Output voltage (off state)		41	V
I_{OL}	Output current (on state)		5	mA
T_J	Operating virtual-junction temperature		150	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.8	40	V
I_{OL}	Low-level output current		3	mA
T_A	Operating free-air temperature	−55	125	°C

6.4 Thermal Information

		TL7700-SEP	UNIT
		PW (TSSOP)	
	THERMAL METRIC[1]	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	172.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	99.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

V_{CC} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_s	SENSE input voltage		−55°C to 125°C	490		520	mV
I_s	SENSE input current	V_s = 0.4 V	25°C	2	2.5	3	µA
			−55°C to 125°C	1.5		3.5	
I_{CC}	Supply current	V_{CC} = 40 V, V_s = 0.6 V, no load	25°C		0.6	1	mA
V_{OL}	Low-level output voltage	I_{OL} = 1.5 mA	25°C			0.4	V
		I_{OL} = 3 mA	25°C			0.8	
I_{OH}	High-level output current	V_{OH} = 40 V, V_s = 0.6 V	−55°C to 125°C			1	µA
I_{CT}	Timing-capacitor charge current	V_s = 0.6 V	25°C	11	15	19	µA

6.6 Switching Characteristics

V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pi}	SENSE pulse duration	C_T = 0.01 µF (see Figure 17)	2			µs
t_{po}	Output pulse duration	C_T = 0.01 µF (see Figure 17)	0.5	1	1.5	ms
t_r	Output rise time	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF (see Figure 17)			15	µs
t_f	Output fall time	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF (see Figure 17)			0.5	µs
t_{pd}	Propagation delay time, SENSE to output	C_T = 0.01 µF (see Figure 17)			10	µs

6.7 Typical Characteristics

Data at high and low temperatures are applicable only within the recommended operating conditions.
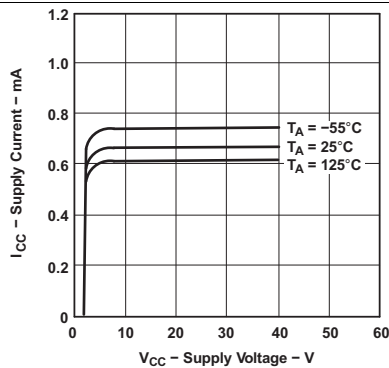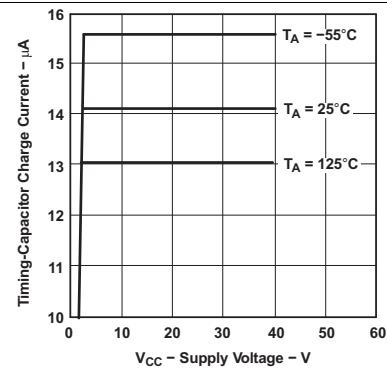

Figure 1. Supply Current vs Supply Voltage

Figure 2. Timing Capacitor Charge Current vs Supply Voltage
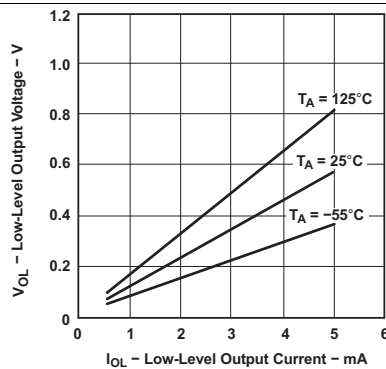

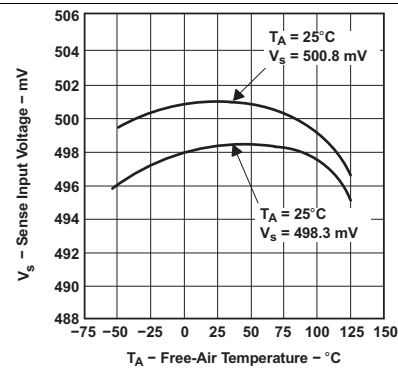Figure 3. V_{OL} vs I_{OL}
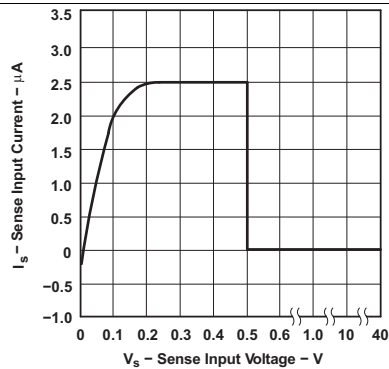

Figure 4. Sense Input Voltage vs Temperature

Figure 5. Sense Input Current vs Sense Input Voltage

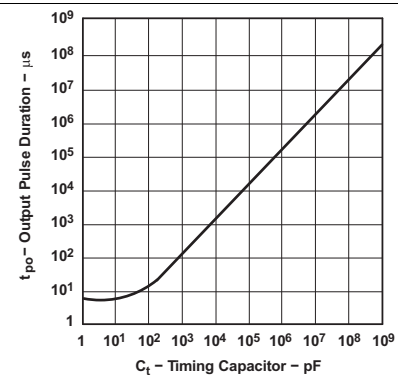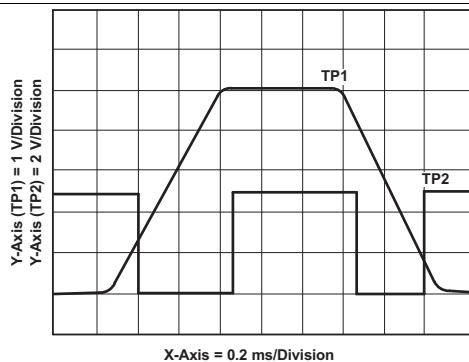Figure 6. Output Pulse Duration vs Timing Capacitor

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the recommended operating conditions.

Figure 7. V_{CC} vs Output Waveform 1 - See Figure 8
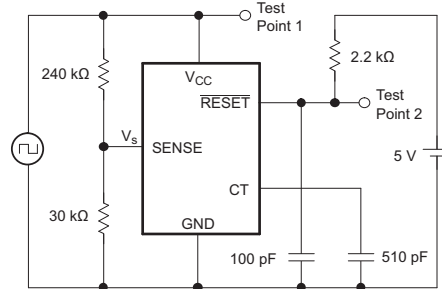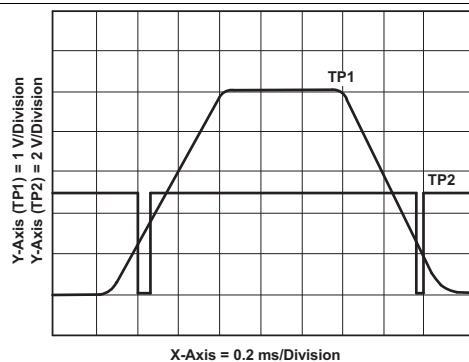

Figure 8. V_{CC} vs Output Test Circuit 1

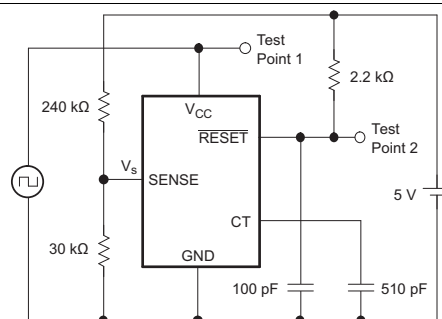**Figure 9. V_{CC} vs Output Waveform 2 - See Figure 10**
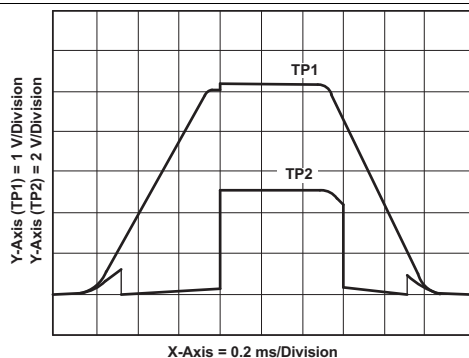

Figure 10. V_{CC} vs Output Test Circuit 2

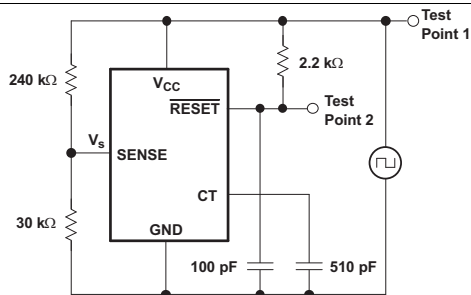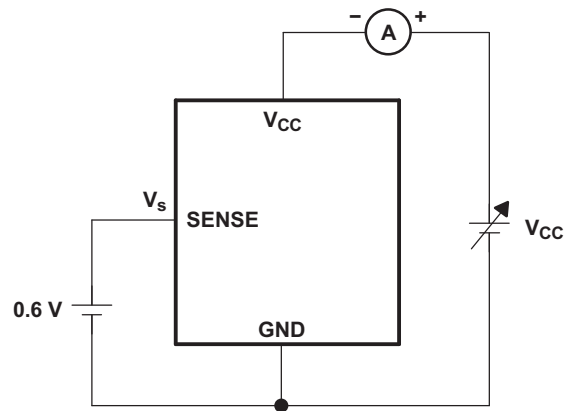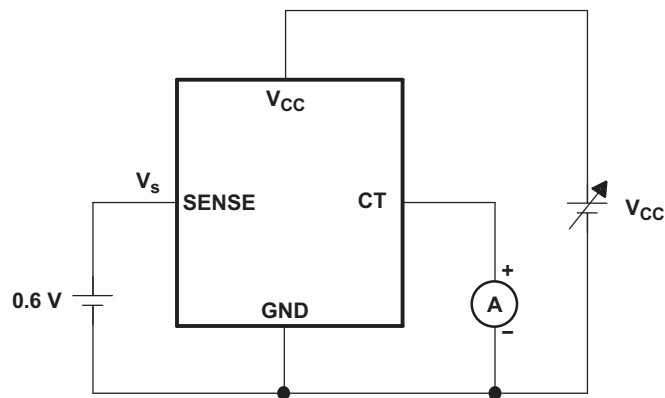**Figure 11. V_{CC} vs Output Waveform 3 - See Figure 12**
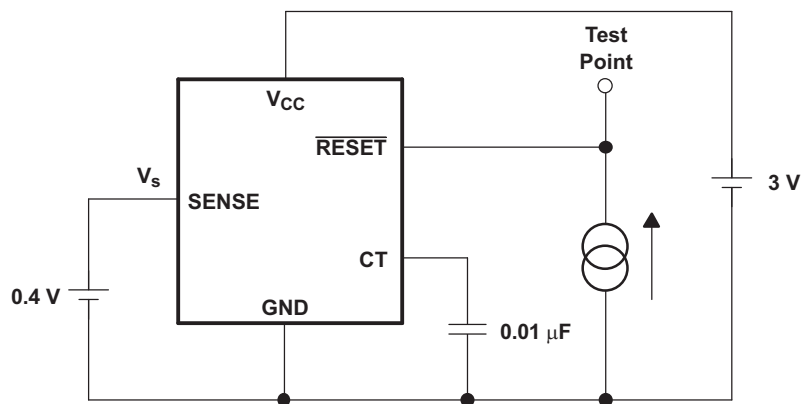

Figure 12. V_{CC} vs Output Test Circuit 3

7 Parameter Measurement Information
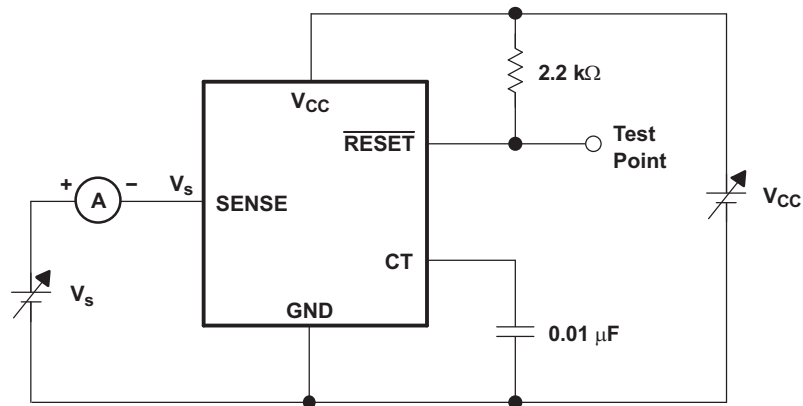

Figure 13. V_{CC} vs I_{CC} Measurement Circuit
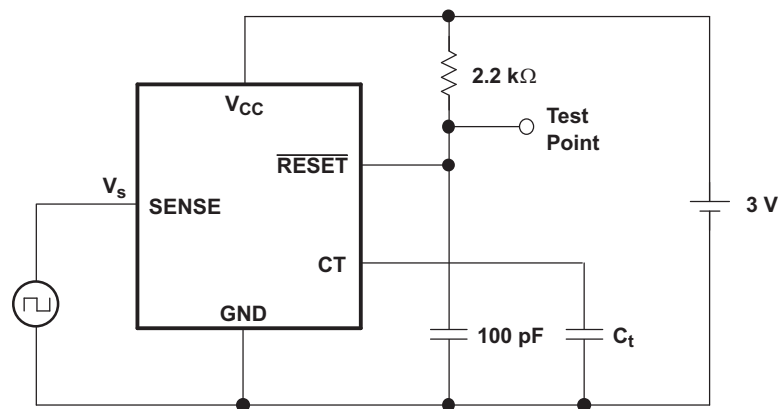

Figure 14. V_{CC} vs I_{CT} Measurement Circuit

Figure 15. I_{OL} vs V_{OL} Measurement Circuit

Parameter Measurement Information (continued)

Figure 16. V_s and I_s Characteristics Measurement Circuit

**Figure 17. Switching Characteristics Measurement Circuit**

8 Detailed Description

8.1 Overview

The TL7700-SEP is a bipolar integrated circuit designed for use as a reset controller in microcomputer and microprocessor systems. The SENSE voltage can be set to any value greater than 0.5 V using two external resistors. The hysteresis value of the sense voltage also can be set by the same resistors. The device includes a precision voltage reference, fast comparator, timing generator, and output driver, so it can generate a power-on reset signal in a digital system.

The TL7700-SEP has an internal 1.5-V temperature-compensated voltage reference from which all function blocks are supplied. Circuit function is very stable, with supply voltage in the 1.8-V to 40-V range. Minimum supply current allows use with ac line operation and portable battery operation.

8.2 Functional Block Diagram
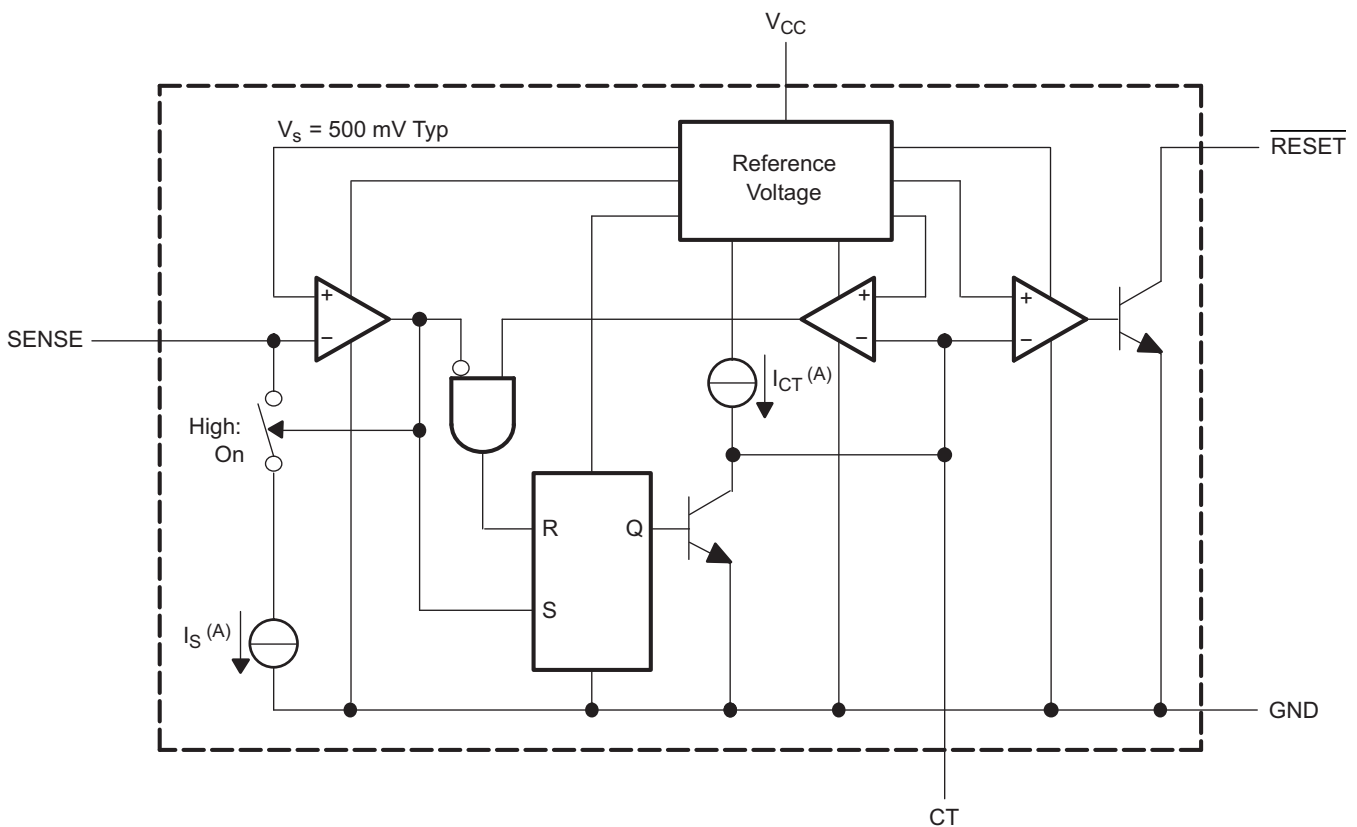
Copyright © 2016, Texas Instruments Incorporated

NOTE: I_{CT} = 15 µA (Typ), I_s = 2.5 µA (Typ)

8.3 Feature Description

8.3.1 Sense-Voltage Setting

The SENSE terminal input voltage, V_s, of the TL7700-SEP typically is 500 mV. By using two external resistors, the circuit designer can obtain any sense voltage over 500 mV. In Figure 18, the sensing voltage, $V_{s'}$, is calculated as:

$$V_{s'} = V_s \times (R1 + R2) / R2$$

where
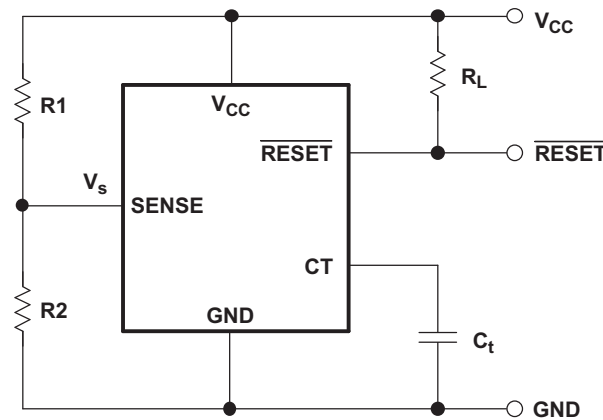
- V_s = 490 mV to 520 mV over temperature range (1)

Figure 18. Setting the Sense Voltage

8.3.2 Sense-Voltage Hysteresis Setting

If the sense voltage ($V_{s'}$) does not have hysteresis in it and the voltage on the sensing line contains ripples, the resetting of TL7700-SEP will be unstable. Hysteresis is added to the sense voltage to prevent such problems. As shown in Figure 19, the hysteresis (V_{hys}) is added and the value is determined as:

$$V_{hys} = I_s \times R1$$

where

- I_s = 1.5 μA to 3.5 μA over temperature range (2)
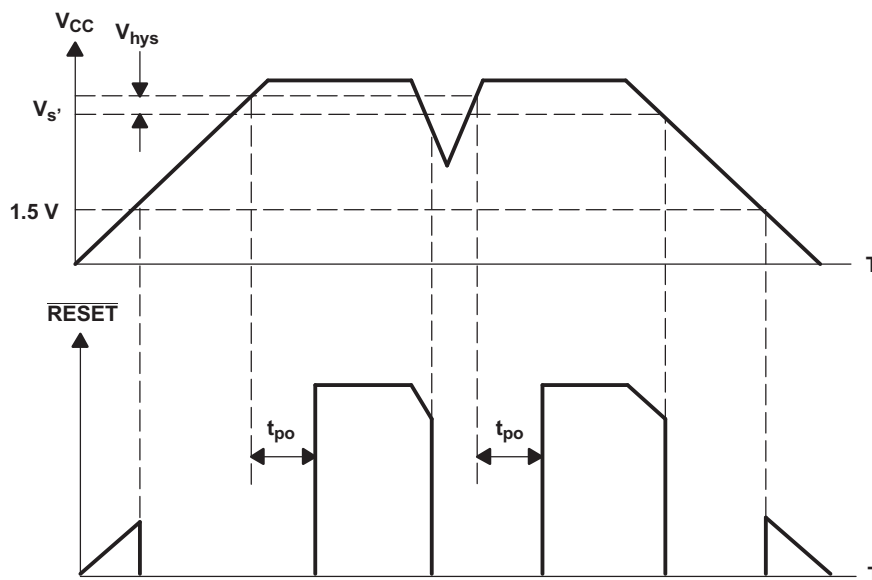
NOTE: The sense voltage, $V_{s'}$, is different from the SENSE terminal input voltage, V_s. V_s normally is 500 mV for triggering.

Figure 19. V_{CC}-RESET Timing Chart

Feature Description (continued)

8.3.3 Output Pulse-Duration Setting

Constant-current charging starts on the timing capacitor when the sensing-line voltage reaches the TL7700-SEP sense voltage. When the capacitor voltage exceeds the threshold level of the output drive comparator, $\overline{\text{RESET}}$ changes from a low to a high level. The output pulse duration is the time between the point when the SENSE-pin voltage exceeds the threshold level and the point when the $\overline{\text{RESET}}$ output changes from a low level to a high level. When the TL7700-SEP is used for system power-on reset, the output pulse duration, t_{po}, must be set longer than the power rise time. The value of t_{po} is:

$$t_{po} = C_t \times 10^5 \text{ seconds}$$

where

- C_t is the timing capacitor in farads (3)

There is a limit on the device response speed. Even if $C_t = 0$, t_{po} is not 0, but approximately 5 µs to 10 µs. Therefore, when the TL7700-SEP is used as a comparator with hysteresis without connecting C_t, switching speeds (t_r/t_f, t_{po}/t_{pd}, and so forth) must be considered.

8.4 Device Functional Modes

Figure 20 describes how the $\overline{\text{RESET}}$ output pin responds to a change in the voltage at the SENSE pin. When the SENSE pin drops below 500 mV, the $\overline{\text{RESET}}$ pin is pulled low.
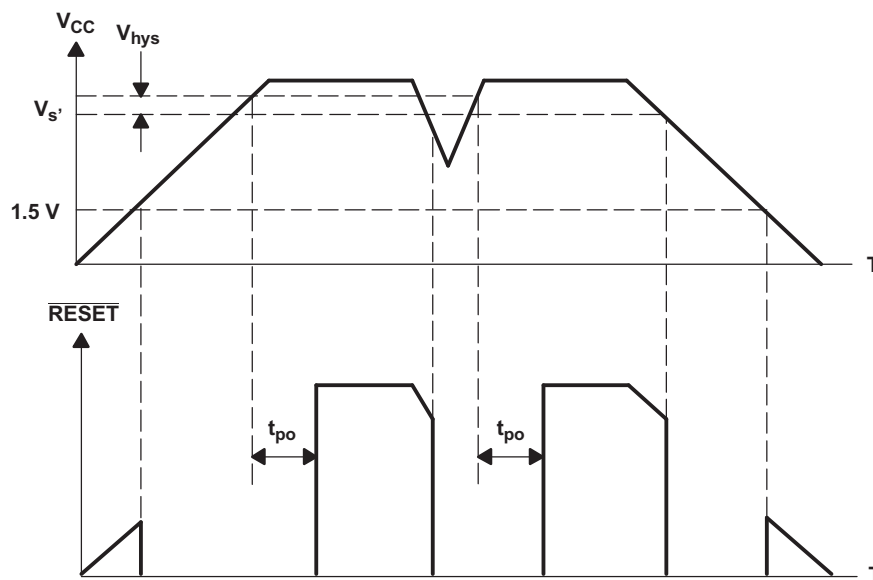
NOTE: The sense voltage, $V_{s'}$, is different from the SENSE terminal input voltage, V_s. V_s normally is 500 mV for triggering.

Figure 20. V_{CC} $\overline{\text{RESET}}$ Response and Timing

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TL7700-SEP supply-voltage supervisor allows for any voltage greater than 500 mV to be monitored. This flexibility allows it to be used in many applications from FPGAs and microcontrollers to supply monitoring.

9.2 Typical Application

Figure 21 shows an application where the TL7700-SEP device is being used to sense the voltage supply for a microcontroller that is supplied with 5 V. If the sense voltage drops below 4.5 V, the $\overline{\text{RESET}}$ pin is pulled LOW, signaling the microcontroller to reset.
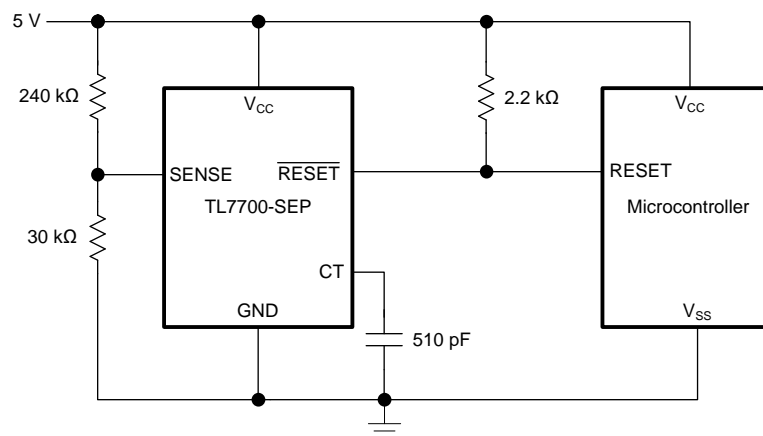

Figure 21. 5-V Supply Voltage Supervision

9.2.1 Design Requirements

- When the TL7700-SEP is used for system power-on reset, the output pulse duration, t_{po}, must be set longer than the power rise time. The value of t_{po} is: $t_{po} = C_t \times 10^5$ seconds.
- The RESET output is an open-collector output, so a pullup resistor is required.

9.2.2 Detailed Design Procedure

The SENSE terminal input voltage, V_s, for TL7700-SEP is typically 500 mV. By using two external resistors, any sense voltage over 500 mV can be sensed.

Resistor R1 should be selected first to set the desired hysteresis. See the *Sense-Voltage Hysteresis Setting* section for detailed information on how to set the hysteresis.

Resistor R2 should then be selected based on the R1 value and the desired $V_{s'}$ voltage. In Figure 18, the sensing voltage, $V_{s'}$, is calculated as: $V_{s'} = V_s \times (R1 + R2) / R2$

Typical Application (continued)

9.2.3 Application Curve
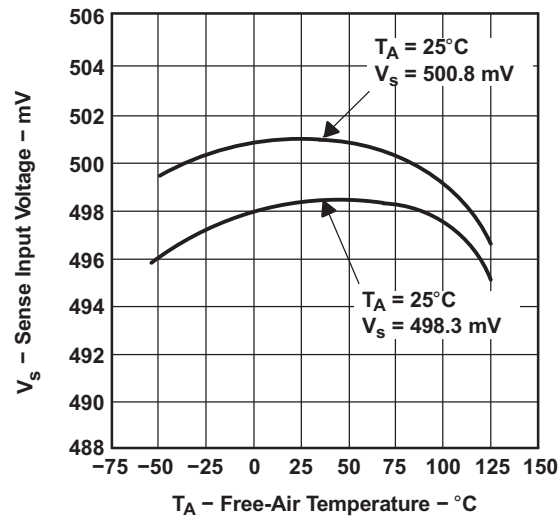
Figure 22. SENSE Input Voltage vs Temperature

10 Power Supply Recommendations

The TL7700-SEP device will operate within the supply range specified in *Recommended Operating Conditions*. The device risks permanent damage over the voltage specified in *Absolute Maximum Ratings*.

11 Layout

11.1 Layout Guidelines

As the $\overline{\text{RESET}}$ pin is an open collector output, a pullup resistor is required to ensure the output is high when the output transistor is off. The SENSE resistors should be placed as close to the SENSE pin as possible to avoid introducing noise to the pin.

11.2 Layout Example
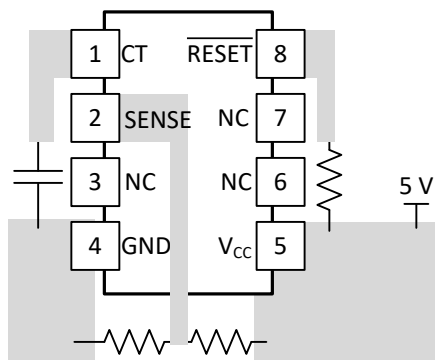
Figure 23. TL7700-SEP Layout

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7700CMPWPSEP	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7700SP	Samples
TL7700CMPWTPSEP	ACTIVE	TSSOP	PW	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7700SP	Samples
V62/19602-01XE	ACTIVE	TSSOP	PW	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7700SP	Samples
V62/19602-01XE-T	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7700SP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
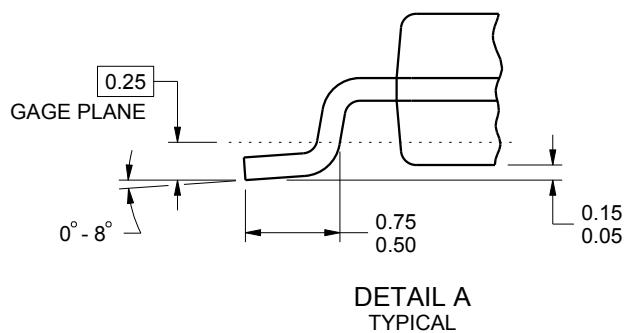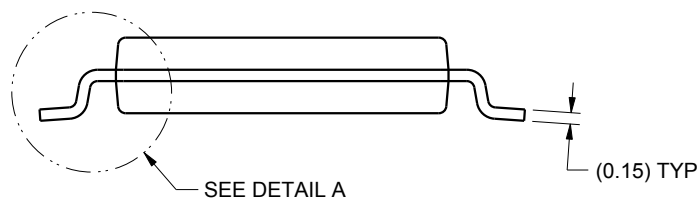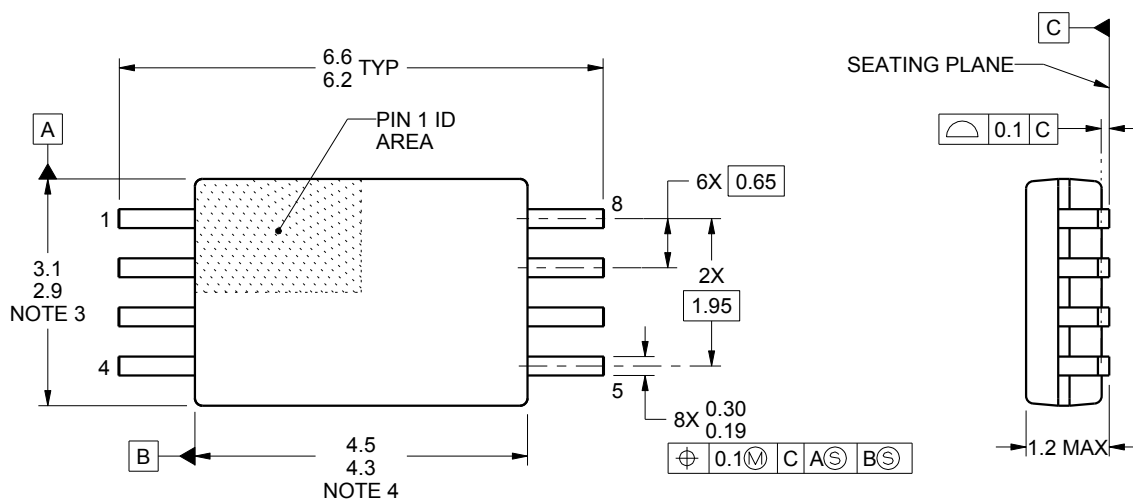
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
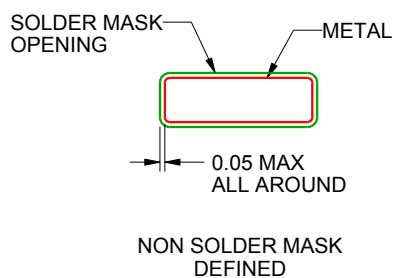5. Reference JEDEC registration MO-153, variation AA.

8X (0.45)

8X (1.5)

SYMM

(R0.05)
TYP

1

8

SYMM

6X (0.65)

5

4

(5.8)
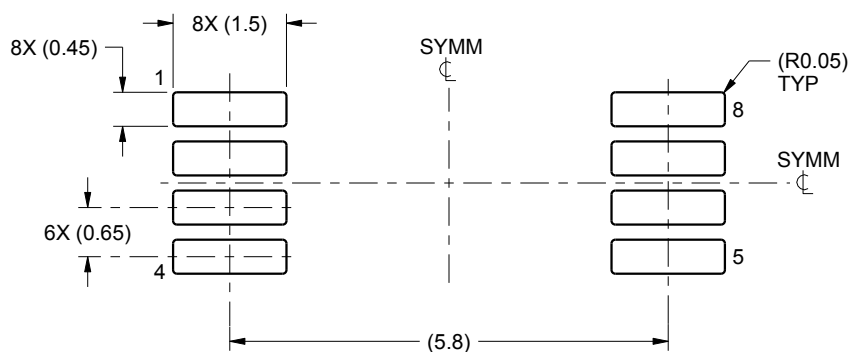
LAND PATTERN EXAMPLE
SCALE:10X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
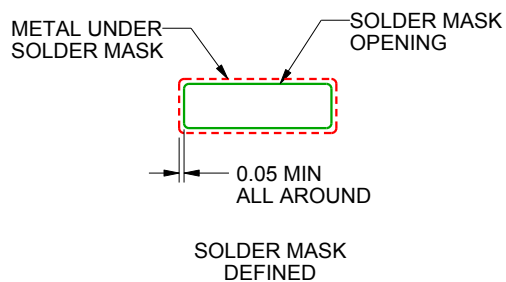
SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)
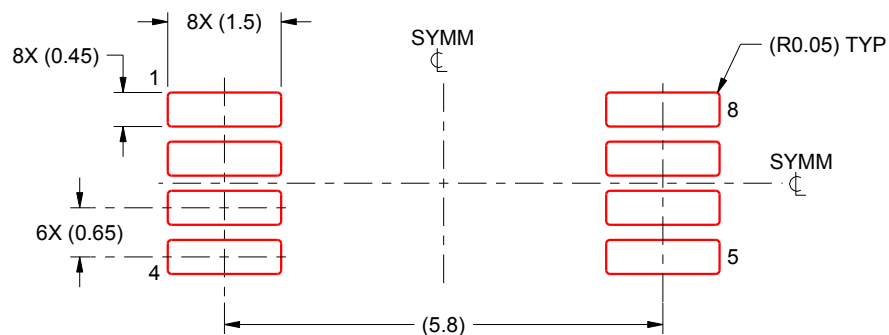
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (1.5)

8X (0.45)

SYMM

(R0.05) TYP

1

8

SYMM

6X (0.65)

4

5

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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