



TPS3847 18V、380nA 电压监视器

1 特性

- 超低电源电流：380nA
- 宽电源电压范围：4.5V 至 18V
- 高阈值精度：±2.5%
- 内部滞后
- 推挽输出
- 延迟时间 20ms（最大值）
- 厂家调整的固定电压阈值
- 特定工作温度范围：
–40°C 至 +85°C
- 工作温度范围：–40°C 至 +105°C
- 封装：5 引脚 SOT

2 应用

- 便携式和电池供电类设备
- 台式机、笔记本电脑和超级本
- 工业系统
- 服务器
- 安防系统

3 说明

TPS3847 系列器件具有宽范围工作电压和超低电流，可监视电源引脚电压。每当 VCC 电源电压降至厂家调整的复位阈值电压以下，器件就会将一个低电平有效复位信号置为有效。当 VCC 电压升至阈值电压以上 20ms（最大值）后，复位输出保持有效。

TPS3847 具有 380nA 超低流耗以及 18V 电压，是低功耗便携式应用的理想选择。

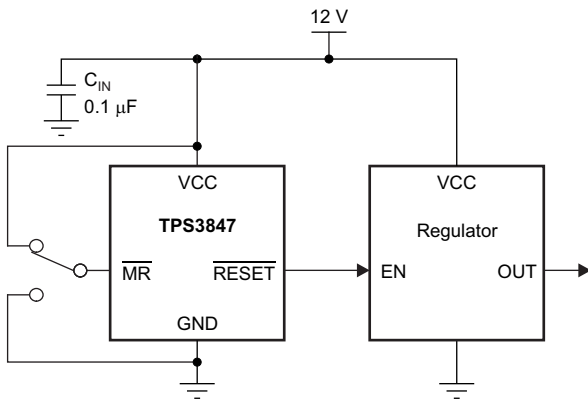
TPS3847 具有精密的厂家调节阈值电压和极低功耗运行特性。TPS3847 采用符合行业标准的 5 引脚 SOT 封装。

器件信息⁽¹⁾

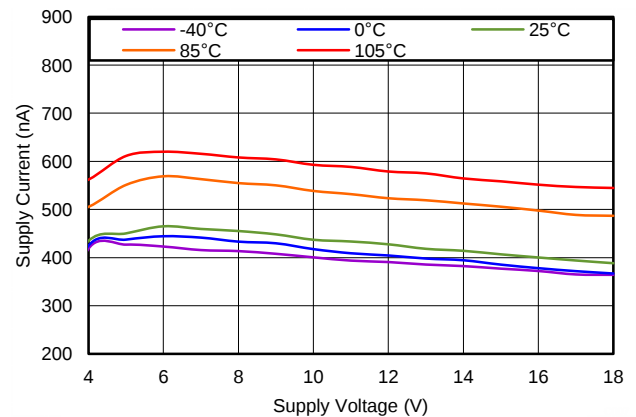
器件型号	封装	封装尺寸（标称值）
TPS3847	小外形尺寸晶体管 (SOT) (5)	2.90mm x 1.60mm

(1) 要了解所有可用封装，请见数据表末尾的封装选项附录。

典型应用



电源电流与电源电压间的关系



目录

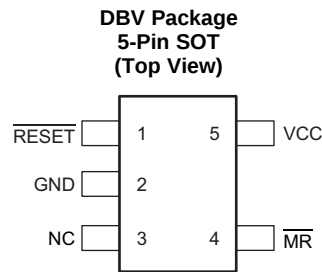
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4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2014) to Revision A	Page
• 已更改器件名称以反映整个器件系列	1
• 已将所有 SOT-23 封装更改为 SOT	1
• Changed $\overline{MR}$ maximum specification in <i>Absolute Maximum Ratings</i> table	4
• Changed $V_{(MR)}$ maximum specification in <i>Recommended Operating Conditions</i> table	4
• Deleted maximum value for C_{IN} in <i>Recommended Operating Conditions</i>	4
• Changed conditions of <i>Electrical Characteristics</i> table: added condition for typical values	5
• Added new row to V_{IT-} for TPS3847108 in <i>Electrical Characteristics</i>	5
• Added new row to V_{HYS} for TPS3847108 in <i>Electrical Characteristics</i>	5
• Added maximum specification to second row of V_{OL} parameter in <i>Electrical Characteristics</i> table	5
• Changed V_{OH} test conditions to $I_{OH} = 2\text{ mA}$ in <i>Electrical Characteristics</i> table	5
• Added conditions to <i>Timing Requirements</i> table	6
• Changed $t_{d(START)}$ maximum specification in <i>Timing Requirements</i> table.....	6
• Added condition to 图 2	7
• Changed Y-axis in 图 12.....	10
• Changed title of <i>Typical Application</i> section	12

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Ground
$\overline{\text{MR}}$	4	I	Manual reset. Pull this pin to a logic low to force the $\overline{\text{RESET}}$ output low regardless of the voltage on VCC. After the $\overline{\text{MR}}$ pin is pulled to a logic high, the $\overline{\text{RESET}}$ output goes high after the $\overline{\text{RESET}}$ delay time (t_d) if the voltage on VCC is higher than the positive-going threshold voltage.
NC	3	—	No internal connection.
$\overline{\text{RESET}}$	1	O	Active low reset output. $\overline{\text{RESET}}$ stays low as long as the voltage on VCC is below the factory trimmed threshold voltage. $\overline{\text{RESET}}$ transitions from low to high once the VCC voltage is above the positive-going threshold voltage for a specified time (t_d). $\overline{\text{RESET}}$ is a push-pull output.
VCC	5	I	Power supply and monitored voltage. TI recommends adding a small 0.1- μF bypass capacitor near the VCC pin.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	VCC	−0.3	+20	V
	$\overline{\text{MR}}$	−0.3	VCC + 0.3	V
	$\overline{\text{RESET}}$	−0.3	+5.5	V
Current	$\overline{\text{RESET}}$		10	mA
Temperature ⁽²⁾	Operating junction, T _J	−40	+105	°C
	Storage, T _{stg}	−65	+150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) As a result of the low dissipated power in this device, it is assumed that the junction temperature is equal to the ambient temperature.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _(VCC)	Power supply voltage	4.5		18	V
V _(MR)	$\overline{\text{MR}}$ pin voltage	0	1.2	VCC	V
V _(RESET)	$\overline{\text{RESET}}$ pin voltage	0		5	V
I _(RESET)	$\overline{\text{RESET}}$ pin current	0		2	mA
C _{IN}	Input capacitor	0	0.1		μF
T _J	Junction temperature	−40	+25	+85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3847	UNIT
		DBV (SOT)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	208.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	123.3	
R _{θJB}	Junction-to-board thermal resistance	37.2	
ψ _{JT}	Junction-to-top characterization parameter	14.6	
ψ _{JB}	Junction-to-board characterization parameter	36.3	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

At $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $4.5\text{ V} < V_{CC} < 18\text{ V}$, and $C_{IN} = 0.1\text{ }\mu\text{F}$ (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V _{VCC}	Input supply voltage range			4.5		18	V
V _{VO}	Minimum V _{VCC} voltage for valid output ⁽¹⁾	I _{OL} = 1 μA, V _{OL} = 400 mV				0.8	V
I _{VCC}	Supply current (into VCC pin)	Output not connected	T _J = 25°C, V _{VCC} = 18 V		380		nA
			T _J = 25°C		750		nA
			−40°C ≤ T _J ≤ +85°C		900		nA
MONITORED THRESHOLD							
V _{IT−}	Negative going input threshold accuracy	T _J = 25°C		±0.5%			
				−2.5%	+2.5%		
	Negative-going threshold voltage	TPS3847085		8.2875	8.5	8.7125	V
		TPS3847108		10.53	10.8	11.07	V
V _{HYS}	Hysteresis voltage	TPS3847085		0.11 × V _{IT−}			V
		TPS3847108		0.035 × V _{IT−}			V
OUTPUT							
V _{OL}	Push-pull low-level output voltage (RESET)	0.9 V < V _{VCC} < 2.4 V, I _{OL} = 10 μA			0.009	0.4	V
		2.4 V ≤ V _{VCC} < 4.5 V, I _{OL} = 250 μA			0.015	0.4	V
		4.5 V ≤ V _{VCC} ≤ 18 V, I _{OL} = 2 mA			0.09	0.4	V
V _{OH}	Push-pull high-level output voltage (RESET)	I _{OH} = −2 mA		1.6		3.1	V
			V _{VCC} = 18 V		2.45		V
		I _{OH} = −10 μA		3		4	V
			V _{VCC} = 18 V		3.55		V
MR PIN							
V _{IL}	Low-level input voltage					0.4	V
V _{IH}	High-level input voltage			1.2			V
I _{lkg(MR)}	MR leakage current	MR High, V _{VCC} = 18 V			−23		nA

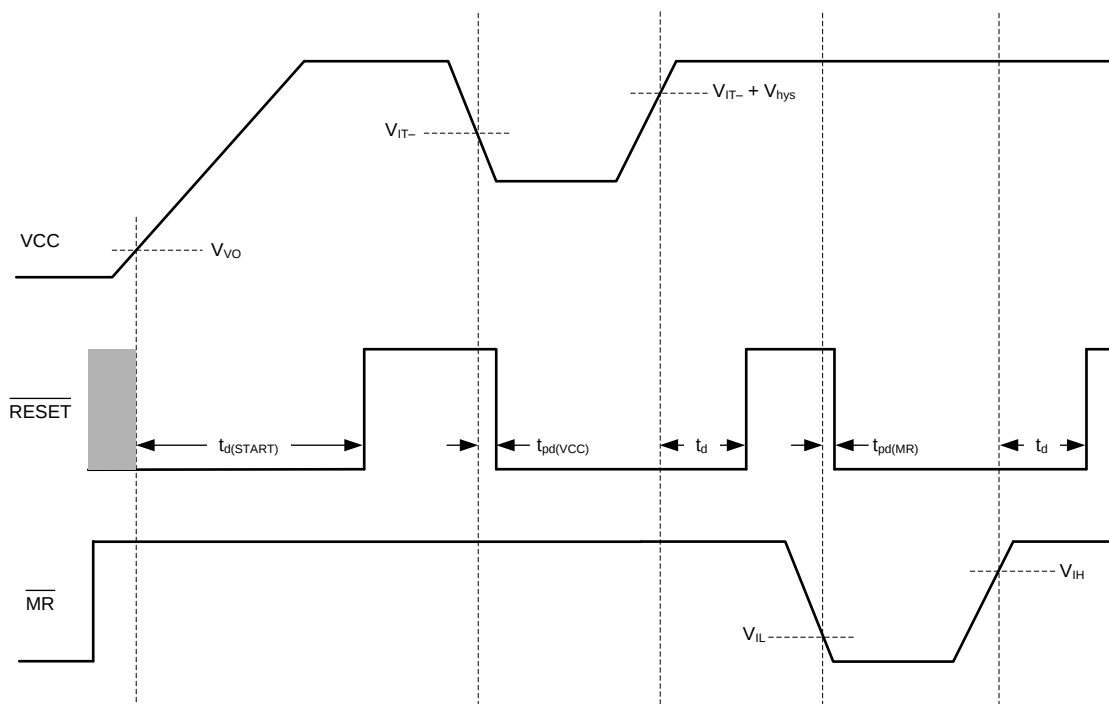
(1) The lowest supply voltage ($V_{(VCC)}$) at which $\overline{\text{RESET}}$ is valid. $t_{RISE(VCC)} \geq 15\text{ }\mu\text{s/V}$, where t_{RISE} is the rise time.

6.6 Timing Requirements

At $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $4.5\text{ V} < V_{CC} < 18\text{ V}$, and $C_{IN} = 0.1\text{ }\mu\text{F}$ (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$.

	PARAMETER	MIN	TYP	MAX	UNIT
t_d	$\overline{\text{RESET}}$ delay time ⁽¹⁾		4.5	20	ms
$t_{d(\text{START})}$	Startup delay time ⁽²⁾		6.5	40	ms
$t_{pd(VCC)}$	Propagation delay for V_{CC} falling ⁽³⁾		55		μs
$t_{pd(MR)}$	Propagation delay $\overline{\text{MR}}$ falling ⁽⁴⁾		50		μs
$t_{P(MR)}$	$\overline{\text{MR}}$ minimum high to low pulse duration for $\overline{\text{RESET}}$ low		50		μs

- (1) Delay from when $V_{(VCC)} \geq V_{IT-}$ or $V_{MR} \geq V_{IH}$ until $\overline{\text{RESET}}$ goes high when $V_{(VCC)}$ starts from above the specified minimum $V_{(VCC)}$. Measured with 5% overdrive.
- (2) When $V_{(VCC)}$ starts from less than the specified minimum $V_{(VCC)}$ and then exceeds V_{th} , $\overline{\text{RESET}}$ goes high after the startup delay ($t_{d(\text{START})}$) instead of the $\overline{\text{RESET}}$ delay time (t_d). Measured with 5% overdrive.
- (3) Delay from $V_{(VCC)} < V_{th}$ until $\overline{\text{RESET}}$ goes low. Measured with 8% overdrive.
- (4) Delay from $V_{MR} < V_{IL}$ until $\overline{\text{RESET}}$ goes low. Measured with 8% overdrive.



Timing Diagram

6.7 Typical Characteristics

At $V_{VCC} = 18\text{ V}$, $\overline{MR} = 1.2\text{ V}$, $\overline{RESET} = \text{open}$, and $C_{IN} = 0.1\text{ }\mu\text{F}$ (unless otherwise noted).

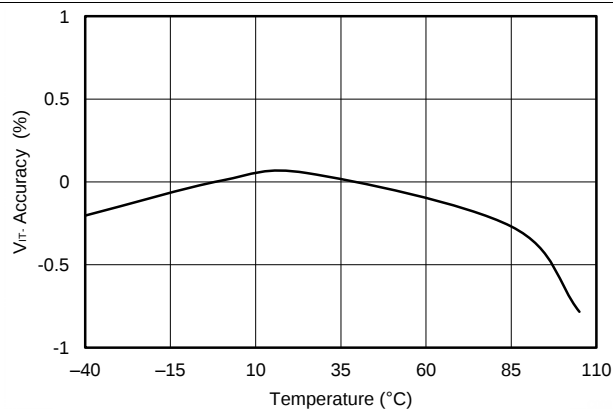


图 1. Negative-Going Threshold Accuracy vs Temperature

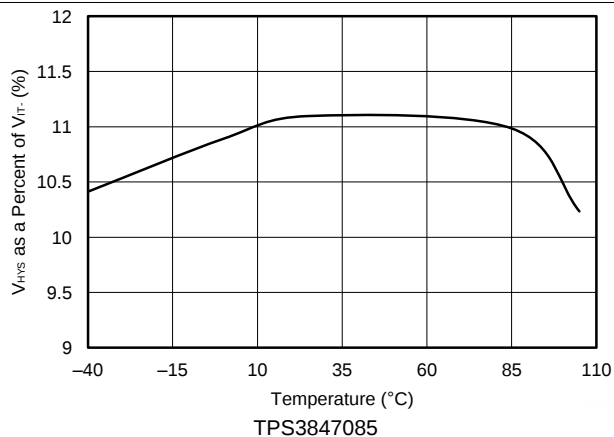


图 2. Hysteresis vs Temperature

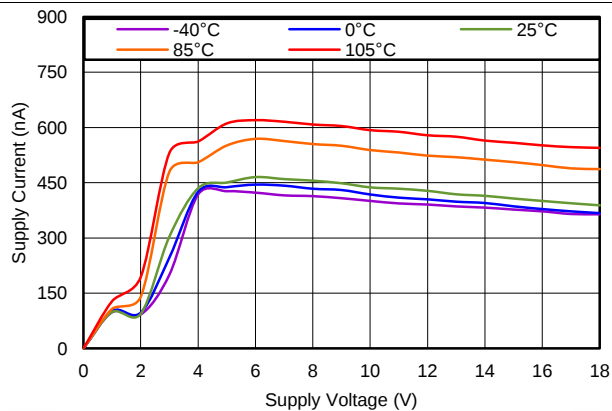


图 3. Supply Current vs V_{VCC} and Temperature

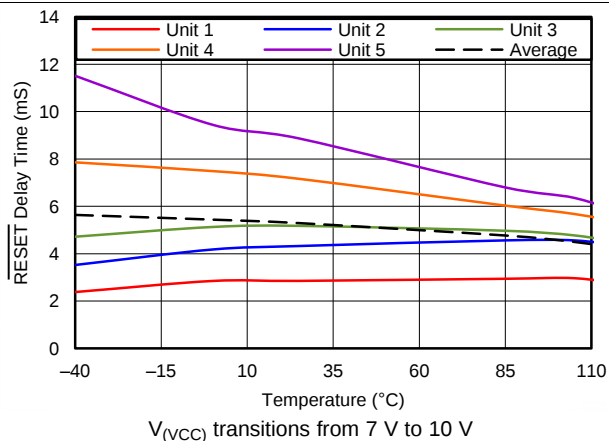


图 4. $\overline{RESET}$ Delay Time vs Temperature Distribution

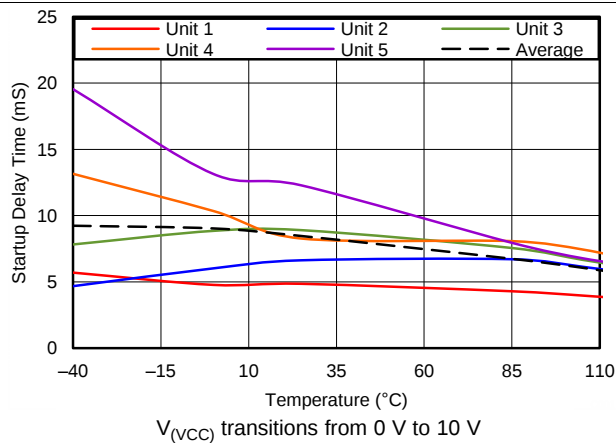


图 5. Startup Delay Time vs Temperature Distribution

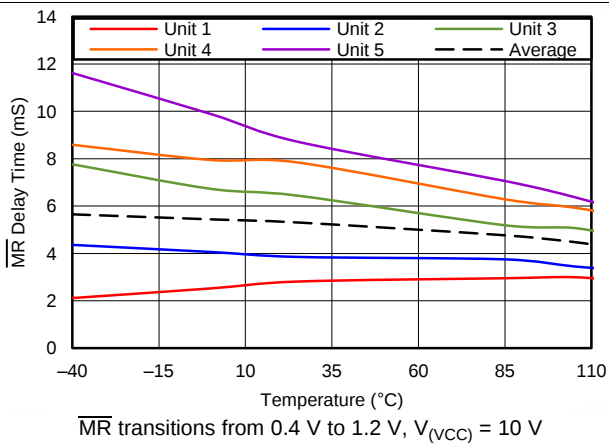


图 6. $\overline{MR}$ Delay Time vs Temperature Distribution

Typical Characteristics (接下页)

At $V_{(VCC)} = 18\text{ V}$, $\overline{\text{MR}} = 1.2\text{ V}$, $\overline{\text{RESET}} = \text{open}$, and $C_{\text{IN}} = 0.1\text{ }\mu\text{F}$ (unless otherwise noted).

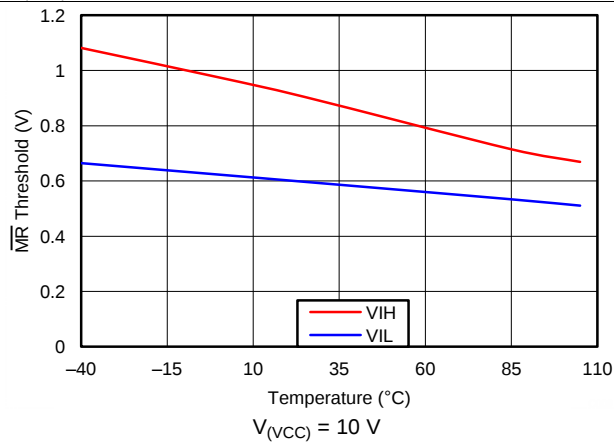


图 7. $\overline{\text{MR}}$ Threshold vs Temperature

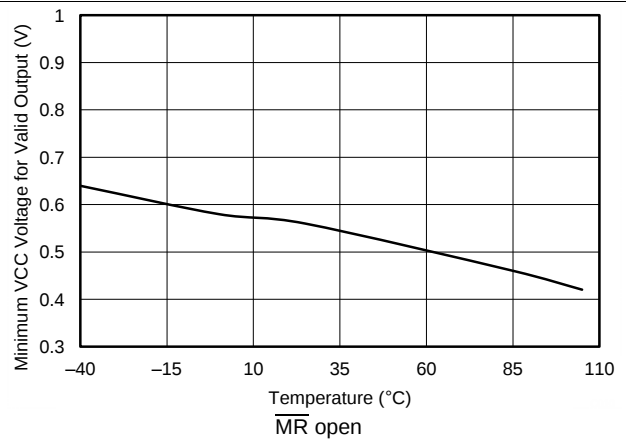


图 8. Minimum $V_{(VCC)}$ for Valid Output vs Temperature

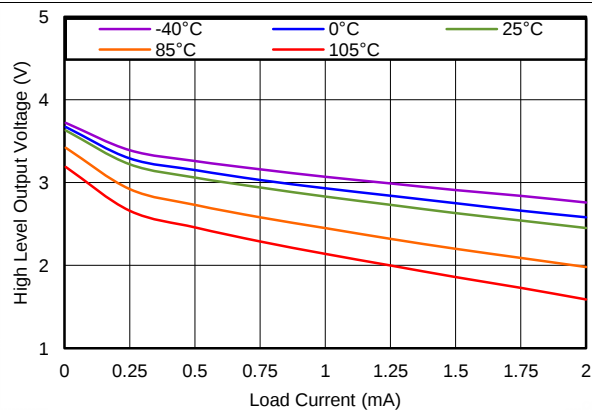


图 9. High-Level Output Voltage vs Load Current

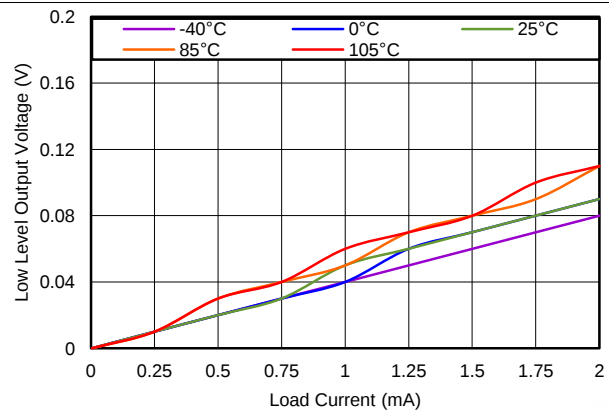


图 10. Low-Level Output Voltage vs Load Current

7 Detailed Description

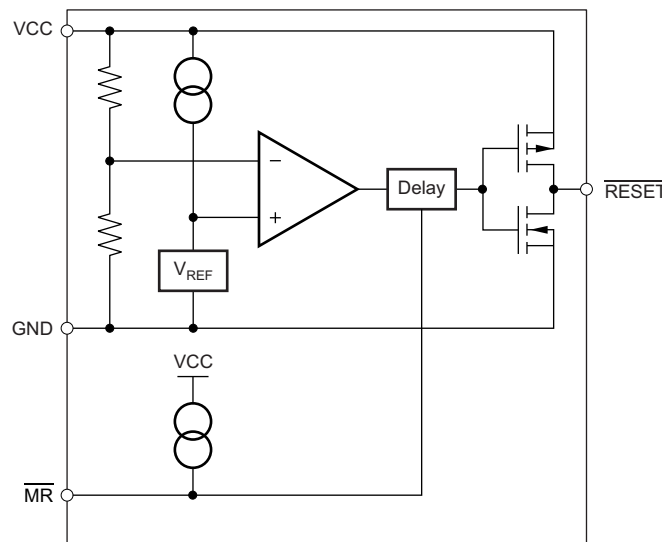
7.1 Overview

The TPS3847 is a family of ultralow-current supervisors for high-voltage applications that are specified from -40°C to $+85^{\circ}\text{C}$ and operational up to 105°C (see the [Typical Characteristics](#) section for typical -40°C to $+105^{\circ}\text{C}$ performance).

The $\overline{\text{RESET}}$ output goes low after the power-supply voltage (V_{VCC}) drops below the negative-going input threshold voltage ($V_{\text{IT-}}$), and after the VCC falling propagation delay ($t_{\text{pd(VCC)}}$) elapses. When V_{VCC} rises above the positive-going reset threshold ($V_{\text{IT+}}$), which is the negative-going threshold voltage plus the hysteresis ($V_{\text{IT-}} + V_{\text{hys}}$), $\overline{\text{RESET}}$ outputs a high signal after the reset delay time (t_{d}) elapses.

The TPS3847 also features a manual reset pin ($\overline{\text{MR}}$) that allows a processor, or other logic devices, to initiate a reset, even when V_{VCC} exceeds $V_{\text{IT-}}$. A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to transition to logic low after the $\overline{\text{MR}}$ propagation delay ($t_{\text{pd(MR)}}$) elapses. When $\overline{\text{MR}}$ returns to a logic high and V_{VCC} exceeds $V_{\text{IT+}}$, $\overline{\text{RESET}}$ transitions to logic high after t_{d} elapses.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Ultralow Supply Current

The TPS3847 uses a unique sampling scheme to maintain an extremely-low average quiescent current of 380 nA. This low quiescent current is ideal for applications that require extremely-low power consumption.

7.3.2 Wide Supply Range

This device has an operational input supply range of 4.5 V to 18 V, allowing for a wide range of applications. This wide supply range is ideal for applications that have either large transients or high dc voltage supplies.

7.3.3 High-Accuracy Negative Threshold

The TPS3847 has a negative threshold accuracy of $\pm 2.5\%$ and uses well-controlled and matched internal resistors to set the threshold voltage in order to eliminate the inaccuracies because of the external resistors. Unlike The TPS3847, voltage supervisors that require external resistors to set the threshold voltage always add inaccuracy to the specified performance.

Feature Description (接下页)

7.3.4 Push-Pull Output

The TPS3847 has a push-pull output stage that covers many of the common digital logic levels. Push-pull outputs simplify many designs compared to open-drain output devices because push-pull outputs do not require a pull-up resistor or an additional low-voltage rail. Compared to open-drain output devices, push-pull devices reduce power consumption when the output is low because open-drain devices sink current through the pull-up resistor to ground in order to create the logic-low signal.

7.3.5 Manual Reset ($\overline{\text{MR}}$) Input

The manual reset ($\overline{\text{MR}}$) input allows a processor, or other logic devices, to initiate a reset even when the voltage on VCC is greater than $V_{\text{IT-}}$. A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to output a logic low. After $\overline{\text{MR}}$ returns to a logic high and the power-supply voltage is greater than $V_{\text{IT+}}$, $\overline{\text{RESET}}$ transitions to logic high after the reset delay time (t_d) elapses.

7.3.6 VCC Transient Rejection

The TPS3847 has built-in rejection of fast transients on the VCC pin. Transient rejection depends on both the duration and overdrive, or amplitude, of the transient. Overdrive of the transient is measured from the bottom of the transient to the negative threshold voltage ($V_{\text{IT-}}$) of the device, as shown in 图 11.

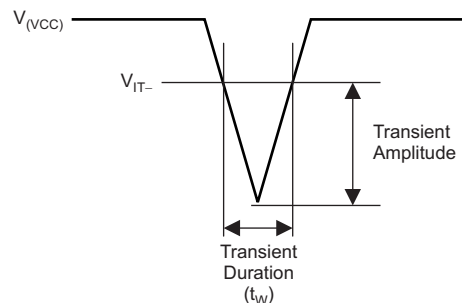


图 11. Voltage Transient Measurement

图 12 shows the relationship between the overdrive and the duration required to trigger a reset. Any combination of duration and amplitude greater than that shown in 图 12 generates a reset signal.

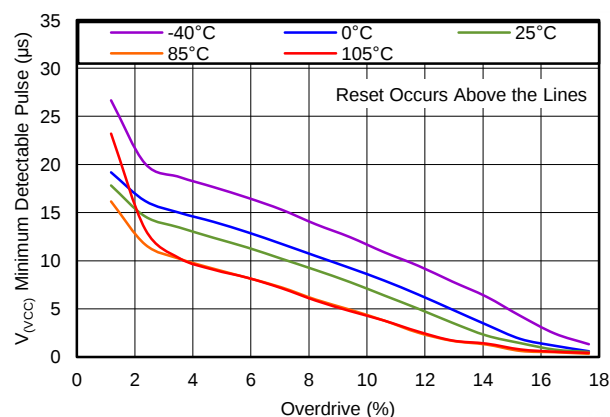


图 12. Minimum Detectable Pulse on VCC vs Overdrive

Feature Description (接下页)

7.3.7 Controlled Startup Current

The input supply current of the TPS3847 is very well controlled, including during startup. Some low-current devices exhibit spikes in the supply current before reaching the minimum supply voltage; this type of startup behavior can cause problems in some applications. 图 13 shows that there are no spikes in supply current, and the device is well controlled all the way from 0 V to minimum $V_{(VCC)}$.

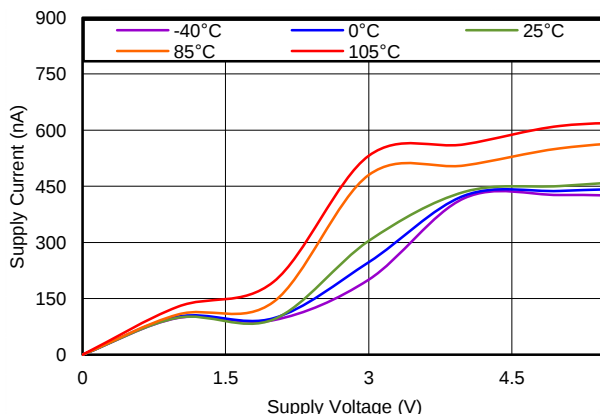


图 13. Supply Current During Startup

7.3.8 Low Minimum Supply Voltage for Valid Output

The TPS3847 is designed to have a valid $\overline{\text{RESET}}$ signal, even with a low input supply voltage. 图 14 shows that even at -40°C , the TPS3847 typically has a valid output with only 0.65 V on the input supply; at 105°C , that input supply voltage goes down to less than 0.45 V.

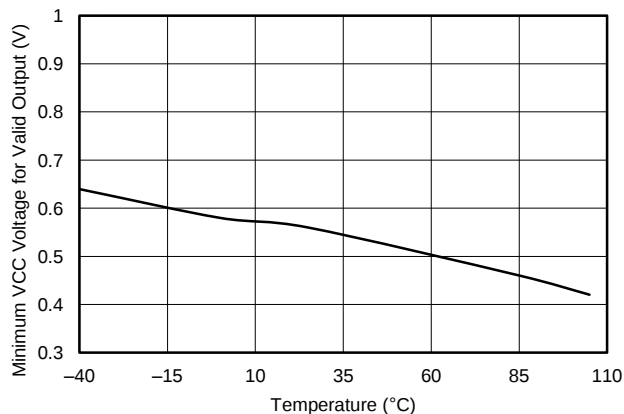


图 14. Minimum Supply Voltage for Valid Output vs Temperature

7.4 Device Functional Modes

The TPS3847 has two functional modes:

1. $\overline{\text{MR}}$ high: in this mode, $\overline{\text{RESET}}$ is high or low depending on the value of $V_{(VCC)}$ relative to V_{IT-} .
2. $\overline{\text{MR}}$ low: in this mode, $\overline{\text{RESET}}$ is held low regardless of the value of $V_{(VCC)}$.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS3847 family consists of wide-operating voltage, ultralow-current devices that monitor the power-supply voltage. The device asserts an active-low reset signal whenever the supply voltage drops below the factory-trimmed reset. The ultralow current consumption of 380 nA combined with 18-V capability makes the TPS3847 ideal for use in low-power and portable applications.

8.2 Typical Application

Wide operating voltage and threshold options make the TPS3847 well suited for monitoring dual- and triple-cell, lithium-ion battery applications. 图 15 shows the TPS3847 used to disable a buck converter when the cell voltage discharges below the threshold voltage. When the cell voltage reaches V_{IT-} , the enable pin of the TPS62120 is driven low, placing the buck converter in a low-current, shutdown state.

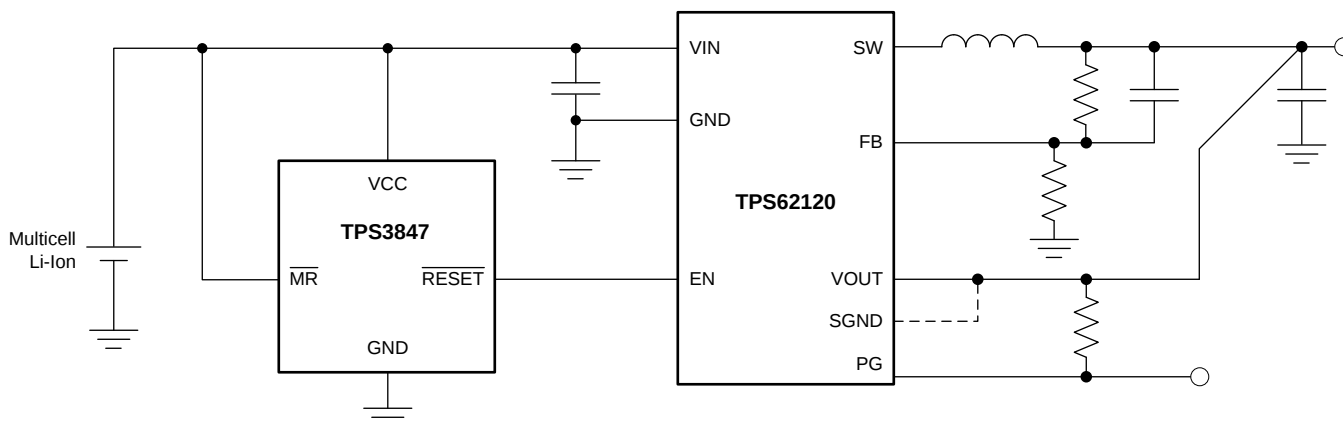


图 15. Disabled Buck Converter

8.2.1 Design Requirements

8.2.1.1 Input Capacitor

The TPS3847 uses a unique sampling scheme to maintain an extremely low average quiescent current of 380 nA. However, this current rises to approximately 12 μ A for approximately 500 μ s while the TPS3847 refreshes the reference voltage. This refresh pulse typically occurs every 200 ms. If the source impedance to the supply voltage is high, then the additional current during sampling may trigger a false reset as a result of the voltage drop from the supply to the VCC pin. For sources with a high impedance, or applications with long or thin VCC traces, add a 0.1- μ F or larger bypass capacitor near the VCC pin. Adding this bypass capacitor effectively keeps the average current supplied from the input source close to 380 nA, reducing the voltage droop caused by the refresh pulse, and is good analog design practice.

Typical Application (接下页)

8.2.1.2 Driving Bidirectional Reset Pins

Some microcontrollers have bidirectional reset pins that act as both an input and an output. When using bidirectional reset pins, place a series resistor between the TPS3847 $\overline{\text{RESET}}$ pin and the microcontroller in order to protect against excessive current flow in case both the TPS3847 and the microcontroller attempt to drive the reset line simultaneously. 图 16 illustrates the connection of the TPS3847 to a microcontroller using a series resistor to drive a bidirectional reset line. Assuming the maximum voltage that the microprocessor outputs is the same as the TPS3847 (4 V), use a resistor value greater than 20 k Ω in order to limit the output current to 2 mA or less when one pin is driven high and the other is driven low. In order to cover the majority of applications, use a resistor value of 47 k Ω .

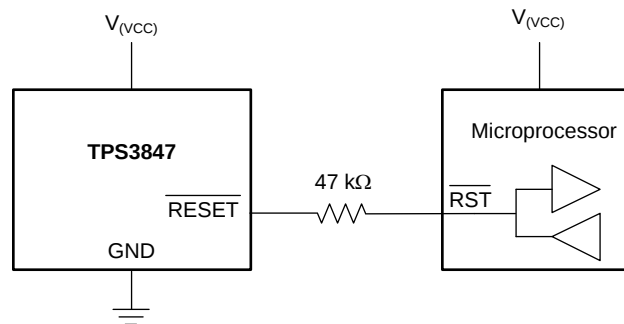


图 16. Connection to Bidirectional Reset Pin

8.2.1.3 Manual Reset ($\overline{\text{MR}}$) Input

The manual reset ($\overline{\text{MR}}$) input allows a processor, or other logic devices, to initiate a reset. A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to transition to logic low. After $\overline{\text{MR}}$ returns to a logic high and $V_{(\text{VCC})}$ is greater than $V_{\text{IT+}}$, $\overline{\text{RESET}}$ transitions to a logic high after the reset delay time, t_d , elapses.

Note that internal to the device $\overline{\text{MR}}$ is connected to a very small current source that goes from the internal sub-regulated voltage to the $\overline{\text{MR}}$ node. If the logic signal driving $\overline{\text{MR}}$ does not exceed 3 V, there is 25 nA of additional current drawn from the input supply because of this current source. Do not leave this pin floating; either drive this pin above or below the $\overline{\text{MR}}$ high and low input levels. Tie $\overline{\text{MR}}$ directly to VCC if not used.

8.2.1.4 Threshold Overdrive

Threshold overdrive is how much $V_{(\text{VCC})}$ exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the $\overline{\text{RESET}}$ response. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 公式 1:

$$\text{Overdrive} = |(V_{(\text{VCC})} / V_{\text{IT}} - 1) \times 100\%|$$

where:

- V_{IT} is either $V_{\text{IT-}}$ or $V_{\text{IT+}}$, depending on whether calculating the overdrive for the negative-going threshold or the positive-going threshold, respectively. (1)

图 12 illustrates the VCC minimum detectable pulse versus overdrive, and is used to visualize the relationship overdrive has on $t_{\text{pd}(\text{VCC})}$ for negative-going events.

For positive-going events, after the overdrive is greater than 5%, the changes to t_d are negligible because of the significantly longer delay time. When overdrive is less than 5%, t_d can increase to 200 ms while the device waits for the next voltage reference refresh pulse.

Typical Application (接下页)

8.2.2 Detailed Design Procedure

- Select desired device based on the threshold voltage.
- Ensure that the trace from the input supply to the VCC pin is low impedance in order to avoid false reset signals during the refresh cycle. If the impedance is too high, add an input capacitor of 0.1- μ F or larger close to the VCC pin (see the [Input Capacitor](#) section).
- If the $\overline{\text{RESET}}$ of the TPS3847 is driving a bidirectional pin, place a resistor between the output of the TPS3847 and the bidirectional pin (see the [Driving Bidirectional Reset Pins](#) section).

8.2.3 Application Curves

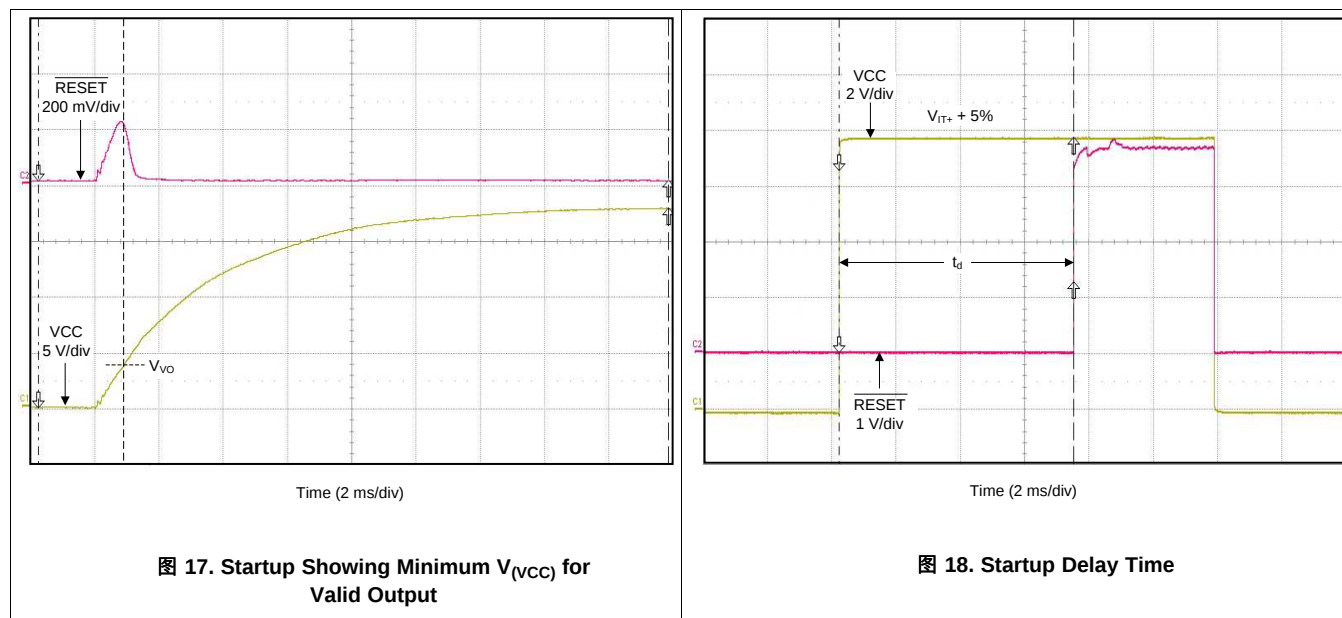


图 17. Startup Showing Minimum $V_{(VCC)}$ for Valid Output

图 18. Startup Delay Time

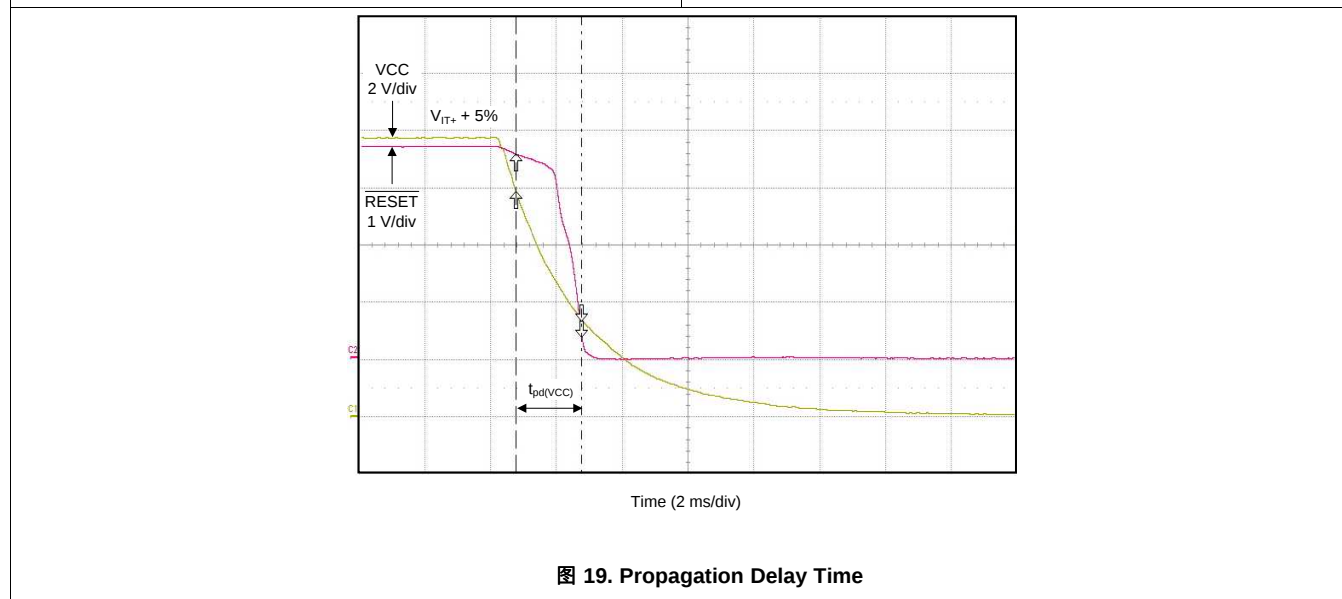


图 19. Propagation Delay Time

8.3 Do's and Don'ts

Connect a 0.1- μ F to 1.0- μ F low equivalent series resistance (ESR) capacitor between the VCC pin and the GND pin.

Connect the $\overline{\text{MR}}$ pin to a voltage higher than 1.2 V in order for $\overline{\text{RESET}}$ to go high or low, depending on the value of $V_{(\text{VCC})}$ relative to $V_{\text{IT-}}$.

Connect the $\overline{\text{MR}}$ pin to a voltage lower than 0.4 V in order to hold $\overline{\text{RESET}}$ low, regardless of the value of $V_{(\text{VCC})}$.

Connect the $\overline{\text{MR}}$ pin to the VCC pin if $\overline{\text{MR}}$ functionality is not used.

Do not connect the VCC pin to a high-impedance supply without a 0.1- μ F to 1.0- μ F low equivalent series resistance (ESR) bypass capacitor.

Do not use a thin, long trace to connect the VCC pin to the input supply without a 0.1- μ F to 1.0- μ F low ESR bypass capacitor.

Do not leave the $\overline{\text{MR}}$ pin floating.

9 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 4.5 V and 18 V. Use a low-impedance power supply to eliminate inaccuracies caused by the current during the voltage-reference refresh.

10 Layout

10.1 Layout Guidelines

Make sure the connection to the VCC pin is low impedance and able to carry 12 μ A without a significant voltage drop. Place a 0.1- μ F bypass capacitor near the VCC pin if the 12- μ A current causes too much voltage droop.

10.2 Layout Example

The layout example in [Figure 20](#) shows how the TPS3847 is laid out on a printed circuit board (PCB). Although not required, use C_{IN} for best device performance.

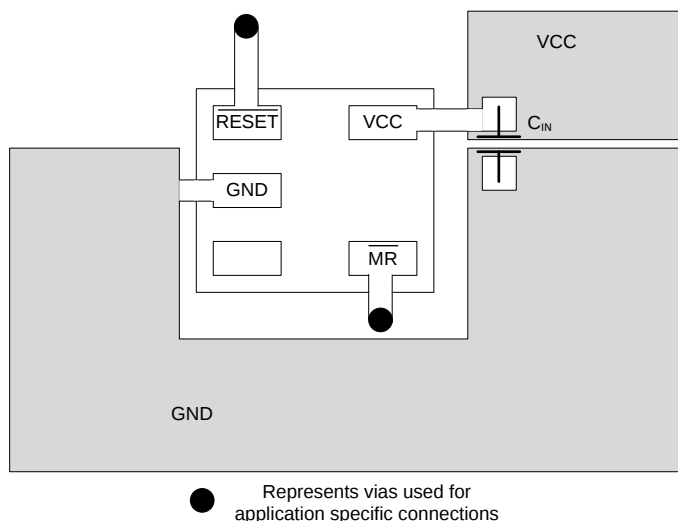


图 20. Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

TPS3847xxxxxx 是此器件的通用命名惯例。TPS3847 代表此类器件所属系列，xxx 用于显示负向阈值电压（第二个数字之后的小数点省略），yyy 保留用于封装标识符。

示例：TPS3847085DBV

系列：TPS3847

负向阈值电压：8.5V

DBV 封装：5 引脚 SOT

11.2 文档支持

11.2.1 相关文档

《TPS3847085EVM-577 评估模块用户指南》，[SBVU023](#)

《TPS62120 数据表》，[SLVSAD5](#)

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11.5 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3847085DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	PC7I	Samples
TPS3847085DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	PC7I	Samples
TPS3847108DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZBYD	Samples
TPS3847108DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZBYD	Samples

⁽¹⁾ The marketing status values are defined as follows:

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⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3847085DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3847085DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS3847108DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3847108DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

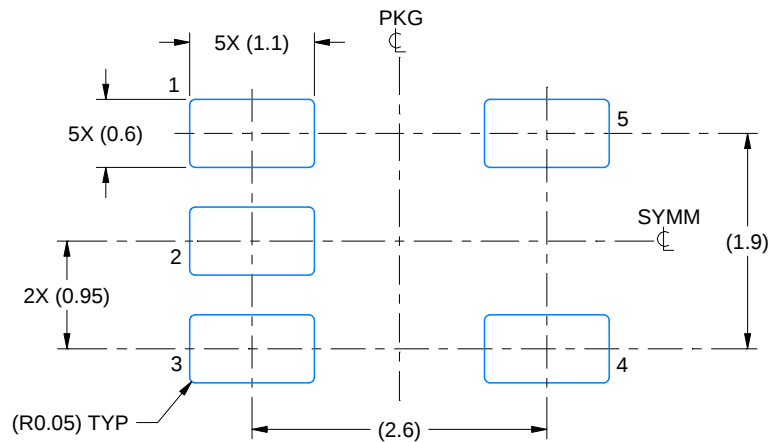
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3847085DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3847085DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3847108DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3847108DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

EXAMPLE BOARD LAYOUT

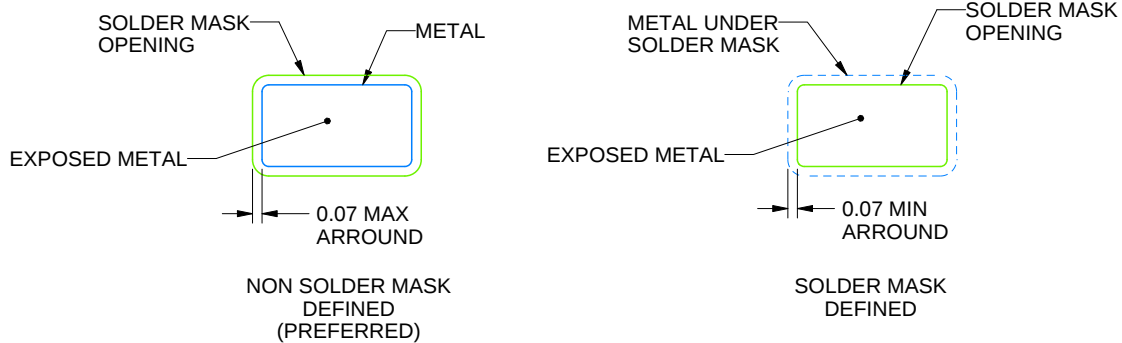
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

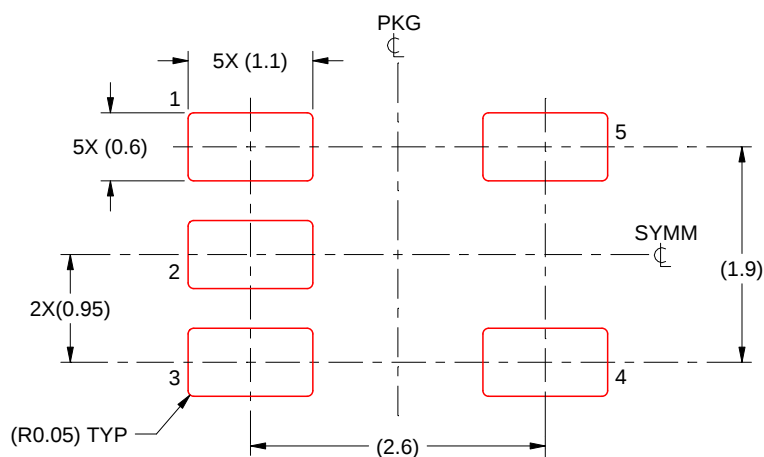
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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