TPS2291xx，5.5V，2A，37mΩ 导通电阻负载开关

1 特性

- 集成单通道负载开关
- 输入电压范围：1.05V 至 5.5V
- 低导通电阻 (R_{ON})
  - V_{IN} = 5V 时，R_{ON} = 37mΩ（典型值）
  - V_{IN}= 3.3V 时，R_{ON} = 38mΩ（典型值）
  - V_{IN} = 1.8V 时，R_{ON} = 43mΩ（典型值）
- 2A 最大持续开关电流
- 低静态电流
  - V_{IN} = 3.3V 时为 7.7μA（典型值）
- 低控制输入阀值允许使用 1.0V 或更高电压的通用输入输出 (GPIO) 接口
- 受控转换率
  - V_{IN} = 3.3V 时，t_R = 64μs
- 快速输出放电（只适用于 TPS22915）
- 超小型晶圆级芯片尺寸封装
  - 0.78mm x 0.78mm，0.4mm 焊球间距，高度 0.5mm (YFP)
- 静电放电 (ESD) 性能经测试符合 JESD 22 规范
  - 2kV 人体模型 (HBM) 和 1kV 充电器件模型 (CDM)

2 应用范围

- 智能手机/手机
- 超薄 / Ultrabook™ / 笔记本电脑
- 平板电脑/平板手机
- 可佩戴技术
- 固态硬盘
- 数码照相机

3 说明

TPS22914B/15B 是一款小型，低 R_{ON}，单通道负载开关，此负载开关具有受控转换率。 此器件包括一个可在 1.05V 至 5.5V 输入电压范围内运行的 N 通道金属氧化物半导体场效应晶体管 (MOSFET)，并可支持 2A 的最大持续电流。此开关由一个开/关输入控制，此输入能够与低电压控制信号直接对接。

小尺寸和低 R_{ON} 使得此器件非常适合于空间受限、电池供电类应用。 此开关的宽输入电压范围使得它成为针对很多不同电压轨的多用途解决方案。 器件的受控上升时间大大减少了由大容量负载电容导致的涌入电流，从而减少或消除了电源消耗。 通过集成一个在开关关闭时实现快速输出放电 (QOD) 的 143Ω 下拉电阻器，TPS22915 进一步减少了总体解决方案尺寸。

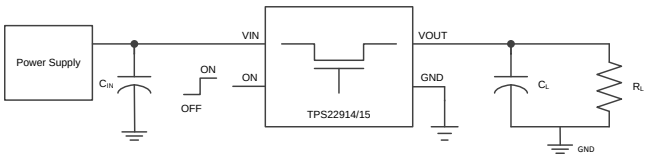
TPS22914B/15B 采用小型、节省空间的 0.78 mm x 0.78 mm，0.4mm 焊球间距，高度 0.5mm，4 引脚晶圆级芯片尺寸 (WCSP) 封装 (YFP)。 器件在自然通风环境下的额定运行温度范围为 -40°C 至 85°C。

器件信息(1)

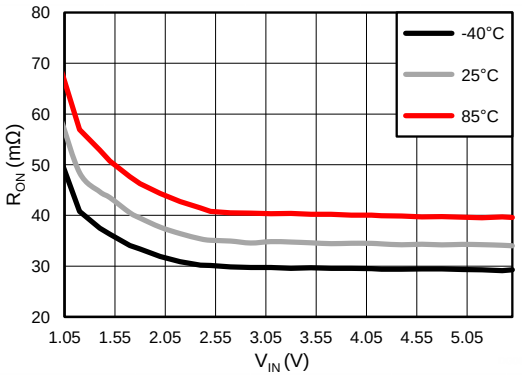
产品型号	封装	封装尺寸（标称值）
TPS22915B	芯片尺寸球状引脚栅格阵列 (DSBGA) (4)	0.78mm x 0.78mm
TPS22914B		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



R_{ON} 与 V_{IN} 之间的关系 (I_{OUT} = -200mA)



目录

5 修订历史记录

Changes from Original (June 2014) to Revision A **Page**

- 完整版的最初发布版本。 ... 1

6 Device Comparison Table

DEVICE	R_{ON} at 3.3V (TYP)	t_R at 3.3V (TYP)	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22914B	38 mΩ	64 µs	No	2 A	Active High
TPS22915B	38 mΩ	64 µs	Yes	2 A	Active High

7 Pin Configuration and Functions

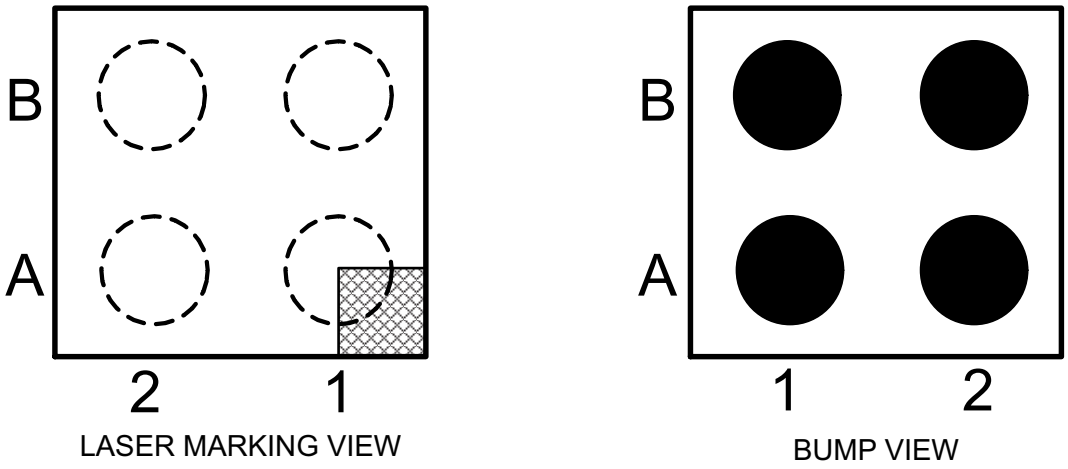


Table 1. Pin Description

B	ON	GND
A	VIN	VOUT
	2	**1**

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VOUT	A1	O	Switch output. Place ceramic bypass capacitor(s) between this pin and GND. See the *Detailed Description* section for more information.
VIN	A2	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND. See the *Detailed Description* section for more information.
GND	B1	-	Device ground.
ON	B2	I	Active high switch control input. Do not leave floating.

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	–0.3	6	V
V_{OUT}	Output voltage range	–0.3	6	V
V_{ON}	ON voltage range	–0.3	6	V
I_{MAX}	Maximum continuous switch current		2	A
I_{PLS}	Maximum pulsed switch current, pulse < 300 µs, 2% duty cycle		2.5	A
T_J	Maximum junction temperature		125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)			300	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2	KV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage range		1.05	5.5	V
V_{ON}	ON voltage range		0	5.5	V
V_{OUT}	Output voltage range			V_{IN}	V
$V_{IH, ON}$	High-level input voltage, ON	V_{IN} = 1.05 V to 5.5 V	1	5.5	V
$V_{IL, ON}$	Low-level input voltage, ON	V_{IN} = 1.05 V to 5.5 V	0	0.5	V
T_A	Operating free-air temperature range(1)		–40	85	°C
C_{IN}	Input Capacitor		1(2)		µF

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(MAX)}$], the maximum power dissipation of the device in the application [$P_{D(MAX)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(MAX)} = T_{J(MAX)} – (\theta_{JA} \times P_{D(MAX)})$.
(2) Refer to *Detailed Description* section

8.4 Thermal Information

THERMAL METRIC(1)		TPS22914 / TPS22915 YFP 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	2.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	36	
ψ_{JT}	Junction-to-top characterization parameter	12	
ψ_{JB}	Junction-to-board characterization parameter	36	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40°C ≤ T_A ≤ 85°C (Full). Typical values are for T_A = 25°C.

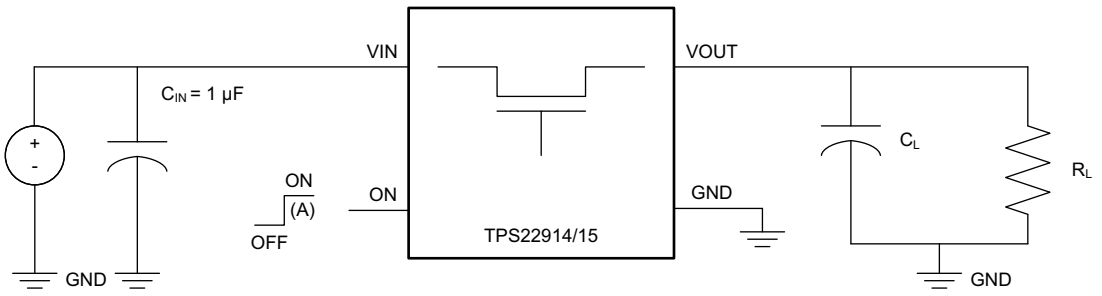
PARAMETER		TEST CONDITION		T_A	MIN	TYP	MAX	UNIT
$I_{Q, VIN}$	Quiescent current	V_{ON} = 5 V, I_{OUT} = 0 A	V_{IN} = 5.5 V	Full		7.7	10.8	µA
			V_{IN} = 5.0 V			7.6	9.6	
			V_{IN} = 3.3 V			7.7	9.6	
			V_{IN} = 1.8 V			8.4	11.0	
			V_{IN} = 1.2 V			7.4	10.4	
			V_{IN} = 1.05 V			6.7	10.9	
$I_{SD, VIN}$	Shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V	V_{IN} = 5.5 V	Full		0.5	2	µA
			V_{IN} = 5.0 V			0.5	2	
			V_{IN} = 3.3 V			0.5	2	
			V_{IN} = 1.8 V			0.5	2	
			V_{IN} = 1.2 V			0.4	2	
			V_{IN} = 1.05 V			0.4	2	
I_{ON}	ON pin input leakage current	V_{IN} = 5.5 V, I_{OUT} = 0 A		Full			0.1	µA
R_{ON}	On-Resistance	V_{IN} = 5.5 V, I_{OUT} = –200 mA		25°C		37	40	mΩ
				Full			51	
		V_{IN} = 5.0 V, I_{OUT} = –200 mA		25°C		37	41	mΩ
				Full			51	
		V_{IN} = 4.2 V, I_{OUT} = –200 mA		25°C		37	41	mΩ
				Full			52	
		V_{IN} = 3.3 V, I_{OUT} = –200 mA		25°C		38	41	mΩ
				Full			52	
		V_{IN} = 2.5 V, I_{OUT} = –200 mA		25°C		38	42	mΩ
				Full			53	
		V_{IN} = 1.8 V, I_{OUT} = –200 mA		25°C		43	48	mΩ
				Full			59	
		V_{IN} = 1.2 V, I_{OUT} = –200 mA		25°C		52	61	mΩ
				Full			73	
		V_{IN} = 1.05 V, I_{OUT} = –200 mA		25°C		63	96	mΩ
				Full			102	
V_{HYS}	ON pin hysteresis	V_{IN} = 5.5 V		Full		102		mV
		V_{IN} = 5.0 V		Full		100		
		V_{IN} = 3.3 V		Full		98		
		V_{IN} = 2.5 V		Full		96		
		V_{IN} = 1.8 V		Full		96		
		V_{IN} = 1.2 V		Full		94		
		V_{IN} = 1.05 V		Full		92		
R_{PD} (1)	Output pull down resistor	V_{IN} = V_{OUT} = 3.3 V, V_{ON} = 0 V		Full		143	200	Ω

(1) TPS22915B only.

8.6 Switching Characteristics

Refer to the timing test circuit in Figure 1 (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where VIN is already in steady state condition before the ON pin is asserted high.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = 5 V, V_{ON} = 5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		104		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		2		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		89		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		2		µs
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		59		µs
V_{IN} = 3.3 V, V_{ON} = 5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		83		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		2		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		64		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		2		µs
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		52		µs
V_{IN} = 1.05 V, V_{ON} = 5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		61		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		3		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		28		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		2		µs
t_D	Delay time	R_L = 10 Ω, C_{IN} = 1 µF, C_{OUT} = 0.1 µF		47		µs



A. Rise and fall times of the control signal is 100ns

Figure 1. Test Circuit

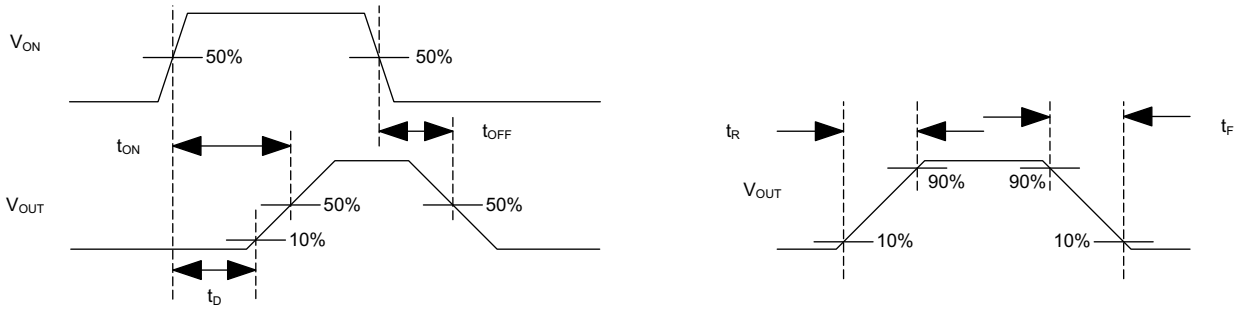
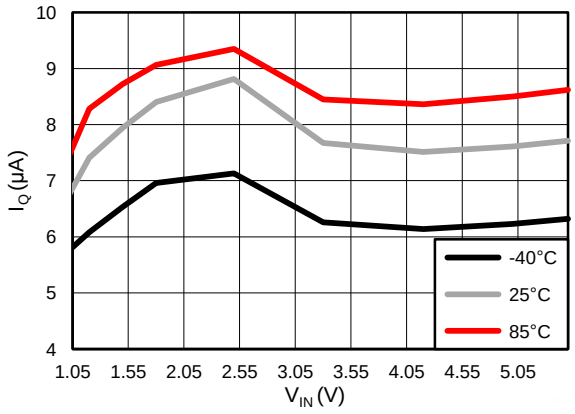


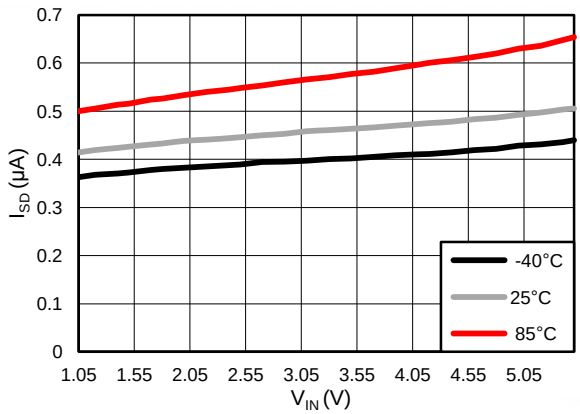
Figure 2. Timing Waveforms

8.7 Typical DC Characteristics



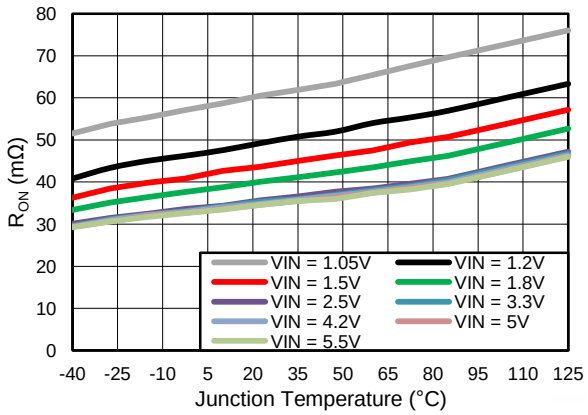
V_{ON} = 5 V I_{OUT} = 0 A

Figure 3. I_Q vs V_{IN}



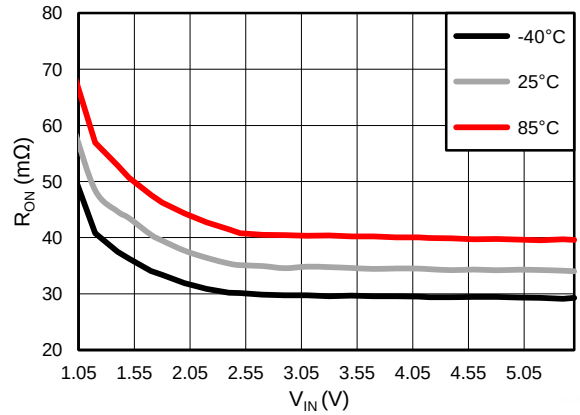
V_{ON} = 0 V I_{OUT} = 0 A

Figure 4. I_{SD} vs V_{IN}



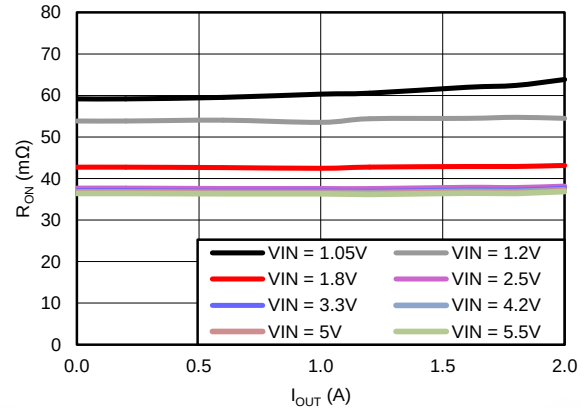
V_{ON} = 5 V I_{OUT} = –200 mA

Figure 5. R_{ON} vs T_J



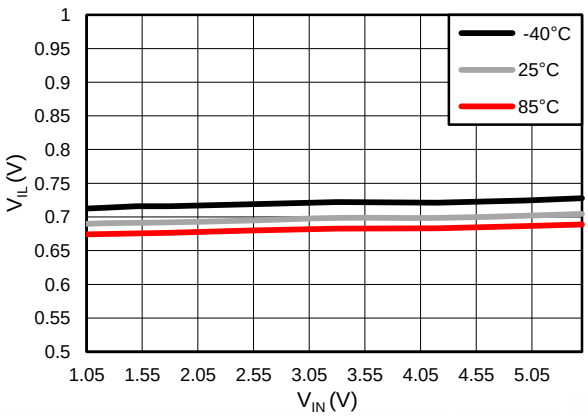
V_{ON} = 5 V I_{OUT} = –200 mA

Figure 6. R_{ON} vs V_{IN}



V_{ON} = 5 V T_A = 25°C

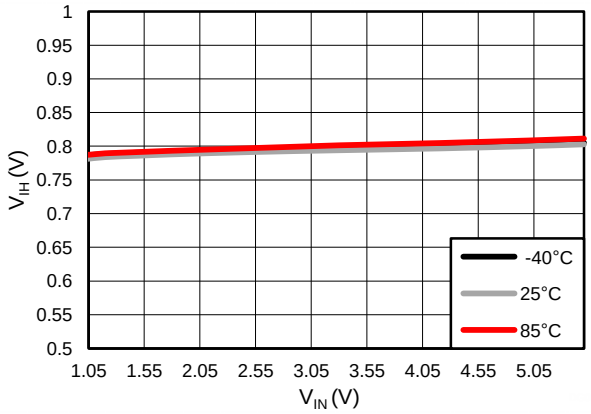
Figure 7. R_{ON} vs I_{OUT}



I_{OUT} = 0 A

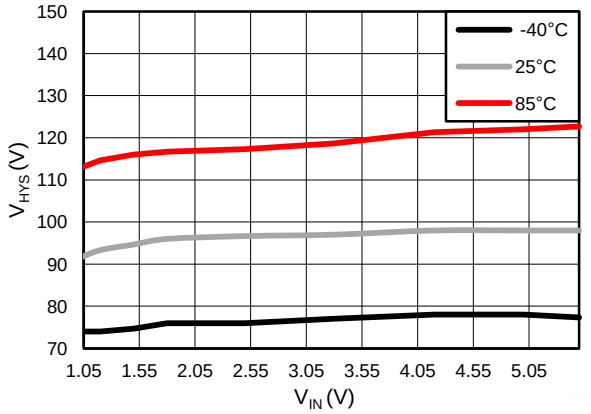
Figure 8. V_{IL} vs V_{IN}

Typical DC Characteristics (continued)



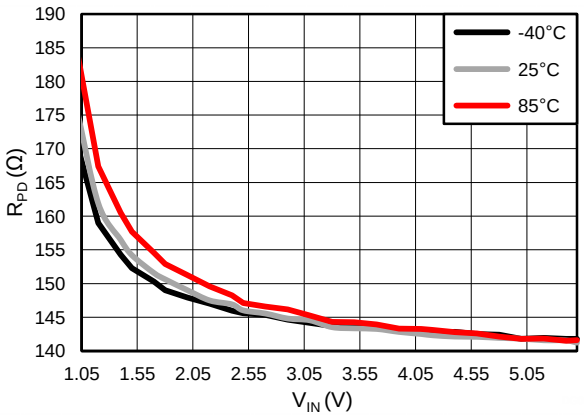
I_{OUT} = 0 A

Figure 9. V_{IH} vs V_{IN}



I_{OUT} = 0 A

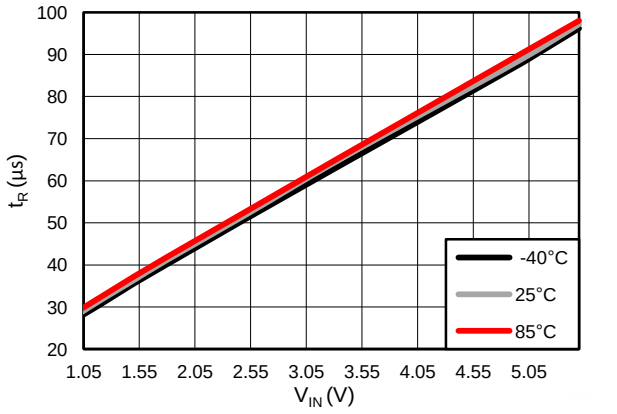
Figure 10. V_{HYS} vs V_{IN}



$V_{IN} = V_{OUT}$ V_{ON} = 0 V

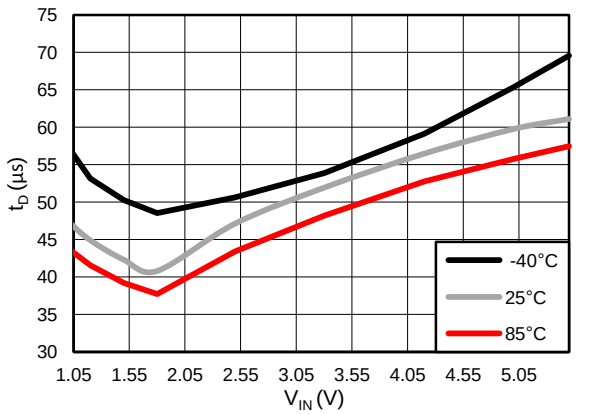
Figure 11. R_{PD} vs V_{IN}

8.8 Typical AC Characteristics



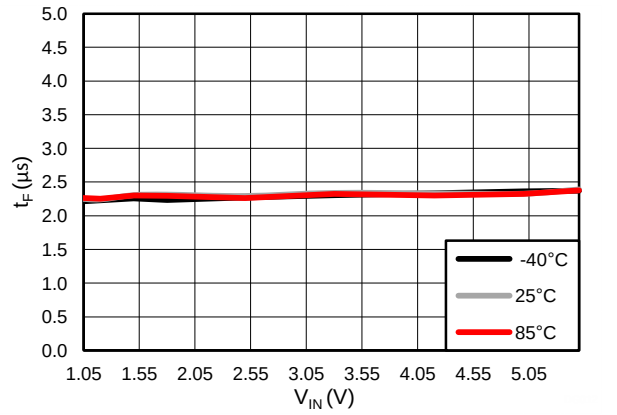
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 12. t_R vs V_{IN}



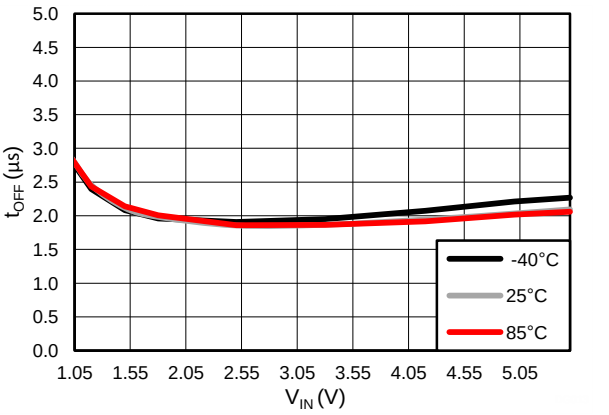
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 13. t_D vs V_{IN}



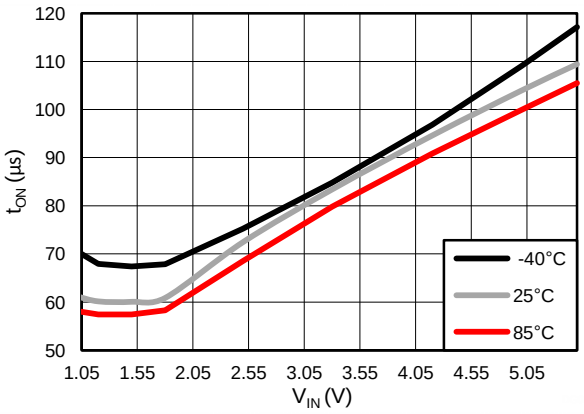
C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 14. t_F vs V_{IN}



C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 15. t_{OFF} vs V_{IN}



C_{IN} = 1 µF R_L = 10 Ω C_L = 0.1 µF

Figure 16. t_{ON} vs V_{IN}

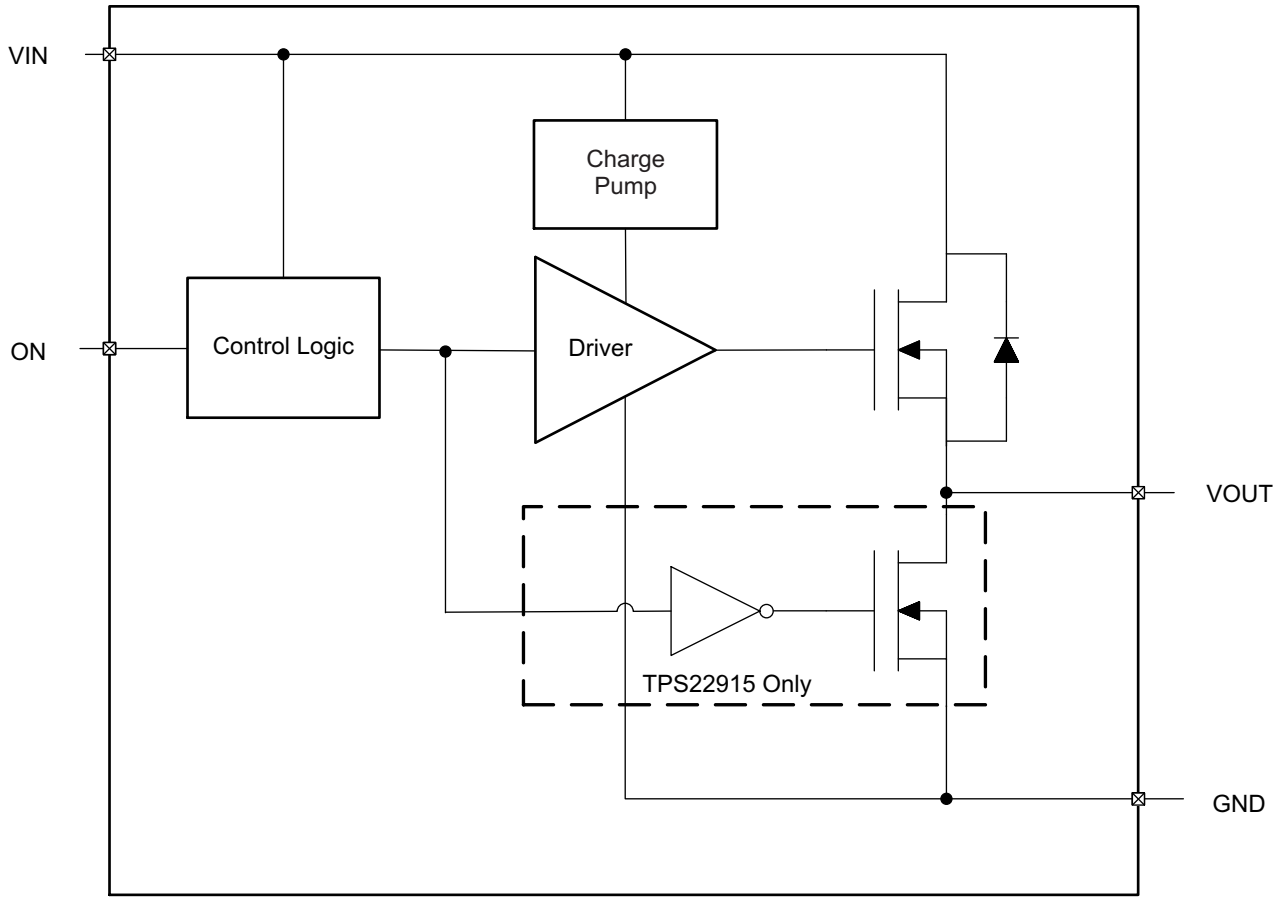
9 Detailed Description

9.1 Overview

The device is a 5.5-V, 2-A load switch in a 4-pin YFP package. To reduce voltage drop for low voltage and high current rails, the device implements an ultra-low resistance N-channel MOSFET which reduces the drop out voltage through the device.

The device has a controlled and fixed slew rate which helps reduce or eliminate power supply droop due to large inrush currents. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 On/Off Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.0-V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

Feature Description (continued)

9.3.2 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.3.3 Output Capacitor (C_L)

Due to the integrated body diode in the MOSFET, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

9.4 Device Functional Modes

Table 2 describes the connection of the VOUT pin depending on the state of the ON pin.

Table 2. VOUT Connection

ON	TPS22914	TPS22915
L	Open	GND
H	VIN	VIN

10 Application and Implementation

10.1 Application Information

This section will highlight some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com for further aid.

10.2 Typical Application

This typical application demonstrates how the TPS22914 and TPS22915 can be used to power downstream modules.

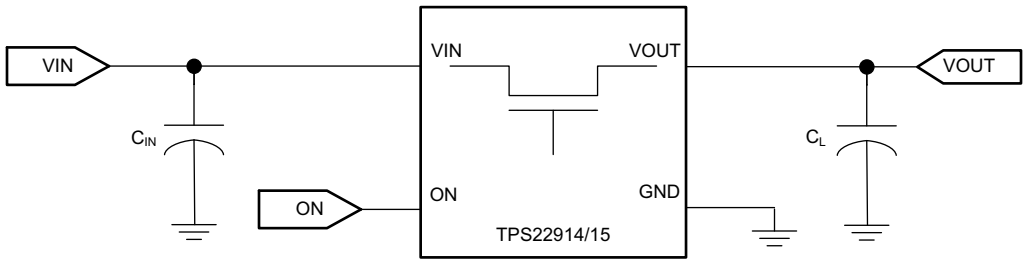


Figure 17. Typical Application Schematic

10.2.1 Design Requirements

For this design example, use the following as the input parameters:

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	5.0 V
Load Current	2 A

10.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- V_{IN} voltage
- Load Current

10.2.2.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN conditions of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table of this datasheet. Once the R_{ON} of the device is determined based upon the VIN conditions, use Equation 1 to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (1)$$

Where:

ΔV = voltage drop from VIN to VOUT
I_{LOAD} = load current
R_{ON} = On-resistance of the device for a specific V_{IN}

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.2.2.2 Inrush Current

To determine how much inrush current will be caused by the C_L capacitor, use Equation 2:

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt} \quad (2)$$

Where:

I_{INRUSH} = amount of inrush caused by C_L
C_L = capacitance on VOUT
dt = rise time in VOUT during the ramp up of VOUT when the device is enabled
dV_{OUT} = change in VOUT during the ramp up of VOUT when the device is enabled

An appropriate C_L value should be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

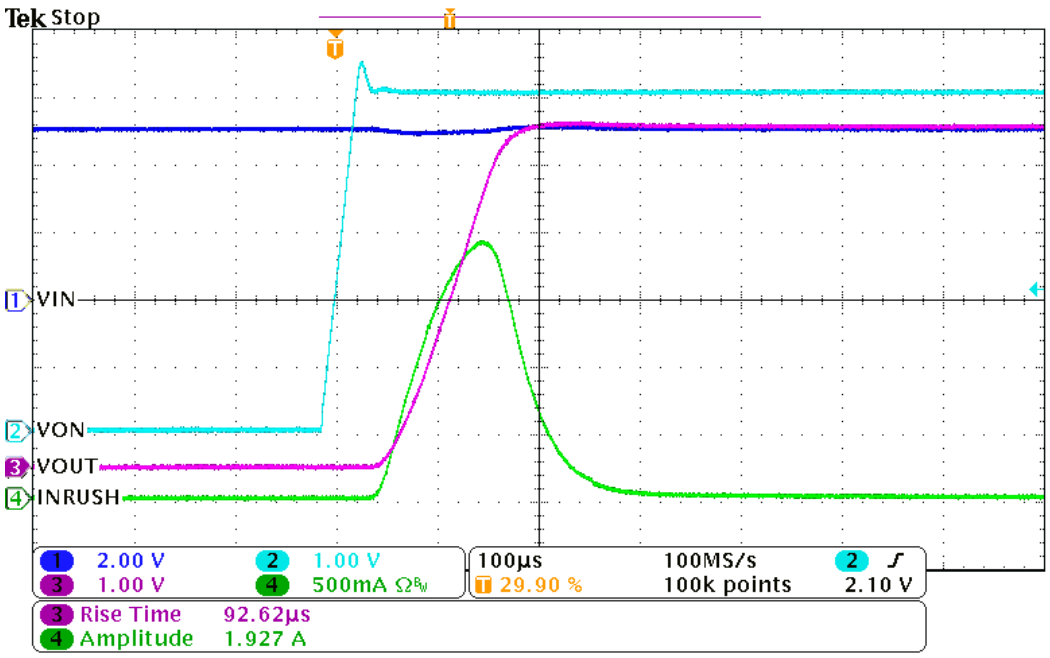
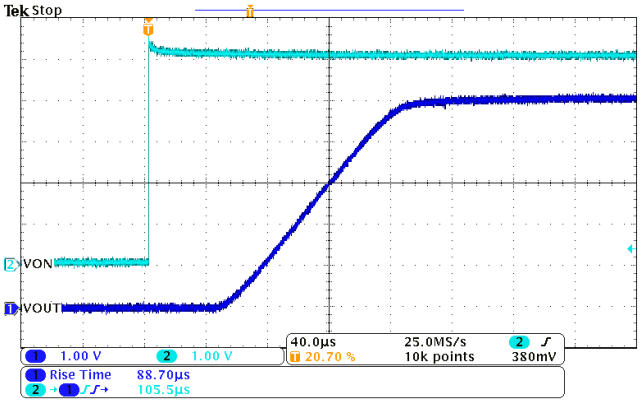


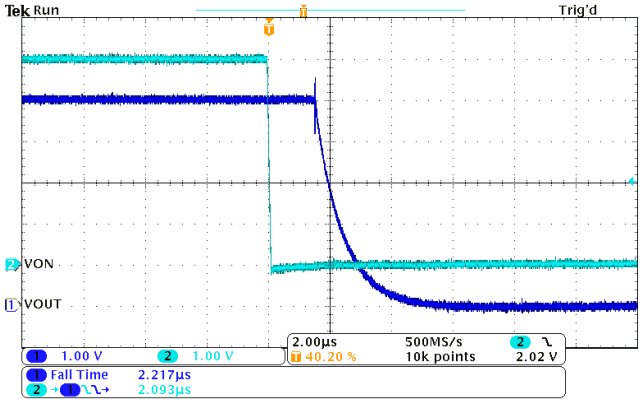
Figure 18. Inrush Current (V_{IN} = 5 V, C_L = 47 µF)

10.2.3 Application Curves



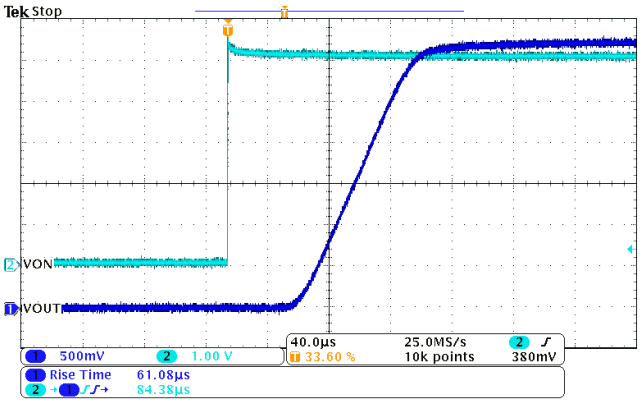
V_{IN} = 5 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 19. t_R at V_{IN} = 5 V



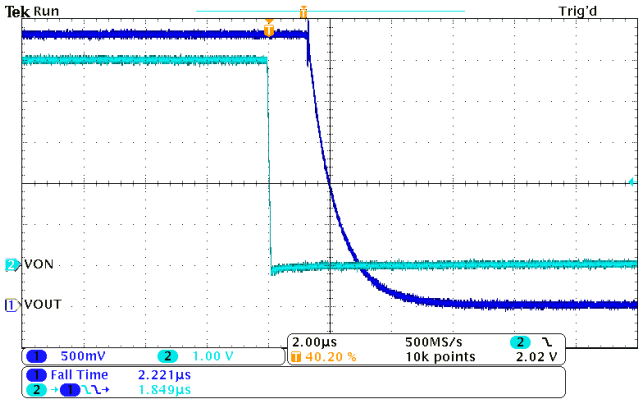
V_{IN} = 5 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 20. t_F at V_{IN} = 5 V



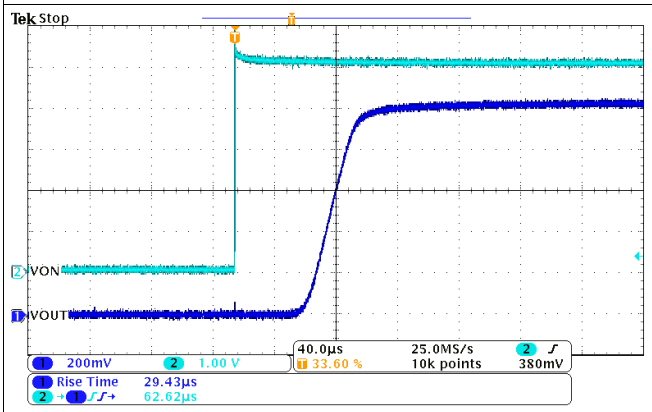
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 21. t_R at V_{IN} = 3.3 V



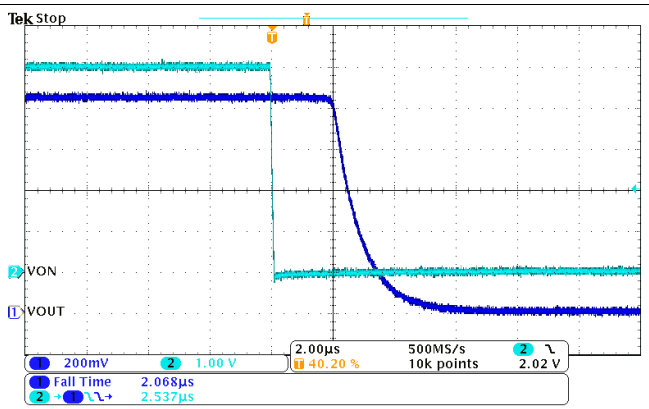
V_{IN} = 3.3 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 22. t_F at V_{IN} = 3.3V



V_{IN} = 1.05 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 23. t_R at V_{IN} = 1.05V



V_{IN} = 1.05 V C_{IN} = 1 µF C_L = 0.1 µF
R_L = 10 Ω

Figure 24. t_F at V_{IN} = 1.05 V

11 Power Supply Recommendations

The device is designed to operate from a VIN range of 1.05 V to 5.5 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1 µF may be sufficient.

12 Layout

12.1 Layout Guidelines

1. VIN and VOUT traces should be as short and wide as possible to accommodate for high current.
2. The VIN pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
3. The VOUT pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.

12.1.1 Thermal Considerations

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 3:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (3)$$

Where:

$P_{D(MAX)}$ = maximum allowable power dissipation
$T_{J(MAX)}$ = maximum allowable junction temperature (125°C for the TPS22914/15)
T_A = ambient temperature of the device
θ_{JA} = junction to air thermal impedance. Refer to the *Thermal Information* table. This parameter is highly dependent upon board layout.

12.2 Layout Example

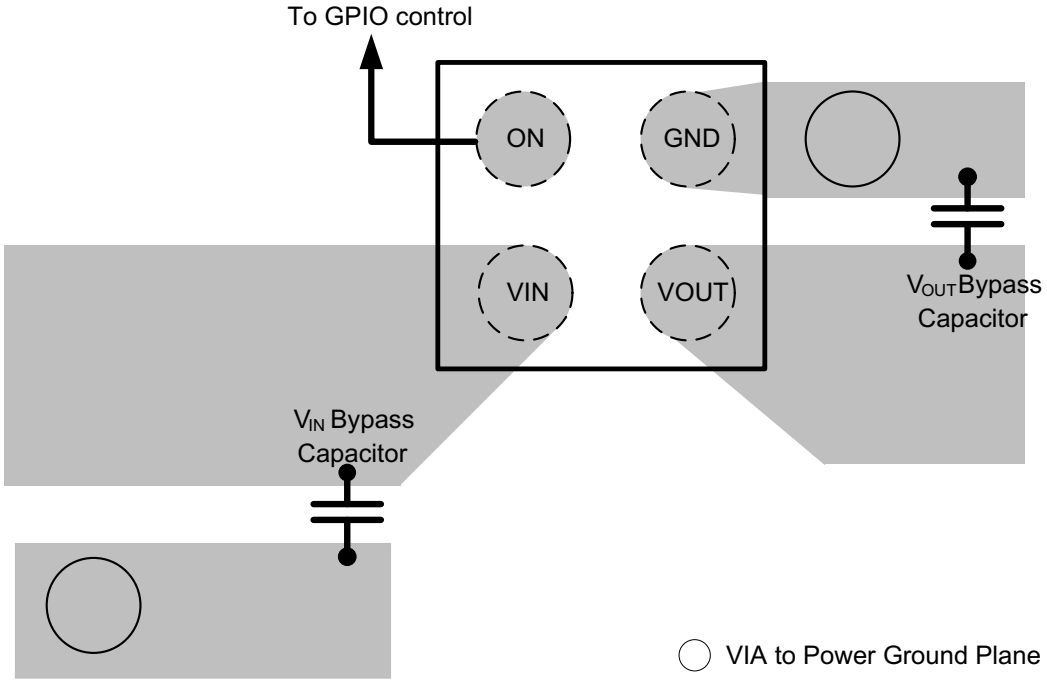


Figure 25. Recommended Board Layout

13 器件和文档支持

13.1 Trademarks

Ultrabook is a trademark of Intel.
All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

14 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22914BYFPR	ACTIVE	DSBGA	YFP	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	S3	Samples
TPS22914BYFPT	ACTIVE	DSBGA	YFP	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	S3	Samples
TPS22914CYFPR	ACTIVE	DSBGA	YFP	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	S6	Samples
TPS22914CYFPT	ACTIVE	DSBGA	YFP	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	S6	Samples
TPS22915BYFPR	ACTIVE	DSBGA	YFP	4	3000	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 105	S4	Samples
TPS22915BYFPT	ACTIVE	DSBGA	YFP	4	250	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 105	S4	Samples
TPS22915CYFPR	ACTIVE	DSBGA	YFP	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	S7	Samples
TPS22915CYFPT	ACTIVE	DSBGA	YFP	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	S7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

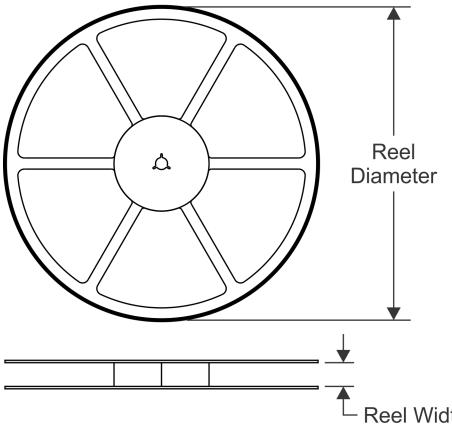
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

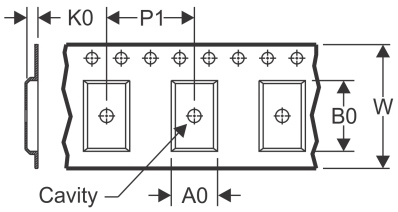
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

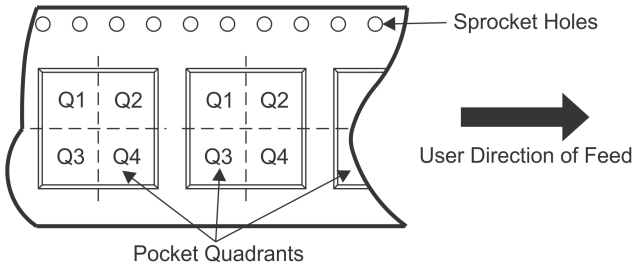


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

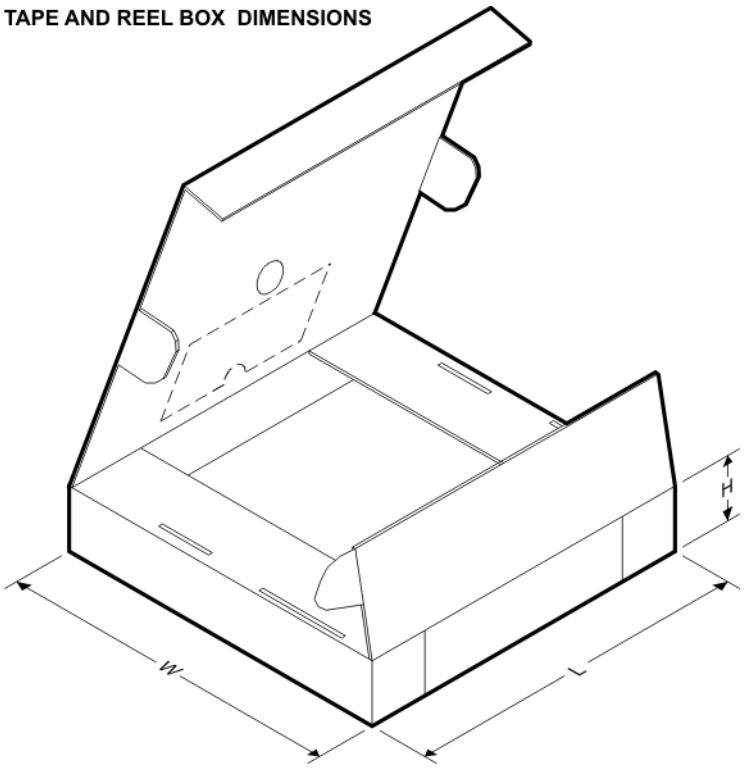
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22914BYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22914BYFPR	DSBGA	YFP	4	3000	178.0	9.2	0.85	0.85	0.59	4.0	8.0	Q1
TPS22914BYFPT	DSBGA	YFP	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22914BYFPT	DSBGA	YFP	4	250	178.0	9.2	0.85	0.85	0.59	4.0	8.0	Q1
TPS22914CYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22914CYFPT	DSBGA	YFP	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22915BYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22915BYFPR	DSBGA	YFP	4	3000	178.0	9.2	0.85	0.85	0.59	4.0	8.0	Q1
TPS22915BYFPT	DSBGA	YFP	4	250	178.0	9.2	0.85	0.85	0.59	4.0	8.0	Q1
TPS22915BYFPT	DSBGA	YFP	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22915CYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TPS22915CYFPT	DSBGA	YFP	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

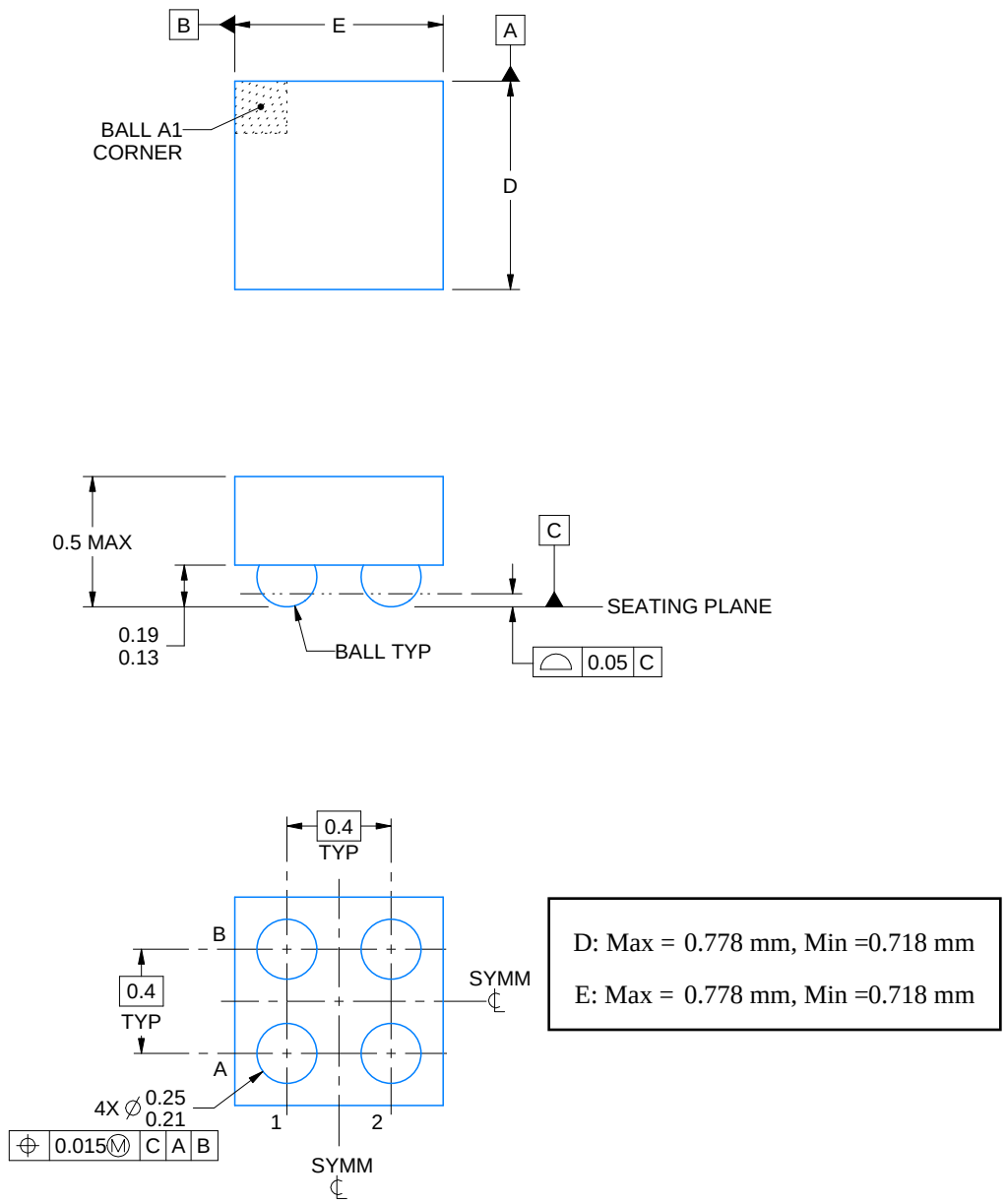
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22914BYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22914BYFPR	DSBGA	YFP	4	3000	220.0	220.0	35.0
TPS22914BYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22914BYFPT	DSBGA	YFP	4	250	220.0	220.0	35.0
TPS22914CYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22914CYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22915BYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22915BYFPR	DSBGA	YFP	4	3000	220.0	220.0	35.0
TPS22915BYFPT	DSBGA	YFP	4	250	220.0	220.0	35.0
TPS22915BYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22915CYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22915CYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFP0004

DSBGA - 0.5 mm max height

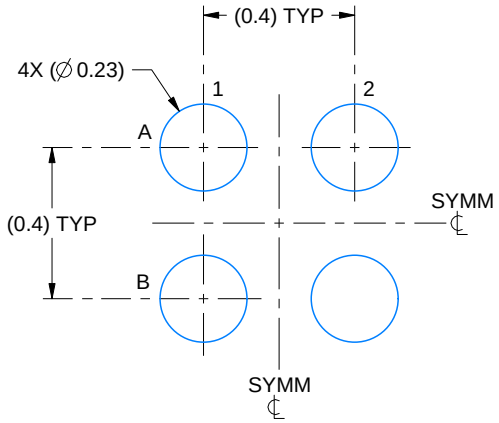
DIE SIZE BALL GRID ARRAY



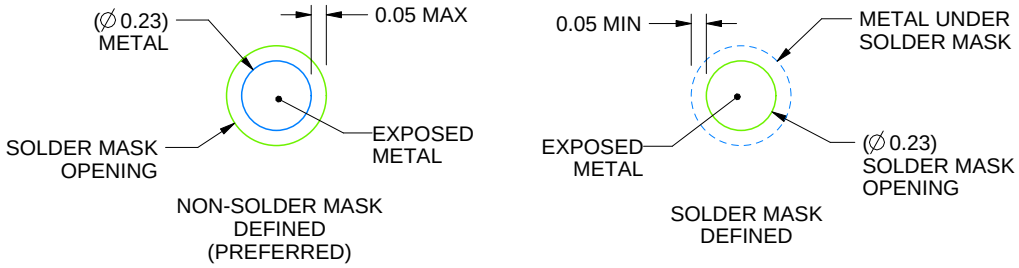
4223507/A 01/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223507/A 01/2017

NOTES: (continued)

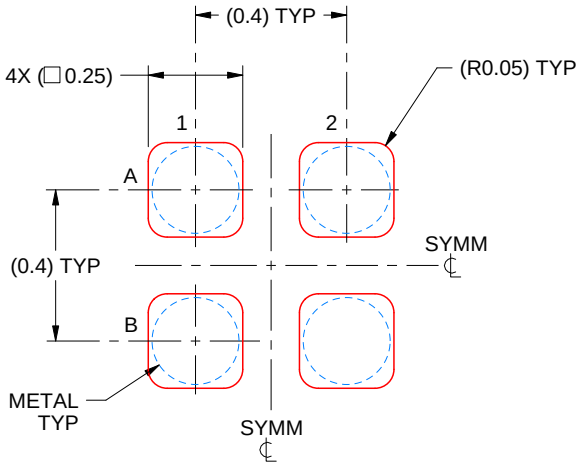
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223507/A 01/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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