

TPS22916xx 1V 至 5.5V、2A、60mΩ 超低泄漏负载开关

1 特性

- 输入工作电压范围 (V_{IN}): 1V 至 5.5V
- 最大持续电流 (I_{MAX}): 2A
- 导通电阻 (R_{ON}):
 - $5V_{IN} = 60m\Omega$ (典型值)、 $100m\Omega$ ($85^{\circ}C$ 最大值)
 - $1.8V_{IN} = 100m\Omega$ (典型值)、 $150m\Omega$ ($85^{\circ}C$ 最大值)
 - $1V_{IN} = 200m\Omega$ (典型值)、 $325m\Omega$ ($85^{\circ}C$ 最大值)
- 超低功耗:
 - ON 状态 (I_Q): $0.5\mu A$ (典型值)、 $1\mu A$ (最大值)
 - OFF 状态 (I_{SD}): $10nA$ (典型值)、 $100nA$ (最大值)
 - TPS22916CL (I_{SD}): $100nA$ (典型值)、 $300nA$ (最大值)
- 智能 ON 引脚下拉电阻 (R_{PD}):
 - $ON \geq V_{IH}$ (I_{ON}): $10nA$ (最大值)
 - $ON \leq V_{IL}$ (R_{PD}): $750k\Omega$ (典型值)
- C 版本的慢时序可限制浪涌电流:
 - 5V 开通时间 (t_{ON}): $5mV/\mu s$ 时为 $1400\mu s$
 - 1.8V 开通时间 (t_{ON}): $1mV/\mu s$ 时为 $3000\mu s$
 - 1V 开通时间 (t_{ON}): $0.3mV/\mu s$ 时为 $6500\mu s$
- B 版本的快时序可减少等待时间:
 - 5V 开通时间 (t_{ON}): $57mV/\mu s$ 时为 $115\mu s$
 - 1.8V 开通时间 (t_{ON}): $12mV/\mu s$ 时为 $250\mu s$
 - 1V 开通时间 (t_{ON}): $3.3mV/\mu s$ 时为 $510\mu s$
- 常开的真反向电流阻断 (RCB):
 - 激活电流 (I_{RCB}): $-500mA$ (典型值)
 - 反向泄漏电流 ($I_{IN,RCB}$): $-300nA$ (最大值)
- 快速输出放电 (QOD): 150Ω (典型值) (N 版本没有 QOD)
- 低电平有效使能选项 (L 版本)

2 应用

- 可穿戴
- 智能电话
- 平板电脑
- 便携式扬声器

3 说明

TPS22916xx 是一款小型单通道负载开关, 采用低漏电流 P 沟道 MOSFET 实现最小的功率损耗。高级门控设计支持低至 1V 的工作电压, 且增加的导通电阻和功率损耗极小。

多个时序选项可支持各种系统负载条件。对于高容性负载, C 版本的慢速导通时序可最大限度减小浪涌电流。而在低容性负载中, B 版本的快速时序可减少所需的等待时间。

开关导通状态由数字输入控制, 此输入可与低压控制信号直接连接。此器件同时提供高电平有效和低电平有效 (L) 版本。首次加电时, 此器件使用智能下拉电阻来保持 ON 引脚不悬空, 直到系统定序完成。一旦 ON 引脚故意驱动为高电平 ($\geq V_{IH}$), 便会断开智能下拉电阻, 从而防止不必要的功率损耗。

器件信息⁽¹⁾

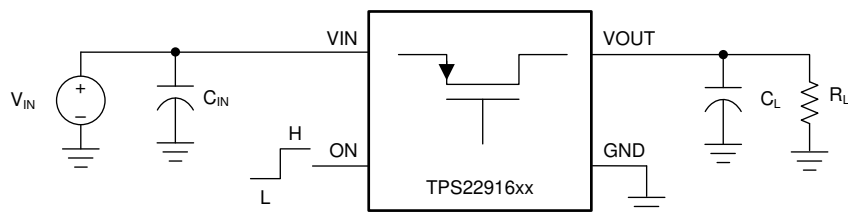
器件型号	封装	封装尺寸 (标称值)
TPS22916xx	WCSP (4)	$0.78mm \times 0.78mm$

(1) 如需了解所有可用封装, 请参阅产品说明书末尾的可订购产品附录。

器件比较表

版本	时序	QOD	使能 (ON)
TPS22916B	快	是	高电平有效
TPS22916C	慢	是	高电平有效
TPS22916CN	慢	否	高电平有效
TPS22916CL	慢	是	低电平有效

简化原理图



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4 修订历史记录

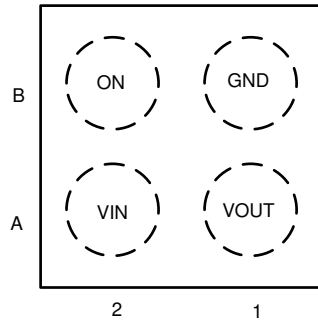
Changes from Revision C (October 2018) to Revision D	Page
• 将封装尺寸从 0.74mm x 0.74mm 更改成了 0.78mm x 0.78mm	3
Changes from Revision B (December 2017) to Revision C	Page
• 已更改 更改了封装图尺寸	22
Changes from Revision A (September 2017) to Revision B	Page
• 已更改 激光打标标记过的引脚图	1
Changes from Original (July 2017) to Revision A	Page
• 已更改 将器件文档从“高级信息”更改为“生产数据”	3

5 说明（续）

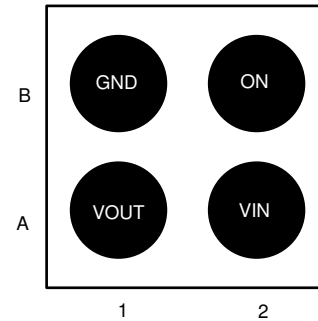
TPS22916xx 采用节省空间的小型 $0.78\text{mm} \times 0.78\text{mm}$ 、 0.4mm 间距、 0.5mm 高度的 4 引脚晶圆芯片级 (WCSP) 封装 (YFP)。此器件的工作温度范围为 -40°C 至 $+85^{\circ}\text{C}$ 。

6 Pin Configuration and Functions

**YFP Package
4-Pin WSON
Laser Marking View**



**YFP Package
4-Pin WSON
Bump View**



TPS22916xx Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	VOUT	Power	Switch output
A2	VIN	Power	Switch input
B1	GND	Ground	Device ground
B2	ON	Digital input	Device enable

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage	−0.3	6	V
V _{OUT}	Output voltage	−0.3	6	V
V _{ON}	Enable voltage	−0.3	6	V
I _{MAX}	Maximum continuous switch current		2	A
I _{PLS}	Maximum pulsed switch current, pulse < 300-μs, 2% duty cycle		2.5	A
T _{J,MAX}	Maximum junction temperature		125	°C
T _{STG}	Storage temperature	−65	150	°C
T _{LEAD}	Maximum Lead temperature (10-s soldering time)		300	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Input voltage	1	5.5	V
V _{OUT}	Output voltage	0	5.5	V
V _{IH}	High-level input voltage, ON	1	5.5	V
V _{IL}	Low-level input voltage, ON	0	0.35	V
T _A	Operating free-air temperature	−40	85	°C

7.4 Thermal Information

Thermal Parameters ⁽¹⁾		TPS22916xx	UNIT
		YFP (WCSP)	
		4 PINS	
θ _{JA}	Junction-to-ambient thermal resistance	193	°C/W
θ _{JCtop}	Junction-to-case (top) thermal resistance	2.3	°C/W
θ _{JB}	Junction-to-board thermal resistance	36	°C/W
ψ _{JT}	Junction-to-top characterization parameter	12	°C/W
ψ _{JB}	Junction-to-board characterization parameter	36	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies for all variants over the entire recommended power supply voltage range of 1 V to 5.5 V unless noted otherwise. Typical Values are at 25°C.

PARAMETER		TEST CONDITIONS	T _J	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VIN)							
I _{Q,VIN}	V _{IN} Quiescent current	Enabled, V _{OUT} = Open	–40°C to +85°C	0.5	1.0		μA
I _{SD,VIN}	V _{IN} Shutdown current	Disabled, V _{OUT} = GND (TPS22916B/C/CN)	–40°C to +85°C	10	100		nA
		Disabled, V _{OUT} = GND (TPS22916CL)	–40°C to +85°C	100	300		nA
ON-RESISTANCE (R _{ON})							
R _{ON}	ON-Resistance	I _{OUT} = 200 mA	V _{IN} = 5 V	25°C	60	80	mΩ
				–40°C to +85°C		100	
				–40°C to +105°C		120	
			V _{IN} = 3.6 V	25°C	70	90	
				–40°C to +85°C		120	
				–40°C to +105°C		140	
			V _{IN} = 1.8 V	25°C	100	125	
				–40°C to +85°C		150	
				–40°C to +105°C		175	
			V _{IN} = 1.2 V	25°C	150	200	
				–40°C to +85°C		250	
				–40°C to +105°C		300	
			V _{IN} = 1 V	25°C	200	275	
				–40°C to +85°C		325	
				–40°C to +105°C		375	
ENABLE PIN (ON)							
I _{ON}	ON Pin leakage	Enabled	–40°C to +85°C	–10		10	nA
R _{PD}	Smart Pull Down Resistance	Disabled	–40°C to +85°C		750		kΩ
REVERSE CURRENT BLOCKING (RCB)							
I _{RCB}	RCB Activation Current	Enabled, V _{OUT} > V _{IN}	–40°C to +85°C	–500			mA
t _{RCB}	RCB Activation time	Enabled, V _{OUT} > V _{IN} + 200mV	–40°C to +85°C	10			μs
V _{RCB}	RCB Release Voltage	Enabled, V _{OUT} > V _{IN}	–40°C to +85°C	25			mV
I _{IN,RCB}	VIN Reverse Leakage Current	0 V ≤ V _{IN} + V _{RCB} ≤ V _{OUT} ≤ 5.5 V	–40°C to +85°C	–300			nA
QUICK OUTPUT DISCHARGE (QOD)							
QOD ⁽¹⁾	Output discharge resistance	Disabled (Not in TPS22916CN)	–40°C to +85°C		150		Ω

(1) For more information on which devices include quick output discharge, see the [Device Functional Modes](#) section.

7.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies over the entire recommended power supply voltage range of 1 V to 5.5 V at 25°C with a load of $C_L = 0.1\mu\text{F}$, $R_L = 10\Omega$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPS22916B						
t_{ON}	Turn On Time	$V_{\text{IN}} = 5\text{ V}$		115		μs
		$V_{\text{IN}} = 3.6\text{ V}$		140		
		$V_{\text{IN}} = 1.8\text{ V}$		250		
		$V_{\text{IN}} = 1.2\text{ V}$		350		
		$V_{\text{IN}} = 1\text{ V}$		510		
t_{RISE}	Rise Time	$V_{\text{IN}} = 5\text{ V}$		70		μs
		$V_{\text{IN}} = 3.6\text{ V}$		80		
		$V_{\text{IN}} = 1.8\text{ V}$		130		
		$V_{\text{IN}} = 1.2\text{ V}$		190		
		$V_{\text{IN}} = 1\text{ V}$		240		
SR_{ON}	Slew Rate	$V_{\text{IN}} = 5\text{ V}$		57		$\text{mV}/\mu\text{s}$
		$V_{\text{IN}} = 3.6\text{ V}$		36		
		$V_{\text{IN}} = 1.8\text{ V}$		12		
		$V_{\text{IN}} = 1.2\text{ V}$		5.1		
		$V_{\text{IN}} = 1\text{ V}$		3.3		
t_{OFF}	Turn Off Time	$V_{\text{IN}} = 5\text{ V}$		5		μs
		$V_{\text{IN}} = 3.6\text{ V}$		5		
		$V_{\text{IN}} = 1.8\text{ V}$		10		
		$V_{\text{IN}} = 1.2\text{ V}$		15		
		$V_{\text{IN}} = 1\text{ V}$		25		
t_{FALL}	Fall Time	$C_L = 0.1\mu\text{F}$, $R_L = 10\Omega$ ⁽¹⁾		2.3		μs
		$C_L = 1\mu\text{F}$, $R_L = \text{Open}$ ⁽¹⁾		315		

(1) See the [Fall Time \(\$t_{\text{FALL}}\$ \)](#) and [Quick Output Discharge \(QOD\)](#) section for information on how R_L and C_L affect Fall Time.

Switching Characteristics (continued)

Unless otherwise noted, the typical characteristics in the following table applies over the entire recommended power supply voltage range of 1 V to 5.5 V at 25°C with a load of $C_L = 0.1\mu\text{F}$, $R_L = 10\Omega$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPS22916C, TPS22916CN, TPS22916CL						
t_{ON}	Turn On Time	$V_{\text{IN}} = 5\text{ V}$		1400		μs
		$V_{\text{IN}} = 3.6\text{ V}$		1700		
		$V_{\text{IN}} = 1.8\text{ V}$		3000		
		$V_{\text{IN}} = 1.2\text{ V}$		5000		
		$V_{\text{IN}} = 1\text{ V}$		6500		
t_{RISE}	Rise Time	$V_{\text{IN}} = 5\text{ V}$		800		μs
		$V_{\text{IN}} = 3.6\text{ V}$		900		
		$V_{\text{IN}} = 1.8\text{ V}$		1400		
		$V_{\text{IN}} = 1.2\text{ V}$		2300		
		$V_{\text{IN}} = 1\text{ V}$		3000		
SR_{ON}	Slew Rate	$V_{\text{IN}} = 5\text{ V}$		5		$\text{mV}/\mu\text{s}$
		$V_{\text{IN}} = 3.6\text{ V}$		3.2		
		$V_{\text{IN}} = 1.8\text{ V}$		1		
		$V_{\text{IN}} = 1.2\text{ V}$		0.4		
		$V_{\text{IN}} = 1\text{ V}$		0.3		
t_{OFF}	Turn Off Time	$V_{\text{IN}} = 5\text{ V}$		5		μs
		$V_{\text{IN}} = 3.6\text{ V}$		5		
		$V_{\text{IN}} = 1.8\text{ V}$		10		
		$V_{\text{IN}} = 1.2\text{ V}$		15		
		$V_{\text{IN}} = 1\text{ V}$		25		
t_{FALL}	Fall Time ⁽²⁾	$C_L = 0.1\mu\text{F}$, $R_L = 10\Omega$ ⁽¹⁾		2.3		μs
		$C_L = 10\mu\text{F}$, $R_L = \text{Open}$ ⁽¹⁾		3150		

(2) Devices without Quick Output Discharge (QOD) may not discharge completely.

7.7 Typical Characteristics

7.7.1 Typical Electrical Characteristics

The typical characteristics curves in this section apply to all devices unless otherwise noted.

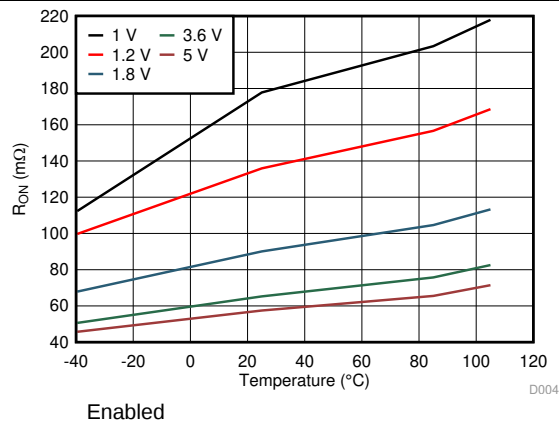


图 1. ON-Resistance vs Temperature

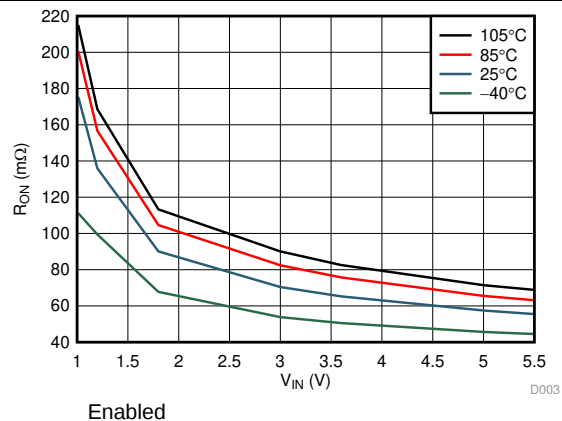


图 2. ON-Resistance vs Input voltage

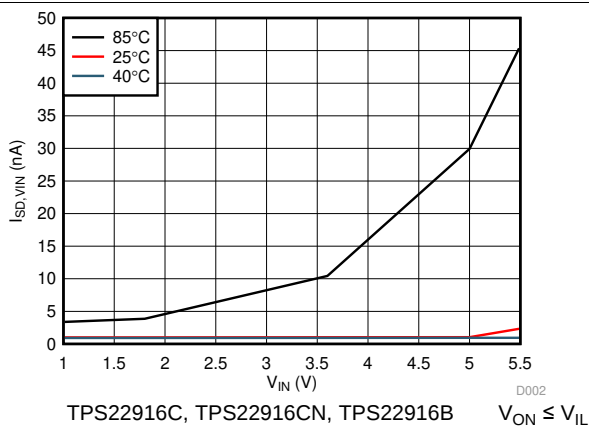


图 3. Shutdown Current

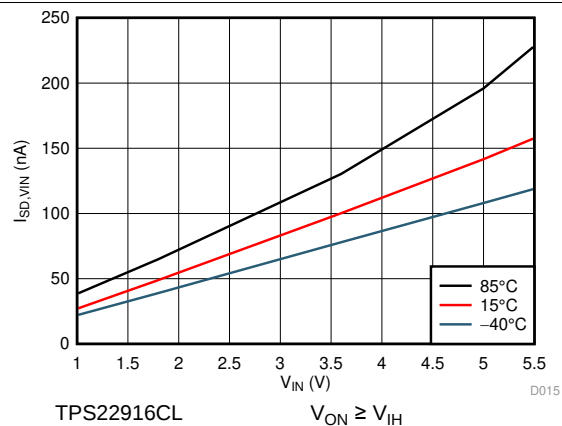


图 4. Shutdown Current (Active Low)

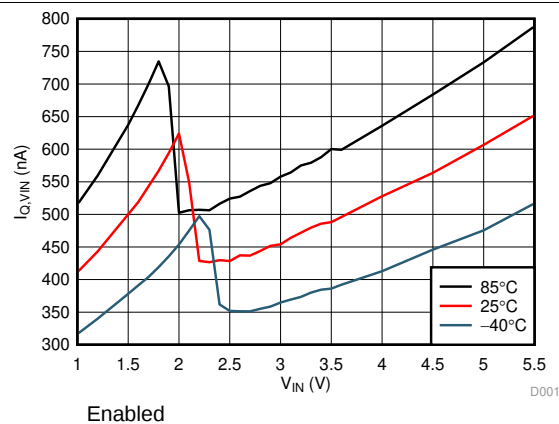


图 5. Quiescent Current

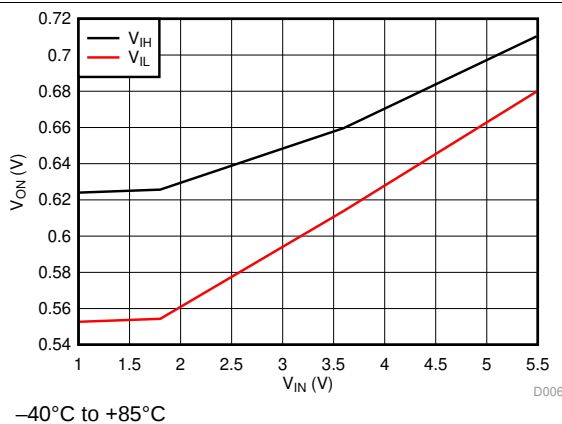


图 6. ON Pin Threshold

Typical Electrical Characteristics (接下页)

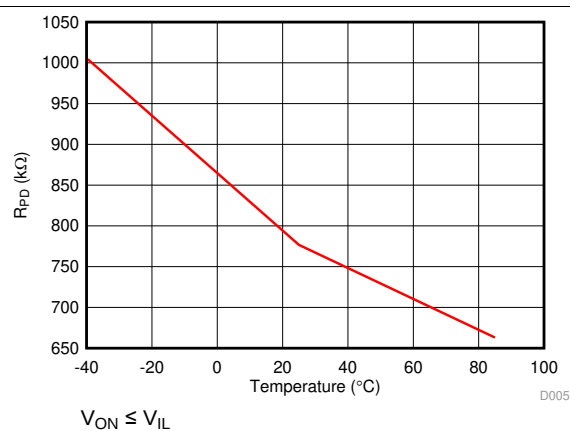


图 7. ON Pin Smart Pull Down

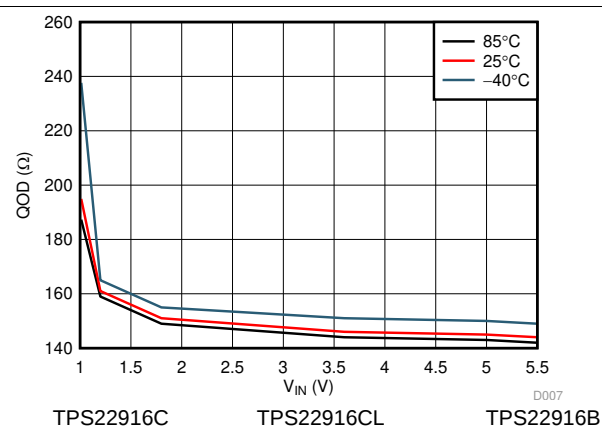


图 8. Quick Output Discharge

7.7.2 Typical Switching Characteristics

The typical data in this section apply to all devices at 25°C unless otherwise noted.

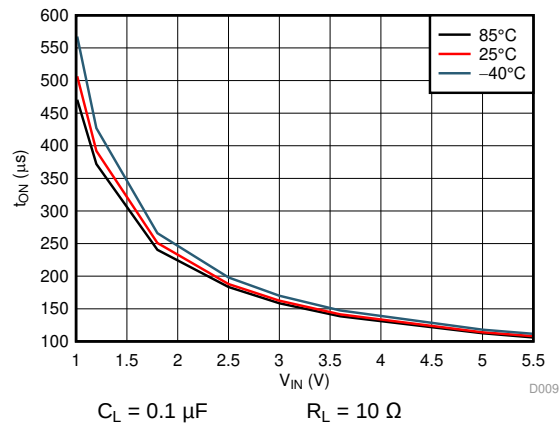


图 9. Fast Turn On Time

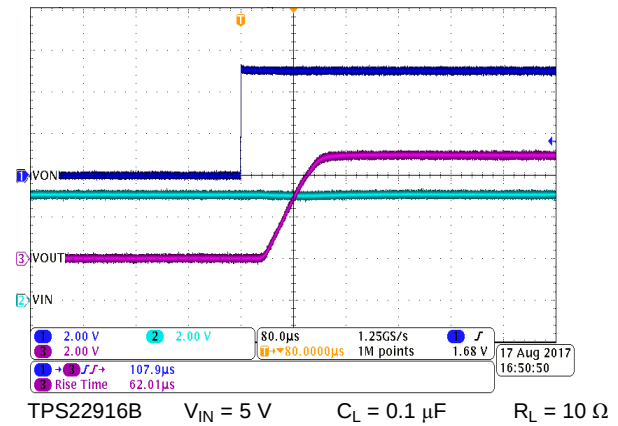


图 10. Fast Turn On at 5 V

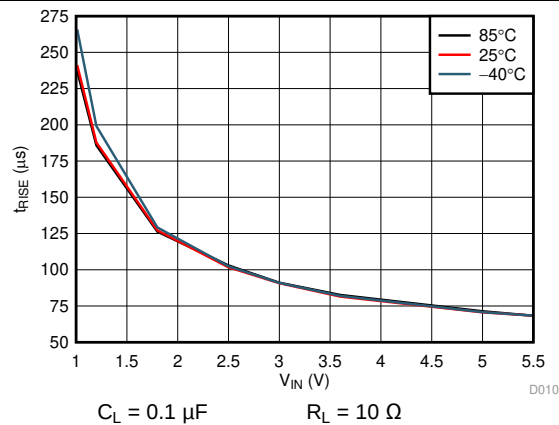


图 11. Fast Rise Time

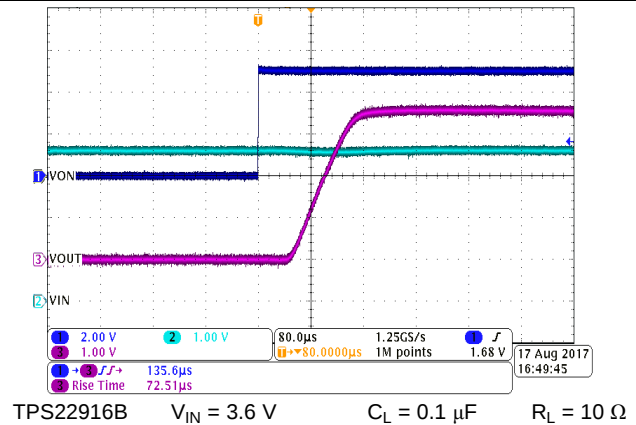


图 12. Fast Turn On at 3.6 V

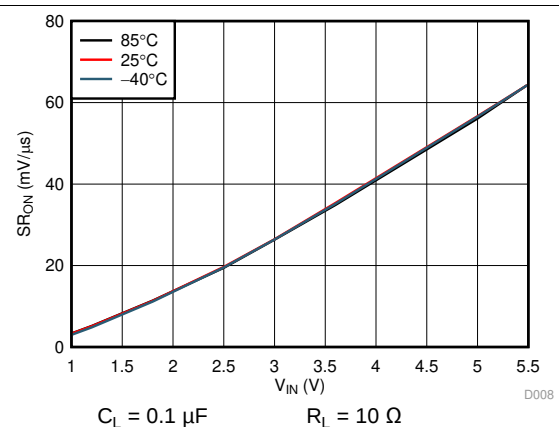


图 13. Fast Slew Rate

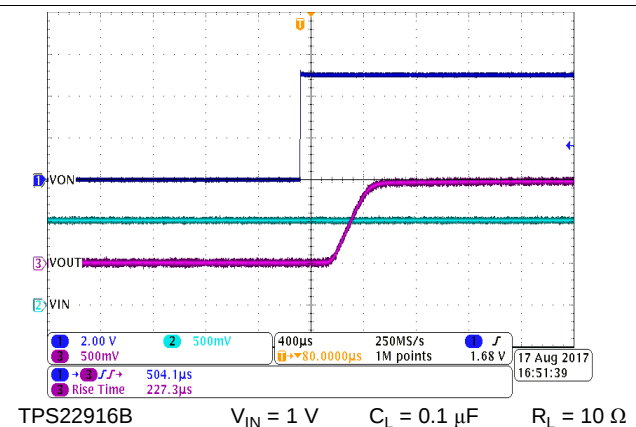


图 14. Fast Turn on at 1 V

Typical Switching Characteristics (接下页)

The typical data in this section apply to all devices at 25°C unless otherwise noted.

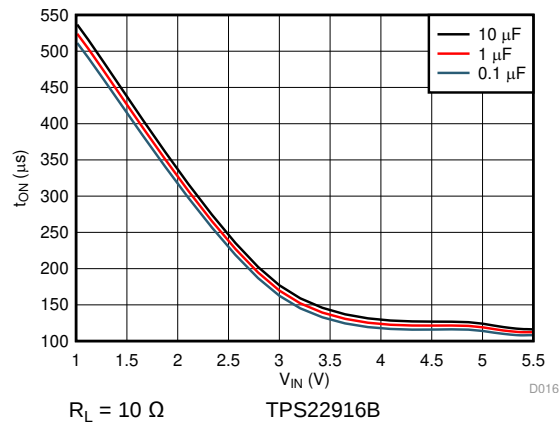


图 15. Fast Turn On vs Load Capacitance

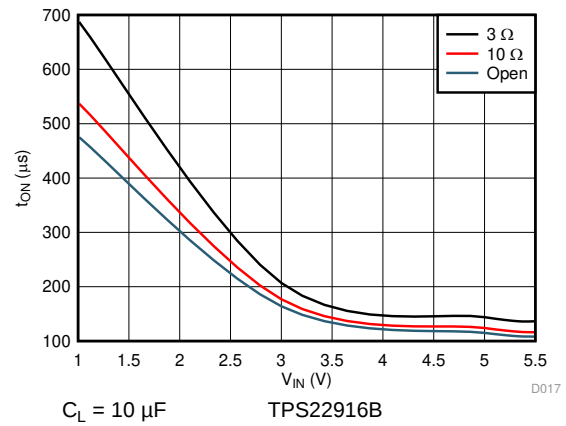


图 16. Fast Turn On vs Load Resistance

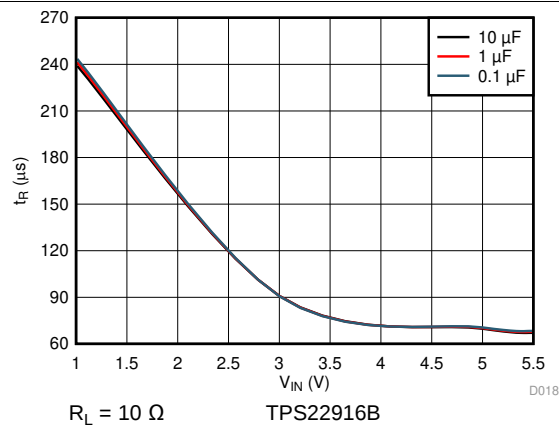


图 17. Fast Rise Time vs Load Capacitance

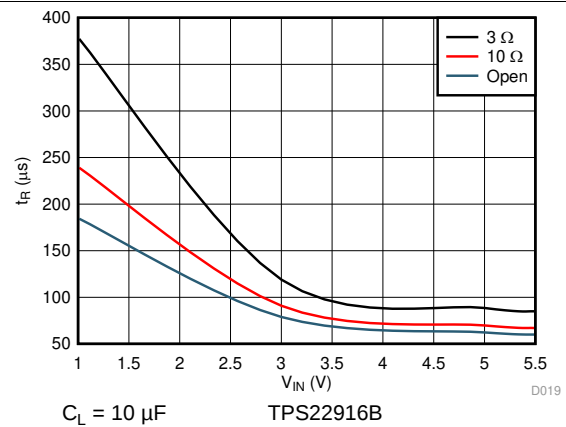


图 18. Fast Rise Time vs Load Resistance

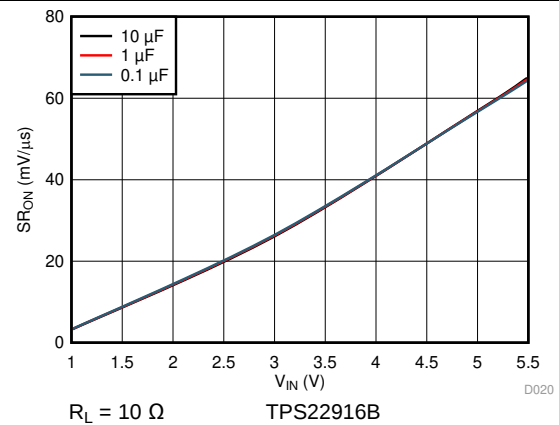


图 19. Fast Slew Rate vs Load Capacitance

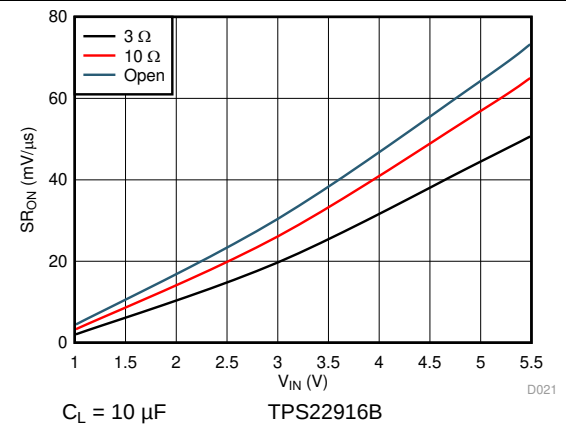


图 20. Fast Slew Rate vs Load Resistance

Typical Switching Characteristics (接下页)

The typical data in this section apply to all devices at 25°C unless otherwise noted.

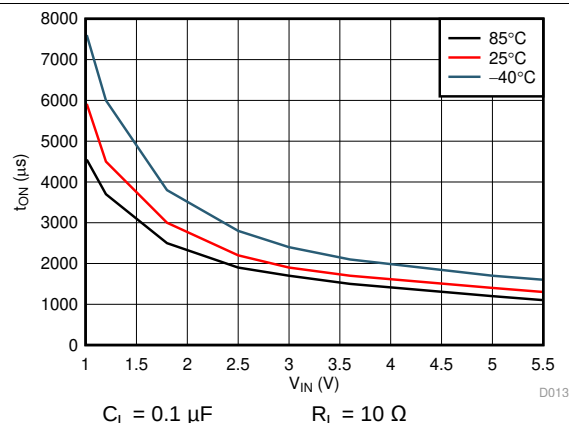


图 21. Slow Turn on Time

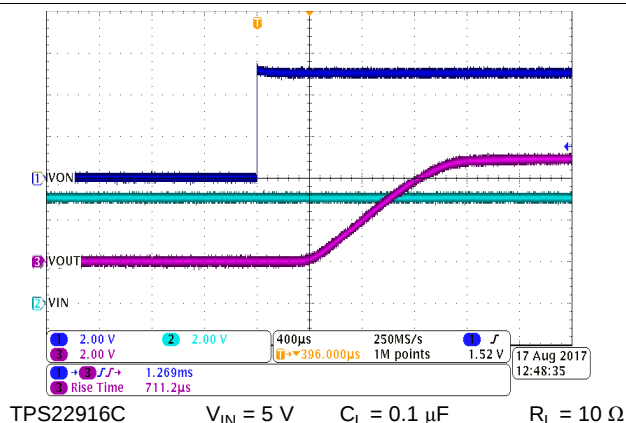


图 22. Slow Turn on at 5 V

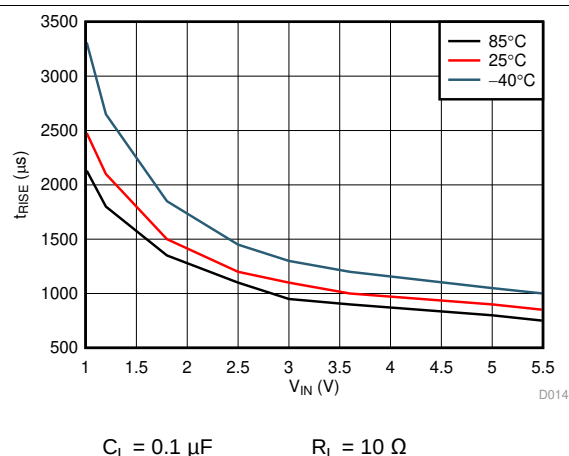


图 23. Slow Rise Time

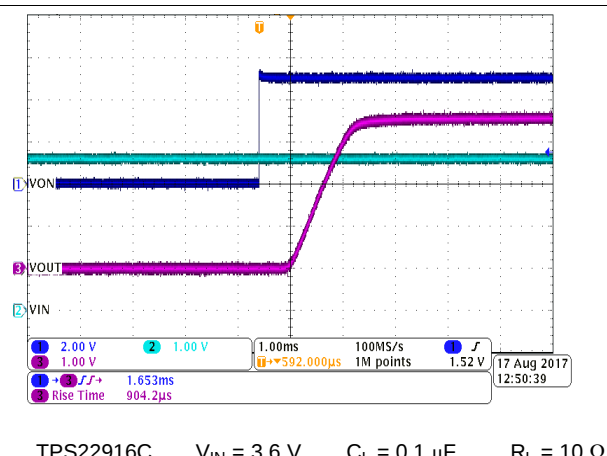


图 24. Slow Turn On at 3.6 V

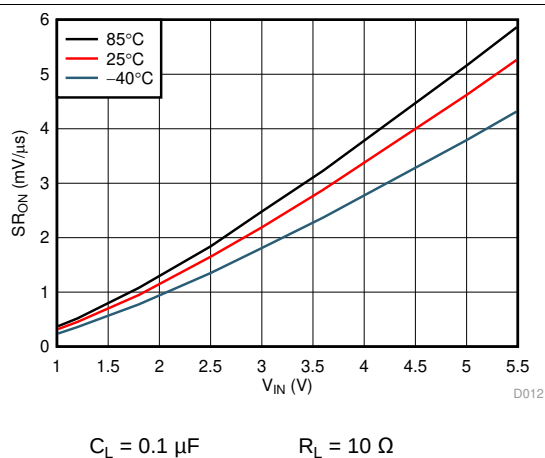


图 25. Slow Slew Rate

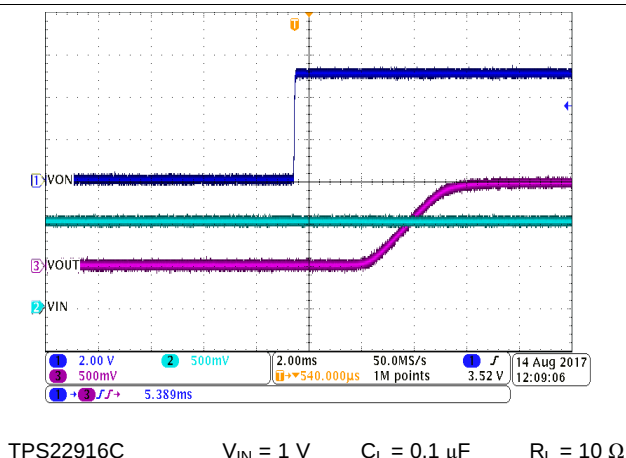


图 26. Slow Turn On at 1 V

Typical Switching Characteristics (接下页)

The typical data in this section apply to all devices at 25°C unless otherwise noted.

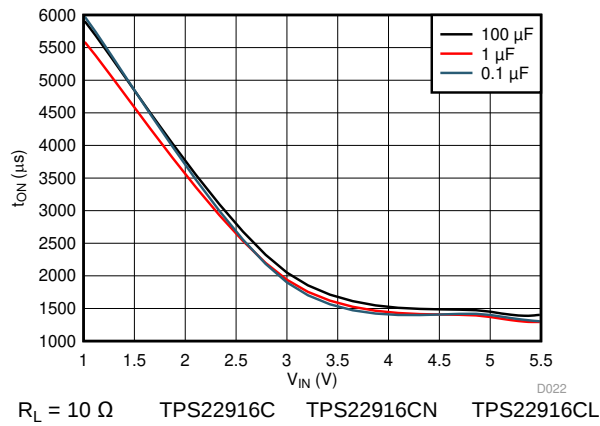


图 27. Slow Turn On vs Load Capacitance

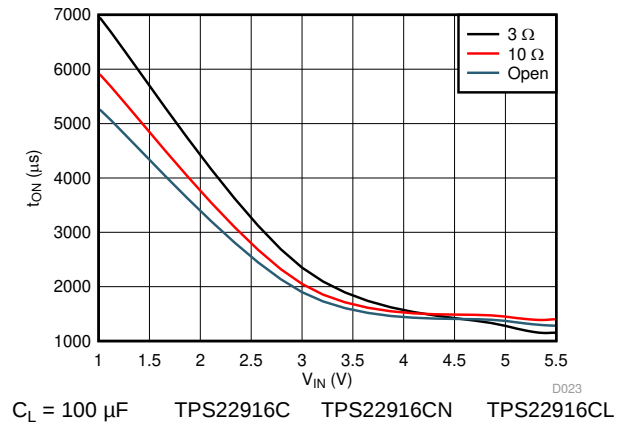


图 28. Slow Turn On vs Load Resistance

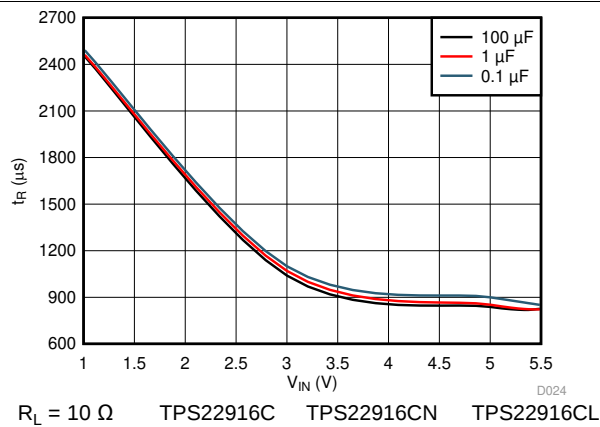


图 29. Slow Rise Time vs Load Capacitance

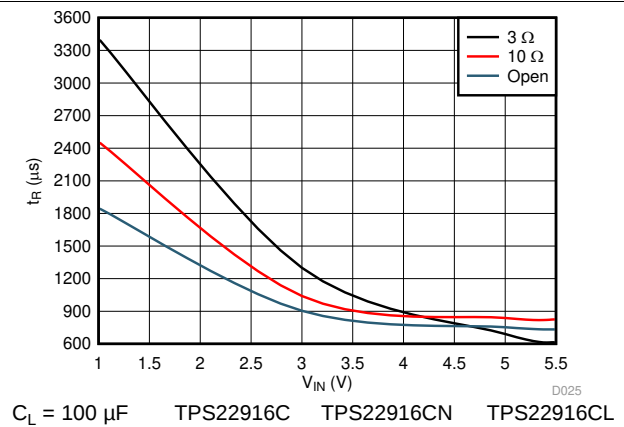


图 30. Slow Rise Time vs Load Resistance

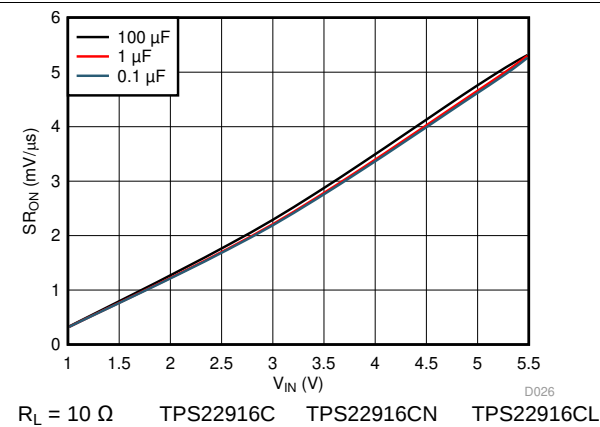


图 31. Slow Slew Rate vs Load Capacitance

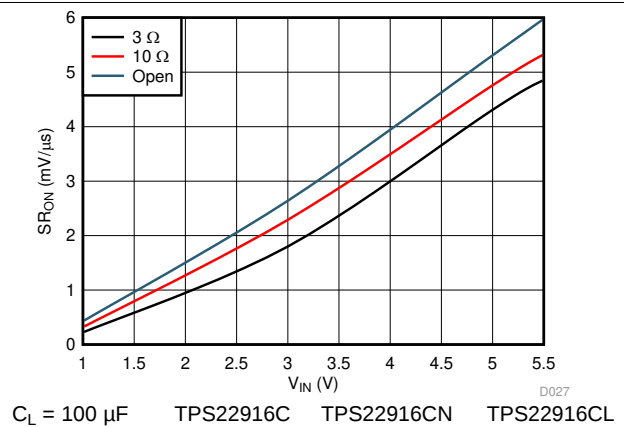


图 32. Slow Slew Rate vs Load Resistance

Typical Switching Characteristics (接下页)

The typical data in this section apply to all devices at 25°C unless otherwise noted.

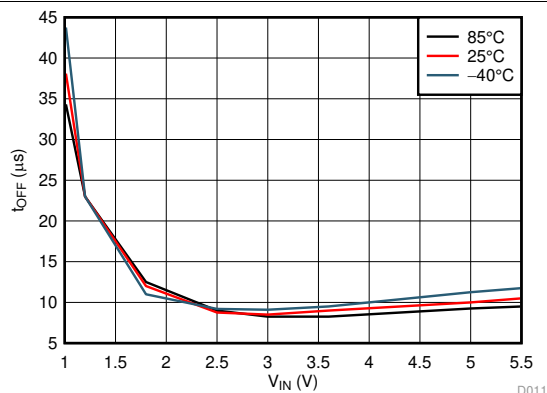


图 33. Turn Off Time

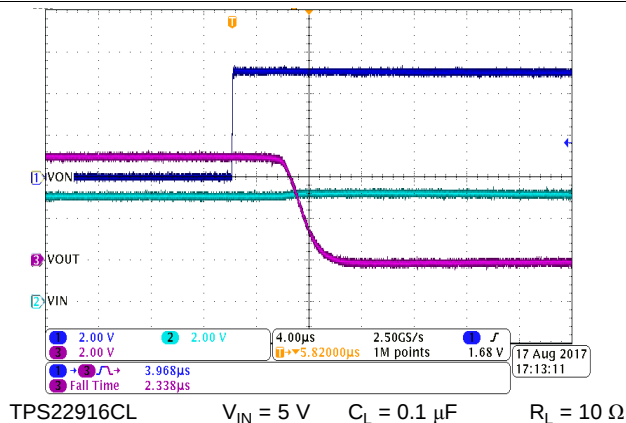


图 34. Turn Off at 5 V (Active Low)

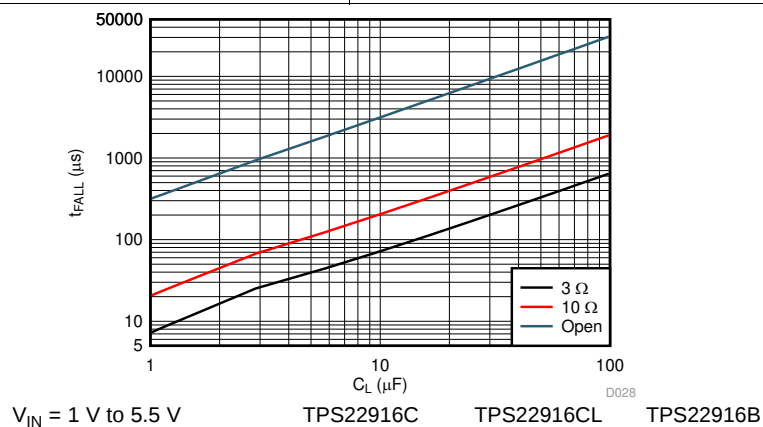
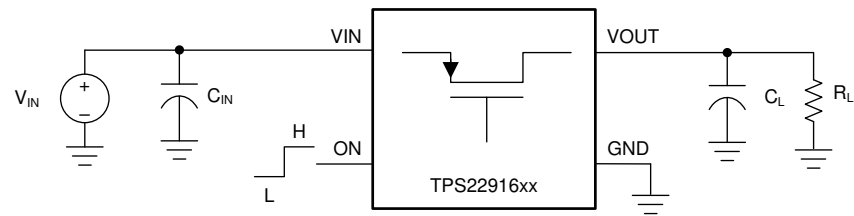


图 35. Fall Time

8 Parameter Measurement Information



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图 36. TPS22916 Test Circuit

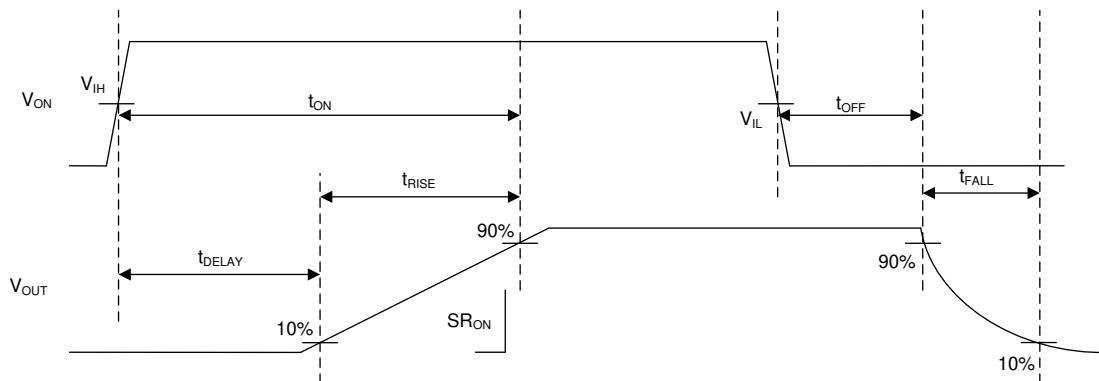


图 37. TPS22916 Timing Waveform

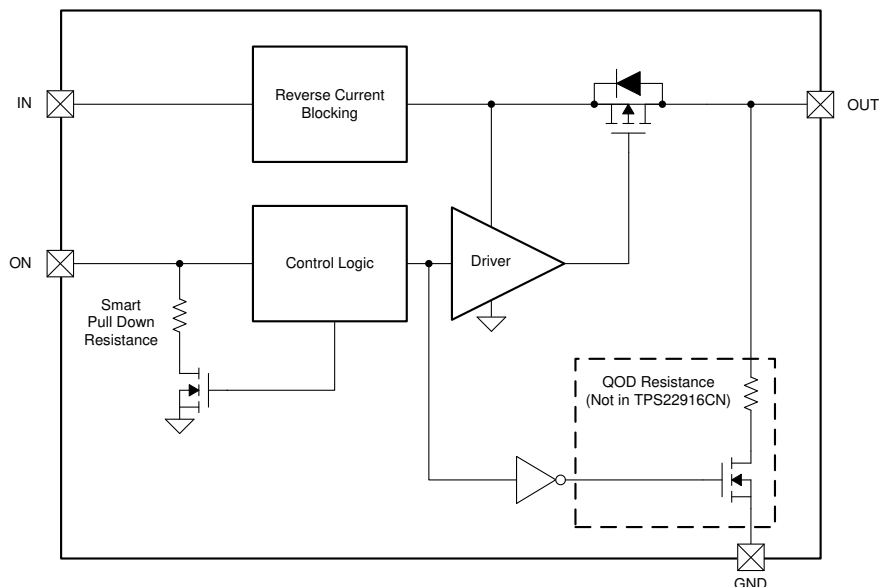
9 Detailed Description

9.1 Overview

This family of devices are single channel, 2-A load switches in ultra-small, space saving 4-pin WCSP package. These devices implement a low resistance P-channel MOSFET with a controlled rise time for applications that need to limit inrush current.

These devices are designed to have very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for additional external components, which reduces solution size and BOM count.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, 3.3-V, or 5.5-V GPIO.

9.3.2 Fall Time (t_{FALL}) and Quick Output Discharge (QOD)

The TPS22916B/C/CL include a Quick Output Discharge feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of QOD and prevents the output from floating while the switch is disabled.

As load capacitance and load resistance increase: t_{FALL} increases. The larger the load resistance or load capacitance is, the longer it takes to discharge the capacitor, resulting in a longer fall time.

Feature Description (接下页)

The output fall time is determined by how quickly the load capacitance is discharged and can be found using [公式 1](#).

$$t_{\text{FALL}} = - (R_{\text{DIS}}) \times C_L \times \ln(V_{10\%}/V_{90\%})$$

Where

- $V_{10\%}$ is 10% of the initial output voltage
 - $V_{90\%}$ is 90% of the initial output voltage
 - R_{DIS} is the result of the QOD resistance in parallel with the Load Resistance R_L
 - C_L is the load capacitance
- (1)

With the Quick Output Discharge feature, the QOD resistance is in parallel with R_L . This provides a lower total load resistance as seen from the load capacitance which discharges the capacitance faster resulting in a smaller t_{FALL} .

9.3.3 Full-Time Reverse Current Blocking

In a scenario where the device is enabled and V_{OUT} is greater than V_{IN} there is potential for reverse current to flow through the pass FET or the body diode. When the reverse current threshold (I_{RCB}) is exceeded, the switch is disabled within t_{RCB} . The Switch will remain off and block reverse current as long as the reverse voltage condition exists. Once V_{OUT} has dropped below the V_{RCB} release threshold the TPS22916xx will turn back on with slew rate control.

9.4 Device Functional Modes

[表 1](#) describes the state for each variant as determined by the ON pin

表 1. Device Function Table

ON	TPS22916B	TPS22916C	TPS22916CN	TPS22916CL
$\leq V_{\text{IL}}$	Disabled	Disabled	Disabled	Enabled
$\geq V_{\text{IH}}$	Enabled	Enabled	Enabled	Disabled

[表 2](#) shows when QOD is active for each variant.

表 2. QOD Function Table

Device	TPS22916B	TPS22916C	TPS22916CN	TPS22916CL
Enabled	No	No	No	No
Disabled	Yes	Yes	No	Yes

[表 3](#) shows when the ON Pin Smart Pull Down is active.

表 3. Smart-ON Pull Down

V_{ON}	Pull Down
$\leq V_{\text{IL}}$	Connected
$\geq V_{\text{IH}}$	Disconnected

10 Application and Implementation

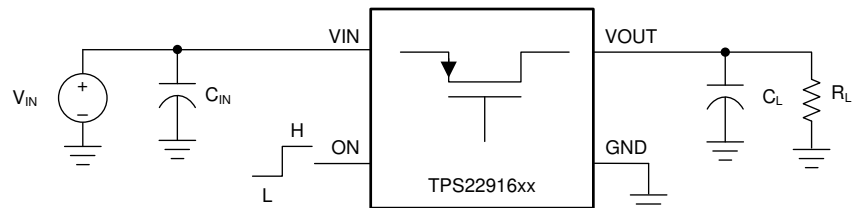
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device.

10.1.1 Typical Application



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图 38. Typical Application

10.1.1.1 Design Requirements

For this design example, below, use the input parameters shown in 表 4.

表 4. Design Parameters

Design Parameter	Example Value
Input Voltage (V_{IN})	3.6 V
Load Capacitance (C_L)	47 μ F
Maximum Inrush Current (I_{RUSH})	300 mA

10.1.1.2 Detailed Design Procedure

10.1.1.2.1 Maximum Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0-V to V_{IN} voltage. This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

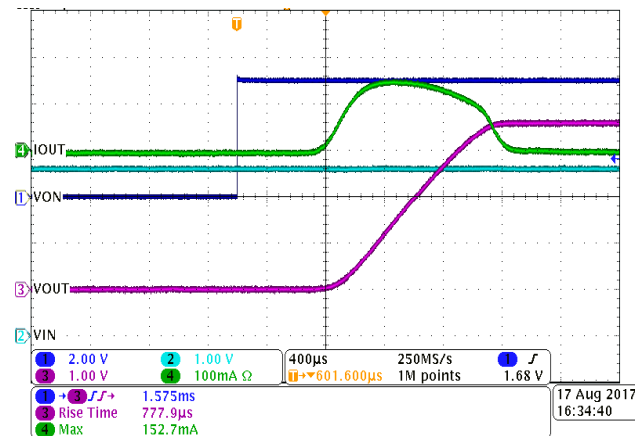
$$I_{RUSH} = C_L \times SR_{ON} \quad (2)$$

$$I_{RUSH} = 47\mu F \times 3.2mV/\mu s \quad (3)$$

$$I_{RUSH} = 150mA \quad (4)$$

The TPS22916x offers multiple rise time options to control the inrush current during turn-on. The appropriate device can be selected based upon the maximum acceptable slew rate which can be calculated using the design requirements and the inrush current equation. In this case, the TPS22916C provides a slew rate slow enough to limit the inrush current to the desired amount.

10.1.1.3 Application Curve



$V_{IN} = 3.6\text{ V}$ $C_L = 47\mu\text{F}$ $R_L = \text{Open}$
 TPS22916C $T_A = 25^\circ\text{C}$

图 39. Inrush Current

11 Power Supply Recommendations

The device is designed to operate with a V_{IN} range of 1 V to 5.5 V. The V_{IN} power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 μF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

12 Layout

12.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

12.2 Layout Example

公式 3 shows an example for these devices. Notice the connection to system ground between the V_{OUT} Bypass Capacitor ground and the GND pin of the load switch, this creates a ground barrier which helps to reduce the ground noise seen by the device.

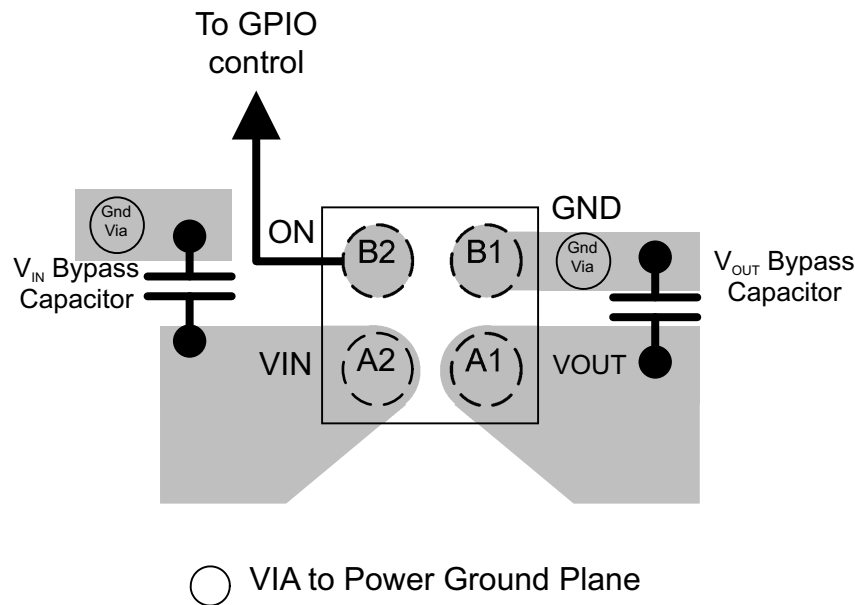


图 40. TPS22916xx Layout

12.3 Thermal Considerations

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, P_{D(max)} for a given output current and ambient temperature, use 公式 5 as a guideline:

$$P_{D(\text{MAX})} = \frac{T_{J(\text{MAX})} - T_A}{R_{\theta JA}} \quad (5)$$

Where,

P_{D(max)} = maximum allowable power dissipation

T_{J(max)} = maximum allowable junction temperature

T_A = ambient temperature for the device

θ_{JA} = junction to air thermal impedance. See the [Thermal Information](#) section.

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

请参阅如下相关文档：

《[TPS22916 负载开关评估模块](#)》

13.2 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 社区资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 商标

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13.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

14.1 Package Option Addendum

14.1.1 Packaging Information

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽³⁾	MSL Peak Temp ⁽⁴⁾	Op Temp (°C)	Device Marking ⁽⁵⁾⁽⁶⁾
TPS22916BYFPR	Active	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	BA
TPS22916BYFPT	Active	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	BA
TPS22916CLYFPR	Active	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	B9
TPS22916CLYFPT	Active	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	B9

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

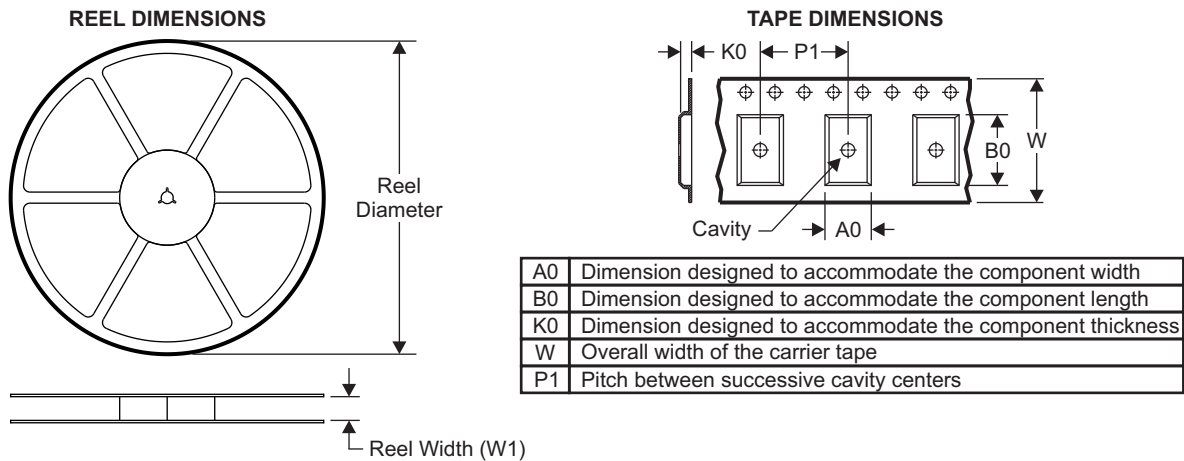
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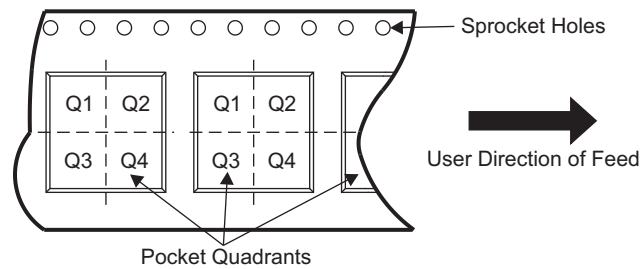
Package Option Addendum (接下页)

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽³⁾	MSL Peak Temp ⁽⁴⁾	Op Temp (°C)	Device Marking ⁽⁵⁾⁽⁶⁾
TPS22916CNYFPR	Active	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B8
TPS22916CNYFPT	Active	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B8
TPS22916CYFPR	Active	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B7
TPS22916CYFPT	Active	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B7

14.1.2 Tape and Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



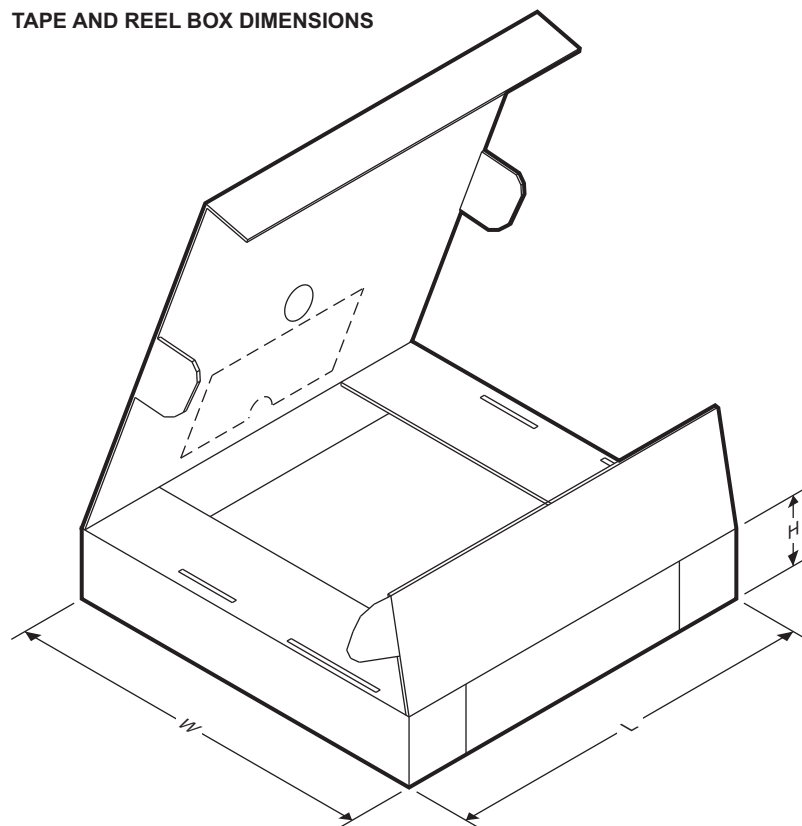
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22916BYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916BYFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CLYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CLYFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CNYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CNYFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CYFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1

TPS22916

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TAPE AND REEL BOX DIMENSIONS



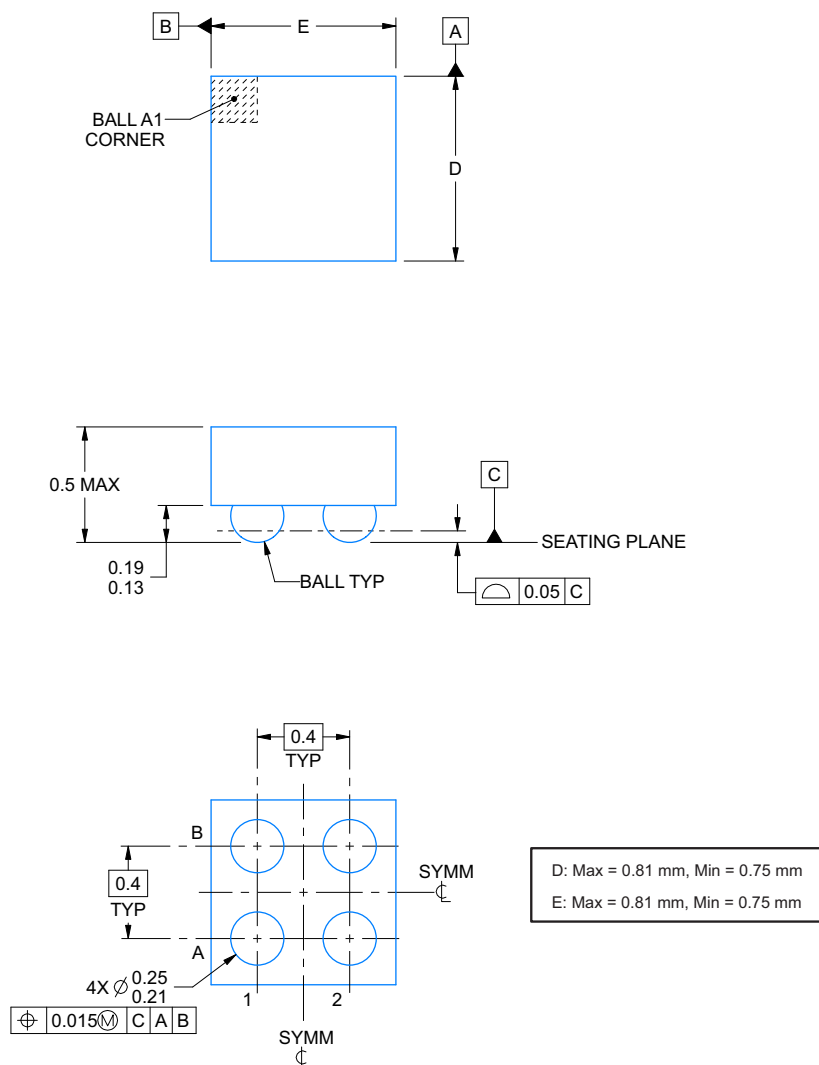
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22916BYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22916BYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22916CLYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22916CLYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22916CNYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22916CNYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22916CYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22916CYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0



YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223507/A 01/2017

NOTES:

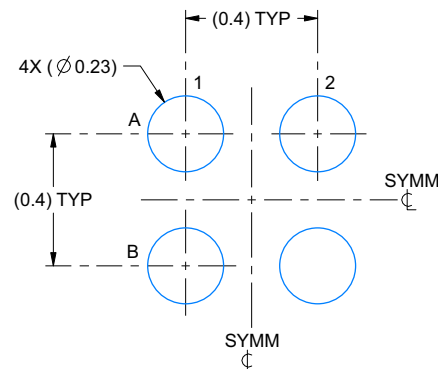
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

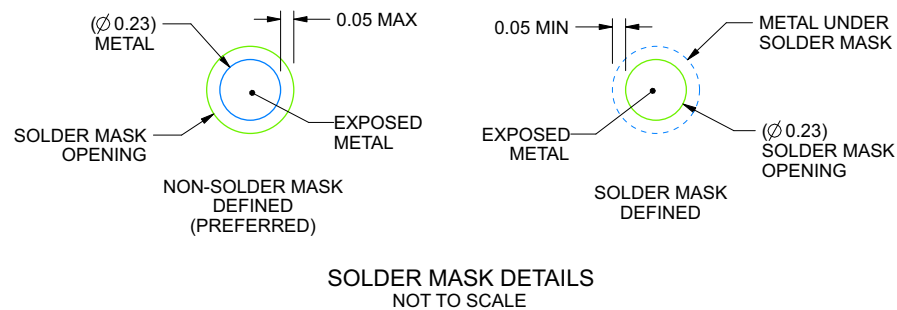
YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223507/A 01/2017

NOTES: (continued)

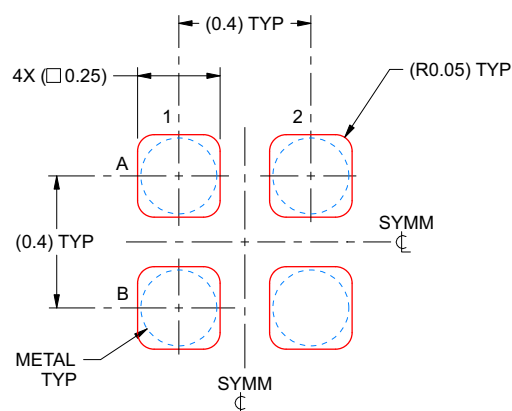
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22916BYFPR	ACTIVE	DSBGA	YFP	4	3000	RoHS & Green	SAC396 SNAGCU	Level-1-260C-UNLIM	-40 to 85	(BA, R)	Samples
TPS22916BYFPT	ACTIVE	DSBGA	YFP	4	250	RoHS & Green	SAC396 SNAGCU	Level-1-260C-UNLIM	-40 to 85	(BA, R)	Samples
TPS22916CLYFPR	ACTIVE	DSBGA	YFP	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 85	B9	Samples
TPS22916CLYFPT	ACTIVE	DSBGA	YFP	4	250	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 85	B9	Samples
TPS22916CNYFPR	ACTIVE	DSBGA	YFP	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 85	B8	Samples
TPS22916CNYFPT	ACTIVE	DSBGA	YFP	4	250	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 85	B8	Samples
TPS22916CYFPR	ACTIVE	DSBGA	YFP	4	3000	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 85	B7	Samples
TPS22916CYFPT	ACTIVE	DSBGA	YFP	4	250	RoHS & Green	SAC396	Level-1-260C-UNLIM	-40 to 85	B7	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

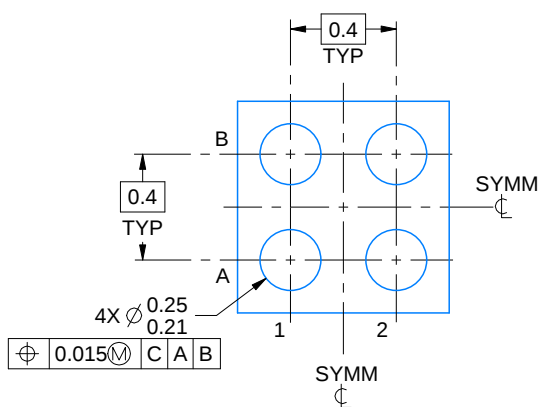
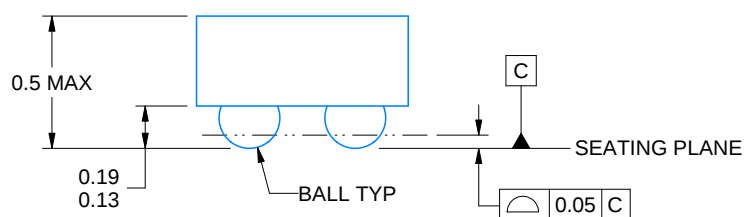
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

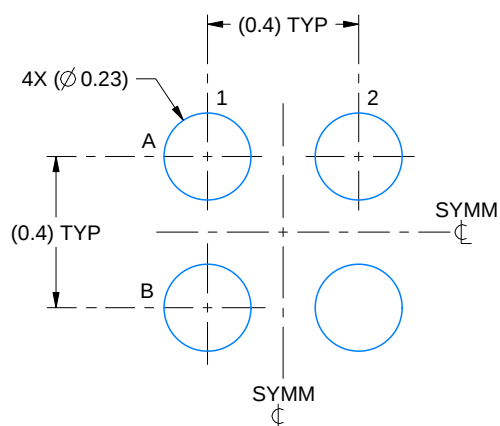
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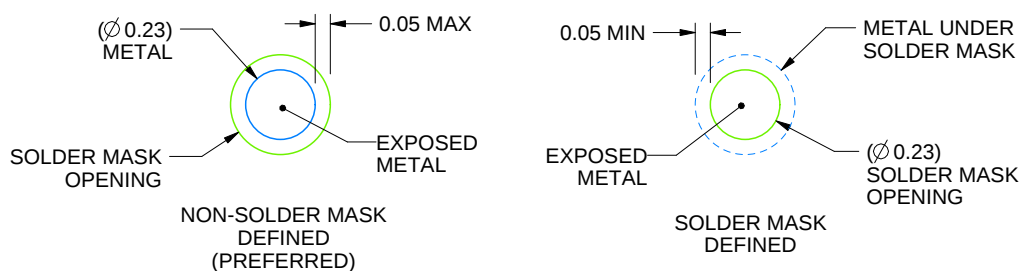


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

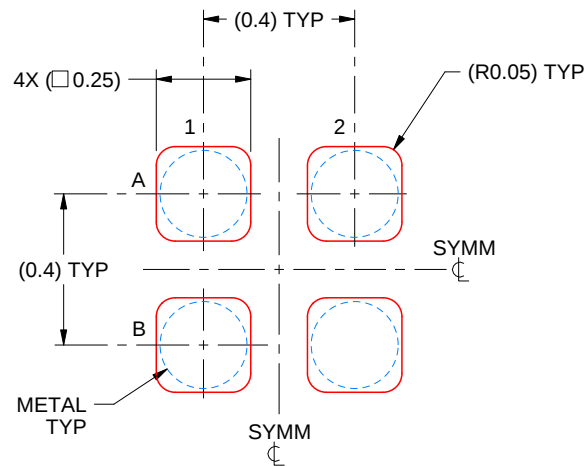
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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