

## SGx524 稳压脉宽调制器

### 1 特性

- 完整的脉宽调制 (PWM) 电源控制电路
- 用于单端或推挽应用的非限定输出
- 8mA (典型值) 待机电流

### 2 应用

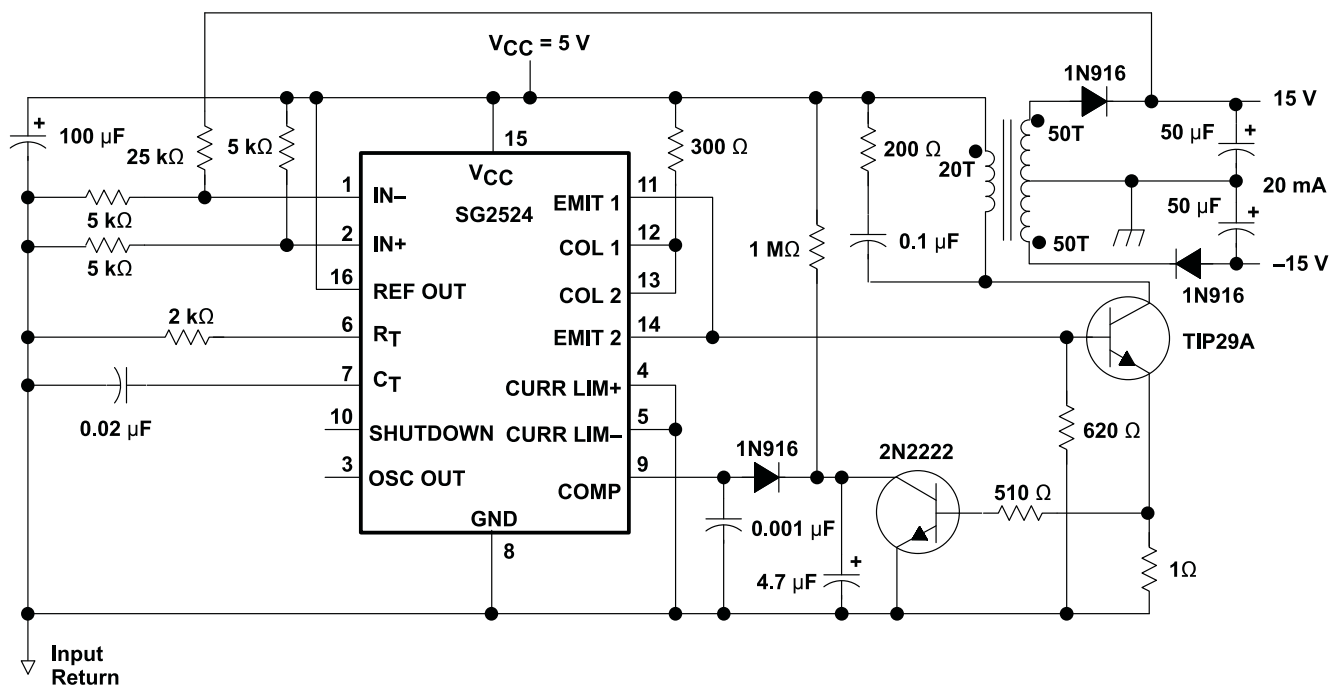
- 变压器耦合直流/直流转换器
- 任意极性的开关稳压器

### 3 说明

SG2524 和 SG3524 器件在单个芯片上包含构建稳压电源、逆变器或开关稳压器所需的一切功能。它们也可以用作高功率输出应用的控制元件。SG2524 和 SG3524 设计用于任一极性的开关稳压器、变压器耦合直流/直流转换器、无变压器电压加倍器以及采用了固定频率、脉宽调制 (PWM) 技术的极性变换器应用。补偿输出支持单端或推挽应用。每个器件包含一个片上稳压器、误差放大器、可编程振荡器、脉冲转向触发器、两个非限定导通晶体管、一个高增益比较器以及电流限制和关断电路。

#### 器件信息

器件型号	封装 (引脚)	封装尺寸 (标称值)
SGx524	SOIC (16)	9.90mm x 3.91mm
	PDIP (16)	9.90mm x 6.35mm
	NS (16)	10.30mm x 5.30mm



典型应用原理图



## Table of Contents

<b>1 特性</b> .....	<b>1</b>	<b>9 Detailed Description</b> .....	<b>9</b>
<b>2 应用</b> .....	<b>1</b>	9.1 Overview.....	9
<b>3 说明</b> .....	<b>1</b>	9.2 Functional Block Diagram.....	9
<b>4 Revision History</b> .....	<b>2</b>	9.3 Feature Description.....	10
<b>5 Pin Configurations and Functions</b> .....	<b>2</b>	9.4 Device Functional Modes.....	11
Pin Functions.....	2	<b>10 Layout</b> .....	<b>19</b>
<b>6 Specifications</b> .....	<b>4</b>	10.1 Layout Guidelines.....	19
6.1 Absolute Maximum Ratings.....	4	10.2 Layout Example.....	20
6.2 ESD Ratings.....	4	<b>11 Device and Documentation Support</b> .....	<b>21</b>
6.3 Recommended Operating Conditions.....	4	11.1 Related Links.....	21
6.4 Thermal Information.....	4	11.2 Trademarks.....	21
<b>8 Parameter Measurement Information</b> .....	<b>8</b>		

## 4 Revision History

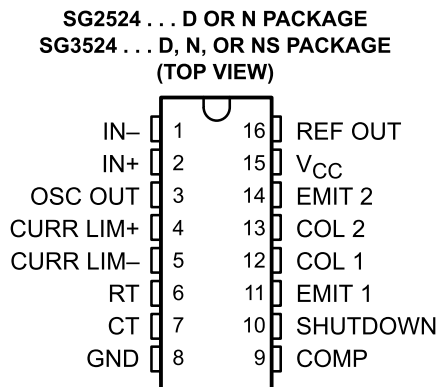
### Changes from Revision E (January 2015) to Revision F (February 2021) Page

- Updated text..... 6

### Changes from Revision D (February 2003) to Revision E (January 2015) Page

- 添加了应用、器件信息表、引脚功能表、ESD 等级表、热性能信息表、典型特性、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分..... 1
- 删除了订购信息表..... 1

## 5 Pin Configurations and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
COL 1	12	O	Collector terminal of BJT output 1
COL 2	13	O	Collector terminal of BJT output 2
COMP	9	I/O	Error amplifier compensation pin
CT	7	—	Capacitor terminal used to set oscillator frequency
CURR LIM+	4	I	Positive current limiting amplifier input
CURR LIM-	5	I	Negative current limiting amplifier input
EMIT 1	11	O	Emitter terminal of BJT output 1
EMIT 2	14	O	Emitter terminal of BJT output 2

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	8	—	Ground
IN+	2	I	Positive error amplifier input
IN-	1	I	Positive error amplifier input
OSC OUT	3	O	Oscillator Output
REF OUT	16	O	Reference regulator output
RT	6	—	Resistor terminal used to set oscillator frequency
SHUTDOWN	10	I	Device shutdown
V <sub>CC</sub>	15	—	Positive supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		40	V
I <sub>CC</sub>	Collector output current		100	mA
I <sub>O(ref)</sub>	Reference output current		50	mA
	Current through CT terminal	– 5		mA
T <sub>J</sub>	Maximum junction temperature		150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
T <sub>stg</sub>	Storage temperature range	– 65	150	°C

- (1) Stresses beyond those listed under [# 6.1](#) table may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [# 6.3](#) table are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply Voltage		8	40	V
	Reference output current		0	50	mA
	Current through CT terminal		– 0.03	– 2	mA
R <sub>T</sub>	Timing resistor		1.8	100	k $\Omega$
C <sub>T</sub>	Timing capacitor		0.001	0.1	$\mu$ F
T <sub>A</sub>	Operating free-air temperature	SG2524	– 25	85	°C
		SG3524	0	70	

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SGx524			UNIT
		D	N	NS	
		16 PINS			
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2) (3)</sup>	73	67	64	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

- (2) Maximum power dissipation is a function of T<sub>J(max)</sub>,  $\theta_{JA}$ , and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is PD = (T<sub>J(max)</sub> – T<sub>A</sub>) /  $\theta_{JA}$ . Operation at the absolute maximum T<sub>J</sub> of 150°C can impact reliability.

- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## 7

### 7.1 Electrical Characteristics

over operating free-air temperature range,  $V_{CC} = 20\text{ V}$ ,  $f = 20\text{ kHz}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(2)</sup>	SG2524			SG3524			UNIT
			MIN	TYP <sup>(2)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
Reference section									
Output voltage			4.8	5	5.2	4.6	5	5.4	V
Input Regulation		V <sub>CC</sub> = 8 V to 40 V		10	20		10	30	mV
Ripple rejection		f = 120 Hz		66			66		dB
Output regulation		I <sub>O</sub> = 0 mA to 20 mA		20	50		20	50	mV
Output voltage change with temperature		T <sub>A</sub> = MIN to MAX		0.3%	1%		0.3%	1%	
Short-circuit output current <sup>(3)</sup>		V <sub>ref</sub> = 0		100			100		mA
Error Amplifier section									
V <sub>IO</sub>	Input offset voltage	V <sub>IC</sub> = 2.5 V		0.5	5		2	10	mV
I <sub>IB</sub>	Input bias current	V <sub>IC</sub> = 2.5 V		2	10		2	10	μA
	Open-loop voltage amplification		72	80		60	80		dB
V <sub>ICR</sub>	Common-mode input voltage range	T <sub>A</sub> = 25°C	1.8 to 3.4			1.8 to 3.4			V
CMMR	Common-mode rejection ratio			70			70		dB
B <sub>1</sub>	Unity-gain bandwidth			3			3		MHz
	Output swing	T <sub>A</sub> = 25°C	0.5		3.8	0.5		3.8	V

- (1) All typical values, except for temperature coefficients, are at  $T_A = 25^\circ\text{C}$ .  
 (2) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.  
 (3) Standard deviation is a measure of the statistical distribution about the mean, as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^N (x_n - \bar{x})^2}{N-1}}$$

## 7.2 Electrical Characteristics — Continued, Both Parts

over operating free-air temperature range,  $V_{CC} = 20\text{ V}$ ,  $f = 20\text{ kHz}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(2)</sup>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
Oscillator section						
f <sub>OSC</sub>	Oscillator frequency	C <sub>T</sub> = 0.001 μ F, R <sub>T</sub> = 2 k Ω		450		kHz
	Standard deviation of frequency <sup>(3)</sup>	All values of voltage, temperature, resistance, and capacitance constant		5		—
Δ f <sub>OSC</sub>	Frequency change with voltage	V <sub>CC</sub> = 8 V to 40 V, T <sub>A</sub> = 25°C			1%	—
	Frequency change with temperature	T <sub>A</sub> = MIN to MAX			2%	
	Output amplitude at OSC OUT	T <sub>A</sub> = 25°C		3.5		V
t <sub>W</sub>	Output pulse duration (width) at OSC OUT	C <sub>T</sub> = 0.01 μ F, T <sub>A</sub> = 25°C		0.5		μs
Output section						
V <sub>(BR)CE</sub>	Collector-emitter breakdown voltage		40			V
	Collector off-state current	V <sub>CE</sub> = 40 V		0.01	50	μA
V <sub>sat</sub>	Collector-emitter saturation voltage	I <sub>C</sub> = 50 mA		1	2	V
V <sub>O</sub>	Emitter output voltage	V <sub>C</sub> = 20 V, I <sub>E</sub> = - 250 μ A	17	18		V
t <sub>r</sub>	Turn-off voltage rise time	R <sub>C</sub> = 2 k Ω		0.2		μs
t <sub>f</sub>	Turn-on voltage fall time	R <sub>C</sub> = 2 k Ω		0.1		μs
Comparator section						
	Maximum duty cycle, each output		45%			
V <sub>IT</sub>	Input threshold voltage at COMP	Zero duty cycle		1		V
		Maximum duty cycle		3.5		
I <sub>IB</sub>	Input bias current			- 1		μA
Current limiting section						
V <sub>I</sub>	Input voltage range		- 1		1	V
V <sub>(SENSE)</sub>	Sense voltage at T <sub>A</sub> = 25°C	V <sub>(IN+)</sub> - V <sub>(IN - )</sub> ≥ 50 mV V <sub>(COMP)</sub> 2 V	175	200	225	mV
	Temperature coefficient of sense voltage			0.2		mV/°C
Total Device						
I <sub>st</sub>	Standby current	V <sub>CC</sub> = 40 V, I <sub>N -</sub> , CURR LIM+, C <sub>T</sub> , GND, COMP, EMIT 1, EMIT 2 grounded, I <sub>N+</sub> at 2 V, All other inputs and outputs open		8	10	mA

## 7.3 Typical Characteristics

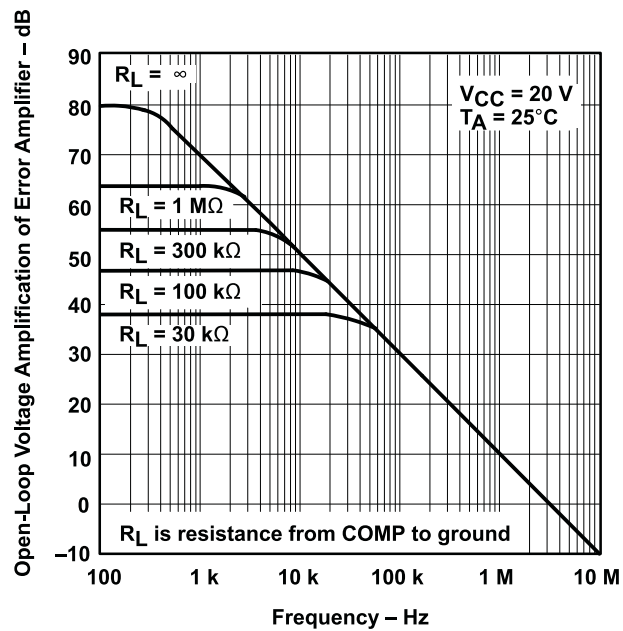


图 7-1. Open-Loop Voltage Amplification of Error Amplifier vs Frequency

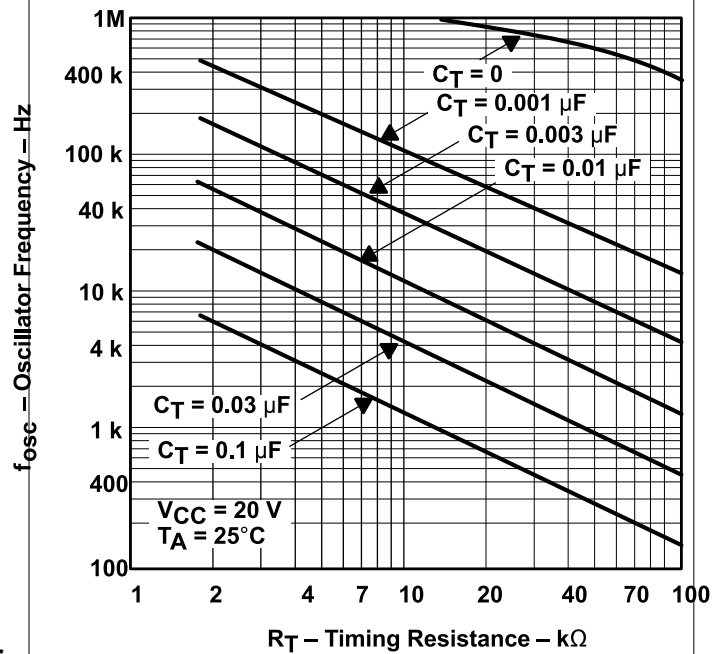


图 7-2. Oscillator Frequency vs Timing Resistance

## 8 Parameter Measurement Information

### 8.1

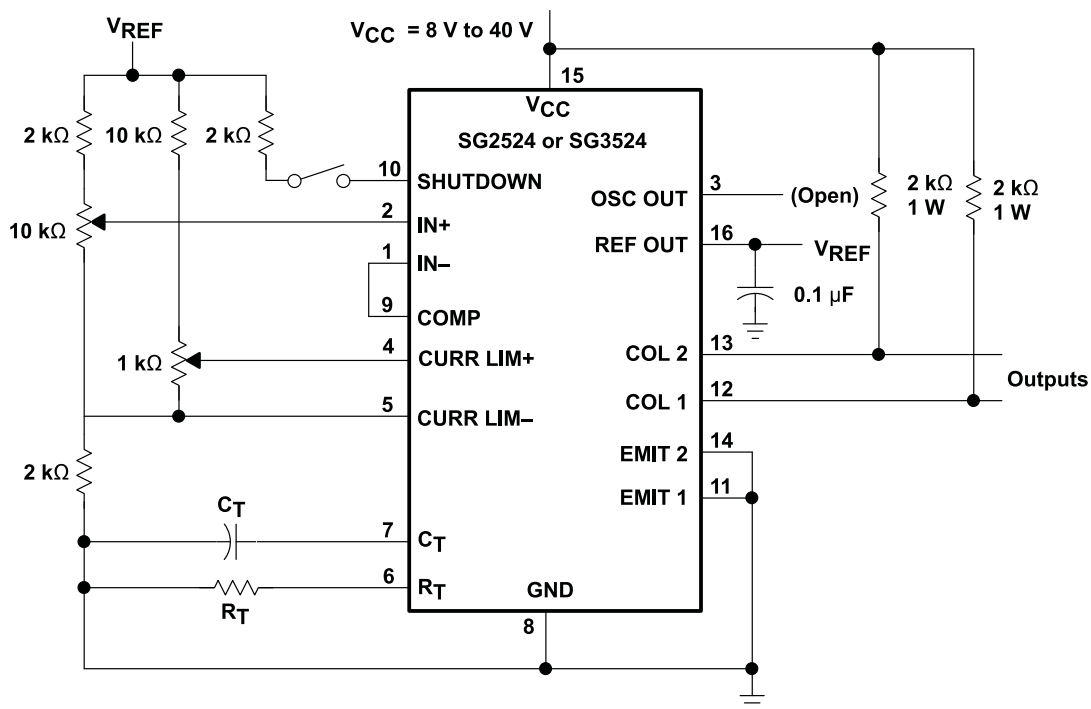


图 8-1. General Test Circuit

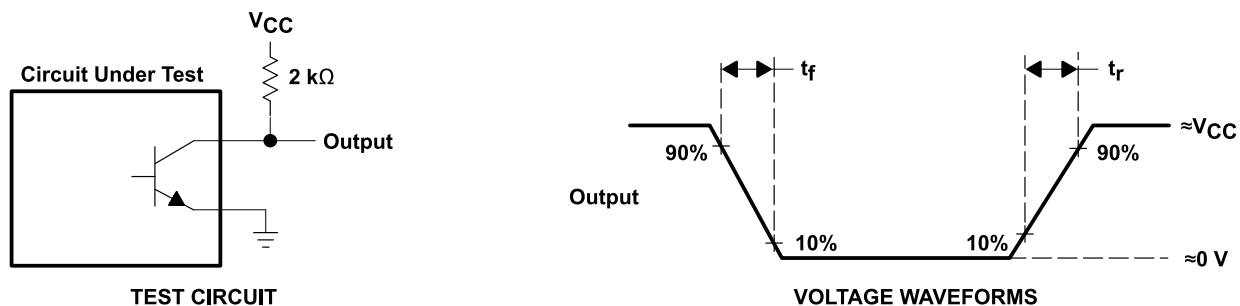


图 8-2. Switching Times



## 9 Detailed Description

### 9.1 Overview

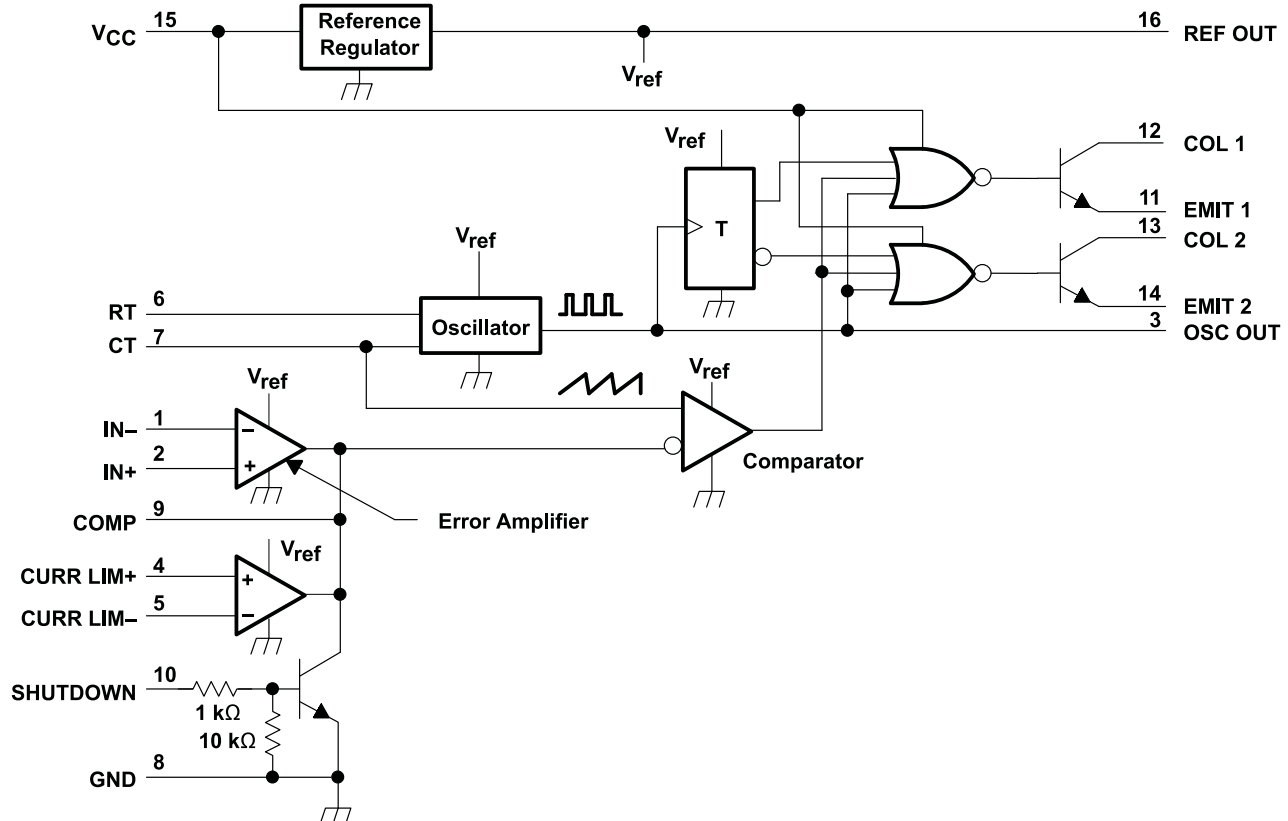
SGx524 is a fixed-frequency pulse-width-modulation (PWM) voltage-regulator control circuit. The regulator operates at a fixed frequency that is programmed by one timing resistor,  $R_T$ , and one timing capacitor,  $C_T$ .  $R_T$  establishes a constant charging current for  $C_T$ . This results in a linear voltage ramp at  $C_T$ , which is fed to the comparator, providing linear control of the output pulse duration (width) by the error amplifier.

The SGx524 contains an onboard 5-V regulator that serves as a reference, as well as supplying the SGx524 internal regulator control circuitry. The internal reference voltage is divided externally by a resistor ladder network to provide a reference within the common-mode range of the error amplifier as shown in Figure 10-5, or an external reference can be used.

The output is sensed by a second resistor divider network and the error signal is amplified. This voltage is then compared to the linear voltage ramp at  $C_T$ . The resulting modulated pulse out of the high-gain comparator then is steered to the appropriate output pass transistor (Q1 or Q2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to ensure both outputs are never on simultaneously during the transition times. The duration of the blanking pulse is controlled by the value of  $C_T$ .

The outputs may be applied in a push-pull configuration in which their frequency is one-half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current-limiting and shut-down circuitry and can be overridden by signals from either of these inputs. This common point is pinned out externally via the COMP pin, which can be employed to either control the gain of the error amplifier or to compensate it. In addition, the COMP pin can be used to provide additional control to the regulator.

### 9.2 Functional Block Diagram



A. Resistor values shown are nominal.

## 9.3 Feature Description

### 9.3.1 Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse duration is controlled by the value of  $C_T$  as shown in 图 7-2. If small values of  $C_T$  are required, the oscillator output pulse duration can be maintained by applying a shunt capacitance from OSC OUT to ground.

### 9.3.2 Error Amplifier

The error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation. The compensation node (COMP) is a high-impedance node ( $R_L = 5\text{ M}\Omega$ ). The gain of the amplifier is  $AV = (0.002\ \Omega - 1)R_L$  and easily can be reduced from a nominal 10,000 by an external shunt resistance from COMP to ground. Refer to 图 7-1 for data.

### 9.3.3 Compensation

COMP, as previously discussed, is made available for compensation. Since most output filters introduce one or more additional poles at frequencies below 200 Hz, which is the pole of the uncompensated amplifier, introduction of a zero to cancel one of the output filter poles is desirable. This can be accomplished best with a series RC circuit from COMP to ground in the range of  $50\text{ k}\Omega$  and  $0.001\ \mu\text{F}$ . Other frequencies can be canceled by use of the formula  $f \approx 1/RC$ .

### 9.3.4 Output Circuitry

SGx524 contains two identical npn transistors, the collectors and emitters of which are uncommitted. Each transistor has antisaturation circuitry that limits the current through that transistor to a maximum of 100 mA for fast response.

### 9.3.5 Current Limiting

A current-limiting sense amplifier is provided in the SGx524 device. The current-limiting sense amplifier exhibits a threshold of  $200\text{ mV} \pm 25\text{ mV}$  and must be applied in the ground line since the voltage range of the inputs is limited to  $1\text{ V}$  to  $-1\text{ V}$ . Caution should be taken to ensure the  $-1\text{ V}$  limit is not exceeded by either input, otherwise, damage to the device may result.

Foldback current limiting can be provided with the network shown in 图 9-1. The current-limit schematic is shown in 图 9-2.

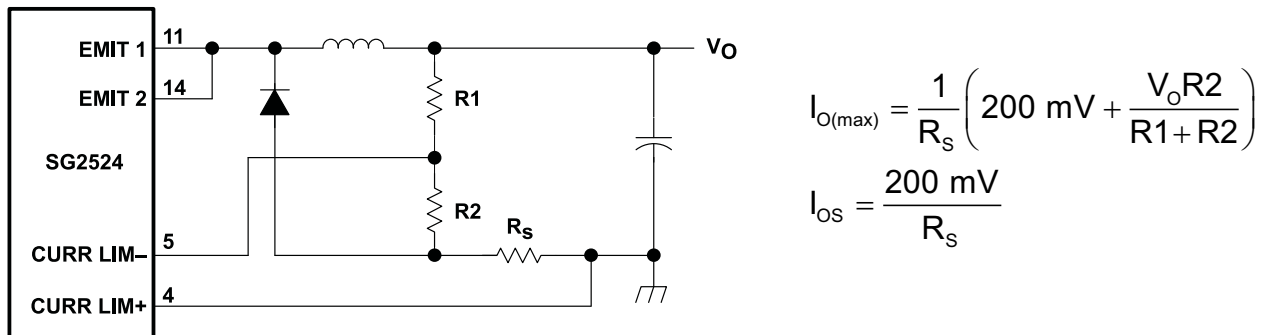


图 9-1. Foldback Current Limiting for Shorted Output Conditions

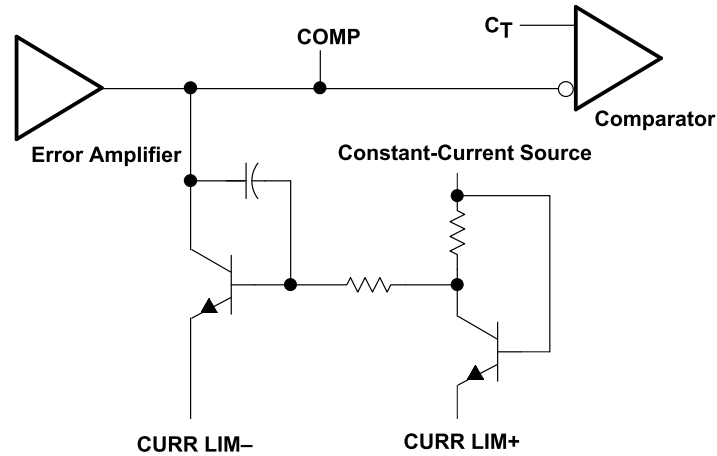


图 9-2. Current-Limit Schematic

## 9.4 Device Functional Modes

### 9.4.1 Synchronous Operation

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 k $\Omega$ . In this configuration,  $R_T C_T$  must be selected for a clock period slightly greater than that of the external clock.

If two or more SGx524 regulators are operated synchronously, all oscillator output terminals must be tied together. The oscillator programmed for the minimum clock period is the master from which all the other SGx524s operate. In this application, the  $C_T R_T$  values of the slaved regulators must be set for a period approximately 10% longer than that of the master regulator. In addition,  $C_T$  (master) = 2  $C_T$  (slave) to ensure that the master output pulse, which occurs first, has a longer pulse duration and, subsequently, resets the slave regulators.

### 9.4.2 Shutdown Circuitry

COMP also can be employed to introduce external control of the SGx524. Any circuit that can sink 200  $\mu$ A can pull the compensation terminal to ground and, thus, disable the SGx524.

In addition to constant-current limiting, CURR LIM+ and CURR LIM - also can be used in transformer-coupled circuits to sense primary current and shorten an output pulse should transformer saturation occur. CURR LIM - also can be grounded to convert CURR LIM+ into an additional shutdown terminal.

## Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

There are a wide variety of output configurations possible when considering the application of the SG2524 as a voltage-regulator control circuit. They can be segregated into three basic categories:

- Capacitor-diode-coupled voltage multipliers
- Inductor-capacitor-implemented single-ended circuits
- Transformer-coupled circuits

Examples of these categories are shown in [图 10-1](#), [图 10-2](#), and [图 10-3](#), respectively. [节 10.2](#) demonstrates how to set up the SG2524 for a capacitor-diode output design. The same techniques for setting up the internal circuitry of the IC may also be used for the other two output stage examples shown [节 10.3](#).

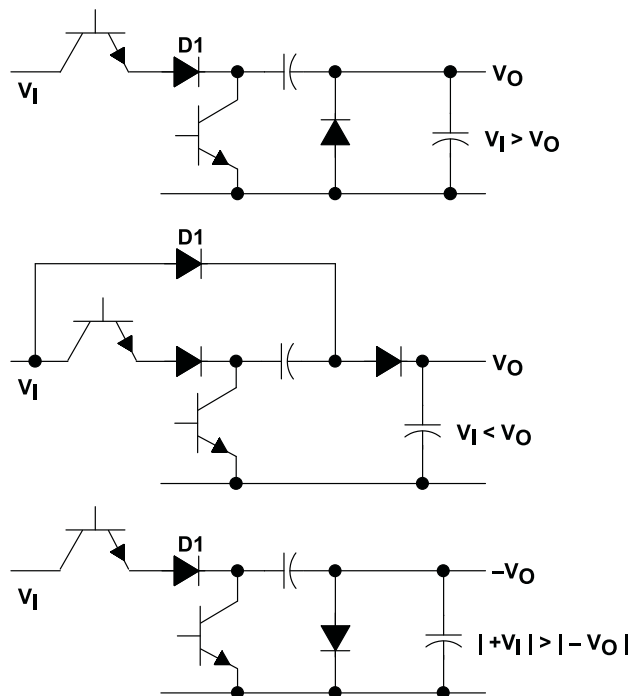


图 10-1. Capacitor-Diode-Coupled Voltage-Multiplier Output Stages

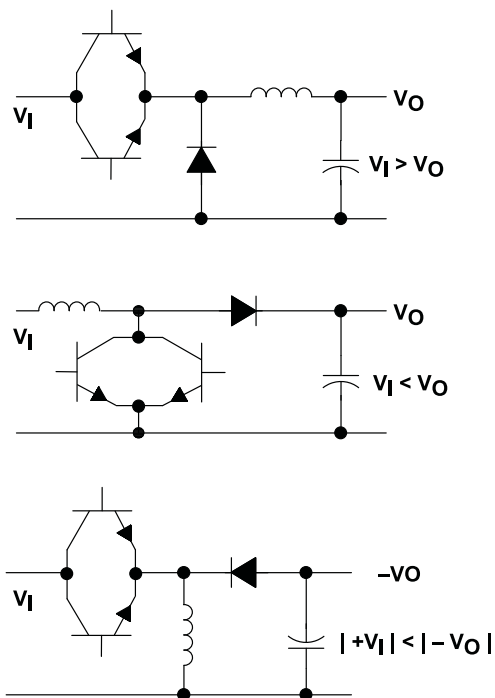


图 10-2. Single-Ended Inductor Circuit

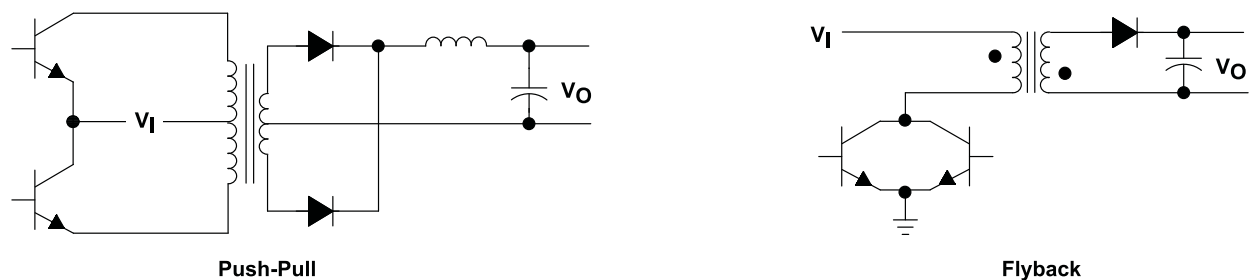


图 10-3. Transformer-Coupled Outputs

## 10.2 Typical Application

### 10.2.1 Capacitor-Diode Output

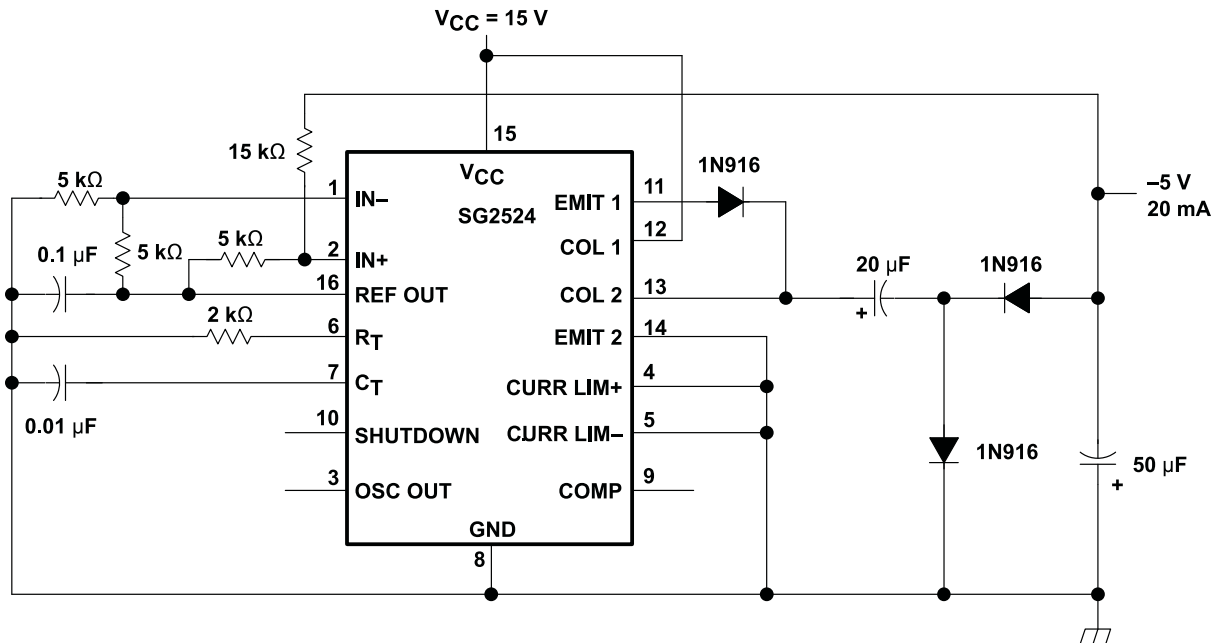


图 10-4. Capacitor-Diode Output Circuit Schematic

#### 10.2.1.1 Design Requirements

- 15-V supply voltage
- -5-V output voltage

#### 10.2.1.2 Detailed Design Procedure

##### 10.2.1.2.1 Oscillator

The oscillator controls the frequency of the SG2524 and is programmed by RT and CT as shown in 图 10-6.

$$f \approx \frac{1.30}{R_T R_C} \quad (1)$$

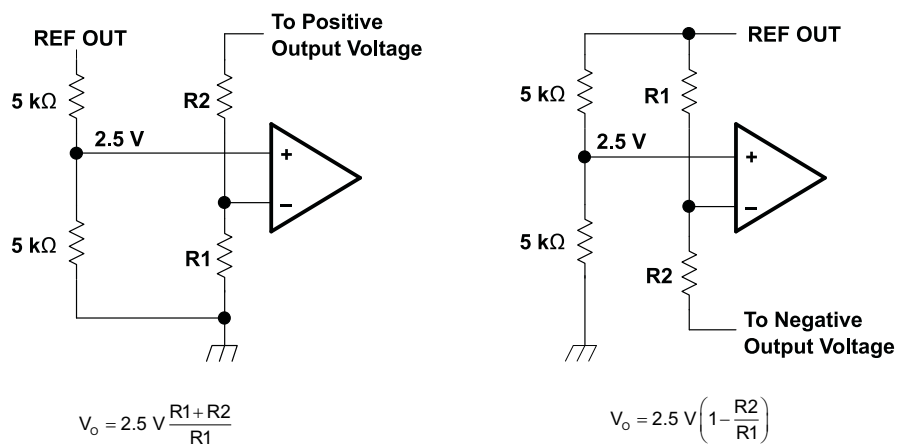
where

- $R_T$  is in  $k\Omega$
- $C_T$  is in  $\mu F$
- $f$  is in kHz

Practical values of CT fall between 0.001  $\mu F$  and 0.1  $\mu F$ . Practical values of RT fall between 1.8  $k\Omega$  and 100  $k\Omega$ . This results in a frequency range typically from 130 Hz to 722 kHz.

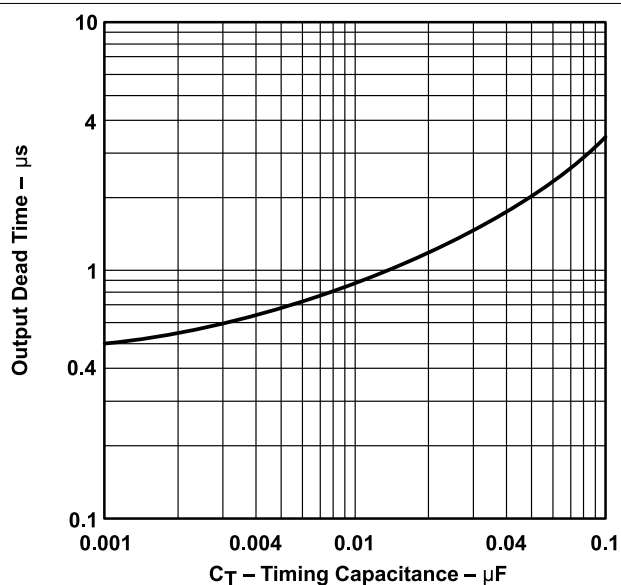
##### 10.2.1.2.2 Voltage Reference

The 5-V internal reference can be employed by use of an external resistor divider network to establish a reference common-mode voltage range (1.8 V to 3.4 V) within the error amplifiers (see 图 10-5), or an external reference can be applied directly to the error amplifier. For operation from a fixed 5-V supply, the internal reference can be bypassed by applying the input voltage to both the VCC and VREF terminals. In this configuration, however, the input voltage is limited to a maximum of 6 V.



**图 10-5. Error-Amplifier Bias Circuits**

### 10.2.1.3 Application Curves



**图 10-6. Output Dead Time vs Timing Capacitance**

## 10.3 Examples of Other Output Stages

### 10.3.1 Flyback Converter

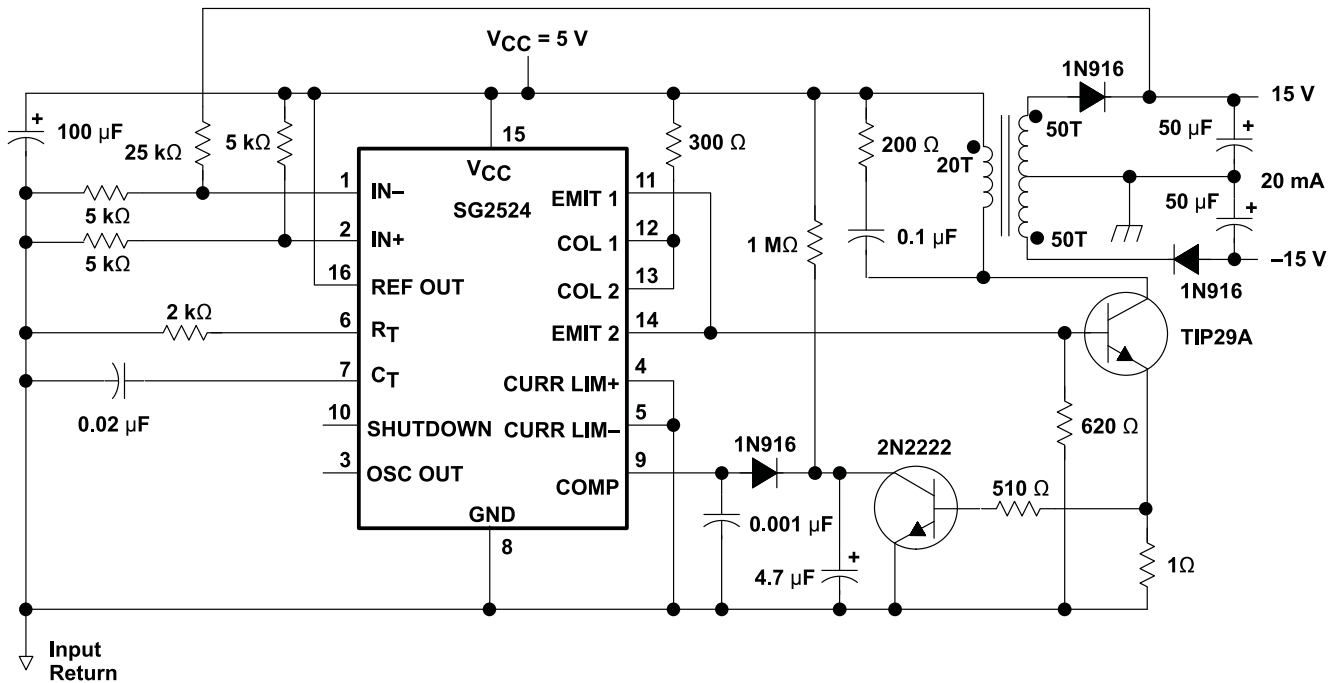


图 10-7. Flyback Converter Circuit Schematic

### 10.3.2 Single-Ended LC

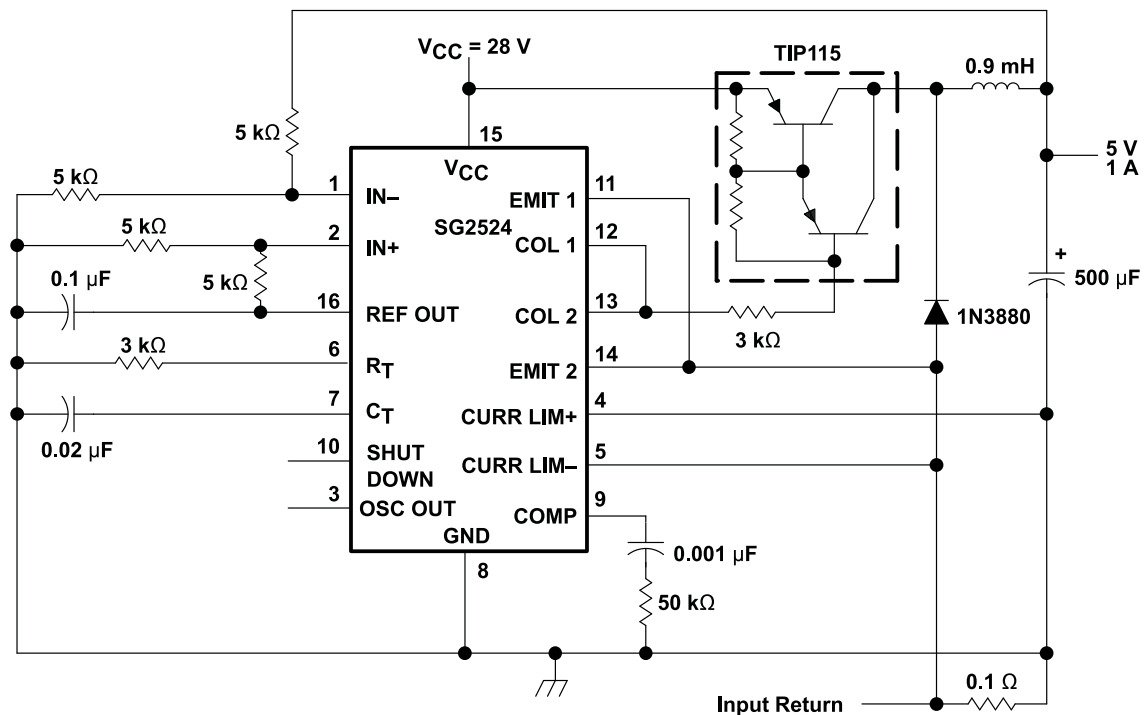


图 10-8. Single-Ended LC Circuit Schematic



### 10.3.3 Push-Pull Transformer-Coupled

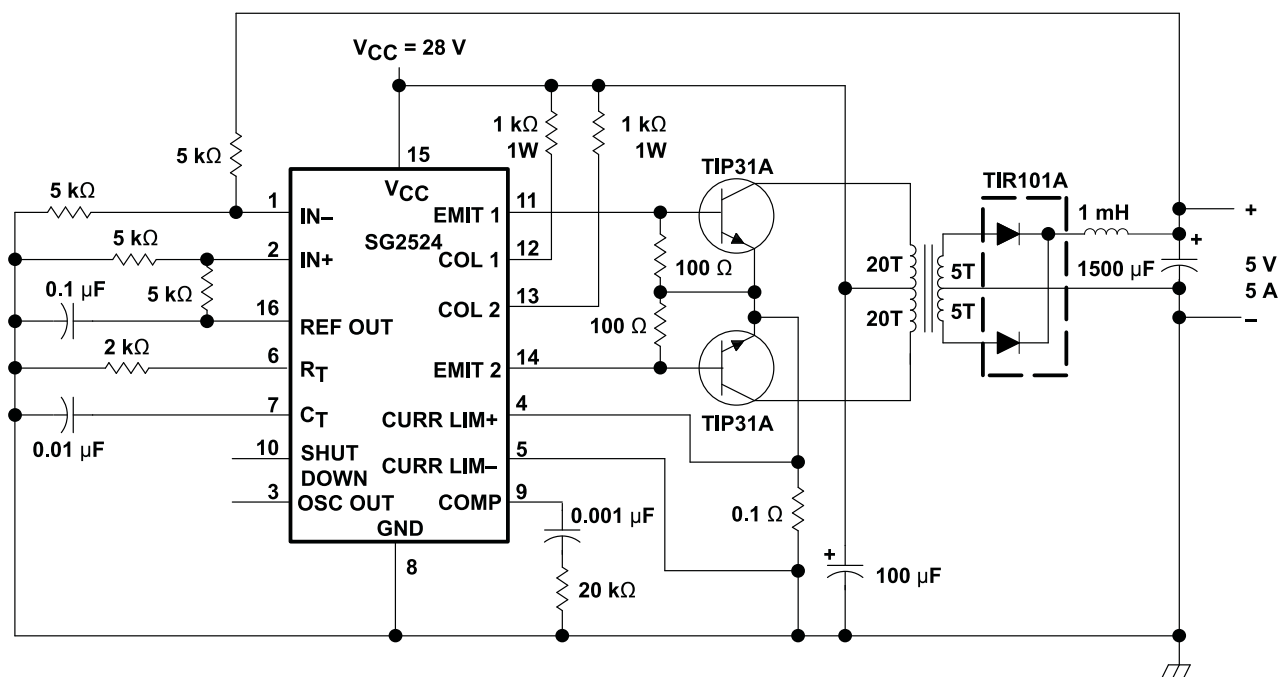


图 10-9. Push-Pull Transformer-Coupled Circuit Schematic

## Power Supply Recommendations

SGx524 is designed to operate from an input voltage supply range between 8 V and 40 V. This input supply should be well regulated. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A tantalum capacitor with a value of 47  $\mu$ F is a typical choice, however this may vary depending upon the output power being delivered.

## 10 Layout

### 10.1 Layout Guidelines

Always try to use a low EMI inductor with a ferrite type closed core. Some examples would be toroid and encased E core inductors. Open core can be used if they have low EMI characteristics and are located a bit more away from the low power traces and components. Make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise.

#### 10.1.1 Feedback Traces

Try to run the feedback trace as far from the inductor and noisy power traces as possible. You would also like the feedback trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from inductor EMI and other noise sources is the more critical of the two. Run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

#### 10.1.2 Input/Output Capacitors

When using a low value ceramic input filter capacitor, it should be located as close to the VIN pin of the IC as possible. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons. In this case it should also be positioned as close to the IC as possible. Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

#### 10.1.3 Compensation Components

External compensation components for stability should also be placed close to the IC. Surface mount components are recommended here as well for the same reasons discussed for the filter capacitors. These should not be located very close to the inductor either.

#### 10.1.4 Traces and Ground Planes

Make all of the power (high-current) traces as short, direct, and thick as possible. It is good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere. The inductor, output capacitors, and output diode should be as close to each other possible. This helps reduce the EMI radiated by the power traces due to the high switching currents through them. This will also reduce lead inductance and resistance as well, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors.

The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This will reduce noise as well by reducing ground loop errors as well as by absorbing more of the EMI radiated by the inductor. For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance. On multi-layer boards the use of vias will be required to connect traces and different planes. It is good practice to use one standard via per 200 mA of current if the trace will need to conduct a significant amount of current from one plane to the other.

Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states. One state when the switch is on and one when the switch is off. During each state there will be a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

## 10.2 Layout Example

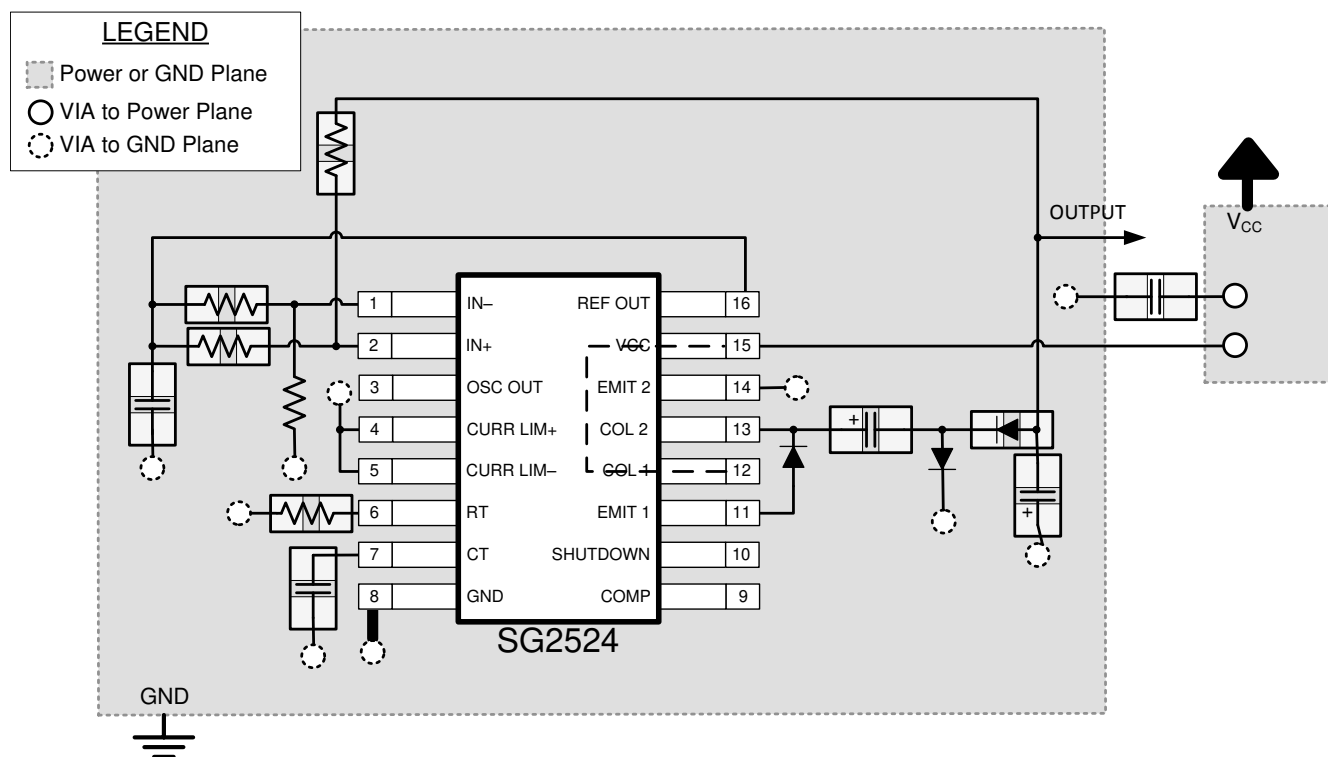


图 10-1. Layout Example for SG2524

## 11 Device and Documentation Support

### 11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 11-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SG2524	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SG3524	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 11.2 Trademarks

所有商标均为其各自所有者的财产。

### Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SG2524D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	SG2524	<a href="#">Samples</a>
SG2524DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	SG2524	<a href="#">Samples</a>
SG2524DRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	SG2524	<a href="#">Samples</a>
SG2524DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	SG2524	<a href="#">Samples</a>
SG2524N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	SG2524N	<a href="#">Samples</a>
SG3524D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SG3524	<a href="#">Samples</a>
SG3524DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SG3524	<a href="#">Samples</a>
SG3524DRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SG3524	<a href="#">Samples</a>
SG3524N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SG3524N	<a href="#">Samples</a>
SG3524NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SG3524N	<a href="#">Samples</a>
SG3524NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SG3524	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SG2524DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SG2524DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SG3524DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SG3524NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SG2524DR	SOIC	D	16	2500	333.2	345.9	28.6
SG2524DRG4	SOIC	D	16	2500	333.2	345.9	28.6
SG3524DR	SOIC	D	16	2500	333.2	345.9	28.6
SG3524NSR	SO	NS	16	2000	853.0	449.0	35.0

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## 重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (<https://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 或 [ti.com.cn](https://www.ti.com.cn) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2021 德州仪器半导体技术（上海）有限公司