

# UC1845A-SP QML V 类 耐辐射电流模式 PWM 控制器

## 1 特性

- 符合 QML V 类 (QMLV) 标准, SMD 5962-86704
- 5962P8670411Vxx: <sup>(1)</sup>
  - 抗辐射加固保障 (RHA) 能力高达 30-krad(Si) 总电离剂量 (TID)
  - 通过了 45krad/LDR (10mrad/s) 测试条件 (符合 MIL-STD-883 测试方法 1019.9 的 3.13.3.b 小节定义的 1.5 倍过量测试) 下的功能性测试且在规定的后辐射参数限值范围内
  - 展现出低剂量率灵敏度 <sup>(2)</sup>但在 30krad 总剂量水平下仍保持在 MIL-STD-883, TM1019 所允许的预辐射电气限制范围内
- 经过优化适用于 DC-DC 转换器 应用
- 低启动电流 (< 0.5mA)
- 修整的振荡器放电电流
- 自动前馈补偿
- 逐脉冲电流限制
- 增强型负载响应特性
- 带滞后的欠压闭锁 (UVLO) 保护
- 双脉冲抑制
- 高电流推挽式输出
- 内部调整的带隙参考
- 500kHz 工作频率
- 低  $R_O$  误差放大器
- 支持军用级温度范围 (-55°C 至 125°C)

- (1) 改进的 TID 辐射性能仅适用于抗辐射加固保障 (RHA) 器件类型 11。
- (2) 受影响的参数参考输出电压,  $V_{REF}$  辐射漂移曲线 (请参见 [VREF 辐射漂移曲线](#))。

## 2 应用

- 抗辐射加固型 DC-DC 转换器
- 卫星本体和有效载荷
- 太空运载火箭
- 水下布线
- 支持多种拓扑结构:
  - 反激、正激、降压、升压
  - 推挽、半桥、全桥 (采用外部接口电路时)

## 3 说明

UC1845A-SP 控制 IC是与 UC184x 系列引脚兼容的抗辐射加固版。它主要适用于卫星和其他恶劣环境应用。该器件提供了控制电流模式开关电源所必需的特性,并改进了多种功能。额定启动电流低于 0.5mA,振荡器放电电流调整为 8.3mA。UVLO 期间,输出级在低于 1.2V 的电压下至少具有 10mA 的灌电流能力 ( $V_{CC}$  高于 5V)。

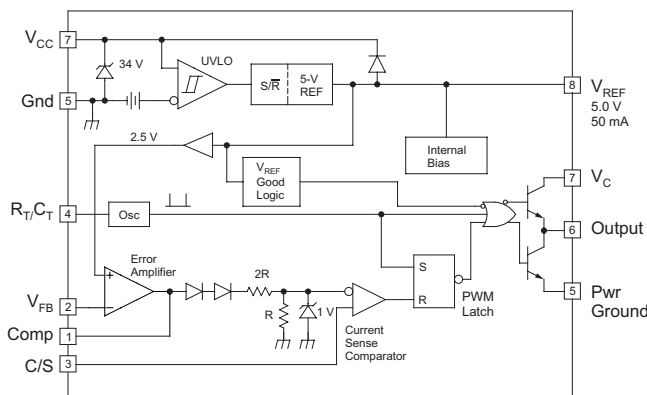
器件比较表显示了该系列各成员器件间的不同之处。要订购辐射改进型版本 (如已提供), 请参考相应的产品数据表。

器件信息<sup>(1)</sup>

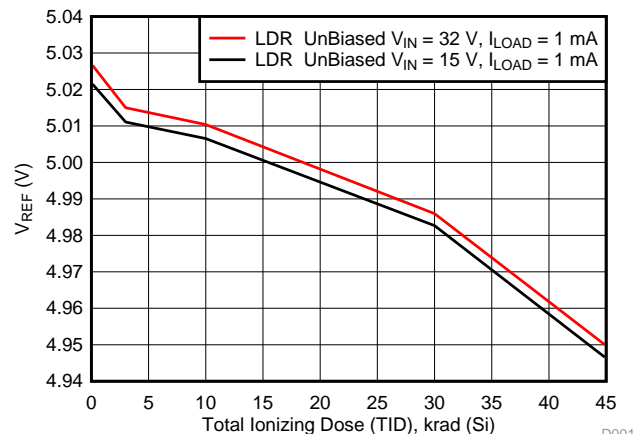
器件型号	封装	封装尺寸 (标称值)
UC1845A-SP	CDIP/JG (8)	6.67mm x 9.60mm
	LCCC/FK (20)	8.89mm x 8.89mm
	CFP/HKU (10)	6.48mm x 7.02mm

- (1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

简化电路原理图



$V_{REF}$  辐射漂移曲线



D001



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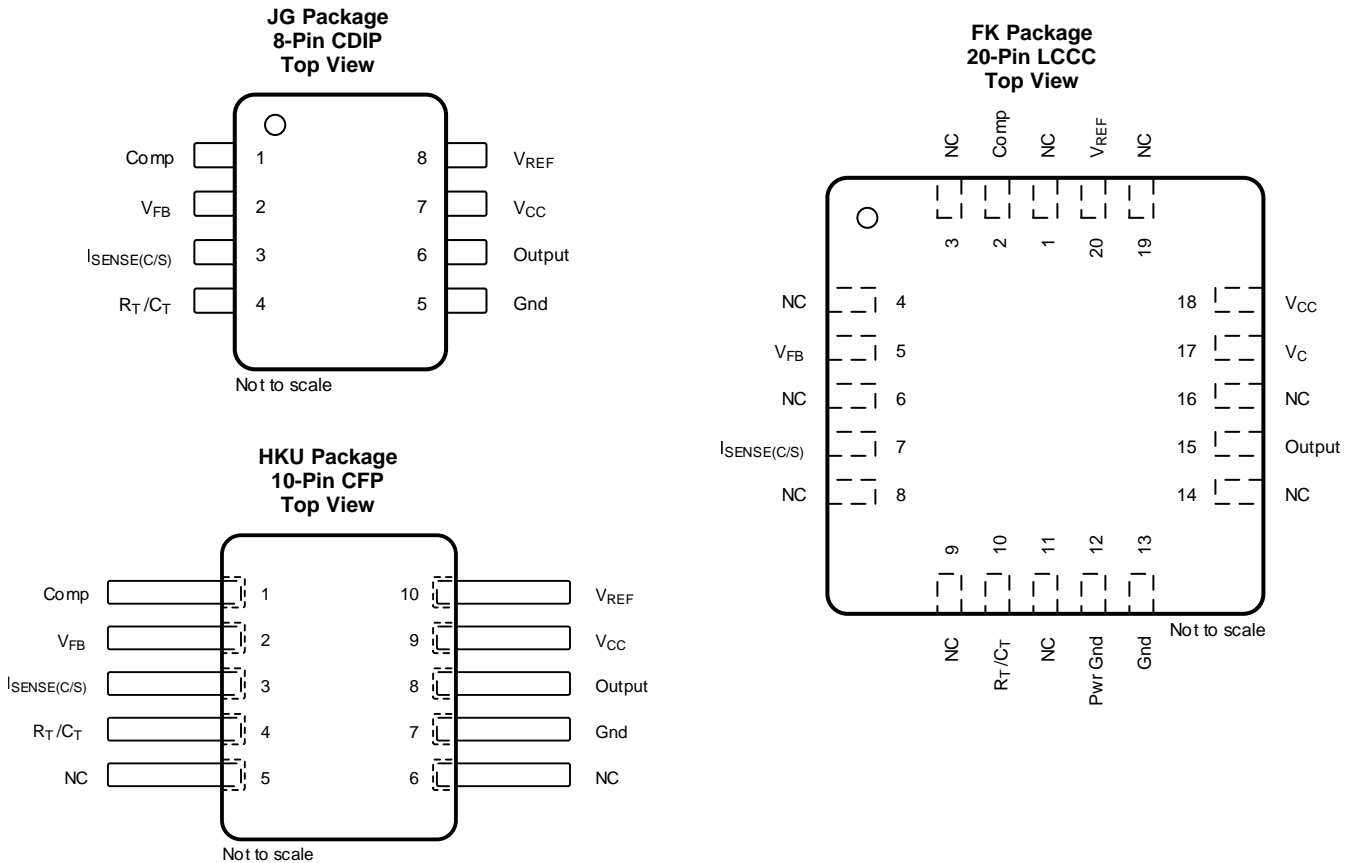
## 4 修订历史记录

Changes from Original (May 2015) to Revision A	Page
• Changed the <i>Pin Configuration</i> images .....	<b>3</b>
• Changed CT (pF) To: CT (μF) in <a href="#">Equation 1</a> .....	<b>15</b>

## 5 Device Comparison Table

PART NO.	UVLO ON	UVLO OFF	MAXIMUM DUTY CYCLE
UC1842A	16 V	10 V	<100%
UC1843A	8.5 V	7.9 V	<100%
UC1844A	16 V	10 V	<50%
UC1845A	8.5 V	7.9 V	<50%

## 6 Pin Configuration and Functions



### Pin Functions

PIN				I/O	DESCRIPTION
NAME	CDIP	LCCC	CFP		
Comp	1	2	1	I	Error amplifier output.
V <sub>FB</sub>	2	5	2	I	Voltage feedback input to error amplifier.
I <sub>SENSE(C/S)</sub>	3	7	3	I	Current sense comparator input pin.
R <sub>T</sub> /C <sub>T</sub>	4	10	4	I	RC time constant input to oscillator.
NC	—	1, 3, 4, 6, 8, 9, 11, 14, 16, 19	5, 6	—	No connect.
Pwr Gnd	—	12	—	—	Output section ground.
Gnd	5	13	7	—	Ground.
Output	6	15	8	O	Regulated output.
V <sub>C</sub>	—	17	—	—	Output section supply voltage.
V <sub>CC</sub>	7	18	9	—	Unregulated supply voltage.

**Pin Functions (continued)**

PIN				I/O	DESCRIPTION
NAME	CDIP	LCCC	CFP		
V <sub>REF</sub>	8	20	10	O	5-V internally generated reference.

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)(2)</sup>

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage, low-impedance source		30	V
V <sub>I</sub>	Input voltage (V <sub>FB</sub> , I <sub>SENSE</sub> )	−0.3	6.3	V
	Supply current	Self limiting		
I <sub>O</sub>	Output current		±1	A
	Error amplifier output sink current		10	mA
	Output energy (capacitive load)		5	μJ
P <sub>D</sub>	Power dissipation (T <sub>A</sub> = 25°C)		1	W
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground. Currents are positive in, negative out of the specified terminal.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

 over operating free-air temperature range (T<sub>A</sub> = T<sub>J</sub> = −55°C to 125°C), unless otherwise noted

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	12	25	V
	Sink/source output current (continuous or time average)	0	200	mA
	Reference load current	0	20	mA

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		UC1845A-SP			UNIT
		JG (CDIP)	FK (LCCC)	HKU (CFP)	
		8 PINS	20 PINS	10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	103	—	51.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	9.6	9.0	6.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	69.2	—	31.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	13.9	—	5.42	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	73	—	31	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

 $V_{CC} = 15\text{ V}^{(1)}$ ,  $R_T = 10\text{ k}\Omega$ ,  $C_T = 3.3\text{ nF}$ ,  $T_A = T_J = -55^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted) <sup>(2)</sup>

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE						
Output voltage	$T_J = 25^{\circ}\text{C}$ , $I_O = 1\text{ mA}$ , $V_{CC} = 15\text{ V}$	5962-8670408VxA	4.95	5	5.06	V
		5962P8670411Vxx Pre-radiation	4.94	5	5.06	
		5962P8670411Vxx Post-radiation	4.85		5.06	
Line regulation	$V_{IN} = 12\text{ to }25\text{ V}$			6	20	mV
Load regulation	$I_O = 1\text{ to }20\text{ mA}$			6	25	mV
Temperature stability <sup>(3)(4)(5)</sup>				0.2	0.4	mV/ $^{\circ}\text{C}$
Total output variation <sup>(3)</sup>	Over line, load, and temperature		4.9		5.1	V
Output noise variation	$10\text{ Hz} \leq f \leq 10\text{ kHz}$ , $T_J = 25^{\circ}\text{C}$			50		$\mu\text{V}$
Long-term stability <sup>(5)</sup>	1000 hours, $T_A = 125^{\circ}\text{C}^{(3)}$			5	25	mV
Short-circuit output current			-30	-100	-180	mA
OSCILLATOR						
Initial accuracy	$T_J = 25^{\circ}\text{C}^{(6)}$		47	52	57	kHz
Voltage stability	$V_{CC} = 12\text{ to }25\text{ V}$			0.2%	1%	
Temperature stability	$T_J = -55^{\circ}\text{C}$ to $125^{\circ}\text{C}^{(3)}$			5%		
Amplitude	$V_{RT/CT}$ peak to peak <sup>(3)</sup>			1.7		V
Discharge current	$V$ pin 4 = $2\text{ V}^{(7)}$	$T_J = 25^{\circ}\text{C}$	7.8	8.3	8.8	mA
		$T_J = \text{Full range}$	7.5		8.8	mA
ERROR AMPLIFIER						
Input voltage	$V_{Comp} = 2.5\text{ V}$		2.45	2.50	2.55	V
Input bias current				-0.3	-1	$\mu\text{A}$
Open-loop voltage gain	$V_O = 2\text{ to }4\text{ V}$		65	90		dB
Unity-gain bandwidth	$T_J = 25^{\circ}\text{C}^{(3)}$		0.7	1		MHz
PSRR	$V_{CC} = 12\text{ to }25\text{ V}$		60	70		dB
Output sink current	$V_{FB} = 2.7\text{ V}$ , $V_{Comp} = 1.1\text{ V}$		2	6		mA
Output source current	$V_{FB} = 2.3\text{ V}$ , $V_{Comp} = 5\text{ V}$		-0.5	-0.8		mA
High-level output voltage	$V_{FB} = 2.3\text{ V}$ , $R_L = 15\text{ k}\Omega$ to ground		5	6		V
Low-level output voltage	$V_{FB} = 2.7\text{ V}$ , $R_L = 15\text{ k}\Omega$ to $V_{REF}$			0.7	1.1	V
CURRENT SENSE						
Gain <sup>(8)(9)</sup>			2.85	3	3.15	V/V
Maximum input signal	$V_{Comp} = 5\text{ V}^{(8)}$		0.9	1	1.1	V
PSRR	$V_{CC} = 12\text{ to }25\text{ V}^{(8)}$			70		dB
Input bias current				-2	-10	$\mu\text{A}$
Delay to output	$V_{ISENSE} = 0\text{ to }2\text{ V}^{(3)}$			150	300	ns

(1) Adjust  $V_{CC}$  above the start threshold before setting at 15 V.

(2) See [机械、封装和可订购信息](#) for radiation improved devices.

(3) Parameters ensured by design and/or characterization, if not production tested.

(4) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:  
Temperature Stability =  $(V_{\text{REF}}(\text{max}) - V_{\text{REF}}(\text{min})) / (T_J(\text{max}) - T_J(\text{min}))$ .  $V_{\text{REF}}(\text{max})$  and  $V_{\text{REF}}(\text{min})$  are the maximum and minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.

(5) Parameter applies only for 5962-8670408VxA.

(6) Output frequency is one-half oscillator frequency for UC1845A.

(7) This parameter is measured with  $R_T = 10\text{ k}\Omega$  to  $V_{\text{REF}}$ . This contributes approximately 300  $\mu\text{A}$  of current to the measurement. The total current flowing into the  $R_T$  or  $C_T$  pin will be approximately 300  $\mu\text{A}$  higher than the measured value.

(8) Parameter measured at trip point of latch with  $V_{FB} = 0\text{ V}$ .

(9) Gain defined as:  $G = \Delta V_{\text{Comp}} / \Delta V_{\text{ISENSE}}$ ;  $V_{\text{ISENSE}} = 0\text{ to }0.8\text{ V}$ .

## Electrical Characteristics (continued)

$V_{CC} = 15\text{ V}^{(1)}$ ,  $R_T = 10\text{ k}\Omega$ ,  $C_T = 3.3\text{ nF}$ ,  $T_A = T_J = -55^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted) <sup>(2)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT</b>					
Output low-level voltage	$I_{SINK} = 20\text{ mA}$		0.1	0.4	V
	$I_{SINK} = 200\text{ mA}$		1.5	2.2	
Output high-level voltage	$I_{SOURCE} = -20\text{ mA}$	13	13.5		V
	$I_{SOURCE} = -200\text{ mA}$	12	13.5		
Rise time	$C_L = 1\text{ nF}$ , $T_J = 25^\circ\text{C}^{(3)}$		50	150	ns
Fall time	$C_L = 1\text{ nF}$ , $T_J = 25^\circ\text{C}^{(3)}$		50	150	ns
UVLO saturation	$V_{CC} = 5\text{ V}$ , $I_{SINK} = 10\text{ mA}$		0.7	1.2	V
<b>UNDervoltage LOCKOUT</b>					
Start threshold		7.8	8.4	9	V
Minimum operation voltage after turnon		7	7.6	8.2	V
<b>PWM</b>					
Maximum duty cycle		47%	48%	50%	
Minimum duty cycle				0%	
<b>TOTAL STANDBY CURRENT</b>					
Start-up current			0.3	0.5	mA
Operating supply current	$V_{FB} = V_{ISENSE} = 0\text{ V}$		11	17	mA
$V_{CC}$ Zener voltage	$I_{CC} = 25\text{ mA}$	30	34		V

## 7.6 Typical Characteristics

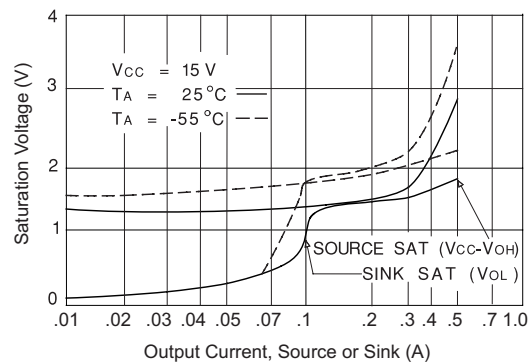


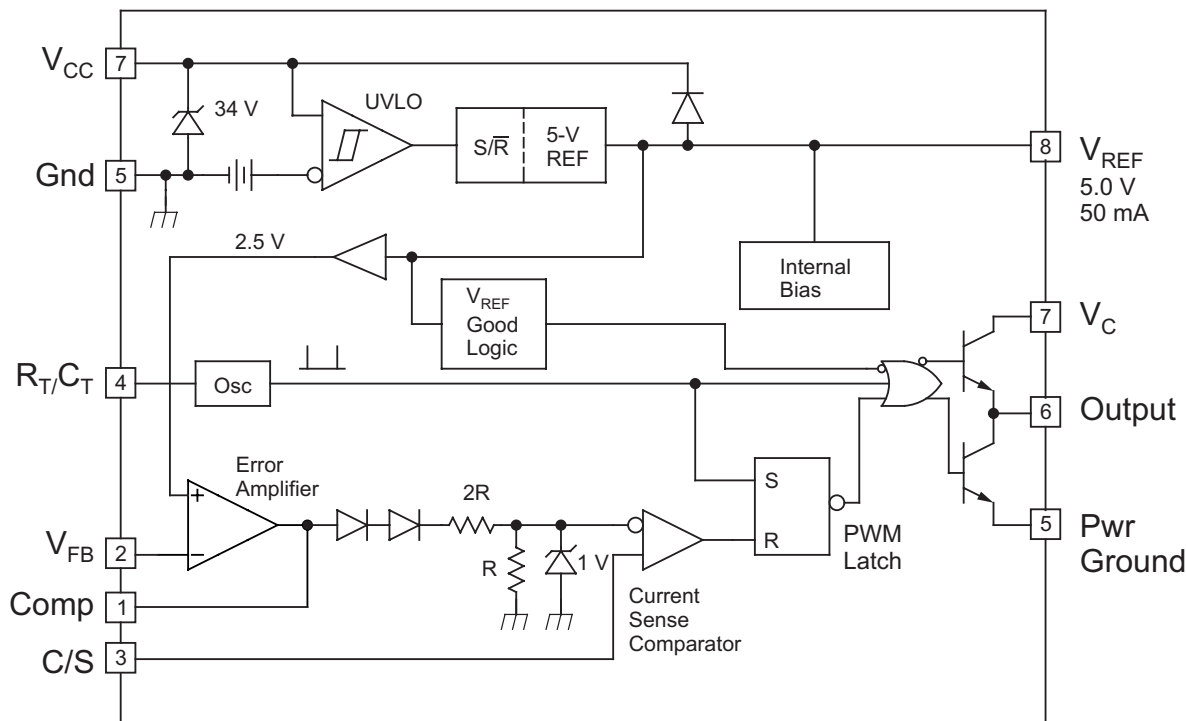
Figure 1. Output Saturation Characteristics

## 8 Detailed Description

### 8.1 Overview

The UC1845A-SP control IC is a pin-for-pin compatible improved version of the UC184x family. Providing the necessary characteristics to control current-mode switched-mode power supplies, this device has improved features. Start-up current is specified to be less than 0.5 mA and oscillator discharge is trimmed to 8.3 mA. During UVLO, the output stage can sink at least 10 mA at less than 1.2 V for  $V_{CC}$  over 5 V.

### 8.2 Functional Block Diagram



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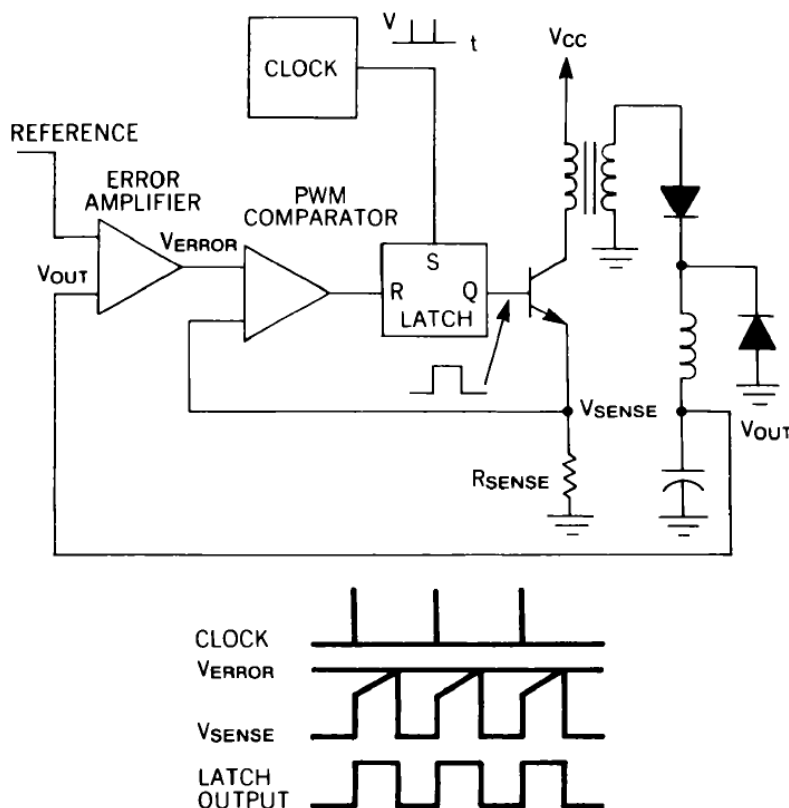
### 8.3 Feature Description

UC1845A-SP is a current mode controller, used to support various topologies such as forward, flyback, buck, boost and using an external interface circuit will also support half-bridge, full-bridge, and push-pull configurations.

Figure 2 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way, the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; that is, the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

## Feature Description (continued)



0019-1

**Figure 2. Two-Loop Current-Mode Control System**

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an error-voltage-controlled-current-source for the purposes of small-signal analysis (see [Figure 3](#)). The two-pole control-to-output frequency response of these converters is reduced to a single-pole (filter capacitor in parallel with load) response. One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gain bandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler, as shown in [Figure 4](#).

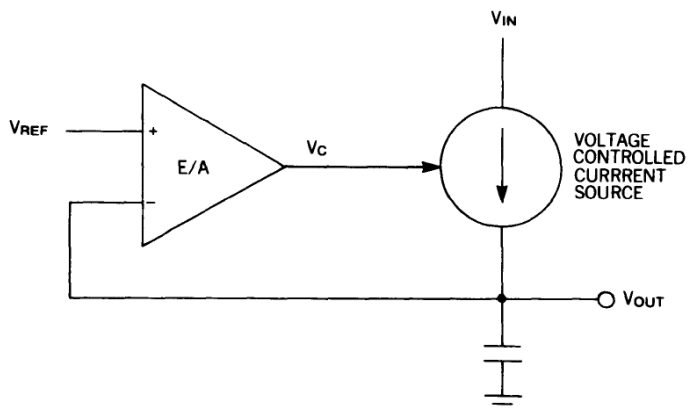
Capacitor  $C_i$  and resistor  $R_i$ , in [Figure 4\(A\)](#), add a low-frequency zero, which cancels one of the two control-to-output poles of non-current-mode converters. For large signal load changes, in which converter response is limited by inductor slew rate, the error amplifier saturates while the inductor is catching up with the load. During this time,  $C_i$  charges to an abnormal level. When the inductor current reaches its required level, the voltage on  $C_i$  causes a corresponding error in supply output voltage. The recovery time is  $R_{iz}C_i$ , which may be long. However, the compensation network of [Figure 4\(B\)](#) can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of  $C_i$ .

Current limiting is greatly simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

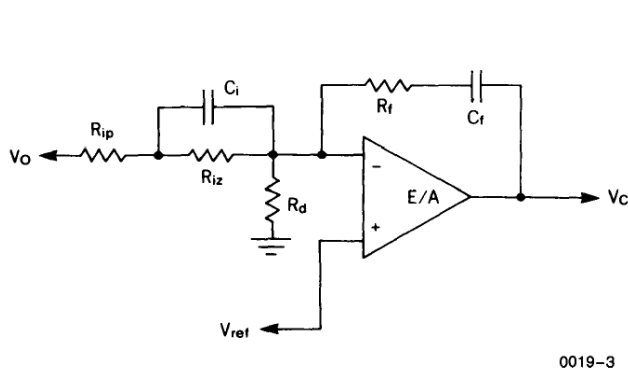


## Feature Description (continued)



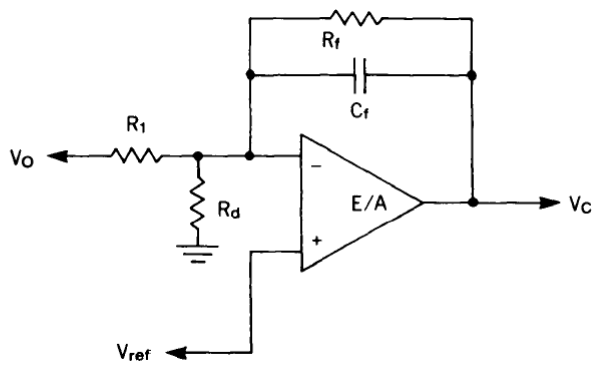
0019-2

Figure 3. Inductor Looks Like a Current Source to Small Signals



0019-3

A. Direct duty cycle control



0019-4

B. Current mode control

Figure 4. Required Error Amplifier Compensation for Continuous Inductor Current Designs

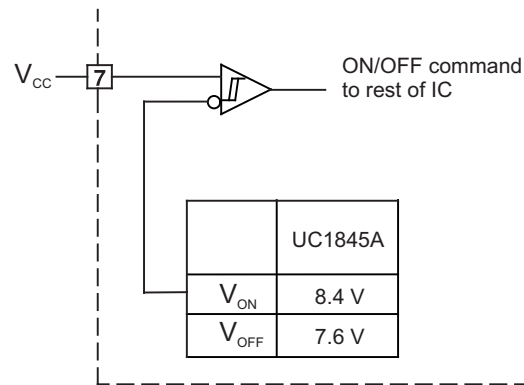
### 8.3.1 UVLO

The UVLO circuit ensures that  $V_{CC}$  is adequate to make the UC1845A-SP fully operational before enabling the output stage. Figure 5 shows that the UVLO turnon and turnoff thresholds are fixed internally at 8.5 V and 7.9 V, respectively. The 0.6-V hysteresis prevents  $V_{CC}$  oscillations during power sequencing.

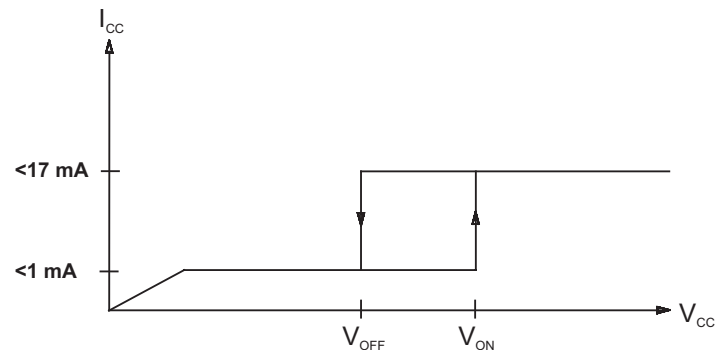
Figure 6 shows supply current requirements. Start-up current is  $< 1$  mA for efficient bootstrapping from the rectified input of an off-line converter, as shown in Figure 7. During normal circuit operation,  $V_{CC}$  is developed from auxiliary winding,  $WAux$ , with  $D_1$  and  $C_{IN}$ . However, at start-up,  $C_{IN}$  must be charged to 16 V through  $R_{IN}$ . With a start-up current of 1 mA,  $R_{IN}$  can be as large as 100 k $\Omega$  and still charge  $C_{IN}$  when  $V_{AC} = 90$ -V RMS (low line). Power dissipation in  $R_{IN}$  would then be less than 350 mW even under high line ( $V_{AC} = 130$ -V RMS) conditions.

During UVLO, the output driver is in a low state. While it does not exhibit the same saturation characteristics as normal operation, it can easily sink 1 mA, enough to ensure the MOSFET is held off.

## Feature Description (continued)

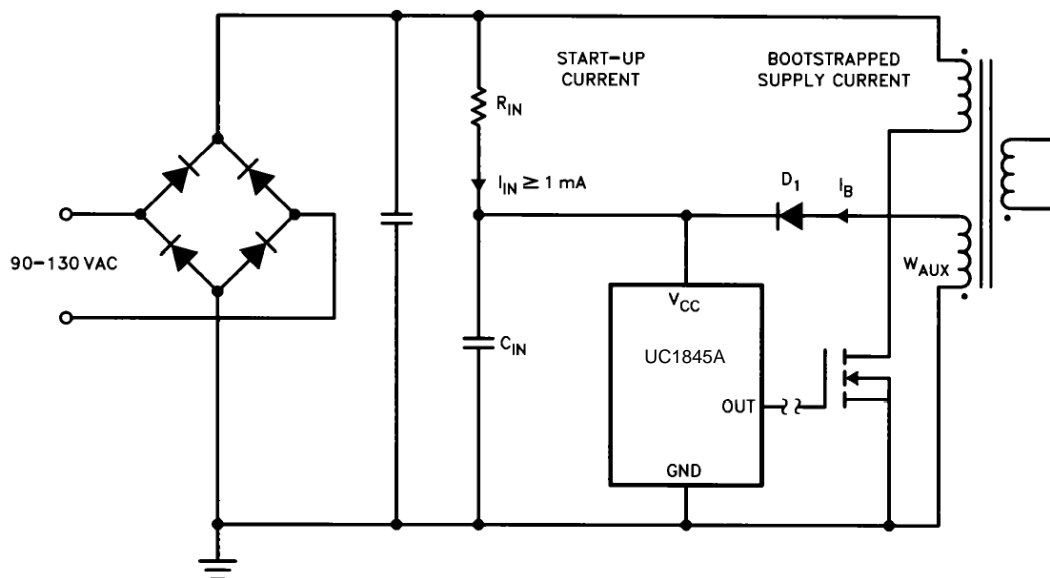


**Figure 5. UVLO Turnon TurnOff Threshold**



During UVLO, the output driver is biased to sink minor amounts of current.

**Figure 6. Supply Current Requirements**



0019-8

**Figure 7. Providing Power to the UC1845A-SP**

## Feature Description (continued)

### 8.3.2 Reference

As highlighted in the [Functional Block Diagram](#), UC1845A-SP incorporates a 5-V internal reference regulator with  $\pm 2\%$  set point variation over temperature.

### 8.3.3 Totem-Pole Output

The UC1845A-SP PWM has a single totem-pole output which can be operated to  $\pm 1$ -A peak for driving MOSFET gates, and a +200 mA average current for bipolar power U-100A transistors. Cross conduction between the output transistors is minimal, the average added power with  $V_{IN} = 30$  V is only 80 mW at 200 kHz.

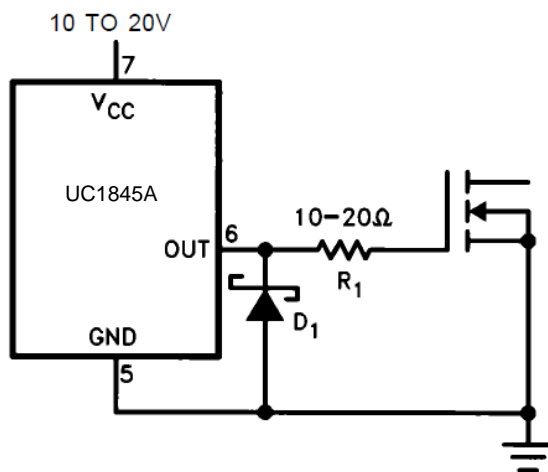
Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage  $V_C$  by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the  $dV/dT$  rate of the totem-pole switching and the FET gate capacitance.

The use of a Schottky diode from the PWM output to ground prevents the output voltage from going excessively below ground, causing instabilities within the IC. To be effective, the diode selected should have a forward drop of less than 0.3 V at 200 mA. Most 1- to 3-A Schottky diodes exhibit these traits above room temperature. Placing the diode as physically close to the PWM as possible enhances circuit performance. Implementation of the complete drive scheme is shown in [Figure 8](#) through [Figure 10](#). Transformer-driven circuits also require the use of the Schottky diodes to prevent a similar set of circumstances from occurring on the PWM output. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

[Figure 8](#) through [Figure 10](#) show suggested circuits for driving MOSFETs and bipolar transistors with the UC1845A-SP output. The simple circuit of [Figure 8](#) can be used when the control IC is not electrically isolated from the MOSFET turnon and turnoff to  $\pm 1$  A. It also provides damping for a parasitic tank circuit formed by the FET input capacitance and series wiring inductance. Schottky diode,  $D_1$ , prevents the output of the IC from going far below ground during turnoff.

[Figure 9](#) shows an isolated MOSFET drive circuit which is appropriate when the drive signal must be level shifted or transmitted across an isolation boundary. Bipolar transistors can be driven efficiently with the circuit of [Figure 10](#). Resistors  $R_1$  and  $R_2$  fix the on-state base current while capacitor  $C_1$  provides a negative base current pulse to remove stored charge at turnoff.

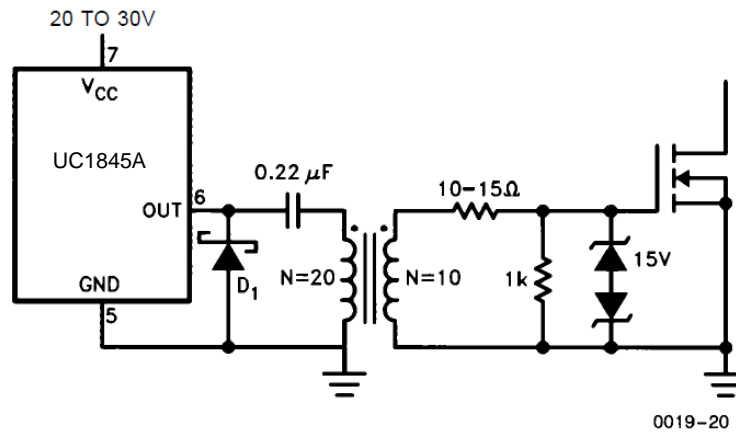
Because the UC1845A-SP series has only a single output, an interface circuit is needed to control push-pull, half-bridge, or full-bridge topologies. The UC1706 dual output driver with internal toggle flip-flop performs this function. [Typical Application](#) shows a typical application for these two ICs. Increased drive capability for driving numerous FETs in parallel, or other loads can be accomplished using one of the UC1705/6/7 driver ICs.



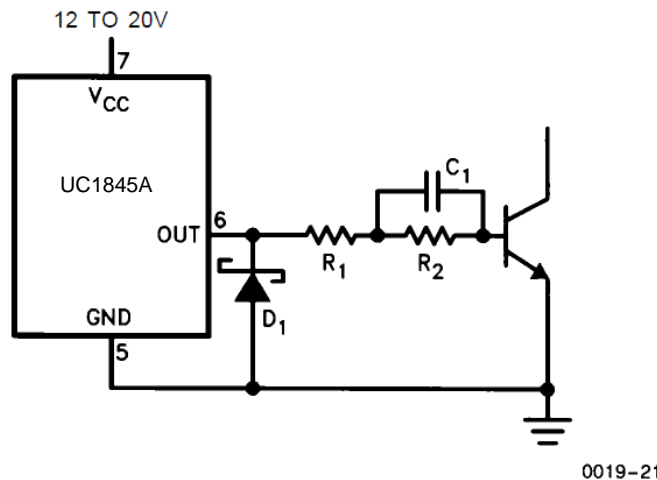
0019-19

Figure 8. Direct MOSFET Drive

## Feature Description (continued)



**Figure 9. Isolated MOSFET Drive**



**Figure 10. Bipolar Drive With Negative turnoff Bias**

## 8.4 Device Functional Modes

The UC1845A-SP uses fixed frequency, peak current mode control. An internal oscillator initiates the turn on of the driver to high-side power switch. The external power switch current is sensed through an external resistor and is compared via internal comparator. The voltage generated at the COMP pin is stepped down via internal resistors (as shown in the functional block diagram). When the sensed current reaches the stepped down COMP voltage, the high-side power switch is turned off.

## 9 Application and Implementation

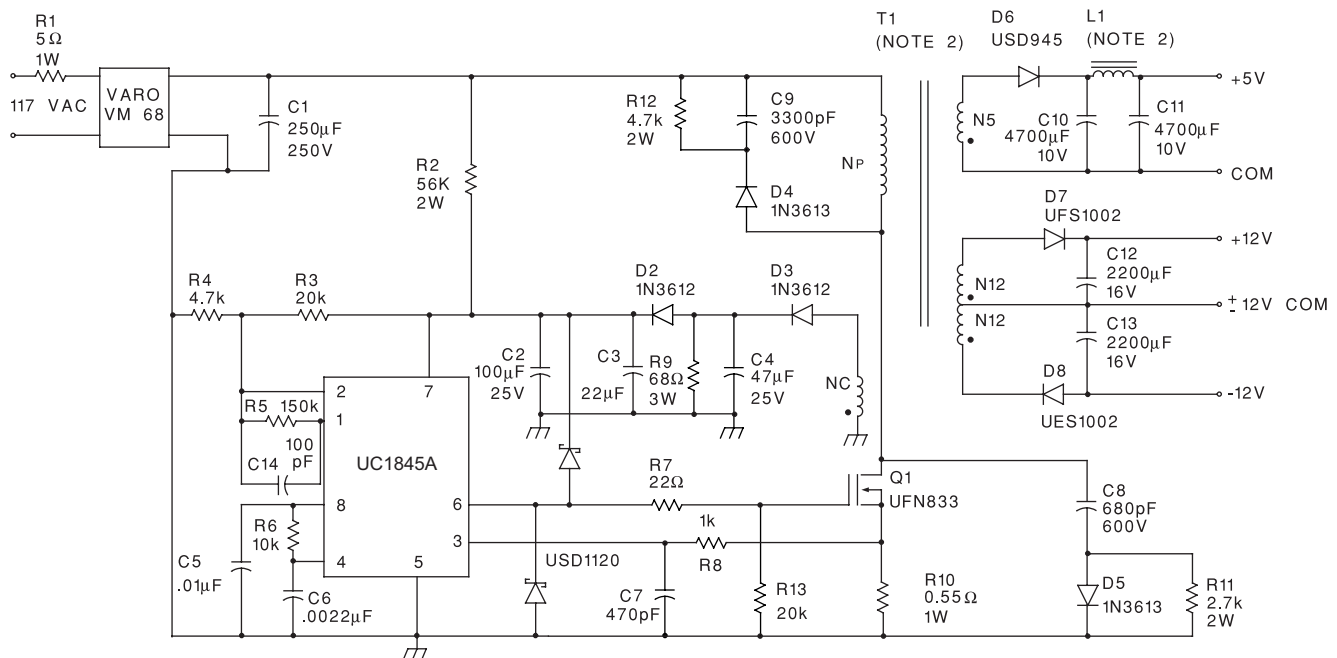
## NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

UC1845A-SP can be used as a controller to design various topologies such as buck, boost, flyback, and forward. Using an external interphase circuit can also support push-pull, half-bridge and full-bridge topologies.

## 9.2 Typical Application



### Figure 11. Typical Application Schematic

### 9.2.1 Design Requirements

See [Table 1](#) for parameter values.

**Table 1. Design Parameters<sup>(1)</sup>**

DESIGN PARAMETER	VALUE
Input voltage	95 VAC to 130 VAC
Line isolation	3750 V
Switching frequency	40 kHz
Efficiency (full load)	70%
Output voltage (A)	+5 V, ±5%; 1-A to 4-A load; Ripple voltage: 50-mV P-P max
Output voltage (B)	+12 V, ±3%; 0.1-A to 0.3-A load; Ripple voltage: 100-mV P-P max
Output voltage (C)	−12 V, ±3%; 0.1-A to 0.3-A load; Ripple voltage: 100-mV P-P max

(1) See Figure 11 for reference.

## 9.2.2 Detailed Design Procedure

See [Table 2](#) for component values.

**Table 2. Components<sup>(1)</sup>**

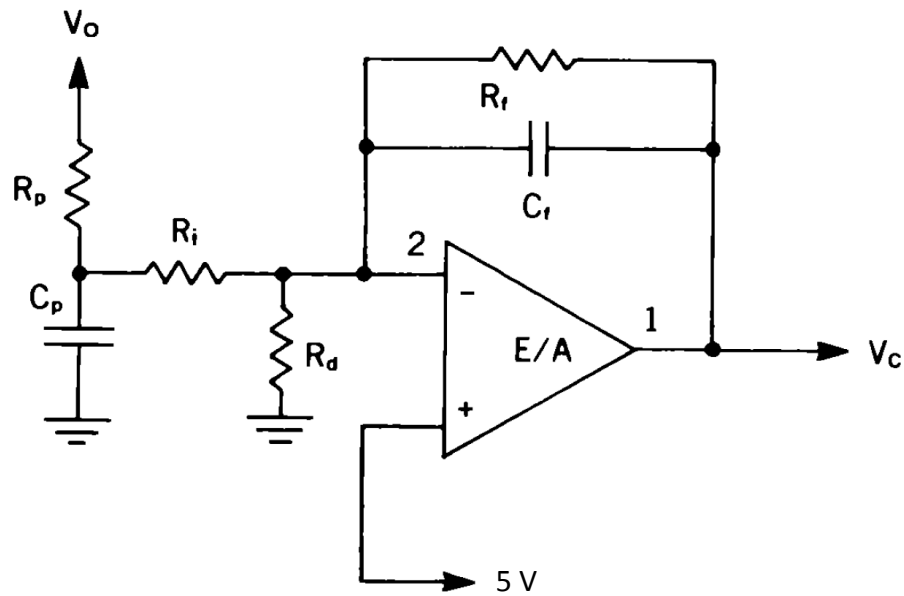
COMPONENT	VALUE
R1	5 $\Omega$ , 1 W
R2	56 k $\Omega$ , 2 W
R3	20 k $\Omega$
R4	4.7 k $\Omega$
R5	150 k $\Omega$
R6	10 k $\Omega$
R7	22 $\Omega$
R8	1 k $\Omega$
R9	68 $\Omega$
R10	0.55 $\Omega$ , 1 W
R11	2.7 k $\Omega$ , 2 W
R12	4.7 k $\Omega$ , 2 W
R13	20 k $\Omega$
C1	250 $\mu$ F, 250 V
C2	100 $\mu$ F, 25 V
C3	22 $\mu$ F
C4	47 $\mu$ F, 25 V
C5	0.1 $\mu$ F
C6	0.0022 $\mu$ F
C7	470 pF
C8	680 pF, 600 V
C9	3300 pF, 600 V
C10	4700 $\mu$ F, 10 V
C11	4700 $\mu$ F, 10 V
C12	2200 $\mu$ F, 10 V
C13	2200 $\mu$ F, 10 V
C14	100 pF
D2	1N3612
D3	1N3612
D4	1N3613
D5	1N3613
D6	USD945
D7	UFS1002
D8	UES1002
Q1	UFN833

(1) See [Figure 11](#) for reference.

### 9.2.2.1 Oscillator

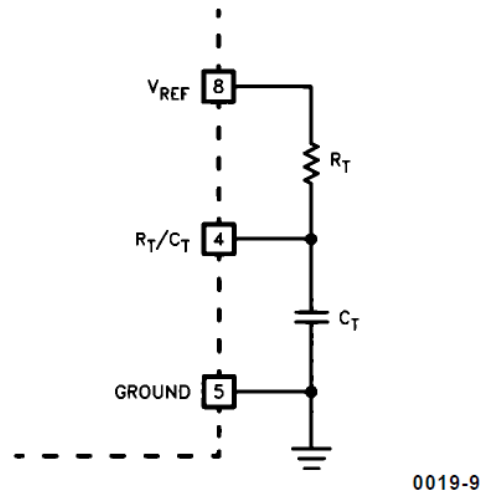
The UC1845A-SP oscillator is programmed as shown in [Figure 13](#). Timing capacitor  $C_T$  is charged from  $V_{REF}$  (5 V) through the timing resistor  $R_T$ , and discharged by an internal current source. The first step in selecting the oscillator components is to determine the required circuit dead time. Once obtained, [Figure 14](#) is used to pinpoint the nearest standard value of  $C_T$  for a given dead time. Next, the appropriate  $R_T$  value is interpolated using the parameters for  $C_T$  and oscillator frequency. [Figure 15](#) shows the  $R_T/C_T$  combinations versus oscillator frequency. The timing resistor can be calculated from the following formula.

$$f_{\text{osc}} \text{ (kHz)} = \frac{1.72}{R_T \text{ (k}\Omega) \times C_T \text{ (}\mu\text{F)}} \quad (1)$$

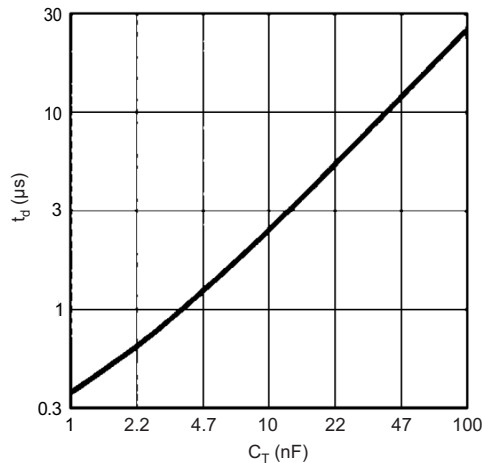
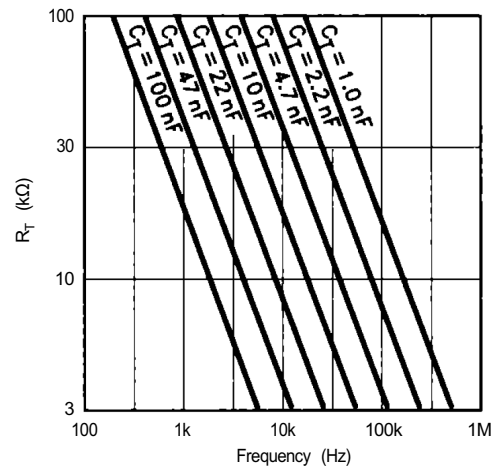


**Figure 12. E/A Compensation Circuit for Continuous Boost and Flyback Topologies**

The UC1845A-SP has an internal divide-by-two flip-flop driven by the oscillator for a 50% maximum duty cycle. Therefore, their oscillators must be set to run at twice the desired power supply switching frequency.



**Figure 13. Oscillator Programming**


**Figure 14. Dead Time vs C<sub>T</sub> (R<sub>T</sub> > 5 kΩ)**

**Figure 15. Timing Resistance vs Frequency**

### 9.2.2.2 Current Sensing and Limiting

The UC1845A-SP current sense input is configured as shown in [Figure 16](#). Current-to-voltage conversion is done externally with ground-referenced resistor R<sub>S</sub>. Under normal operation, the peak voltage across R<sub>S</sub> is controlled by the E/A according to the following relation:

$$I_P = \frac{V_C - 1.4 \text{ V}}{3 R_S}$$

where

- V<sub>C</sub> = Control voltage = E/A output voltage (2)

R<sub>S</sub> can be connected to the power circuit directly or through a current transformer, as [Figure 16](#) shows. While a direct connection is simpler, a transformer can reduce power dissipation in R<sub>S</sub>, reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-referenced sensing. The relation between V<sub>C</sub> and peak current in the power stage is given by:

$$i_{(pk)} = N \left( \frac{V_{R_S(pk)}}{R_S} \right) = \frac{N}{3 R_S} (V_C - 1.4 \text{ V})$$

where

- N = Current sense transformer turns ratio = 1 when transformer not used. (3)

For purposes of small-signal analysis, the control-to-sensed-current gain is:

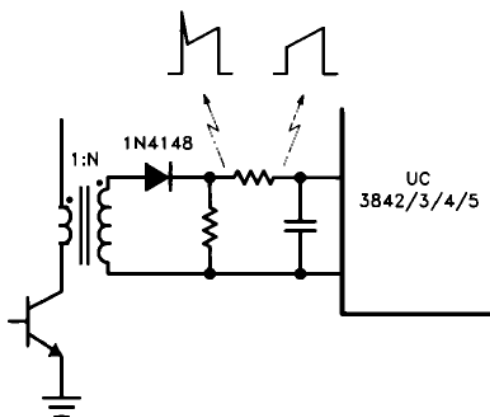
$$\frac{i_{(pk)}}{V_C} = \frac{N}{3 R_S} \quad (4)$$

When sensing current in series with the power transistor, as shown in [Figure 16](#), the current waveform often has a large spike at its leading edge. This spike is due to rectifier recovery and/or inter-winding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC1845A-SP current-sense comparator is internally clamped to 1 V ([Figure 16](#)). Current limiting occurs if the voltage at pin 3 reaches this threshold value, that is, the current limit is defined by:

$$i_{max} = \frac{N \times 1 \text{ V}}{R_S} \quad (5)$$





0019-13

Figure 16. Transformer-Coupled Current Sensing

### 9.2.2.3 Error Amplifier

The error amplifier (E/A) configuration is shown in Figure 17. The non-inverting input is not brought out to a pin, but is internally biased to  $5\text{ V} \pm 2\%$ . The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 18 shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with inductor current. The feedback components add a pole to the loop transfer function at  $f_p = \frac{1}{2} \pi R_F$ .  $R_F$  and  $C_F$  are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit.  $R_I$  and  $R_F$  fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to unity (0 dB) at  $f \approx f_{\text{SWITCHING}} / 4$ . This technique ensures converter stability while providing good dynamic response.

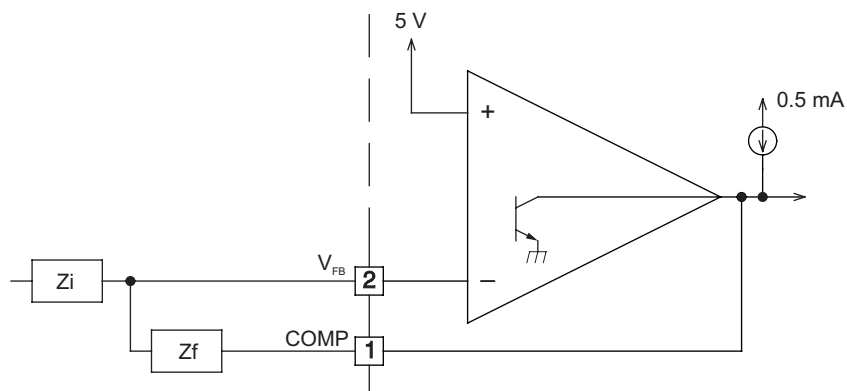
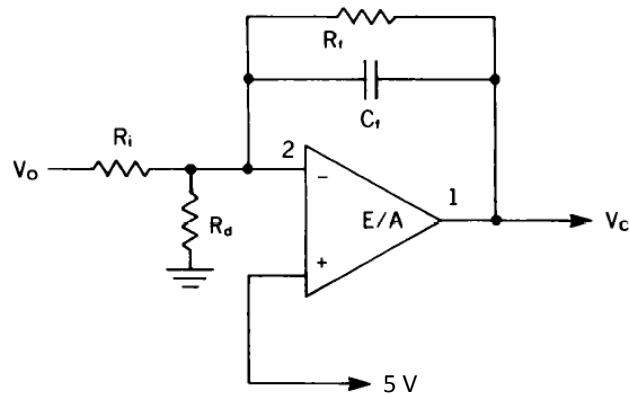


Figure 17. E/A Configuration



0019–15

**Figure 18. Compensation**

The E/A output sources 0.5 mA and sinks 2 mA. A lower limit for  $R_F$  is given by:

$$R_{F(MIN)} \approx \frac{V_{EA\ OUT(MAX)} - 2.5\ V}{0.5\ mA} = \frac{6\ V - 2.5\ V}{0.5\ mA} = 7\ k\Omega \quad (6)$$

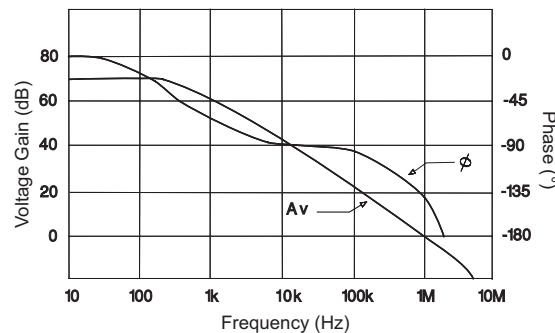
E/A input bias current (2- $\mu$ A max) flows through  $R_i$ , resulting in a DC error in output voltage ( $V_O$ ) given by:

$$\Delta V_{O(MAX)} = (2\ \mu A) R_i \quad (7)$$

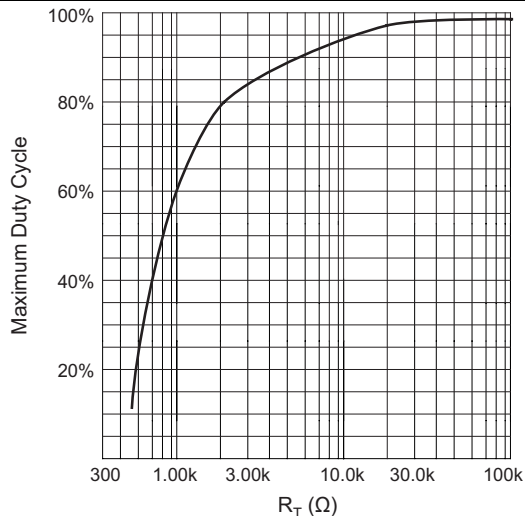
Therefore, the designer should keep the value of  $R_i$ , as low as possible.

Figure 19 shows the open-loop frequency response of the UC1845A-SP E/A. The gain represents an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1 MHz due to second-order poles at about 10 MHz and above.

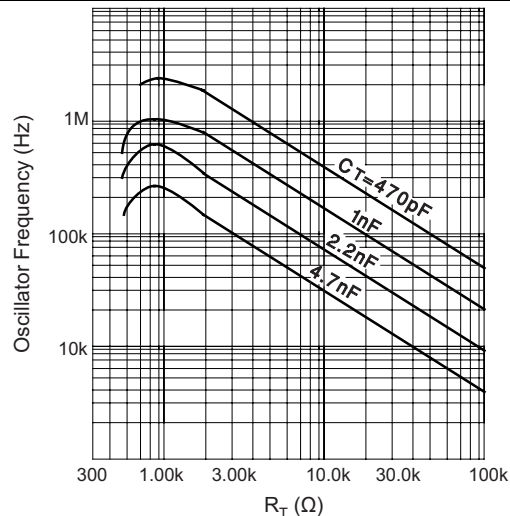
Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero.  $R_P$  and  $C_P$  in the circuit of Figure 12 provide this pole.


**Figure 19. Error Amplifier Open-Loop Frequency Response**

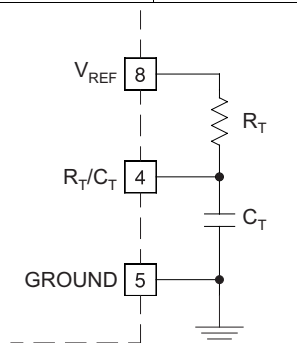
### 9.2.3 Application Curves



**Figure 20. Oscillator Frequency vs Timing Resistance**



**Figure 21. Maximum Duty Cycle vs Timing Resistor**



For  $R_T > 5k$   $f \approx 1.72 / (R_T C_T)$

**Figure 22. Oscillation Schematic**





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### 12.5 术语表

**SLYZ022** — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

## 13 机械、封装和可订购信息

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8670408VPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8670408VPA UC1845A	<a href="#">Samples</a>
5962-8670408VXA	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 8670408VXA UC1845AL QMLV	<a href="#">Samples</a>
5962P8670411VPA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	-55 to 125	P8670411VPA UC1845A-SP	<a href="#">Samples</a>
5962P8670411VYC	ACTIVE	CFP	HKU	10	1	TBD	Call TI	Call TI	-55 to 125	P8670411VYC UC1845A-SP	<a href="#">Samples</a>

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(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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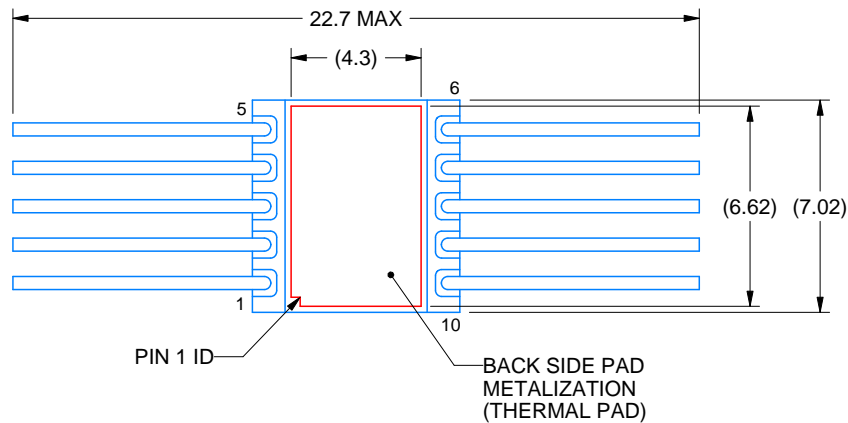
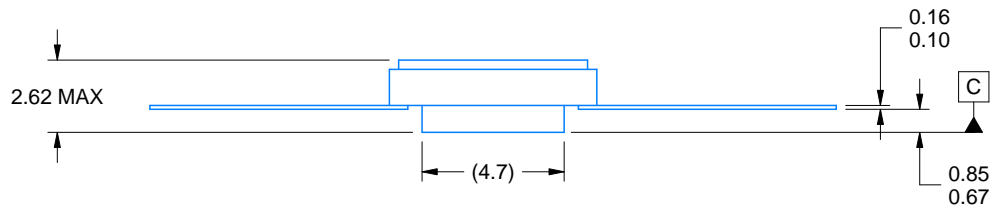
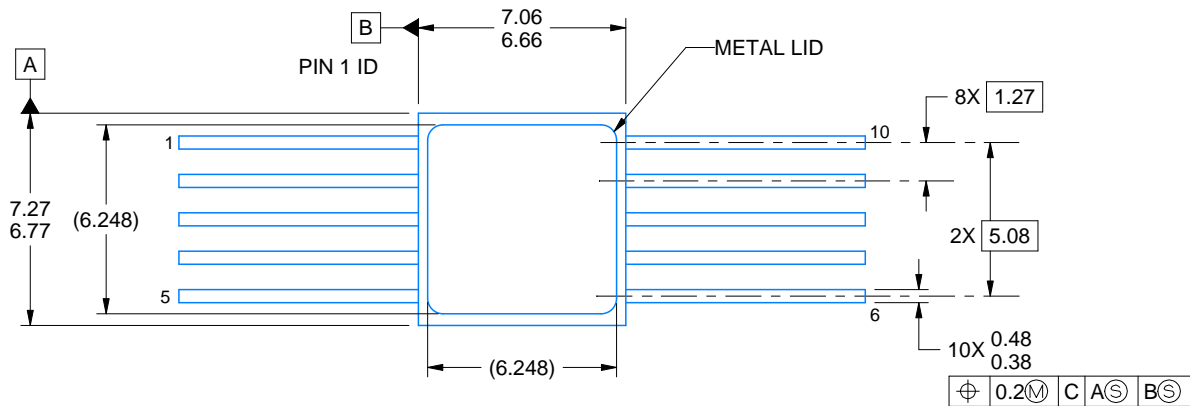


HKU0010A

# PACKAGE OUTLINE

CFP - 2.63mm max height

CERAMIC DUAL FLATPACK



4226200/A 09/2020

## NOTES:

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2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The terminals are gold plated.
5. This drawing does not comply with MIL STD 1835. Do not use this package for compliant product.
6. Metal lid is connected to back side pad metalization.



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
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  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## JG (R-GDIP-T8)

## CERAMIC DUAL-IN-LINE



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  - D. Index point is provided on cap for terminal identification.
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