DLPC300 适用于 DLP3000 DMD 的 DLP® 数字控制器

1 特性

- 用于确保 DLP3000 数字微镜器件 (DMD) 可靠运行
- 多模式，24 位输入端口：
  - 支持最高像素时钟为 33.5MHz 的并行 RGB 和 3 个输入颜色位深选项：
    - 24 位 RGB8888 或者 4:4:4 YCrCb888
    - 18 位 RGB666 或者 4:4:4 YCrCb666
    - 16 位 RGB565 或者 4:2:2 YCrCb565
  - 支持最高像素时钟为 33.5MHz 的 8 位 BT.656 总线模式
- 支持的输入分辨率包括 608 × 684、864 × 480、854 × 480 (WVGA)、640 × 480 (VGA)、320 × 240 (QVGA)
- 样式输入模式
  - 输入数据到微镜的一到一映射
  - 1 位二进制模式速率高达 4000Hz
  - 高达 120Hz 的最高 8 位灰度样式速率
- 具有像素数据处理功能的视频输入模式
  - 支持 1Hz 至 60Hz 的帧速率
  - 可编程后期色彩校正 (Degamma)
  - 空间-时间复用（抖动显示）
  - 自动增益控制
  - 颜色空间转换
- 输出触发信号，用于同步摄像机、传感器等外设
- 系统控制：
  - 器件配置的 I^2C 控制
  - 高达 3 LED 的可编程电流控制
  - 集成的 DMD 复位驱动器控制
  - DMD 水平和垂直显示图像抖动
- 低功耗：低于 93mW（典型值）
- 支持外部存储器：
  - 166MHz 移动 DDR SDRAM
  - 33.3MHz 串行闪存
- 176 引脚、7mm × 7mm、0.4mm 间距、NFBGA 封装

2 应用

- 3D 计量
- 3D 扫描
- 工厂自动化
- 指纹识别
- 条纹投影
- 工业联机检验
- 机器人视觉
- 立体视觉
- 化学检测
- 移动传感
- 光谱分析
- 扩增实境
- 信息叠加
- 医疗仪器
- 虚拟量规

3 说明

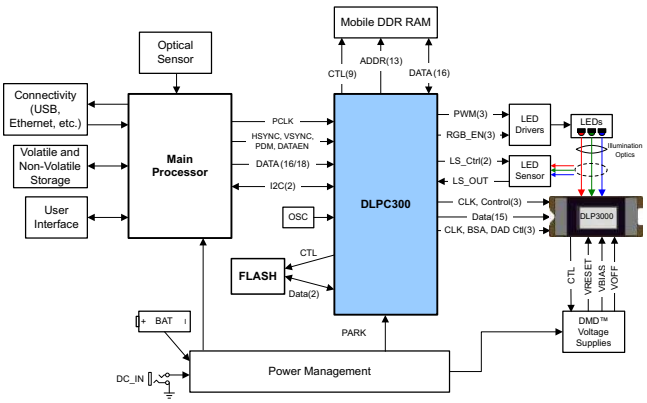
DLPC300 控制器在用户电子设备与 DMD 之间提供一个方便的多功能接口，支持高速模式速率（最高可达 4kHz，二进制模式）并提供 LED 控制和数据格式化，适用于多种输入分辨率。DLPC300 数字控制器属于 DLP3000 芯片组，用于支持 DLP3000 DMD 的可靠运行。DLPC300 还提供输出触发信号，用于将显示的图案与摄像机、传感器等外设同步。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DLPC300	NFBGA (176)	7.00mm x 7.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型嵌入式系统框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (July 2013) to Revision C **Page**

- 已添加 *ESD 额定值表*，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1
- Added active low to $\overline{MEM\_RAS}$, $\overline{MEM\_CAS}$, and $\overline{MEM\_CS}$ in Figure 7 21

Changes from Revision A (July 2012) to Revision B **Page**

- 已更改 GPIO4_INF 至 INIT_DONE 1
- Deleted “RESERVED0” and “RESERVED1” rows in 4
- Deleted “d” from Terminal No. R12 in 4
- Deleted “RESERVED0” and “RESERVED1” rows in 5
- Deleted “d” from Terminal No. R12 in 5
- Changed pin name GPIO4_INTF to INIT_DONE 5
- Changed INIT_DONE (formerly GPIO4_INTF) pin description 5
- Deleted “RESERVED0” and “RESERVED1” rows in 6
- Deleted “d” from Terminal No. R12 in 6
- Deleted “RESERVED0” and “RESERVED1” rows in 7
- Deleted “d” from Terminal No. R12 in 7
- Deleted “RESERVED0” and “RESERVED1” rows in 8
- Deleted “d” from Terminal No. R12 in 8
- Deleted “RESERVED0” and “RESERVED1” rows in 9

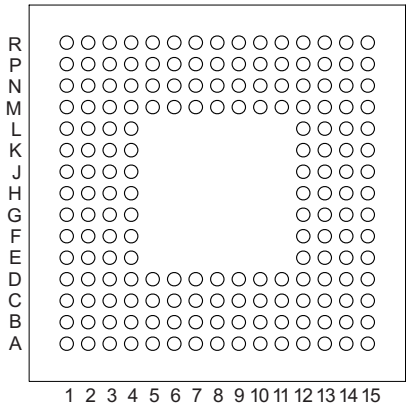
- Deleted “d” from Terminal No. R12 in 9
- Changed pin name GPIO0_CMPPWR to CMP_PWR 9
- Deleted “RESERVED0” and “RESERVED1” rows in 10
- Deleted “d” from Terminal No. R12 in 10
- Changed pin name $\overline{\text{JTAGRSTZ}}$ to $\overline{\text{JTAGRST}}$ 10
- Changed the "Reserved" row information in 10
- Changed Note 1 From: "6 total reserved pins" To: "7 total reserved pins" 10
- Added video mode non-linear gamma correction description 23
- Added structured light mode linear gamma description 23
- Added DDR DRAM devices to Table 6 29
- Changed GPIO4_INTF to INIT_DONE 30
- Changed GPIO4_INTF to INIT_DONE 33
- Changed GPIO4_INTF to INIT_DONE 36
- Changed GPIO4 to INIT_DONE 36

Changes from Original (January 2012) to Revision A **Page**

- 已更改 特性 项，从“支持的输入分辨率包括 608 × 684、854 × 480 (WVGA)、640 × 480 (VGA)、320 × 240 (QVGA)” 改为“支持的输入分辨率包括 608 × 684、864 × 480、854 × 480 (WVGA)、640 × 480 (VGA)、320 × 240 (QVGA)” 1
- Changed unit values from ms to µs in *I^2C Interface Timing Requirements* 13
- Changed Equation 1 33

5 Pin Configuration and Functions

ZVB Package
176-Pin NFBGA
Bottom View



Pin Functions

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NO.				
SIGNALS					
$\overline{\text{RESET}}$	J14	VCC18	I_1	Async	DLPC300 power-on reset. Self configuration starts when a low-to-high transition is detected on this pin. All device power and clocks must be stable and within recommended operating conditions before this reset is deasserted. Note that the following 7 signals are high-impedance while $\overline{\text{RESET}}$ is asserted: DMD_PWR_EN, LEDDVR_ON, LED_SEL_0, LED_SEL_1, SPICLK, SPIDOUT, and $\overline{\text{SPICS0}}$ External pullups/pulldowns should be added as needed to these signals to avoid floating inputs where these signals are driven.
$\overline{\text{PARK}}$	B8	VCC_ INTF	I_3	Async	DMD park control (active-low). Is set high to enable normal operation. $\overline{\text{PARK}}$ must be set high within 500 µs after releasing $\overline{\text{RESET}}$. $\overline{\text{PARK}}$ must be set low a minimum of 500 µs before any power is to be removed from the DLPC300 or DLP3000. See *System Power-Up/Power-Down Sequence* for more details.
PLL_REFCLK_I	K15	VCC18 (filter)	I_4	N/A	Reference clock crystal input. If an external oscillator is used in place of a crystal, then this pin should be used as the oscillator input.
PLL_REFCLK_O	J15	VCC18 (filter)	O_{14}	N/A	Reference clock crystal return. If an external oscillator is used in place of a crystal, then this pin should be left unconnected (floating).
FLASH INTERFACE(1)					
SPICLK	A4	VCC_FLSH	O_{24}	N/A	SPI master clock output
SPIDIN	B4	VCC_FLSH	I_2	SPICLK	Serial data input from the external SPI slave FLASH device
$\overline{\text{SPICS0}}$	A5	VCC_FLSH	O_{24}	SPICLK	SPI master chip select 0 output. Active-low
RESERVED	C6	VCC_FLSH	O_{24}	SPICLK	Not used. Reserved for future use. Should be left unconnected
SPIDOUT	C5	VCC_FLSH	O_{24}	SPICLK	Serial data output to the external SPI slave flash device. This pin sends address and control information as well as data when programming.

(1) Each device connected to the SPI bus must operate from VCC_FLSH.

Pin Functions (continued)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION	
NAME	NO.					
CONTROL						
SCL	A10	VCC_ INTF	B_{38}	N/A	I^2C clock. Bidirectional, open-drain signal. An external pullup is required. No I^2C activity is permitted for a minimum of 100 ms after PARK and RESET are set high.	
SDA	C10	VCC_ INTF	B_{38}	SCL	I^2C data. Bidirectional, open-drain signal. An external pullup is required.	
INIT_DONE	C9	VCC_ INTF	B_{34}	Async	Primary usage is to indicate when auto-initialization is complete, which is when INIT_DONE transitions high then low following release of RESET. INIT_DONE also helps flag a detected error condition in the form of a logic-high, pulsed interrupt flag.	
PARALLEL RGB INTERFACE					**PARALLEL RGB MODE**	**BT.656 I/F MODE**
PCLK	D13	VCC_ INTF	I_3	N/A	Pixel clock(2)	Pixel clock(2)
PDM	H15	VCC_ INTF	B34	ASYNC	Not used, pulldown through an external resistor.	Not used, pulldown through an external resistor.
VSYNC	H14	VCC_ INTF	I_3	ASYNC	VSync(3)	Unused(4)
HSYNC	H13	VCC_ INTF	I_3	PCLK	HSync(3)	Unused(4)
DATEN	G15	VCC_ INTF	I_3	PCLK	Data valid(2)	Unused(4)
PDATA[0]	G14	VCC_ INTF	I_3	PCLK	Data0(5)	Data0(5)
PDATA[1]	G13	VCC_ INTF	I_3	PCLK	Data1(5)	Data1(5)
PDATA[2]	F15	VCC_ INTF	I_3	PCLK	Data2(5)	Data2(5)
PDATA[3]	F14	VCC_ INTF	I_3	PCLK	Data3(5)	Data3(5)
PDATA[4]	F13	VCC_ INTF	I_3	PCLK	Data4(5)	Data4(5)
PDATA[5]	E15	VCC_ INTF	I_3	PCLK	Data5(5)	Data5(5)
PDATA[6]	E14	VCC_ INTF	I_3	PCLK	Data6(5)	Data6(5)
PDATA[7]	E13	VCC_ INTF	I_3	PCLK	Data7(5)	Data7(5)
PDATA[8]	D15	VCC_ INTF	I_3	PCLK	Data8(5)	Unused(4)
PDATA[9]	D14	VCC_ INTF	I_3	PCLK	Data9(5)	Unused(4)
PDATA[10]	C15	VCC_ INTF	I_3	PCLK	Data10(5)	Unused(4)
PDATA[11]	C14	VCC_ INTF	I_3	PCLK	Data11(5)	Unused(4)
PDATA[12]	C13	VCC_ INTF	I_3	PCLK	Data12(5)	Unused(4)
PDATA[13]	B15	VCC_ INTF	I_3	PCLK	Data13(5)	Unused(4)
PDATA[14]	B14	VCC_ INTF	I_3	PCLK	Data14(5)	Unused(4)
PDATA[15]	A15	VCC_ INTF	I_3	PCLK	Data15(5)	Unused(4)
PDATA[16]	A14	VCC_ INTF	I_3	PCLK	Data16(5)	Unused(4)
PDATA[17]	B13	VCC_ INTF	I_3	PCLK	Data17(5)	Unused(4)
PDATA[18]	A13	VCC_ INTF	I_3	PCLK	Data18(5)	Unused(4)
PDATA[19]	C12	VCC_ INTF	I_3	PCLK	Data19(5)	Unused(4)
PDATA[20]	B12	VCC_ INTF	I_3	PCLK	Data20(5)	Unused(4)
PDATA[21]	A12	VCC_ INTF	I_3	PCLK	Data21(5)	Unused(4)
PDATA[22]	C11	VCC_ INTF	I_3	PCLK	Data22(5)	Unused(4)
PDATA[23]	B11	VCC_ INTF	I_3	PCLK	Data23(5)	Unused(4)

(2) Pixel clock capture edge is software programmable.
(3) VSYNC, HSYNC and data valid polarity is software programmable.
(4) Unused inputs should be pulled down to ground through an external resistor.
(5) PDATA[23:0] bus mapping is pixel-format and source-mode dependent. See later sections for details.

Pin Functions (continued)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NO.				
DMD INTERFACE					
DMD_D0	M15	VCC18	O_{58}	DMD_DCLK	DMD data pins. DMD data pins are double data rate (DDR) signals that are clocked on both edges of DMD_DCLK. All 15 DMD data signals are use to interface to the DLP3000.
DMD_D1	N14				
DMD_D2	M14				
DMD_D3	N15				
DMD_D4	P13				
DMD_D5	P14				
DMD_D6	P15				
DMD_D7	R15				
DMD_D8	R12				
DMD_D9	N11				
DMD_D10	P11				
DMD_D11	R11				
DMD_D12	N10				
DMD_D13	P10				
DMD_D14	R10				
DMD_DCLK	N13	VCC18	O_{58}	N/A	DMD data clock (DDR)
$\overline{\text{DMD\_LOADB}}$	R13	VCC18	O_{58}	DMD_DCLK	DMD data load signal (active-low). This signal requires an external pullup to VCC18.
DMD_SCTRL	R14	VCC18	O_{58}	DMD_DCLK	DMD data serial control signal
DMD_TRC	P12	VCC18	O_{58}	DMD_DCLK	DMD data toggle rate control
DMD_DRC_BUS	L13	VCC18	O_{58}	DMD_SAC_CLK	DMD reset control bus data
DMD_DRC_STRB	K13	VCC18	O_{58}	DMD_SAC_CLK	DMD reset control bus strobe
$\overline{\text{DMD\_DRC\_OE}}$	M13	VCC18	O_{58}	Async	DMD reset control enable (active-low). This signal requires an external pullup to VCC18.
DMD_SAC_BUS	L15	VCC18	O_{58}	DMD_SAC_CLK	DMD stepped-address control bus data
DMD_SAC_CLK	L14	VCC18	O_{58}	N/A	DMD stepped-address control bus clock
DMD_PWR_EN	K14	VCC18	O_{14}	Async	DMD power regulator enable (active-high). This is an active-high output that should be used to control DMD V_{OFFSET}, V_{BIAS}, and V_{RESET} voltages. DMD_PWR_EN is driven high as a result of the $\overline{\text{PARK}}$ input signal being set high. However, DMD_PWR_EN is held high for 500 µs after the $\overline{\text{PARK}}$ input signal is set low before it is driven low. A weak external pulldown resistor is recommended to keep this signal at a known state during power-up reset.

Pin Functions (continued)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NO.				
SDRAM INTERFACE					
MEM_CLK_P	D1	VCC18	O_{74}	N/A	mDDR memory, differential memory clock
MEM_CLK_N	E1	VCC18	O_{74}	N/A	
MEM_A0	P1	VCC18	O_{64}	MEM_CLK	mDDR memory, multiplexed row and column address
MEM_A1	R3				
MEM_A2	R1				
MEM_A3	R2				
MEM_A4	A1				
MEM_A5	B1				
MEM_A6	A2				
MEM_A7	B2				
MEM_A8	D2				
MEM_A9	A3				
MEM_A10	P2				
MEM_A11	B3				
MEM_A12	D3				
MEM_BA0	M3	VCC18	O_{64}	MEM_CLK	mDDR memory, bank select
MEM_BA1	P3				
$\overline{\text{MEM\_RAS}}$	P4	VCC18	O_{64}	MEM_CLK	mDDR memory, row address strobe (active-low)
$\overline{\text{MEM\_CAS}}$	R4	VCC18	O_{64}	MEM_CLK	mDDR memory, column address strobe (active-low)
$\overline{\text{MEM\_WE}}$	R5	VCC18	O_{64}	MEM_CLK	mDDR memory, write enable (active-low)
$\overline{\text{MEM\_CS}}$	J3	VCC18	O_{64}	MEM_CLK	mDDR memory, chip select (active-low)
MEM_CKE	C1	VCC18	O_{64}	MEM_CLK	mDDR memory, clock enable (active-high)
MEM_LDQS	J2	VCC18	B_{64}	N/A	mDDR memory, lower byte, R/W data strobe
MEM_LDM	J1	VCC18	O_{64}	MEM_LDQS	mDDR memory, lower byte, write data mask
MEM_UDQS	G1	VCC18	B_{64}	N/A	mDDR memory, upper byte, R/W data strobe
MEM_UDM	H1	VCC18	O_{64}	MEM_UDQS	mDDR memory, upper byte, write data mask
MEM_DQ0	N1	VCC18	B_{64}	MEM_LDQS	mDDR memory, lower byte, bidirectional R/W data
MEM_DQ1	M2				
MEM_DQ2	M1				
MEM_DQ3	L3				
MEM_DQ4	L2				
MEM_DQ5	K2				
MEM_DQ6	L1				
MEM_DQ7	K1				
MEM_DQ8	H2	VCC18	B_{64}	MEM_UDQS	mDDR memory, upper byte, bidirectional R/W data
MEM_DQ9	G2				
MEM_DQ10	H3				
MEM_DQ11	F3				
MEM_DQ12	F1				
MEM_DQ13	E2				
MEM_DQ14	F2				
MEM_DQ15	E3				

Pin Functions (continued)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NO.				
LED DRIVER INTERFACE					
RPWM	N8	VCC18	O_{14}	Async	Red LED PWM signal used to control the LED current(6).
GPWM	P9	VCC18	O_{14}	Async	Green LED PWM signal used to control the LED current(6).
BPWM	R8	VCC18	O_{14}	Async	Blue LED PWM signal used to control the LED current(6).
LED_SEL_0	R6	VCC18	O_{14}	Async	LED enable SELECT. Controlled by DMD sequence timing. LED_SEL(1:0) Selected LED 00 None 01 Red 10 Green 11 Blue A decode circuit is required to decode the selected LED enable.
LED_SEL_1	N6				
LEDDRV_ON	P7	VCC18	O_{14}	Async	LED driver master enable. Active-high output control to external LED driver logic. This signal is driven high 100 ms after LED_ENABLE is driven high. Driven low immediately when either LED_ENABLE or $\overline{\text{PARK}}$ is driven low.
LED_ENABLE	A11	VCC_ INTF	I_3	Async	LED enable (active-high input). A logic low on this signal forces LEDDRV_ON low and LED_SEL(1:0) = 00b. These signals are enabled 100 ms after LED_ENABLE transitions from low to high.
RED_EN	B5	VCC18	B_{18}	Async	When not used with an optional FPGA, this signal should be connected to the RED LED enable circuit. When RED_EN is high, the red LED is enabled. When RED_EN is low, the red LED is disabled. When used with the optional FPGA, this signal should be pulled down to ground through an external resistor. This signal is configured as output and driven low when the DLPR300 serial flash PROM is loaded by the DLPC300, but the signal is not enabled. To enable this output, a write to I^2C LED Enable and Buffer Control register.
GREEN_EN	A7				When not used with an optional FPGA, this signal should be connected to the green LED enable circuit. When GREEN_EN is high, the green LED is enabled. When GREEN_EN is low, the green LED is disabled. When used with the optional FPGA, this signal should be pulled down to ground through an external resistor. This signal is configured as output and driven low when the DLPR300 serial flash PROM is loaded by the DLPC300, but the signal is not enabled. To enable this output, a write to I^2C LED Enable and Buffer Control register.
BLUE_EN	C8				When not used with an optional FPGA, this signal should be connected to the blue LED enable circuit. When BLUE_EN is high, the blue LED is enabled. When BLUE_EN is low, the blue LED is disabled. When used with the optional FPGA, this signal should be pulled down to ground through an external resistor. This signal is configured as output and driven low when the DLPR300 serial flash PROM is loaded by the DLPC300, but the signal is not enabled. To enable this output, a write to I^2C LED Enable and Buffer Control register.

(6) All LED PWM signals are forced high when LEDDRV_ON = 0, SW LED control is disabled, or the sequence stops.

Pin Functions (continued)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NO.				
WHITE POINT CORRECTION LIGHT SENSOR I/F					
CMP_OUT	A6	VCC18	I_1	Async	Successive approximation ADC comparator output (DLPC300 input). Assumes a successive approximation ADC is implemented with a light sensor and/or thermocouple feeding one input of an external comparator and the other side of the comparator driven from the DLPC300 CMP_PWM pin. If not used, this signal should be pulled down to ground.
CMP_PWM	B7	VCC18	O_{14}	Async	Successive approximation comparator pulse-duration modulation input. Supplies a PWM signal to drive the successive approximation ADC comparator used in light-to-voltage light sensor applications. Should be left unconnected if this function is not used.
CMP_PWR	P5	VCC18	B_{14}	Async	Power control signal for the WPC light sensor and other analog support circuits using the DLPC300 ADC. Alternatively, it provides general-purpose I/O to the WPC microprocessor internal to the DLPC300. Should be left unconnected if not used.
TRIGGER CONTROL					
OUTPUT_TRIGGER	N9	VCC18	B_{18}	Async	Trigger output. Indicates that a pattern or image is displayed on the screen and is ready to be captured. With an optional FPGA, this signal is connected to the FPGA trigger input. This signal is configured as output and driven low when the DLPR300 serial flash PROM is loaded by the DLPC300, but the signal is not enabled. To enable this output, a write to I^2C LED Enable and Buffer Control register. If not used, this signal should be pulled down to ground through an external resistor.
PATTERN CONTROL					
PATTERN_INVERT	C7	VCC18	B_{18}	Async	Inverts the current 1-bit pattern held in the DLPC300 buffer. When used with an optional FPGA, this signal should be connected to DMC_TRC of the FPGA. This signal is configured as output and driven low when the DLPR300 serial flash PROM is loaded by the DLPC300, but the signal is not enabled. To enable this output, a write to I^2C LED Enable and Buffer Control register. If not used, this signal should be pulled down to ground through an external resistor.
OPTIONAL FPGA BUFFER MANAGEMENT INTERFACES					
RD_BUF0	B6	VCC18	B_{18}	Async	When not used with an optional FPGA, this signal should be pulled down to ground through an external resistor. When used with an optional FPGA, this signal should be connected to RD_PTR_SDC[0] of the FPGA. RD_BUFF1 and RD_BUFF0 indicate to the FPGA one of the four buffers currently in use. This signal is configured as output and driven low when the DLPR300 serial flash PROM is loaded by the DLPC300, but the signal is not enabled. To enable this output, a write to I^2C LED Enable and Buffer Control register.
RD_BUF1/I2C_ADDR_SEL	R9				This signal is sampled when $\overline{\text{RESET}}$ is deasserted to choose between two predefined 7-bit I^2C slave addresses. If I2C_ADDR_SEL signal is pulled-low, then the DLPC300's I^2C slave address is 1Bh. If I2C_ADDR_SEL signal is pulled-high, then the DLPC300's I^2C slave address is 1Dh. When used with an optional FPGA, this signal should be connected to RD_PTR_SDC[1] of the FPGA. RD_BUFF1 and RD_BUFF0 indicate to the FPGA one of the four buffers currently in use. This signal is set to input upon deassertion of $\overline{\text{RESET}}$ and configured as output and driven low when the DLPR300 serial flash PROM is loaded by the DLPC300, but the signal is not enabled. To enable this output, a write to I^2C LED Enable and Buffer Control register.
BUFFER_SWAP	A8				When not used with an optional FPGA, this signal should be pulled down to ground through an external resistor. When used with an optional FPGA, this signal should be connected to BUFF_SWAP_SEQ of the FPGA. BUFFER_SWAP indicates to the FPGA when to advance the buffer. This signal is configured as output and driven low when the DLPR300 serial flash PROM is loaded by the DLPC300, but the signal is not enabled. To enable this output, a write to I^2C LED Enable and Buffer Control register.
CONTROLLER MANUFACTURER TEST SUPPORT					

Pin Functions (continued)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NO.				
TEST_EN	A9	VCC_INTF	I_3	N/A	Reserved for test. Should be connected directly to ground on the PCB for normal operation. Includes weak internal pulldown
BOARD LEVEL TEST AND DEBUG					
JTAGTDI	P6	VCC18	I_1	JTAGTCK	JTAG, serial data in. Includes weak internal pullup
JTAGTCK	N5	VCC18	I_1	N/A	JTAG, serial data clock. Includes weak internal pullup
JTAGTMS	N7	VCC18	I_1	JTAGTCK	JTAG, test mode select. Includes weak internal pullup
JTAGTDO	R7	VCC18	I_{14}	JTAGTCK	JTAG, serial data out
$\overline{\text{JTAGRST}}$	P8	VCC18	I_1	ASYNC	JTAG, RESET (active-low). Includes weak internal pullup. This signal must be tied to ground, through an external 15-kΩ or less resistor for normal operation.

Pin Functions — Power and Ground (1)

POWER GROUP	PIN NUMBERS	DESCRIPTION
VDD10	D5, D9, F4, F12, J4, J12, M6, M8, M11	1-V core logic power supply (9)
VDD_PLL	H12	1-V power supply for the internal PLL (1)
VCC18	C4, D8, E4, G3, K3, K12, L4, M5, M9, M12, N4, N12	1.8-V power supply for all I/O other than the host/ video interface and the SPI flash buses (12)
VCC_FLSH	D6	1.8- , 2.5- or 3.3-V power supply for SPI flash bus I/O (1)
VCC_INTF	D11, E12	1.8- , 2.5- or 3.3-V power supply for all I/Os on the host/video interface (includes I^2C, PDATA, video syncs, $\overline{\text{PARK}}$ and LED_ENABLE pins) (2)
GND	D4, D7, D10, D12, G4, G12, H4, K4, L12, M4, M7, M10	Common ground (12)
RTN_PLL	J13	Analog ground return for the PLL (This should be connected to the common ground GND through a ferrite (1)
Reserved	B9, C2, C3, C6, N2, N3	
Reserved	B10	This pin must be pulled up to VCC_INTF

(1) 132 total signal I/O pins, 38 total power/ground pins, 7 total reserved pins

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted).(1)

		MIN	MAX	UNIT
ELECTRICAL				
Voltage applied to(2)	VDD10	–0.5	1.32	V
	VDD_PLL	–0.5	1.32	V
	VCC18	–0.5	2.75	V
	VCC_FLSH	–0.5	3.60	V
	VCC_INTF	–0.5	3.60	V
	All other input terminals, V_O	–0.5	3.60	V
ENVIRONMENTAL				
T_J	Junction temperature	–30	105	ºC
T_{stg}	Storage temperature	–40	125	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to VSS (ground).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the recommended operating conditions limits.

			MIN	NOM	MAX	UNIT
ELECTRICAL						
VDD10	Core logic supply voltage		0.95	1	1.05	V
VDD_PLL	Analog PLL supply voltage		0.95	1	1.05	V
VCC18	I/O supply voltage (except flash and 24-bit RGB interface signals)		1.71	1.8	1.89	V
VCC_FLSH	Configuration and control I/O supply voltage	1.8-V LVCMOS	1.71	1.8	1.89	V
		2.5-V LVCMOS	2.375	2.5	2.625	
		3.3-V LVCMOS	3.135	3.3	3.465	
VCC_INTF	24-bit RGB interface supply voltage	1.8-V LVCMOS	1.71	1.8	1.89	V
		2.5-V LVCMOS	2.375	2.5	2.625	
		3.3-V LVCMOS	3.135	3.3	3.465	
V_I	Input voltage, all other pins		–0.3		VCCIO(1) + 0.3	V
V_O	Output voltage, all other pins		0		VCCIO(1)	V
ENVIRONMENTAL						
T_J	Operating junction temperature		–20		85	ºC

(1) VCCIO represents the actual supply voltage applied to the corresponding I/O.

6.4 Thermal Information

THERMAL METRIC(1)		DLPC300 ZVB (NFBGA) 176 PINS	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance	19.52	°C/W
$R_{\theta JA}$	Junction-to-air thermal resistance (with no forced airflow)	64.96	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 I/O Electrical Characteristics

Voltage and current characteristics for each I/O type signal listed in *Pin Configuration and Functions*. All inputs and outputs are LVCMOS.

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{IH}	High-level input voltage	B_{64} inputs	VCC = 1.8 V		1.19	VCC + 0.3	V
		I_1, I_2, I_3, I_4, B_{14}, B_{18}, B_{34}, B_{38} inputs			1.2	VCC + 0.3	
		I_2, I_3, B_{34}, B_{38} inputs	VCC = 2.5 V		1.7	VCC + 0.3	
		I_2, I_3, B_{34}, B_{38} inputs	VCC = 3.3 V		2	VCC + 0.3	
V_{IL}	Low-level input voltage	I_1, I_2, I_3, I_4, B_{14}, B_{18}, B_{34}, B_{38} inputs	VCC = 1.8 V		–0.3	0.5	V
		B_{64} inputs			–0.3	0.57	
		I_2, I_3, B_{34}, B_{38} inputs	VCC = 2.5 V		–0.3	0.7	
		I_2, I_3, B_{34}, B_{38} inputs	VCC = 3.3 V		–0.3	0.8	
V_{OH}	High-level output voltage	O_{14}, O_{24}, B_{14}, B_{34} outputs	VCC = 1.8 V	I_{OH} = –2.58 mA	1.25		V
		O_{58} outputs		I_{OH} = = –6.41 mA	1.25		
		B_{18}, B_{38} outputs		I_{OH} = = –5.15 mA	1.25		
		O_{64}, O_{74}, B_{64} outputs		I_{OH} = = –4 mA	1.53		
		O_{24}, B_{34} outputs	VCC = 2.5 V	I_{OH} = = –6.2 mA	1.7		
		B_{38} outputs		I_{OH} = –12.4 mA	1.7		
		B_{38} outputs		I_{OH} = –10.57 mA	2.4		
		B_{38} outputs	VCC = 3.3 V	I_{OH} = –10.57 mA	1.25		
		O_{24}, B_{34} outputs		I_{OH} = –-5.29 mA	2.4		
V_{OL}	Low-level output voltage	O_{64}, O_{74}, B_{64} outputs	VCC = 1.8 V	I_{OL} = 4 mA		0.19	V
		O_{14}, O_{24}, B_{14}, B_{34} outputs		I_{OL} = 2.89 mA		0.4	
		B_{18}, B_{38} outputs		I_{OL} = 5.72 mA		0.4	
		O_{58} outputs		I_{OL} = 5.78 mA		0.4	
		O_{24}, B_{34} outputs	VCC = 2.5 V	I_{OL} = 6.3 mA		0.7	
		B_{38} outputs		I_{OL} = 12.7 mA		0.7	
		O_{24}, B_{34} outputs	VCC = 3.3 V	I_{OL} = 9.38 mA		0.4	
		B_{38} outputs		I_{OL} = 18.68 mA		0.4	

6.6 Crystal Port Electrical Characteristics

PARAMETER	NOM	UNIT
PLL_REFCLK_I TO GND capacitance	4.5	pF
PLL_REFCLK_O TO GND capacitance	4.5	pF

6.7 Power Consumption

assumes the transfer of a 12 × 6 checkerboard image in 864 × 480 land scape mode at periodic 30 frames per second over the parallel RGB interface at 25ºC(1)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
VCC_INTF	1.8 V		0.1		mW
VCC_FLSH	2.5 V		0		
VCC18	1.8 V		50.8		
VDD_PLL	1 V		2.8		
VDD10	1 V		39		

(1) This table lists the typical current and power consumption of the individual supplies. Note that VCC_FLSH power is 0 because the serial flash is only accessed upon device configuration and not during normal operation.

6.8 I^2C Interface Timing Requirements

			MIN	MAX	UNIT
f_{scl}	I^2C clock frequency		0	400	kHz
t_{sch}	I^2C clock high time		1		µs
t_{scl}	I^2C clock low time		1		µs
t_{sp}	I^2C spike time			20	ns
t_{sds}	I^2C serial-data setup time		100		ns
t_{sdh}	I^2C serial-data hold time		100		ns
t_{icr}	I^2C input rise time		100		ns
t_{ocf}	I^2C output fall time	50 pF	30	200	ns
t_{buf}	I^2C bus free time between stop and start conditions		1.3		µs
t_{sts}	I^2C start or repeat start condition setup		1		µs
t_{sth}	I^2C start or repeat start condition hold		1		µs
t_{sph}	I^2C stop condition setup		1		µs
t_{vd}	Valid-data time	SCL low to SDA output valid		1	µs
	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low		1	µs
t_{sch}	I^2C bus capacitive load		0	100	pF

6.9 Parallel Interface Frame Timing Requirements

			MIN	MAX	UNIT
t_{p_vsw}	Pulse duration – VSYNC high	50% reference points	1		lines
t_{p_vbp}	Vertical back porch – Time from the leading edge of VSYNC to the leading edge HSYNC for the first active line(1)	50% reference points	2		lines
t_{p_vfp}	Vertical front porch – Time from the leading edge of the HSYNC following the last active line in a frame to the leading edge of VSYNC(1)	50% reference points	1		lines
t_{p_tvb}	Total vertical blanking – Time from the leading edge of HSYNC following the last active line of one frame to the leading edge of HSYNC for the first active line in the next frame. (This is equal to the sum of vertical back porch (t_{p_vbp}) + vertical front porch (t_{p_vfp}).)	50% reference points	12		lines
t_{p_hsw}	Pulse duration – HSYNC high	50% reference points	4	128	PCLKs
t_{p_hbp}	Horizontal back porch – Time from rising edge of HSYNC to rising edge of DATAEN	50% reference points	4		PCLKs
t_{p_hfp}	Horizontal front porch – Time from falling edge of DATAEN to rising edge of HSYNC	50% reference points	8		PCLKs
t_{p_thh}	Total horizontal blanking – Sum of horizontal front and back porches	50% reference points		See(2)	PCLKs

(1) The programmable parameter *Vertical Sync Line Delay* (I^2C: 0x23) must be set such that: 6 – *Vertical Front Porch* (t_{p_vfp}) (min 0) ≤ *Vertical Sync Line Delay* ≤ *Vertical Back Porch* (t_{p_vbp}) – 2 (max 15). The default value for *Vertical Sync Line Delay* is set to 5; thus, only a *Vertical Back Porch* less than 7 requires potential action.
(2) Total horizontal blanking is driven by the maximum line rate for a given source, which is a function of resolution and orientation. See *Parallel I/F Maximum Supported Horizontal Line Rate* for the maximum line rate for each source/display combination. t_{p_thb} = Roundup[(1000 × f_{clock}) / LR] – APPL where f_{clock} = Pixel clock rate in MHz, LR = Line rate in kHz, and APPL is the number of active pixels per (horizontal) line. If t_{p_thb} is calculated to be less than t_{p_hbp} + t_{p_hfp}, then the pixel clock rate is too low or the line rate is too high and one or both must be adjusted.

6.10 Parallel Interface General Timing Requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1	33.5	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	29.85	1000	ns
t_{p_clkjit}	Clock jitter, PCLK	Maximum f_{clock}		See(1)	
t_{p_wh}	Pulse duration low, PCLK	50% reference points	10		ns
t_{p_wl}	Pulse duration high, PCLK	50% reference points	10		ns
t_{p_su}	Setup time – HSYNC, DATEN, PDATA(23:0) valid before the active edge of PCLK(2) (3)	50% reference points	3		ns
t_{p_h}	Hold time – HSYNC, DATEN, PDATA(23:0) valid after the active edge of PCLK(2) (3)	50% reference points	3		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	4	ns

(1) Clock jitter (in ns) should be calculated using this formula: Jitter = [1 / f_{clock} – 28.35 ns]. Setup and hold times must be met during clock jitter.
(2) The active (capture) edge of PCLK for HSYNC, DATEN, and PDATA(23:0) is software programmable, but defaults to the rising edge.
(3) See Figure 3.

6.11 Parallel I/F Maximum Supported Horizontal Line Rate

DMD	PARALLEL BUS SOURCE RESOLUTION	LANDSCAPE FORMAT(1)		PORTRAIT FORMAT(1)	
		RESOLUTION (H × V)	MAX LINE RATE (kHz)	RESOLUTION (H × V)	MAX LINE RATE (kHz)
0.3 WVGA diamond	NSTC(2)	720 × 240	17	Not supported	N/A
	PAL(2)	720 × 288	20	Not supported	N/A
	QVGA	320 × 240	17	240 × 320	22
	QWVGA	427 × 240	17	240 × 427(2)	27
	3:2 VGA	640 × 430	30	430 × 640	45
	4:3 VGA	640 × 480	34	480 × 640	45
	WVGA-720	720 × 480	34	480 × 720	51
	WVGA-752	752 × 480	34	480 × 752	53
	WVGA-800	800 × 480	34	480 × 800	56
	WVGA-852	852 × 480	34	480 × 852	56
	WVGA-853	853 × 480	34	480 × 853	56
	WVGA-854	854 × 480	34	480 × 854	56
	WVGA-864	864 × 480	34	480 × 864	56
	Optical test	608 × 684	48	Not supported	N/A

(1) See the *DLPC300 Software Programmer's Guide* (DLPU004) to invoke the appropriate input and output resolutions.
(2) NTSC and PAL are assumed to be interlaced sources.

6.12 BT.565 I/F General Timing Requirements

The DLPC300 controller input interface supports the industry standard BT.656 parallel video interface. See the appropriate ITU-R BT.656 specification for detailed interface timing requirements.(1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1	33.5	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	29.85	1000	ns
t_{p_clkjit}	Clock jitter, PCLK	Maximum f_{clock}		See(2)	
t_{p_wh}	Pulse duration low, PCLK	50% reference points	10		ns
t_{p_wl}	Pulse duration high, PCLK	50% reference points	10		ns
t_{p_su}	Setup time – HSYNC, DATEN, and PDATA(23:0) valid before the active edge of PCLK	50% reference points	3		ns
t_{p_h}	Hold time – HSYNC, DATEN, and PDATA(23:0) valid after the active edge of PCLK	50% reference points	3		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	4	ns

(1) The BT.656 I/F accepts 8-bit per color, 4:2:2 YCb/Cr data encoded per the industry standard by PDATA(7:0) on the active edge of PCLK (that is, programmable) as shown in Figure 3.
(2) Clock jitter (in ns) should be calculated using this formula: Jitter = [1 / f_{clock} – 28.35 ns]. Setup and hold times must be met during clock jitter.

6.13 Flash Interface Timing Requirements

see (1) (2)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, SPICLK(3)		33.3266	33.34	MHz
t_{p_clkper}	Clock period, SPICLK	50% reference points	29.994	30.006	ns
t_{p_wh}	Pulse duration low, SPICLK	50% reference points	10		ns
t_{p_wl}	Pulse duration high, SPICLK	50% reference points	10		ns
t_t	Transition time – All signals	20% to 80% reference points	0.2	4	ns
t_{p_su}	Setup time – SPIDIN valid before SPICLK falling edge	50% reference points	10		ns
t_{p_h}	Hold time – SPIDIN valid after SPICLK falling edge	50% reference points	0		ns
t_{p_clqv}	SPICLK clock low to output valid time – SPIDOUT and $\overline{\text{SPICS0}}$	50% reference points		1	ns
t_{p_clqx}	SPICLK clock low output hold time – SPI_DOUT and $\overline{\text{SPICS0}}$	50% reference points	–1		ns

(1) Standard SPI protocol is to transmit data on the falling edge of SPICLK and to capture data on the rising edge. The DLPC300 does transmit data on the falling edge, but it also captures data on the falling edge rather than the rising edge. This provides support for SPI devices with long clock-to-Q timing. DLPC300 hold capture timing has been set to facilitate reliable operation with standard external SPI protocol devices.
(2) With the above output timing, DLPC300 provides the external SPI device 14-ns input setup and 14-ns input hold relative to the rising edge of SPICLK.
(3) This range includes the 200 ppm of the external oscillator (but no jitter).

6.14 DMD Interface Timing Requirements

The DLPC300 controller DMD interface consists of a 76.19-MHz (nominal) DDR output-only interface with LVCMOS signaling.(1)

			FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock}	Clock frequency(2)		n/a	DMD_DCLK and DMD_SAC_CLK	76.198	76.206	MHz
t_{p_clkper}	Clock period	50% reference points	n/a	DMD_DCLK and DMD_SAC_CLK	13.123	15	ns
t_{p_wh}	Pulse duration low	50% reference points	n/a	DMD_DCLK and DMD_SAC_CLK	6.2		ns
t_{p_wl}	Pulse duration high	50% reference points	n/a	DMD_DCLK and DMD_SAC_CLK	6.2		ns
t_t	Transition time	20% to 80% reference points	n/a	all signals	0.3	2	ns
t_{p_su}	Output setup time (3) (4)	50% reference points	Both rising and falling edges of DMD_DCLK	DMD_D(14:0), $\overline{\text{DMD\_SCTRL}}$, $\overline{\text{DMD\_LOADB}}$ and DMD_TRC		1.5	ns
t_{p_h}	Output hold time(3) (4)	50% reference points	Both rising and falling edges of DMD_DCLK	DMD_D(14:0), $\overline{\text{DMD\_SCTRL}}$, $\overline{\text{DMD\_LOADB}}$, and DMD_TRC		1.5	ns
$t_{p\_d1\_skew}$	DMD data skew(5)	50% reference points	Relative to each other	DMD_D(14:0), $\overline{\text{DMD\_SCTRL}}$, $\overline{\text{DMD\_LOADB}}$, and DMD_TRC		0.2	ns
$t_{p\_clk\_skew}$	Clock skew	50% reference points	Relative to each other	DMD_DCLK and DMD_SAC_CLK		0.2	ns
$t_{p\_d2\_skew}$	DAD/SAC data skew	50% reference points	Relative to DMD_SAC_CLK	$\overline{\text{DMD\_SAC\_BUS}}$, $\overline{\text{DMD\_DRC\_OE}}$, DMD_DRC_BUS, and DMD_DRC_STRB		0.2	ns

(1) Assumes a 30-Ω series termination for all DMD interface signals
(2) This range includes the 200 ppm of the external oscillator (but no jitter).
(3) Assumes minimum DMD setup time = 1 ns and minimum DMD hold time = 1 ns
(4) Output setup/hold numbers already account for controller clock jitter. Only routing skew and DMD setup/hold need be considered in system timing analysis.
(5) Assumes DMD data routing skew = 0.1 ns max

6.15 Mobile Dual Data Rate (mDDR) Memory Interface Timing Requirements

see (1) (2) (3)

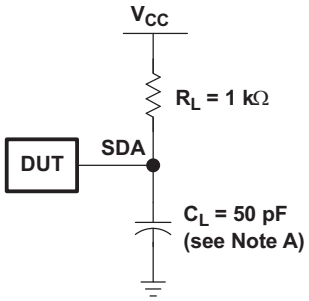
		MIN	MAX	UNIT
t_{CYCLE}	Cycle-time reference	7500		ps
t_{CH}	CK high pulse duration(4)	2700		ps
t_{CL}	CK low pulse duration(4)	2700		ps
t_{DQSH}	DQS high pulse duration(4)	2700		ps
t_{DQSL}	DQS low pulse duration(4)	2700		ps
t_{WAC}	CK to address and control outputs active	–2870	2870	ps
t_{QAC}	CK to DQS output active		200	ps
t_{DAC}	DQS to DQ and DM output active	–1225	1225	ps
t_{DQSRS}	Input (read) DQS and DQ skew(5)		1000	ps

(1) This includes the 200 ppm of the external oscillator (but no jitter).
(2) Output setup/hold numbers already account for controller clock jitter. Only routing skew and memory setup/hold must be considered in system timing analysis.
(3) Assumes a 30-Ω series termination on all signal lines
(4) CK and DQS pulse duration specifications for the DLPC300 assume it is interfacing to a 166-MHz mDDR device. Even though these memories are only operated at 133.33 MHz, according to memory vendors, the rated t_{CK} specification (that is, 6 ns) can be applied to determine minimum CK and DQS pulse duration requirements to the memory.
(5) Note that DQS must be within the t_{DQSRS} read data-skew window, but need not be centered.

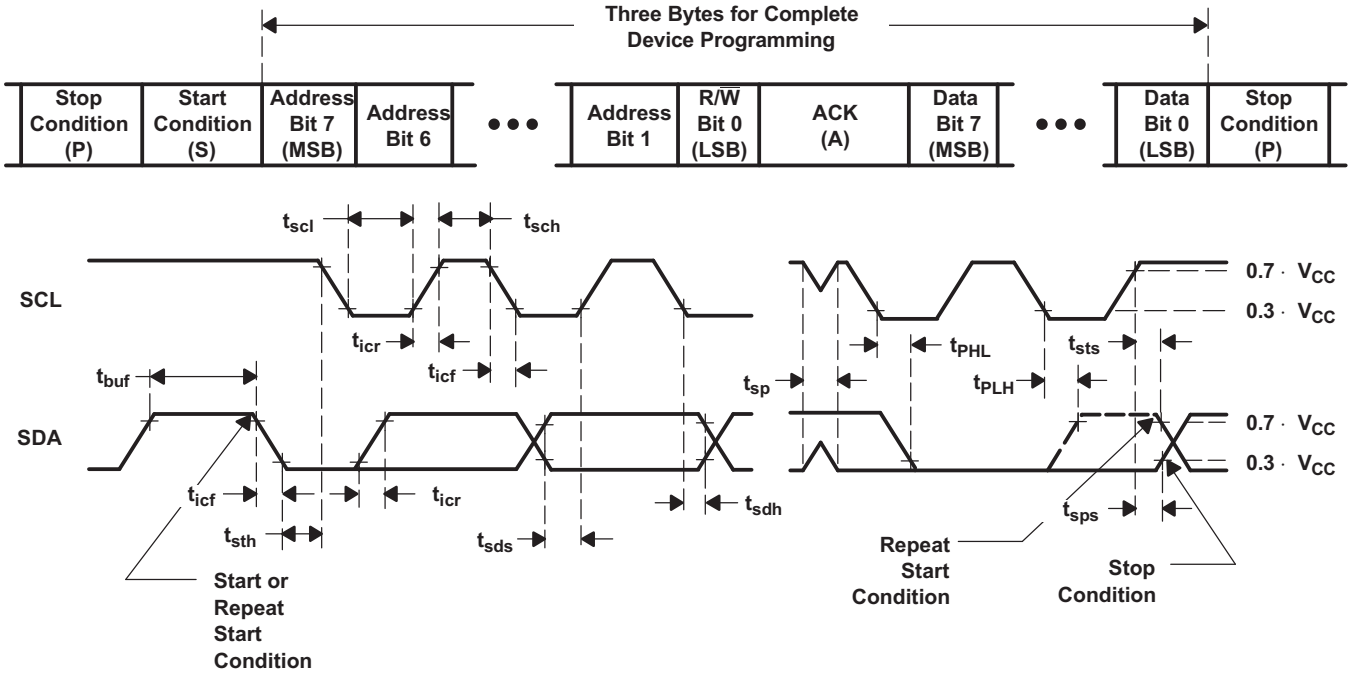
6.16 JTAG Interface: I/O Boundary Scan Application Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(clock)}$	Clock frequency, JTAGTCK			10	MHz
t_c	Cycle time, JTAGTCK		100		ns
$t_{w(L)}$	Pulse duration low, PCLK	50% reference points	40		ns
$t_{w(H)}$	Pulse duration high, PCLK	50% reference points	40		ns
t_{su}	Setup time – JTAGTDI, JTAGTMS; Valid before JTAGTCK↑↓	20% to 80% reference points	8		ns
t_h	Hold time – JTAGTDI, JTAGTMS; Valid after JTAGTCK↑↓		2		ns
t_t	Transition time			5	ns
t_{pd} (1)	Output propagation, Clock to Q	From (Input) JTAGTCK↓ to (Output) JTAGTDO	3	12	ns

(1) Switching characteristics over *Recommended Operating Conditions*, C_L (minimum timing) = 5 pF, C_L (maximum timing) = 85 pF (unless otherwise noted).



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

A. C_L includes probe and jig capacitance.

Figure 1. I^2C Interface Load Circuit and Voltage Waveforms

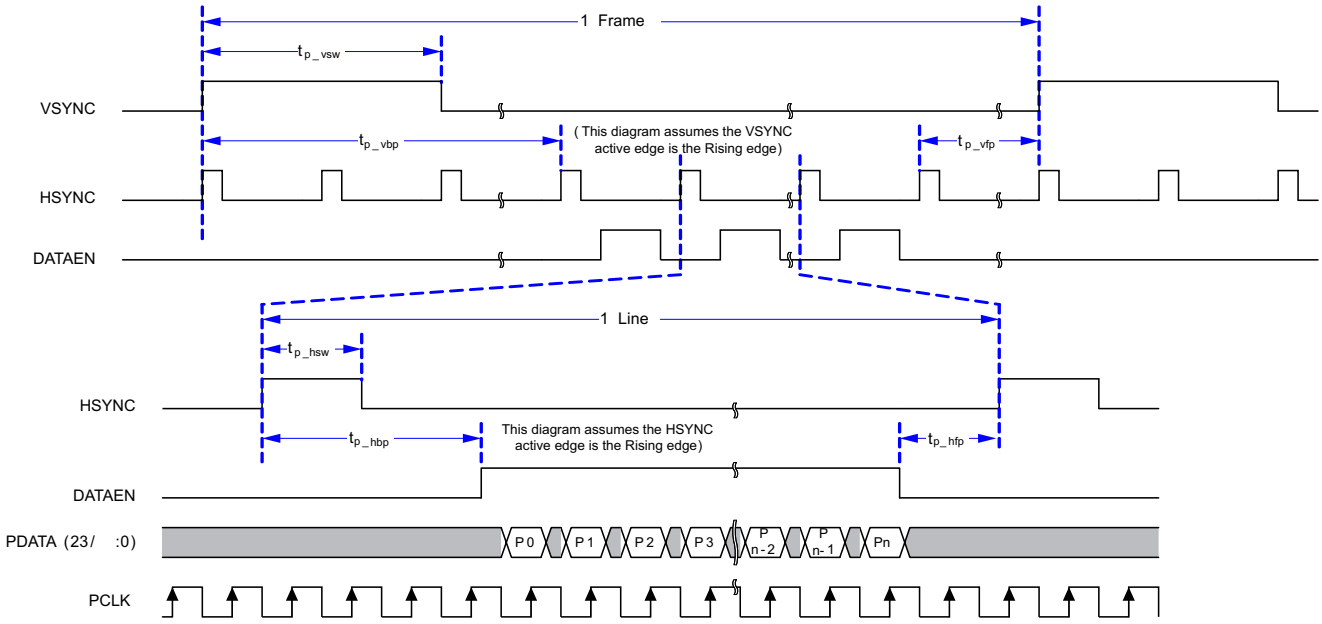


Figure 2. Parallel I/F Frame Timing

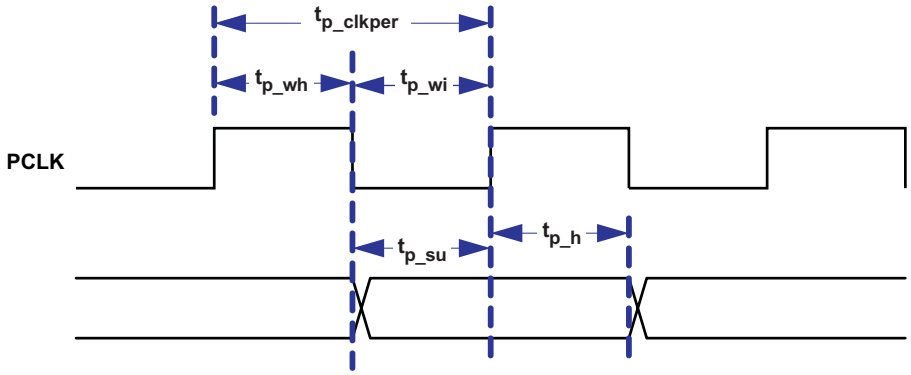


Figure 3. Parallel and BT.656 I/F General Timing

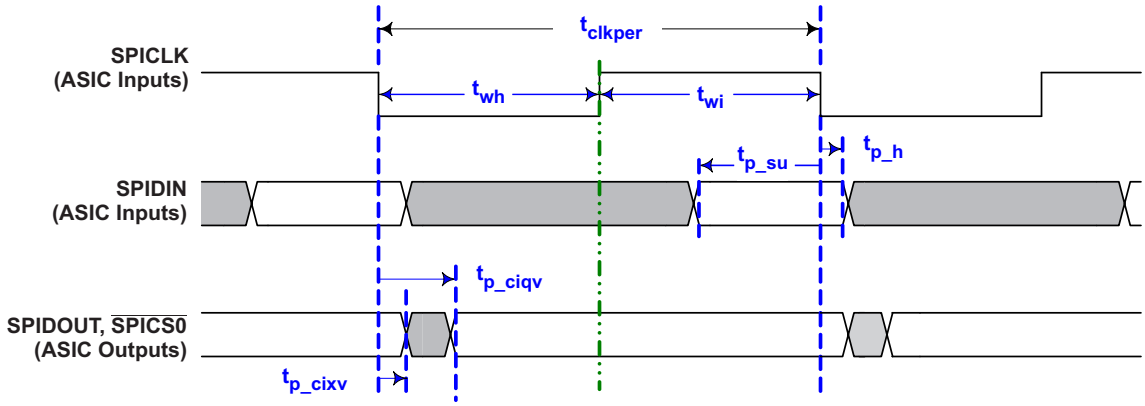


Figure 4. Flash Interface Timing

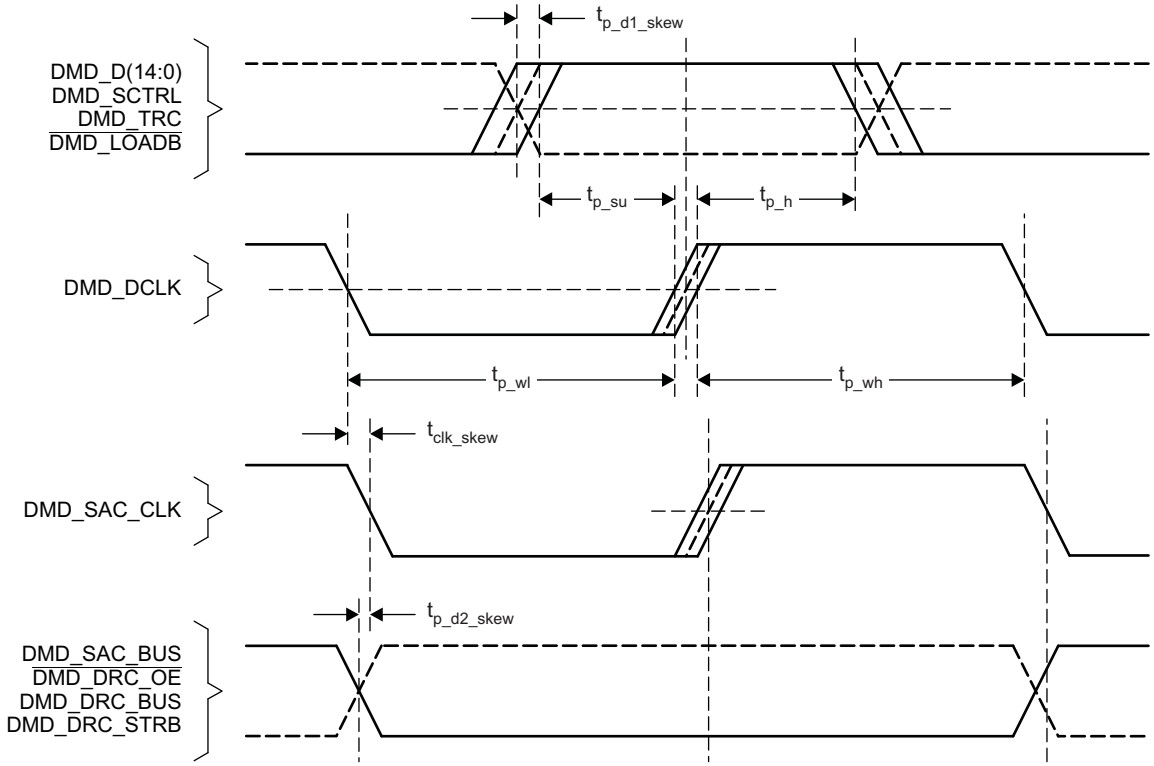


Figure 5. DMD Interface Timing

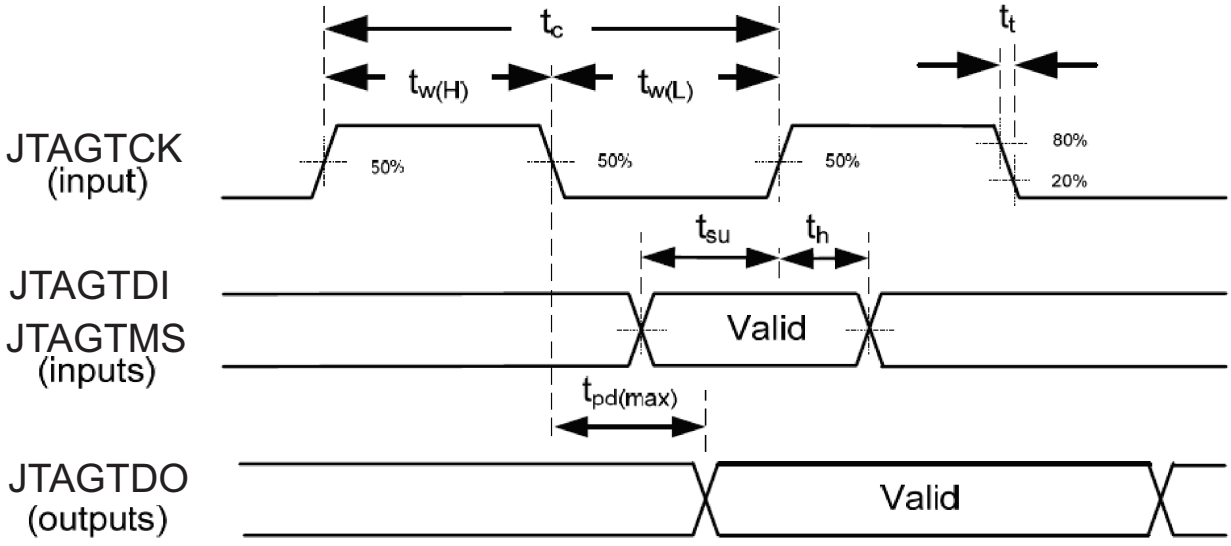
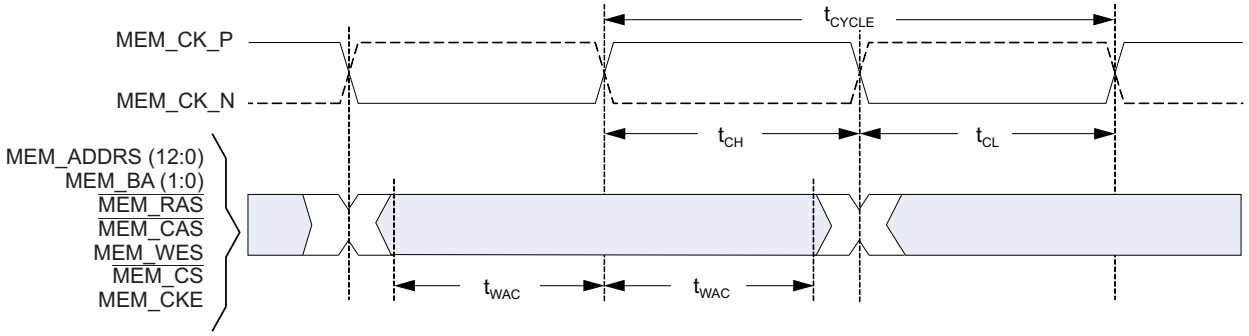
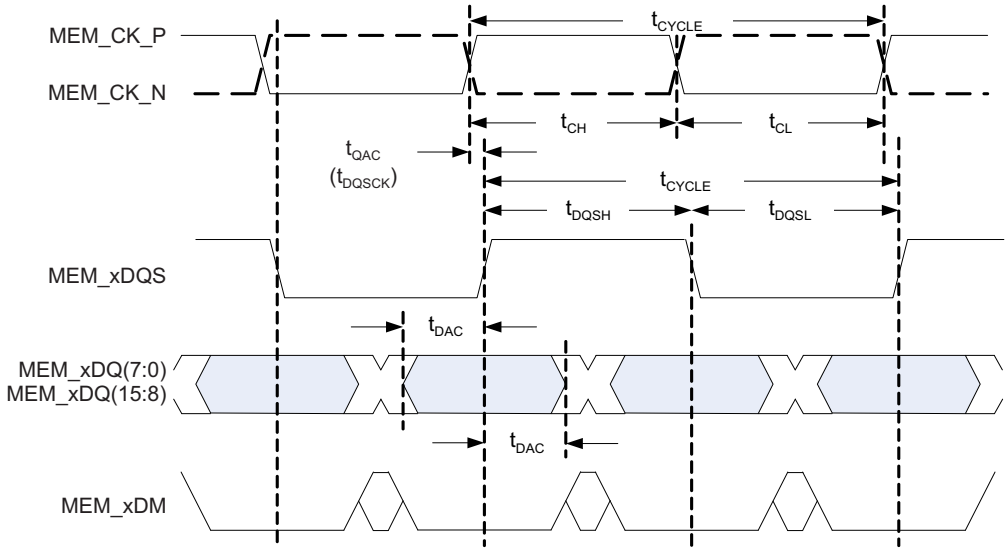


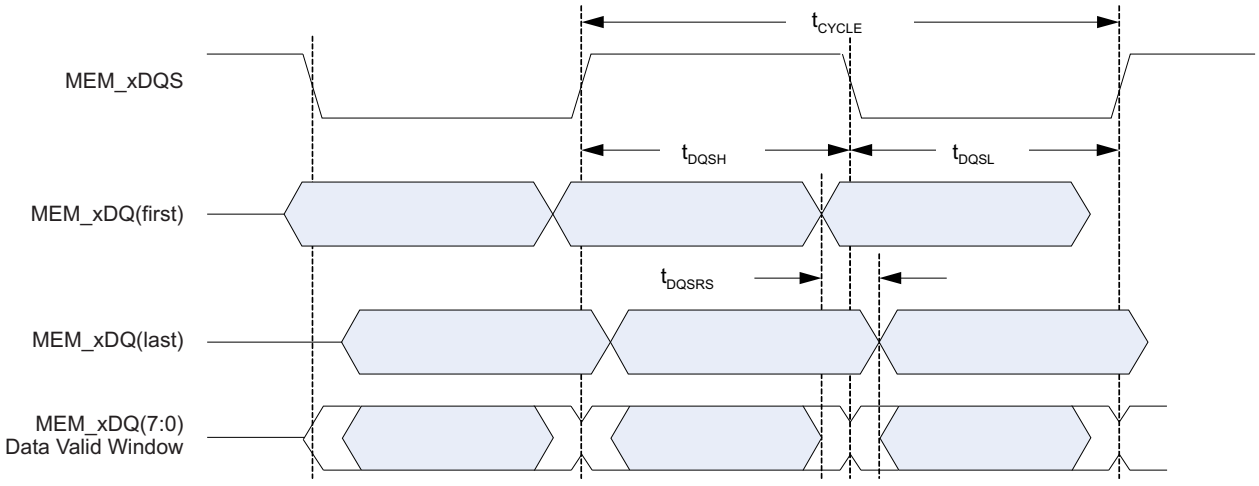
Figure 6. Boundary Scan Timing



mDDR Memory Address and Control Timing



mDDR Memory Write Data Timing



mDDR Memory Read Data Timing

Figure 7. mDDR Memory Interface Timing

7 Detailed Description

7.1 Overview

In DLP-based solutions, image data is 100% digital from the DLPC300 input port to the image on the DMD. The image stays in digital form and is never converted into an analog signal. The DLPC300 processes the digital input image and converts the data into a format needed by the DLP3000. The DLP3000 then steers light by using binary pulse-width-modulation (PWM) for each pixel mirror. Refer to the DLP3000 data sheet (DLPS022) for further details.

Figure 8 shows the DLPC300 functional block diagram. As part of the pixel processing functions, the DLPC300 offers format conversion functions: chroma interpolation for 4:2:2 and 4:4:4, color-space conversion, and gamma correction. The DLPC300 also offers several image-enhancement functions: programmable degamma, automatic gain control, and image resizing. Additionally, the DLPC300 offers an artifact migration function through spatial-temporal multiplexing (dithering). Finally, the DLPC300 offers the necessary functions to format the input data to the DMD. The pixel processing functions allow the DLPC300 and DLP3000 to support a wide variety of resolutions including NTSC, PAL, QVGA, QWVGA, VGA, and WVGA. The pixel processing functions can be optionally bypassed with the native 608 × 684 pixel resolution.

7.2 Functional Block Diagram

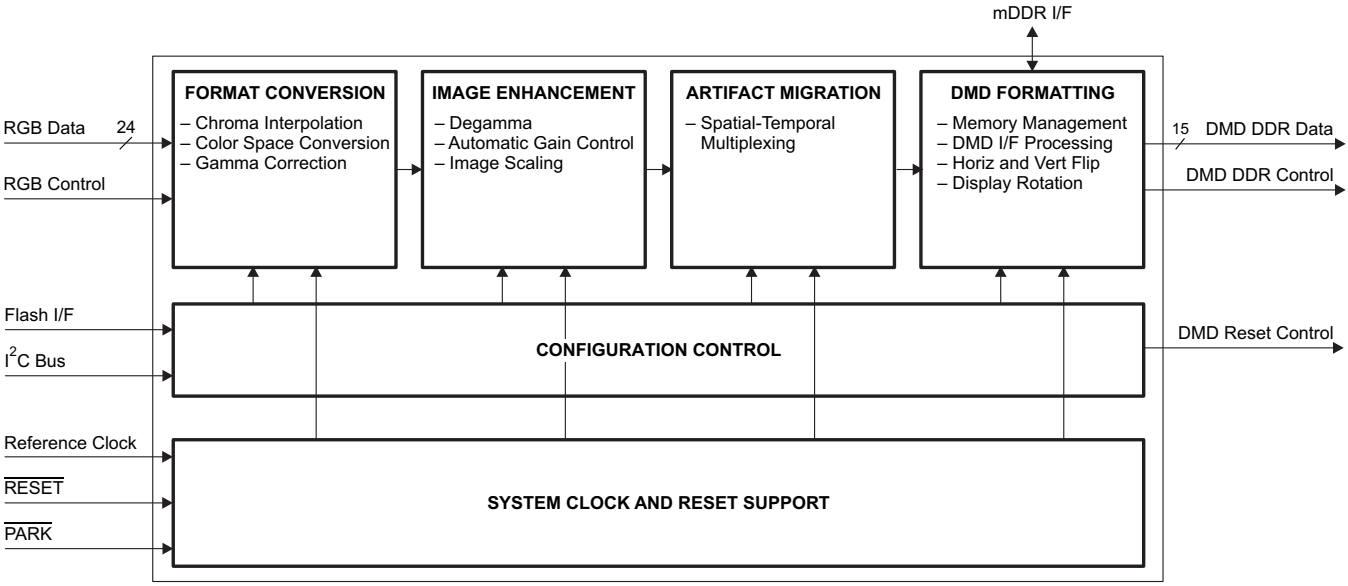


Figure 8. DLPC300 Functional Block Diagram

7.3 Feature Description

When accurate pattern display is needed, the native 608 × 684 input resolution pattern has a one-to-one association with the corresponding micromirror on the DLP3000. The DLPC300 enables high-speed display of these patterns: up to 1440 Hz for binary (1-bit) patterns and up to 120 Hz for 8-bit patterns. This functionality is well-suited for techniques such as structured light, rapid manufacturing, or digital exposure.

The DLPC300 takes as input 16-, 18-, or 24-bit RGB data at up to 60-Hz frame rate. This frame rate is composed of three colors (red, green, and blue) with each color equally divided in the 60-Hz frame rate. Thus, each color has a 5.55-ms time slot allocated. Because each color has 5-, 6-, or 8-bit depth, each color time slot is further divided into bit-planes. A bit-plane is the 2-D arrangement of one-bit extracted from all the pixels in the full color 2D image. See Figure 9.

Feature Description (continued)

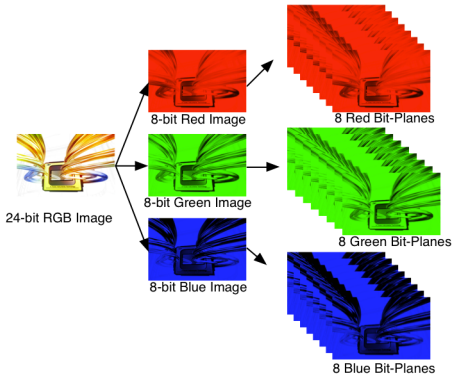


Figure 9. Bit Slices

The length of each bit-plane in the time slot is weighted by the corresponding power of 2 of its binary representation. This provides a binary pulse-width modulation of the image. For example, a 24-bit RGB input has three colors with 8-bit depth each. Each color time slot is divided into 8 bit-planes, with the sum of all bit planes in the time slot equal to 256. See Figure 10 for an illustration of this partition of the bits in a frame.

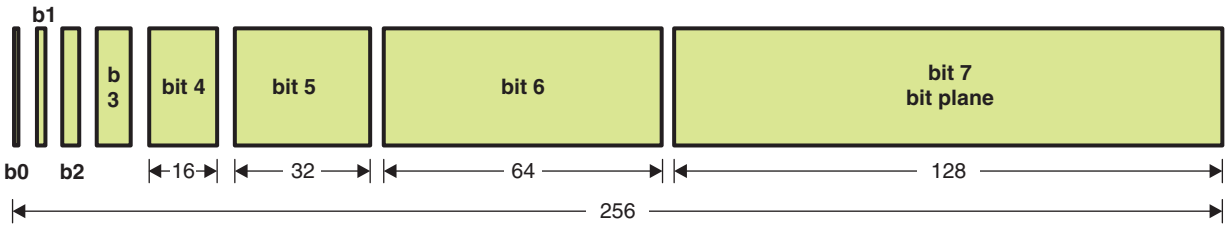


Figure 10. Bit Partition in a Frame for an 8-Bit Color

Therefore, a single video frame is composed of a series of bit-planes. Because the DMD mirrors can be either on or off, an image is created by turning on the mirrors corresponding to the bit set in a bit-plane. With the binary pulse-width modulation, the intensity level of the color is reproduced by controlling the amount of time the mirror is on. For a 24-bit RGB frame, the DLPC300 creates 24 bit planes, stores them on the mDDR, and sends them to the DLP3000 DMD, one bit-plane at a time. Depending on the bit weight of the bit-plane, the DLPC300 controls the time this bit-plane is exposed to light, controlling the intensity of the bit-plane. To improve image quality in video frames, these bit-planes, time slots, and color frames are intertwined and interleaved with spatial-temporal algorithms by the DLPC300. In external video mode, the controller applies non-linear gamma correction.

7.4 Device Functional Modes

For applications where image enhancement is not desired, the video processing algorithms can be bypassed and replaced with a specific set of bit-planes. The bit-depth of the pattern is then allocated into the corresponding time slots. Furthermore, an output trigger signal is also synchronized with these time slots to indicate when the image is displayed. For structured light applications, this mechanism provides the capability to display a set of patterns and signal a camera to capture these patterns overlaid on an object. In this structured light mode, the controller applies linear gamma correction.

Figure 11 shows the bit planes and corresponding output triggers for 3-bit, 6-bit, and 12-bit RGB. Table 1 shows the allowed pattern combinations in relation to the bit depth of the pattern.

Device Functional Modes (continued)

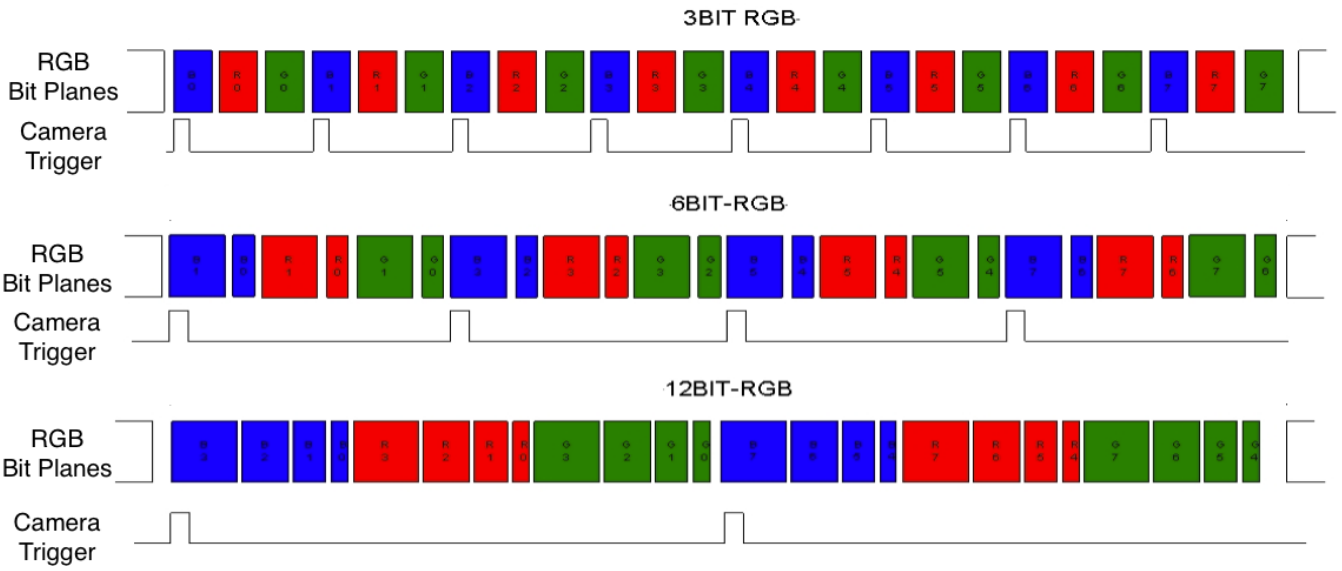


Figure 11. Bit Planes and Output Trigger for 3-, 6-, and 12-Bit RGB Input

Table 1. Allowed Pattern Combinations

External Video Sequence		Number of Images per Frame	Frame Rate	Pattern Rate
Monochrome	1 bit per pixel	24	15, 30, 40, or 60 Hz	24 × Frame rate
	2 bits per pixel	12		12 × Frame rate
	3 bits per pixel	8	15, 30, 45, or 60 Hz	8 × Frame rate
	4 bits per pixel	6	15, 30, 40, or 60 Hz	6 × Frame rate
	5 bits per pixel	4	15, 30, 45, or 60 Hz	4 × Frame rate
	6 bits per pixel	4		4 × Frame rate
	7 bits per pixel	3	15, 30, 40, or 60 Hz	3 × Frame rate
	8 bits per pixel	2	15, 30, 45, or 60 Hz	2 × Frame rate
RGB	1-bit per color pixel (3-bit per pixel)	8		8 × Frame rate
	2-bit per color pixel (6-bit per pixel)	4		4 × Frame rate
	4-bit per color pixel (12-bit per pixel)	2		2 × Frame rate
	5/6/5-bit RGB pixel (16-bit per pixel)	1		Frame rate
	6-bit per color pixel (18-bit per pixel)			
	8-bit per color pixel (24-bit per pixel)			

7.4.1 Configuration Control

The primary configuration control mechanism for the DLPC300 is the I^2C interface. See the *DLPC300 Software Programmer's Guide* (DLPU004) for details on how to configure and control the DLPC300.

7.4.2 Parallel Bus Interface

Parallel bus interface supports six data transfer formats:

- 16-bit RGB565

- 18-bit RGB666
- 18-bit 4:4:4 YCrCb666
- 24-bit RGB888
- 24-bit 4:4:4 YCrCb888
- 16-bit 4:2:2 YCrCb (standard sampling assumed to be Y0Cb0, Y1Cr0, Y2Cb2, Y3Cr2, Y4Cb4, Y5Cr4, …)

Figure 12 shows the required PDATA(23:0) bus mapping for these six data transfer formats.

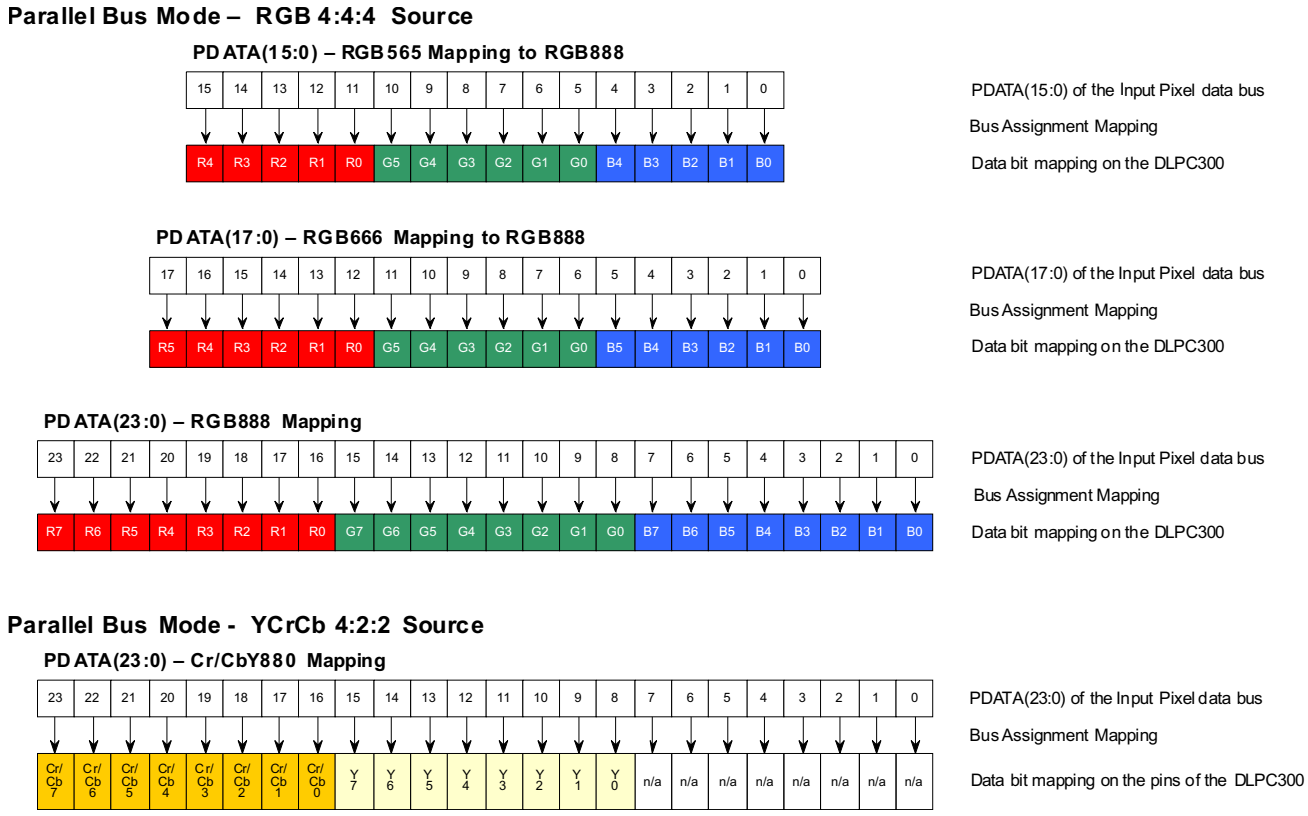


Figure 12. PDATA Bus – Parallel I/F Mode Bit Mapping

The parallel bus interface complies with the standard graphics interface protocol, which includes a vertical sync signal (VSYNC), horizontal sync signal (HSYNC), optional data-valid signal (DATAEN), a 24-bit data bus (PDATA), and a pixel clock (PCLK). The polarities of both syncs are programmable, as is the active edge of the clock. Figure 2 shows the relationship of these signals. The data-valid signal (DATAEN) is optional, in that the DLPC300 provides auto-framing parameters that can be programmed to define the data-valid window, based on pixel and line counting relative to the horizontal and vertical syncs.

7.4.3 BT.656 Interface

BT.656 data bits should be mapped to the DLPC300 PDATA bus as shown in Figure 13.

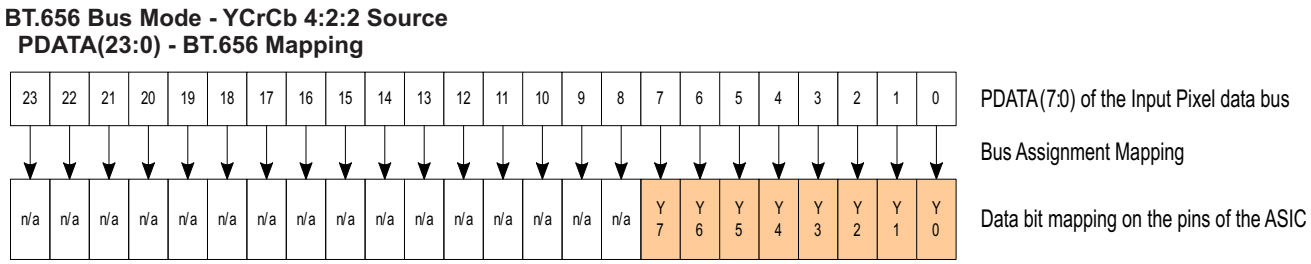


Figure 13. PDATA Bus – BT.656 I/F Mode Bit Mapping

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLPC300 controller enables integration of the DLP3000 WVGA chipset into small-form-factor and low-cost light steering applications. Example end equipments for the 0.3 WVGA chipset include 3D scanning or metrology systems with structured light, interactive displays, chemical analyzers, medical instruments, and other end equipments requiring spatial light modulation (or light steering and patterning).

8.2 Typical Application

The DLPC300 is one of the two devices in the DLP3000 WVGA chipset (see Figure 14). The other device is the DLP3000 DMD. For proper operation of the chipset, the DLPC300 requires a serial flash device with configuration information. This information is loaded after $\overline{\text{RESET}}$ is released. The configuration information is available for download from the DLPR300 product folder.

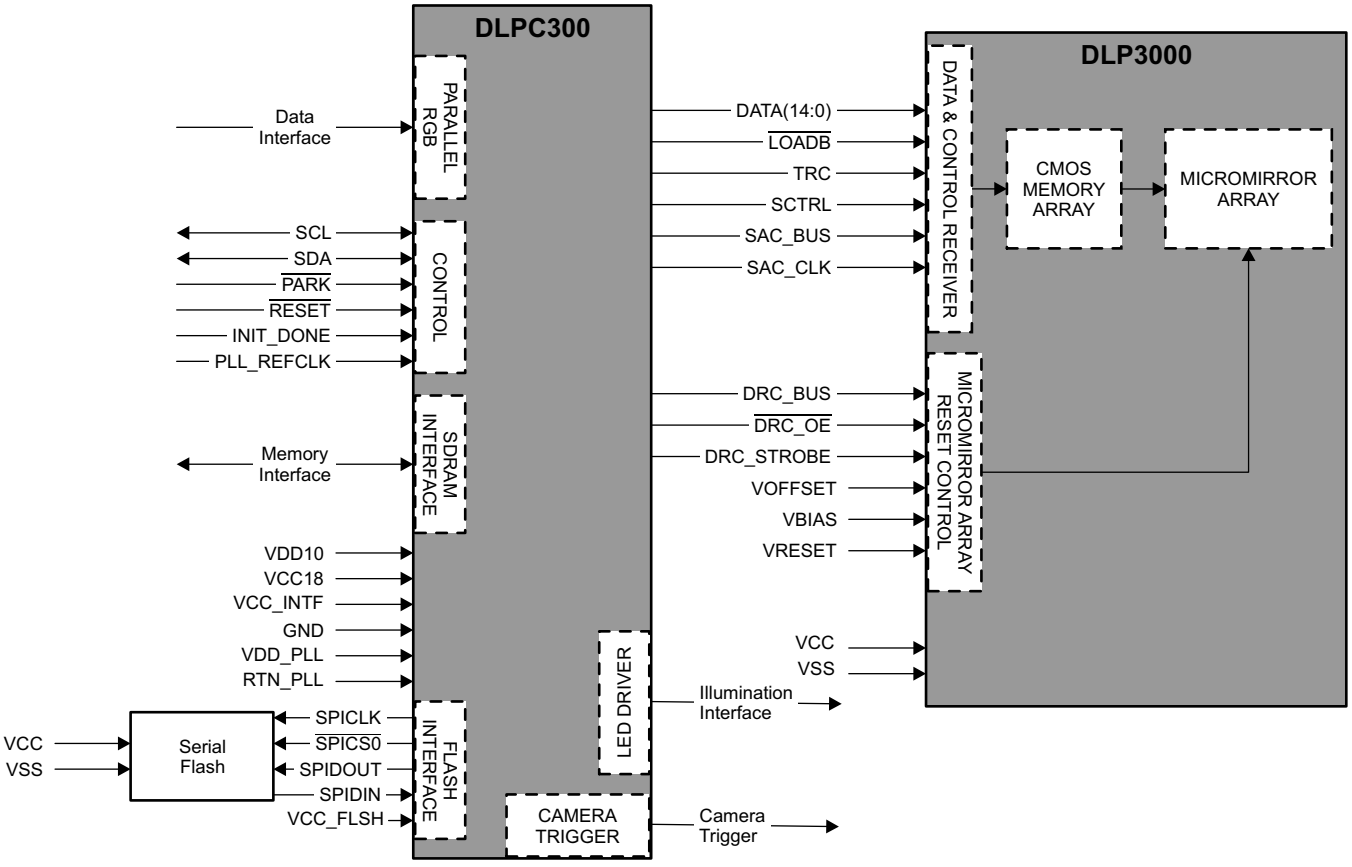


Figure 14. Chipset Block Diagram

8.2.1 Design Requirements

The DLP3000 WVGA chipset consists of two individual components:

- DLP3000 – 0.3 WVGA series 220 DMD
- DLPC300 – DLP3000 controller

Typical Application (continued)

Plus two additional components:

- SPI serial configuration flash loaded with the DLPC300 Configuration and Support Firmware
- Mobile DDR SDRAM

Detailed specifications for the components can be found in the individual component data sheets.

Figure 14 illustrates the connectivity between the individual components in the chipset, which include the following internal chipset interfaces:

- DLPC300 to DLP3000 data and control interface (DMD pattern data)
- DLPC300 to DLP3000 micromirror array reset control interface
- DLPC300 to mobile DDR SDRAM
- DLPC300 to SPI serial flash

Figure 15 illustrates the connectivity between the chipset and other key system-level components, which include the following external chipset interfaces:

- Data Interface, consisting of:
  - 24-bit data bus (PDATA[23:0])
  - Vertical sync signal (VSYNC)
  - Horizontal sync signal (HSYNC)
  - Data valid signal (DATAEN)
  - Data clock signal (PCLK)
  - Data mask (PDM)
- Control Interface, consisting of:
  - I^2C signals (SCL and SDA)
  - Park signal (PARK)
  - Reset signal (RESET)
  - Oscillator signals (PLL_REFCLK)
  - Mobile DDR SDRAM interface (mDDR)
  - Serial configuration flash interface
  - Illumination driver control interface

8.2.2 Detailed Design Procedure

8.2.2.1 System Input Interfaces

The DLP3000 WVGA Chipset supports a single 24-bit parallel RGB interface for data transfers from another device. The system input also requires that proper configuration of the $\overline{\text{PARK}}$ and $\overline{\text{RESET}}$inputs to ensure reliable operation.

See *Specifications* for further details on each of the following interfaces.

8.2.2.1.1 Control Interface

The DLP3000 WVGA chipset supports I^2C commands to control its operation. The control interface allows another master processor to send commands to the DLP3000 WVGA chipset to configure the chipset, query system status or perform real-time operations, such as set the LED drive current or display splash screens stored in serial flash memory. The DLPC300 offers two different slave addresses. The I2C_ADDR_SEL pin provides the ability to select an alternate set of 7-bit I^2C slave address. If I2C_ADDR_SEL is low, then the DLPC300 slave address is 1Bh. If I2C-ADDR_SEL pin is high, then the DLPC300 slave address is 1Dh. See the *DLPC300 Programmer's Guide* (DLPU004) for detailed information about these operations.

Table 2 provides a description for active signals used by the DLPC300 to support the I^2C interface.

Table 2. Active Signals – I^2C Interface

SIGNAL NAME	DESCRIPTION
SCL	I^2C clock. Bidirectional open-drain signal
SDA	I^2C data. Bidirectional open-drain signal

8.2.2.2 Input Data Interface

The data Interface is a digital video input port with up to 24-bit RGB, and has a nominal I/O voltage of 3.3 V. The data interface also supports a 24-bit BT656 video interface. As shown in Figure 15 (system block diagram), the data Interface can be configured to connect to an external processor or a video decoder device through an 8-, 16-, 18-, or 24-bit parallel interface.

Table 3 provides a description of the signals associated with the data interface.

Table 3. Active Signals – Data Interface

SIGNAL NAME	DESCRIPTION
PDATA(23:0)	24-bit data inputs (8 bits for each of the red, green, and blue channels)
PCLK	Pixel clock; all input signals on data interface are synchronized with this clock.
VSYNC	Vertical sync
HSYNC	Horizontal sync
DATAEN	Input data valid
PDM	Parallel data mask

Maximum and minimum input timing specifications are provided in *Parallel Interface Frame Timing Requirements* and *Parallel Interface General Timing Requirements*. The mapping of the red-, green-, and blue-channel data bits is shown in Figure 12.

8.2.2.3 System Output Interfaces

There are two primary output interfaces: illumination driver control interface and sync outputs.

8.2.2.3.1 Illumination Interface

An illumination interface is provided that supports up to a three (3) channel LED driver.

The illumination interface provides signals that support: LED driver enable, LED enable, LED enable select, and PWM signals to control the LED current.

Table 4 describes the active signals for the illumination interface.

Table 4. Active Signals – Illumination Interface

SIGNAL NAME	DESCRIPTION
LED_ENABLE	LED enable
LEDDRV_ON	LED driver master enable
LED_SEL(1:0)	Red, Green, or Blue LED enable select
RED_EN	Red LED enable
GREEN_EN	Green LED enable
BLUE_EN	Blue LED enable
RPWM	Red LED PWM signal used to control the LED current
GPWM	Green LED PWM signal used to control the LED current
BPWM	Blue LED PWM signal used to control the LED current

8.2.2.4 System Support Interfaces

8.2.2.4.1 Mobile DDR Synchronous Dram (MDDR)

The DLP3000 WVGA chipset relies on the use of mobile DDR SDRAM to store DMD formatted patterns. The SDRAM interface is a 16-bit wide bus and nominally operates at a frequency of 166 MHz. The data bus is routed in a point-to-point fashion between the DLPC300 and the mDDR devices, where each data line only makes a single connection between the DLPC300 and the mDDR device.

Listed below are the compatibility requirements for the mDDR:

SDRAM memory Type: Mobile DDR

Size: 128 M-bit minimum. DLPC300 can only address 128 Mb . Use of larger memories requires bit A13 to be grounded

Organization: N x 16-bits wide with 4 equally sized banks

Burst Length: 4

Refresh period: ≥ 64 ms

Speed Grade t_{CK}: 6 ns max

CAS Latency (C_L): 3 clocks

t_{RCD}: 3 clocks

t_{RP}: 3 clocks

Table 5 describes the signals for the SDRAM interface.

Table 5. Active Signals – Mobile DDR Synchronous Dram (MDDR)

SIGNAL NAME	DESCRIPTION
MEM_A(12:0)	13-bit address bus
MEM_BA(1:0)	Bank select signals
MEM_CKE	Clock enable
$\overline{\text{MEM\_CAS}}$	Column address strobe
$\overline{\text{MEM\_RAS}}$	Row address strobe
$\overline{\text{MEM\_CS}}$	Chip select
$\overline{\text{MEM\_WE}}$	Write enable
MEM_LDQS	R/W data strobe for lower byte
MEM_LDM	Write data mask for lower byte
MEM_UDQS	R/W data strobe for upper byte
MEM_UDM	Write data mask for upper byte
MEM_DQ(15:0)	16-bit data bus
MEM_CLK_N	Negative signal of the differential clock pair
MEM_CLK_P	Positive signal of the differential clock pair

Table 6 shows the mDDR DRAM devices recommended for use with the DLPC300.

Table 6. Compatible MDDR Dram Device Options(1)(2)

Vendor	Part Number(3)	Size	Organization	Speed Grade(4) (t_{CK})	CAS Latency (C_L) t_{RCD}, t_{RP} Parameters (Clocks)
Elpida	EDD25163HBH-6ELS-F(5)	256 Mb	16M × 16	6 ns	3, 3, 3
Samsung	K4X56163PN-FGC6(5)	256 Mb	16M × 16	6 ns	3, 3, 3
Micron	MT46H16M16LFBF-6IT:H	256 Mb	16M × 16	6 ns	3, 3, 3
Micron	MT46H32M16LF-6 IT:B	512 MB	32M × 16	6 ns	3, 3, 3
Micron	MT46H32M16LFBF-6:B	512 MB	32M × 16	6 ns	3, 3, 3

(1) All the SDRAM devices listed have been verified to be compatible with the DLPC300.
(2) The DLPC300 does not use partial-array self-refresh or temperature-compensated self-refresh options.
(3) These part numbers reflect a Pb-free package.
(4) A 6-ns speed grade corresponds to a 166-MHz mDDR device.
(5) These devices are EOL and should not be used in new designs.

Table 6. Compatible MDDR Dram Device Options(00) (continued)

Vendor	Part Number(3)	Size	Organization	Speed Grade(4) (t_{CK})	CAS Latency (C_L) t_{RCD}, t_{RP} Parameters (Clocks)
Micron	MT46H64M16LFCK-5:A(5)	1 Gb	64M × 16	6 ns	3, 3, 3
Hynix	H5MS2562JFR-J3M	256 Mb	16M × 16	6 ns	3, 3, 3
Winbond	W947D6HBHX6E	128 Mb	8M × 16	6 ns	3, 3, 3

8.2.2.4.2 Flash Memory Interface

DLPC300 uses an external 16-Mb SPI serial flash slave memory device for configuration support. The contents of this flash memory can be downloaded from the DLPC300 product folder. The DLPC300 uses a single SPI interface, employing SPI mode 0 protocol, operating at a nominal frequency of 33.3 MHz.

When $\overline{\text{RESET}}$ is released, the DLPC300 reads the contents of the serial flash memory and executes an auto-initialization routine. During this time, INIT_DONE is set high to indicate auto-initialization is busy. Upon completion of the auto-initialization routine, the DLPC300 sets INIT_DONE low to indicate that the auto-initialization routine successfully completed.

The DLPC300 should support any flash device that is compatible with standard SPI mode 0 protocol and meet the timing requirement shown in *Flash Interface Timing Requirements*. However, the DLPC300 does not support the normal (slow) read opcode, and thus cannot automatically adapt protocol and clock rate based on the electronic signature ID of the flash. The flash instead uses a fixed SPI clock and assumes certain attributes of the flash have been ensured by PCB design. The DLPC300 also assumes the flash supports address auto-incrementing for all read operations. Table 7 lists the specific Instruction opcode and timing compatibility requirements for a DLPC300-compatible flash.

Table 7. SPI Flash Instruction Opcode and Timing Compatibility Requirements

SPI Flash Command	Opcode (hex)	Address Bytes	Dummy Bytes	Clock Rate
Fast READ (single output)	0x0B	3	1	33.3 MHz
All others	Can vary	Can vary	Can vary	33.3 MHz

The DLPC300 does not have any specific page, block or sector size requirements except that programming through the I^2C interface requires the use of page-mode programming. However, if the user would like to dedicate a portion of the serial flash for storing external data (such as calibration data) and access it through the DLPC300's I^2C interface, then the minimum sector size must be considered, as it drives minimum erase size.

Note that the DLPC300 does not drive the $\overline{\text{HOLD}}$ (active-low hold) or $\overline{\text{WP}}$ (active-low write protect) pins on the flash device, and thus these pins should be tied to a logic high on the PCB by an external pullup.

The DLPC300 supports 1.8-, 2.5-, or 3.3-V serial flash devices. To do so, VCC_FLSH must be supplied with the corresponding voltage.

Table 8 describes the signals used to support this interface.

Table 8. Active Signals – DLPC300 Serial Configuration Flash Prom

SIGNAL NAME	DESCRIPTION
SPIDOUT	Serial configuration flash data output (from DLPC300 to flash)
SPIDIN	Serial configuration flash data input (from flash to DLPC300)
SPICLK	Serial configuration flash clock
$\overline{\text{SPICS0}}$	Serial configuration flash chip select

Table 9 contains a list of 1.8-, 2.5-, and 3.3-V compatible SPI serial flash devices supported by DLPC300.

Table 9. Compatible SPI Flash Device Options(1)

Density	Vendor	Part Number(2)	Supply Voltage Supported(3)	Min Chip Select High Time (t_{CSH})	Max Fast Read FREQ(4)	Compatible With OpCode and Timing in Table 7
4 Mb	Macronix	MX25U4035	1.65 V–2 V	30 ns	40 MHz	Yes
8 Mb	Macronix	MX25U8035	1.65 V–2 V	30 ns	40 MHz	Yes
16 Mb	Winbond	W25Q16BLxxxx	2.3 V–3.6 V	100 ns	50 MHz	Yes
8 Mb	Macronix	MX25L8005ZUx-xxG	2.7 V–3.6 V	100 ns	66 MHz	Yes

(1) All the SPI devices listed have been verified to be compatible with DLPC300.
(2) Lower case *x* is used as a wildcard placeholder and indicates an option that is selectable by the user. Note that the use of an upper case *X* is part of the actual part number.
(3) The flash supply voltage must match VCC_FLSH on the DLPC300. 1.8-V and 2.5-V SPI device options are limited. Take care when ordering devices to be sure the desired supply voltage is attained, as multiple voltage options are often available under the same base part number.
(4) Maximum supported fast read frequency at the minimum supported supply voltage

8.2.2.4.3 DLPC300 Reference Clock

The DLPC300 requires a 16.667-MHz 1.8-V external input from an oscillator. This signal is the DLP3000 WVGA chipset reference clock from which the majority of the interfaces derive their timing. This includes mDDR SDRAM, DMD interfaces, and serial interfaces.

See *Specifications* for reference clock specifications.

8.2.2.5 DMD Interfaces

8.2.2.5.1 DLPC300 to DLP3000 Digital Data

The DLPC300 provides the DMD pattern data to the DMD over a double data rate (DDR) interface.

Table 10 describes the signals used for this interface.

Table 10. Active Signals – DLPC300 to DLP3000 Digital Data Interface

DLPC300 SIGNAL NAME	DLP3000 SIGNAL NAME
DMD_D(14:0)	DATA(14:0)
DMD_DCLK	DCLK

8.2.2.5.2 DLPC300 to DLP3000 Control Interface

The DLPC300 provides the control data to the DMD over a serial bus.

Table 11 describes the signals used for this interface.

Table 11. Active Signals – DLPC300 to DLP3000 Control Interface

DLPC300 SIGNAL NAME	DLP3000 SIGNAL NAME	DESCRIPTION
DMD_SAC_BUS	SAC_BUS	DMD stepped-address control (SAC) bus data
DMD_SAC_CLK	SAC_CLK	DMD stepped-address control (SAC) bus clock
$\overline{\text{DMD\_LOADB}}$	$\overline{\text{LOADB}}$	DMD data load signal
DMD_SCTRL	SCTRL	DMD data serial control signal
DMD_TRC	TRC	DMD data toggle rate control

8.2.2.5.3 DLPC300 to DLP3000 Micromirror Reset Control Interface

The DLPC300 controls the micromirror clock pulses in a manner to ensure proper and reliable operation of the DMD.

Table 12 describes the signals used for this interface.

Table 12. Active Signals – DLPC300-to-DLP3000 Micromirror Reset Control Interface

DLPC300 SIGNAL NAME	DLP3000 SIGNAL NAME	DESCRIPTION
DMD_DRC_BUS	DRC_BUS	DMD reset control serial bus
$\overline{\text{DMD\_DRC\_OE}}$	$\overline{\text{DRC\_OE}}$	DMD reset control output enable
DMD_DRC_STRB	DRC_STRB	DMD reset control strobe

8.2.2.6 Maximum Signal Transition Time

Unless otherwise noted, 10 ns is the maximum recommended 20% to 80% rise/fall time to avoid input buffer oscillation. This applies to all DLPC300 input signals. However, the $\overline{\text{PARK}}$ input signal includes an additional small digital filter that ignores any input-buffer transitions caused by a slower rise or fall time for up to 150 ns.

8.3 System Examples

8.3.1 Video Source System Application

Figure 15 shows a typical embedded system application using the DLPC300. In this configuration, the DLPC300 controller supports a 24-bit parallel RGB, typical of LCD interfaces, from the main processor chip. This system supports both still and motion video sources. For this configuration, the controller only supports periodic sources. This is ideal for motion video sources, but can also be used for *still images* by maintaining periodic syncs but only sending a frame of data when needed. The *still image* must be fully contained within a single video frame and meet frame timing constraints. The DLPC300 refreshes the displayed image at the source frame rate and repeats the last active frame for intervals in which no new frame has been received.

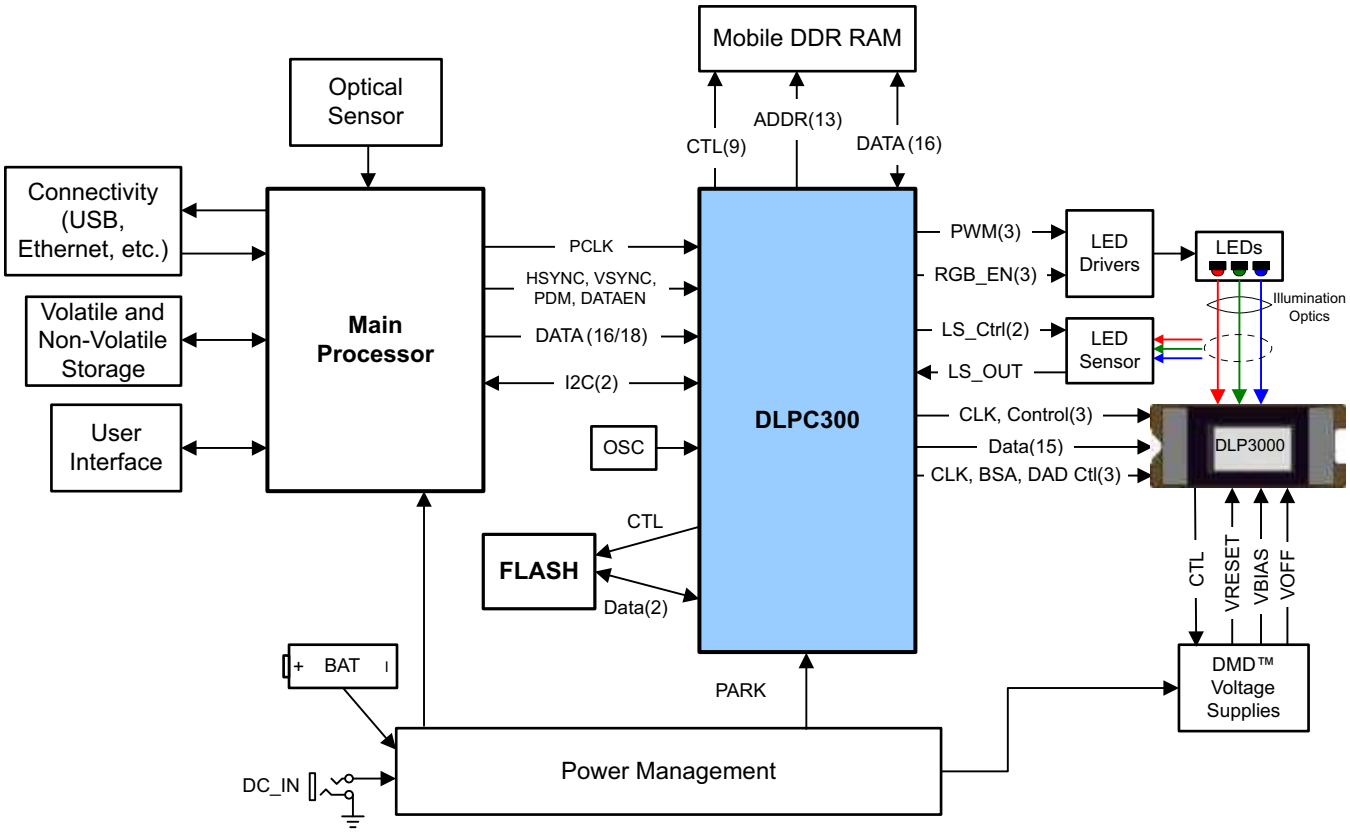


Figure 15. Typical Embedded System Block Diagram

System Examples (continued)

8.3.2 High Pattern Rate System With Optional Fpga

An optional FPGA (see the DLPR300 software folder) can be added to the system to manage the bit-planes stored in the mDDR. The mDDR accommodates four 608 × 684 images of 24-bit RGB data or 96 bit-planes (24 bit-planes × 4 images). By preloading the mDDR with these bit-planes, faster frame rates can be achieved. The 96 bit-plane buffer is arranged in a circular buffer style, meaning that the last bit-plane addition to the buffer replaces the oldest stored bit-plane. Figure 16 shows the overall system with the optional FPGA.

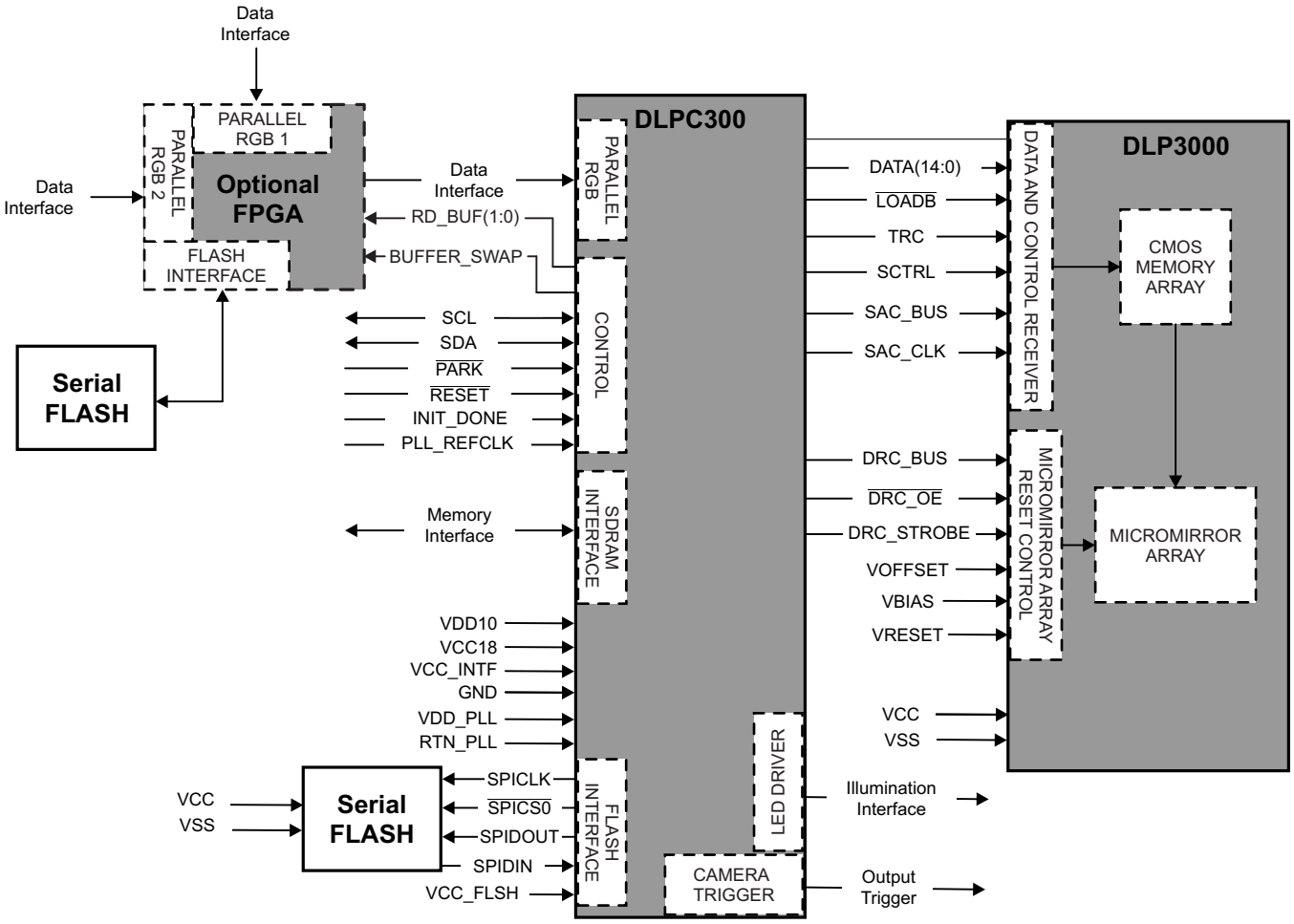


Figure 16. DLP3000 Chipset with Optional FPGA

With this FPGA, the pattern frame rate can be calculated with Equation 1.

$$\text{Pattern rate} = \frac{1}{(\text{Pattern exposure period}) + (\text{Bit plane load time})} \quad ; \text{if } \left[(\text{Number of images}) \times (\text{Bit depth})\right] \le 24$$

$$\text{Pattern rate} = \frac{1}{\begin{pmatrix}\text{Pattern exposure}\\ \text{period}\end{pmatrix} + \begin{pmatrix}\text{Bit plane}\\ \text{load time}\end{pmatrix} + \begin{pmatrix}\text{Buffer rotate}\\ \text{overhead}\end{pmatrix}} \quad ; \text{if } \left[(\text{Number of images}) \times (\text{Bit depth})\right] > 24$$

where

- Typical first bit plane load time = 215 µs
- Typical buffer rotate overhead = 135 µs (1)

Table 13 shows the maximum pattern rate that can be achieved by using a single FPGA internal buffer in continuous mode.

Table 13. Maximum Pattern Rate with Optional FPGA

Color Mode		Maximum Number of Patterns	Maximum Pattern Rate
Monochrome	1 bit per pixel	96	4000 Hz
	2 bits per pixel	48	1100 Hz
	3 bits per pixel	32	590 Hz
	4 bits per pixel	24	550 Hz
	5 bits per pixel	16	450 Hz
	6 bits per pixel	16	365 Hz
	7 bits per pixel	12	210 Hz
	8 bits per pixel	12	115 Hz

The digital RGB input interface operates at 1.8 V, 2.5 V, or 3.3 V nominal, depending on the VCC_INTF supply. The SPI flash interface operates at 1.8 V, 2.5 V, or 3.3 V nominal, depending on the VCC_FLSH supply. The DMD and mDDR interface operates at 1.8 V nominal (VCC18). The core transistors operate at 1 V nominal (VDD10). The analog PLL operates at 1 V nominal (VDD_PLL).

9 Power Supply Recommendations

9.1 System Power-Up and Power-Down Sequence

Although the DLPC300 requires an array of power supply voltages, (for example, VDD, VDD_PLL, VCC_18, VCC_FLSH, VCC_INTF), there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC300. This is true for both power-up and power-down scenarios. Similarly, there is no minimum time between powering up or powering down the different supplies feeding the DLPC300. Note, however, that it is not uncommon for there to be power-sequencing requirements for the devices that share the supplies with the DLPC300.

Although there is no risk of damaging the DLPC300 as a result of a given power sequence, from a functional standpoint, there is one specific power-sequencing recommendation to ensure proper operation. In particular, all controller power should be applied and allowed to reach minimum specified voltage levels before $\overline{\text{RESET}}$ is deasserted to ensure proper power-up initialization is performed. All I/O power should remain applied as long as 1-V core power is applied and $\overline{\text{RESET}}$ is deasserted.

Note that when VDD10 core power is applied but I/O power is not applied, additional leakage current may be drawn.

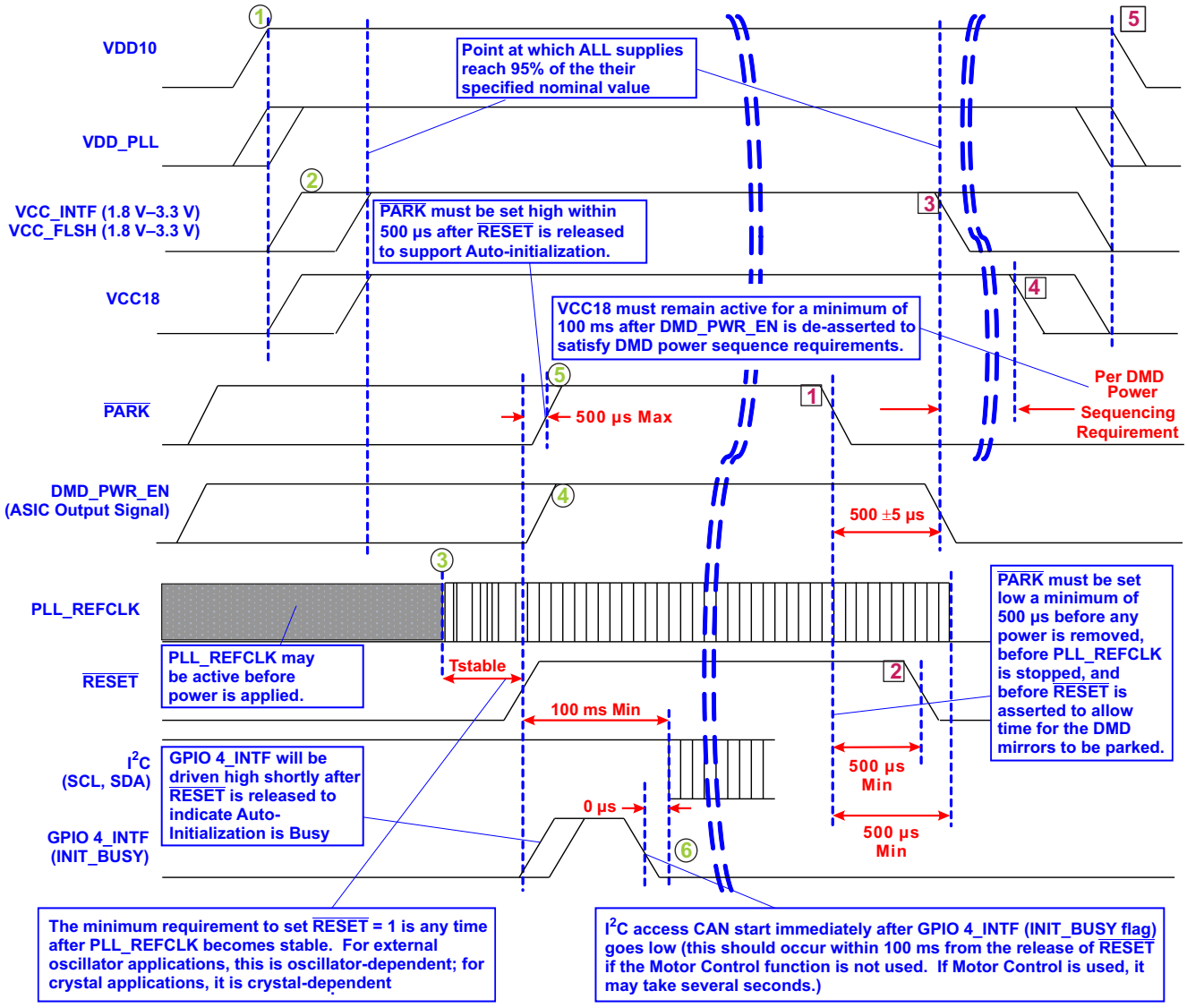


Figure 17. Power-Up/Down Timing

System Power-Up and Power-Down Sequence (continued)

9.1.1 Power Up Sequence

To minimize leakage currents and ensure proper operation, apply the following power up sequence. These steps are numbered in green with a circle around the step number in Figure 17.

1. Apply power to VDD10 and VDD_PLL while driving RESET low
2. After VDD10 power has reached minimum operating voltage, apply power to VCC18, VCC_INTF, and VCC_FLSH
3. After VCC18, VCC_INTF, and VCC_FLSH have reached minimum operating voltage, wait for the reference clock to stabilize (PLL_REFCLK). The time for the clock to stabilize depend on the external crystal or oscillator. Refer to the corresponding crystal or oscillator data sheet for appropriate time
4. Once the reference clock is stable, release reset to DLPC300 by driving RESET high. GPIO4_INTF will be driven high by the DLPC300 to indicate that Auto-Initialization is Busy
5. Drive PARK high within 500usec after RESET is driven high
6. Wait for DLPC300 to drive GPIO4_INTF low (a minimum of 100 ms) to indicate that the DLPC300 has completed the auto-Initialization and the device is ready to accept I2C commands

9.1.2 Power Down Sequence

To minimize leakage currents and ensure proper operation, apply the following power down sequence. These steps are numbered in red with a square around the step number in Figure 17.

1. Drive PARK low. This starts the park sequence which takes a maximum of 500 usec
2. Wait a minimum of 500 usec after driving PARK low before driving RESET low
3. Wait for DLPC300 to drive DMD_PWR_EN low before removing power to VCC_INTF and VCC_FLSH
4. Wait a minimum of 100 ms after DLPC300 drives DMD_PWR_EN low before removing power to VCC18
5. Once power has been removed from VCC18, remove power to VDD10 and VDD_PLL

9.1.3 Additional Power-Up Initialization Sequence Details

It is assumed that an external power monitor holds the DLPC300 in system reset during power-up. It must do this by driving $\overline{\text{RESET}}$ to a logic-low state. It should continue to assert system reset until all controller voltages have reached minimum specified voltage levels, PARK is asserted high, and input clocks are stable. During this time, most controller outputs are driven to an inactive state and all bidirectional signals are configured as inputs to avoid contention. Controller outputs that are not driven to an inactive state are in the high-impedance state. These include DMD_PWR_EN, LEDDVR_ON, LED_SEL_0, LED_SEL_1, SPICLK, SPIDOUT, and $\overline{\text{SPICS0}}$. After power is stable and the PLL_REFCLK clock input to the DLPC300 is stable, then $\overline{\text{RESET}}$ should be deactivated (set to a logic high). The DLPC300 then performs a power-up initialization routine that first locks its PLL followed by loading self-configuration data from the external flash. On release of $\overline{\text{RESET}}$, all DLPC300 I/Os become active. Immediately following the release of $\overline{\text{RESET}}$, the INIT_BUSY signal is driven high to indicate that the auto-initialization routine is in progress. On completion of the auto-initialization routine, the DLPC300 drives INIT_BUSY low to signal INITIALIZATION DONE.

Note that the host processor can start sending standard I^2C commands after INIT_BUSY goes low, or a 100-ms timer expires in the host processor, whichever is earlier.

See Figure 18 for a visualization of this sequence.

System Power-Up and Power-Down Sequence (continued)

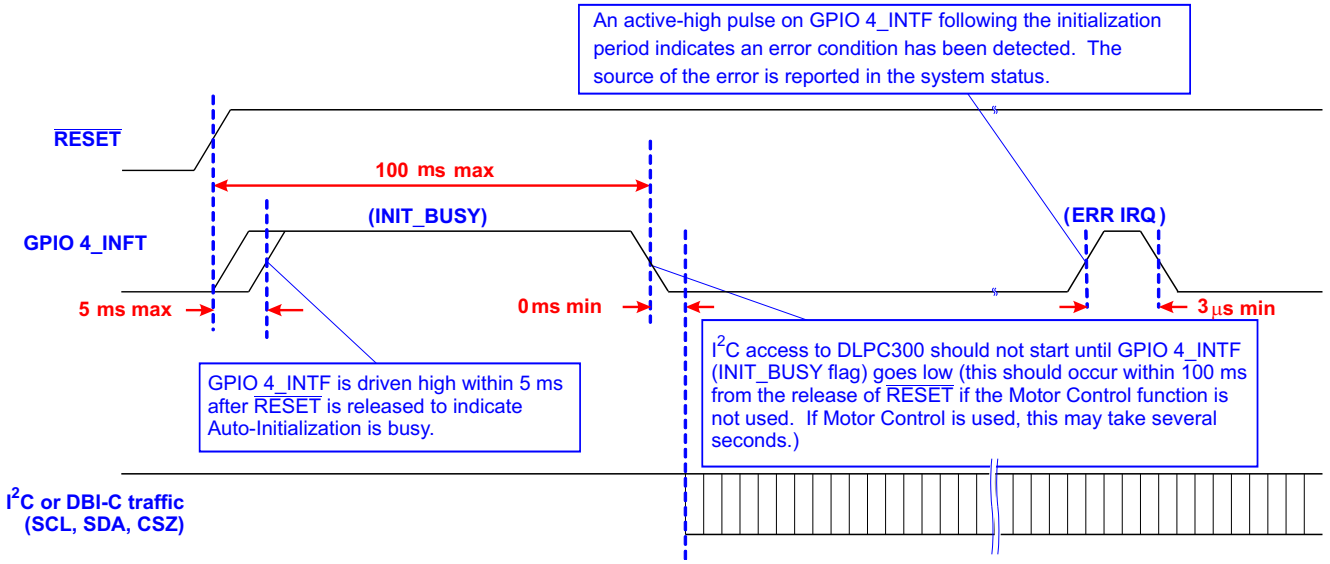


Figure 18. Initialization Timeline

9.2 System Power I/O State Considerations

Note that:

- If VCC18 I/O power is applied when VDD10 core power is not applied, then all mDDR (non fail-safe) and non-mDDR (fail-safe) output signals associated with the VCC18 supply are in a high-impedance state.
- If VCC_INTF or VCC_FLSH I/O power is applied when VDD10 core power is not applied, then all output signals associated with these inactive I/O supplies are in a high-impedance state.
- If VDD10 core power is applied but VCC_INTF or VCC_FLSH I/O power is not applied, then all output signals associated with these inactive I/O supplies are in a high-impedance state.
- If VDD10 core power is applied but VCC18 I/O power is not applied, then all mDDR (non fail-safe) and non-mDDR (fail-safe) output signals associated with the VCC18 I/O supply are in a high-impedance state; however, if driven high externally, only the non-mDDR (fail-safe) output signals remain in a high-impedance state, and the mDDR (non fail-safe) signals are shorted to ground through clamping diodes.

9.3 Power-Good ($\overline{\text{PARK}}$) Support

The $\overline{\text{PARK}}$ signal is defined to be an early warning signal that should alert the controller 500 µs before dc supply voltages have dropped below specifications. This allows the controller time to park the DMD, ensuring the integrity of future operation. Note that the reference clock should continue to run and $\overline{\text{RESET}}$ should remain deactivated for at least 500 µs after $\overline{\text{PARK}}$ has been deactivated (set to a logic low) to allow the park operation to complete.

10 Layout

10.1 Layout Guidelines

10.1.1 Printed Circuit Board Design Guidelines

The PCB design may vary depending on system design. Table 14 provides general recommendations on the PCB design.

Table 14. PCB General Recommendations for MDDR and DMD Interfaces

DESCRIPTION	RECOMMENDATION
Configuration	Asymmetric dual stripline
Etch thickness (T)	0.5-oz. (0.18-mm thick) copper
Single-ended signal impedance	50 Ω (± 10%)
Differential signal impedance	100 Ω differential (± 10%)

10.1.2 Printed Circuit Board Layer Stackup Geometry

The PCB layer stack may vary depending on system design. However, careful attention is required in order to meet design considerations listed in the following sections. Table 15 provides general guidelines for the mDDR and DMD interface stackup geometry.

Table 15. PCB Layer Stackup Geometry for MDDR and DMD Interfaces

PARAMETER	DESCRIPTION	RECOMMENDATION
Reference plane 1	Ground plane for proper return	
Er	Dielectirc FR4	4.2 (nominal)
H1	Signal trace distance to reference plane 1	5 mil (0.127 mm)
H2	Signal trace distance to reference plane 2	34.2 mil (0.869 mm)
Reference plane 2	I/O power plane or ground	

10.1.3 Signal Layers

The PCB signal layers should follow these recommendations:

- Layer changes should be minimized for single-ended signals.
- Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.
- Stubs should be avoided.
- Only voltage or low-frequency signals should be routed on the outer layers, except as noted previously in this document.
- Double data rate signals should be routed first.

10.1.4 Routing Constraints

In order to meet the specifications listed in Table 16 and Table 17, typically the PCB designer must route these signals manually (not using automated PCB routing software). In case of length matching requirements, the longer signals should be routed in a serpentine fashion, keeping the number of turns to a minimum and the turn angles no sharper than 45 degrees. Avoid routing long traces all around the PCB.

Table 16. Signal Length Routing Constraints for MDDR and DMD Interfaces

SIGNALS	MAX SIGNAL SINGLE-BOARD ROUTING LENGTH	MAX SIGNAL MULTI-BOARD ROUTING LENGTH
DMD_D(14:0), DMD_CLK, DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_OE, DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_CLK, and DMD_SAC_BUS	4 in (10.15 cm)	3.5 in (8.8891 cm)

Table 16. Signal Length Routing Constraints for MDDR and DMD Interfaces (continued)

SIGNALS	MAX SIGNAL SINGLE-BOARD ROUTING LENGTH	MAX SIGNAL MULTI-BOARD ROUTING LENGTH
MEM_CLK_P, MEM_CLK_N, MEM_A(12:0), MEM_BA(1:0), MEM_CKE, MEM_CS, MEM_RAS, MEM_CAS, and MEM_WE	2.5 in (6.35 cm)	Not recommended
MEM_DQ(15:0), MEM_LDM, MEM_UDM, MEM_LDQS, MEM_UDQS	1.5 in (3.81 cm)	Not recommended

Each high-speed, single-ended signal must be routed in relation to its reference signal, such that a constant impedance is maintained throughout the routed trace. Avoid sharp turns and layer switching while keeping lengths to a minimum. The following signals should follow these signal matching requirements.

Table 17. High-Speed Signal Matching Requirements for MDDR and DMD Interfaces

SIGNALS	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD_D(14:0), DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_OE,	DMD_DCLK	±500 (12.7)	mil (mm)
DMD_DRC_STRB, DMD_DRC_BUS	DMD_DCLK	±750 (19.05)	mil (mm)
DMD_SAC_CLK	DMD_DCLK	±500 (12.7)	mil (mm)
DMD_SAC_BUS	DMD_SAC_CLK	±750 (19.05)	mil (mm)
MEM_CLK_P	MEM_CLK_N	±150 (3.81)	mil (mm)
MEM_DQ(7:0), MEM_LDM	MEM_LDQS	±300 (7.62)	mil (mm)
MEM_DQ(15:8), MEM_UDM	MEM_UDQS	±300 (7.62)	mil (mm)
MEM_A(12:0), MEM_BA(1:0), MEM_CKE, MEM_CS, MEM_RAS, MEM_CAS, MEM_WE	MEM_CLK_P, MEM_CLK_N	±1000 (25.4)	mil (mm)
MEM_LDQS, MEM_UDQS	MEM_CLK_P, MEM_CLK_N	±300 (7.62)	mil (mm)

10.1.5 Termination Requirements

Table 18 lists the termination requirements for the DMD and mDDR interfaces.

For applications where the routed distance of the mDDR or DMD signal can be kept less than 0.75 inches, then this signal is short enough not to be considered a transmission line and should not need a series terminating resistor.

Table 18. Termination Requirements for MDDR and DMD Interfaces

SIGNALS	SYSTEM TERMINATION
DMD_D(14:0), DMD_CLK, DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_CLK, and DMD_SAC_BUS	Terminated at source with 10-Ω to 30-Ω series resistor. 30 Ω is recommended for most applications as this minimizes over/under-shoot and reduces EMI.
MEM_CLK_P and MEM_CLK_N	Terminated at source with 30-Ω series resistor. The pair should also be terminated with an external 100-Ω differential termination across the two signals as close to the mDDR as possible.
MEM_DQ(15:0), MEM_LDM, MEM_UDM, MEM_LDQS, MEM_UDQS	Terminated with 30-Ω series resistor located midway between the two devices
MEM_A(12:0), MEM_BA(1:0), MEM_CKE, MEM_CS, MEM_RAS, MEM_CAS, and MEM_WE	Terminated at the source with a 30-Ω series resistor

10.1.6 PLL

The DLPC300 contains one internal PLL that has a dedicated analog supply (VDD_PLL, VSS_PLL). As a minimum, the VDD_PLL power and VSS_PLL ground pins should be isolated using an RC-filter consisting of two 50-Ω series ferrites and two shunt capacitors (to widen the spectrum of noise absorption). TI recommends that one capacitor be a 0.1-µF capacitor and the other be a 0.01-µF capacitor. All four components should be placed as close to the controller as possible, but it is especially important to keep the leads of the high-frequency capacitors as short as possible. Note that both capacitors should be connected across VDD_PLL and VSS_PLL on the controller side of the ferrites.

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD_PLL must be a single trace from the DLPC300 to both capacitors and then through the series ferrites to the power source. The power and ground traces should be as short as possible, parallel to each other and as close as possible to each other. See Figure 20.

10.1.7 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends that unused controller input pins be tied through a pullup resistor to its associated power supply or through a pulldown to ground. For controller inputs with internal pullup or pulldown resistors, it is unnecessary to add an external pullup/pulldown unless specifically recommended. Note that internal pullup and pulldown resistors are weak and should not be expected to drive the external line. The DLPC300 implements very few internal resistors and these are noted in the pin list.

Unused output-only pins can be left open.

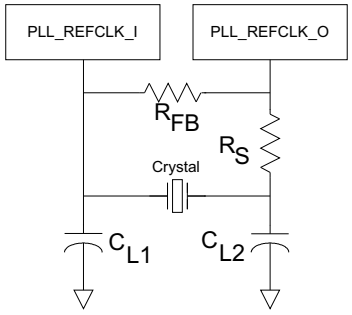
When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled up (or pulled down) using an appropriate resistor.

10.1.8 Hot-Plug Usage

Note that the DLPC300 provides fail-safe I/O on all host-interface signals (signals powered by VCC_INTF). This allows these inputs to be driven high even when no I/O power is applied. Under this condition, the DLPC300 does not load the input signal nor draw excessive current that could degrade controller reliability. Thus, for example, the I^2C bus from the host to other components would not be affected by powering off VCC_INTF to the DLPC300. Note that TI recommends weak pullups or pulldowns on signals feeding back to the host to avoid floating inputs.

10.1.9 External Clock Input Crystal Oscillator

The DLPC300 requires an external reference clock to feed its internal PLL. This reference may be supplied via a crystal or oscillator. The DLPC300 accepts a reference clock of 16.667 MHz with a maximum frequency variation of 200 ppm (including aging, temperature, and trim component variation). When a crystal is used, several discrete components are also required as shown in Figure 19.



A. CL = Crystal load capacitance (Farads)
B. CL1 = 2 × (CL – Cstray_pll_refclk_i)
C. CL2 = 2 × (CL – Cstray_pll_refclk_o)
D. Where
   - Cstray_pll_refclk_i = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_i.
   - Cstray_pll_refclk_o = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_o.

Figure 19. Recommended Crystal Oscillator Configuration

If an external oscillator is used, then the oscillator output must drive the PLL_REFCLK_I pin on the DLPC300 controller, and the PLL_REFCLK_O pins should be left unconnected. The benefit of an oscillator is that it can be made to provide a spread-spectrum clock that reduces EMI. However, the DLPC300 can only accept between 0% to –2% spreading (that is, down spreading only) with a modulation frequency between 20 and 65 kHz and a triangular waveform.

Similar to the crystal option, the oscillator input frequency is limited to 16.667 MHz.

It is assumed that the external crystal or oscillator stabilizes within 50 ms after stable power is applied.

Table 19 contains the recommended crystal configuration parameters.

Table 19. Recommended Crystal Configuration

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	16.667	MHz
Crystal frequency tolerance (including accuracy, temperature, aging, and trim sensitivity)	±200	PPM
Crystal drive level	100 max	uW
Crystal equivalent series resistance (ESR)	80 max	Ω
Crystal load	12	pF
R_S drive resistor (nominal)	100	Ω
R_{FB} feedback resistor (nominal)	1	MΩ
C_{L1} external crystal load capacitor	See Figure 19	pF
C_{L2} external crystal load capacitor	See Figure 19	pF
PCB layout	A ground isolation ring around the crystal is recommended	

10.2 Layout Example

A complete schematic and layout example is provided in the DLP 0.3 WVGA Chipset Reference Design, which is implemented in the DLP LightCrafter EVM. The PCB stack up for this design can be seen in Table 20.

Table 20. Driver Board PCB Stackup and Impedance(1)

Layer	Material Type	Thickness (mil)	Refer Layer	Impedance	
				50 Ω (Single End)	100 Ω (Differential Pair)
	SolderMask	0.80			
	Add Plating	1.04			
L1 - Top	L1	0.46	L2	5.5 mil (50.4 Ω)	4 mil /6 mil spacing /4 mil (99.1 Ω)
	Prepreg	3.49			
L2 - GND	L2	1.10			
	Prepreg	3.39			
L3 - Signal	L3	1.10	L2/L4	3.5 mil (49.5 Ω)	
	Prepreg	5.32			
L4 - GND	L4	0.70			
	Core	12			
L5 - PWR	L5	0.70			
	Prepreg	5.27			
L6 - Signal	L6	1.10	L5/L7	3.5 mil (49.5 Ω)	
	Prepreg	3.45			
L7 - GND	L7	1.10			
	Prepreg	3.5			
L8 - Bottom	L8	0.46	L7	5.5 mil (50.4 Ω)	4 mil /6 mil spacing /4 mil (99.1 Ω)

(1) Total thickness = 46.82 mil; Total thickness = 1.19 mm

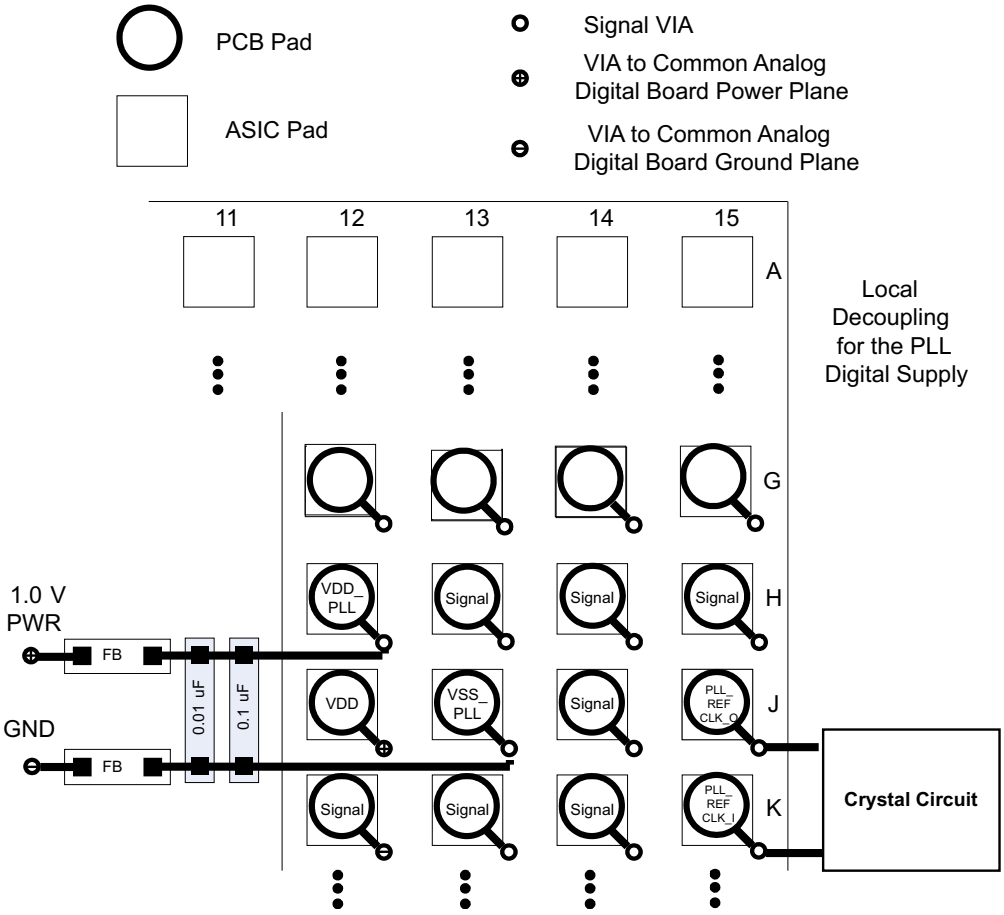


Figure 20. PLL Filter Layout

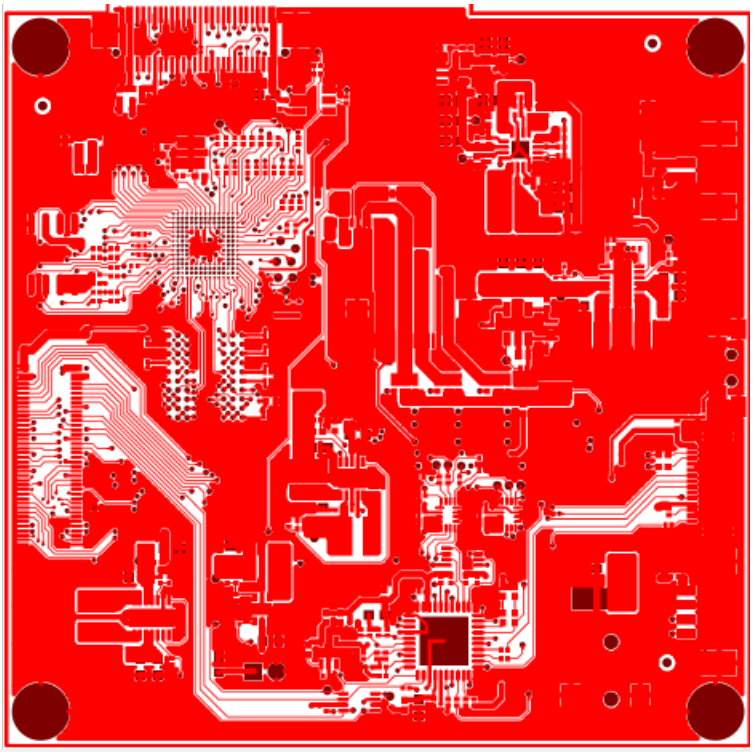


Figure 21. Top Board Layer

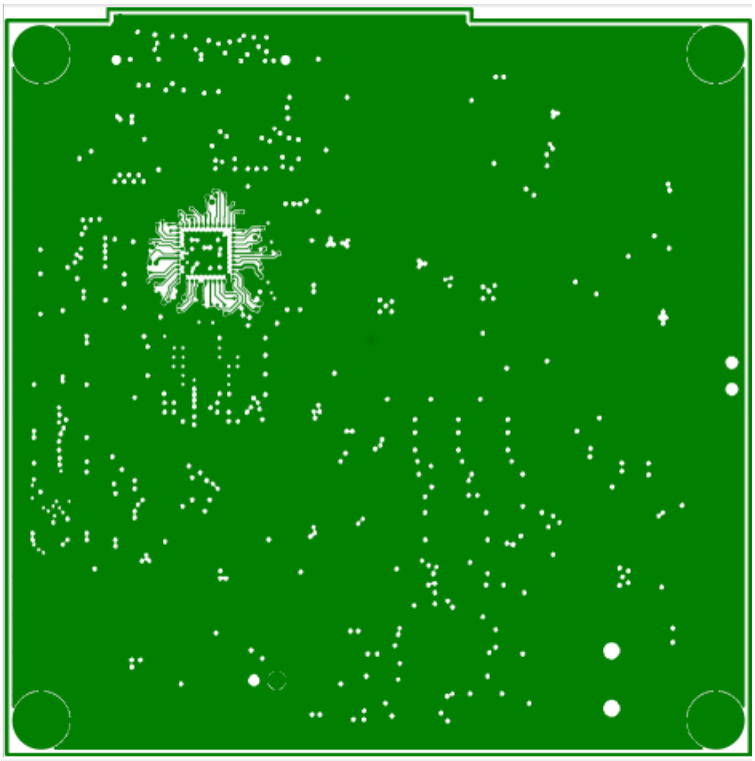


Figure 22. Internal Layer

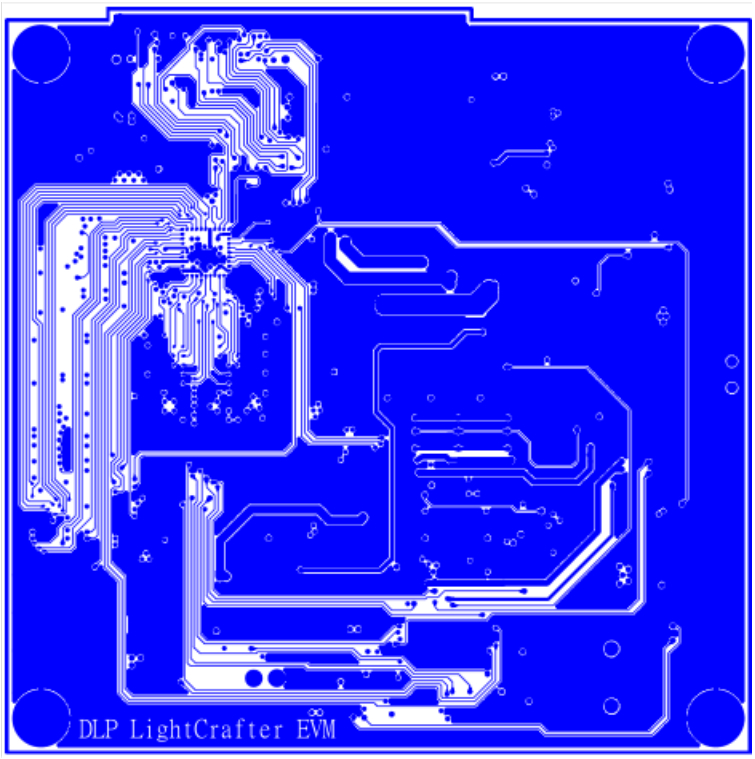


Figure 23. Bottom Board Layer

10.3 Thermal Considerations

The underlying thermal limitation for the DLPC300 is that the maximum operating junction temperature (T_J) not be exceeded (see *Recommended Operating Conditions*). This temperature depends on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC300, and power dissipation of surrounding components. The DLPC300 package is designed primarily to extract heat through the power and ground planes of the PCB. Thus, copper content and airflow over the PCB are important factors.

11 器件和文档支持

11.1 器件支持

11.1.1 Third-Party Products Disclaimer

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11.1.2 器件命名规则

图 24 提供了读取任一 DLP 器件完整器件名称的图例。

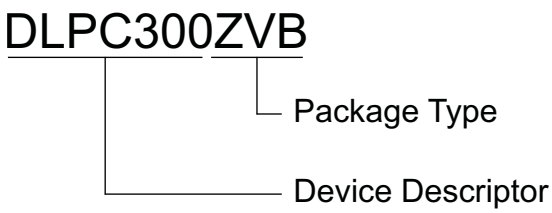

图 **24.** 器件命名规则

11.1.3 器件标记

器件标记由 图 25 中显示的字段组成。

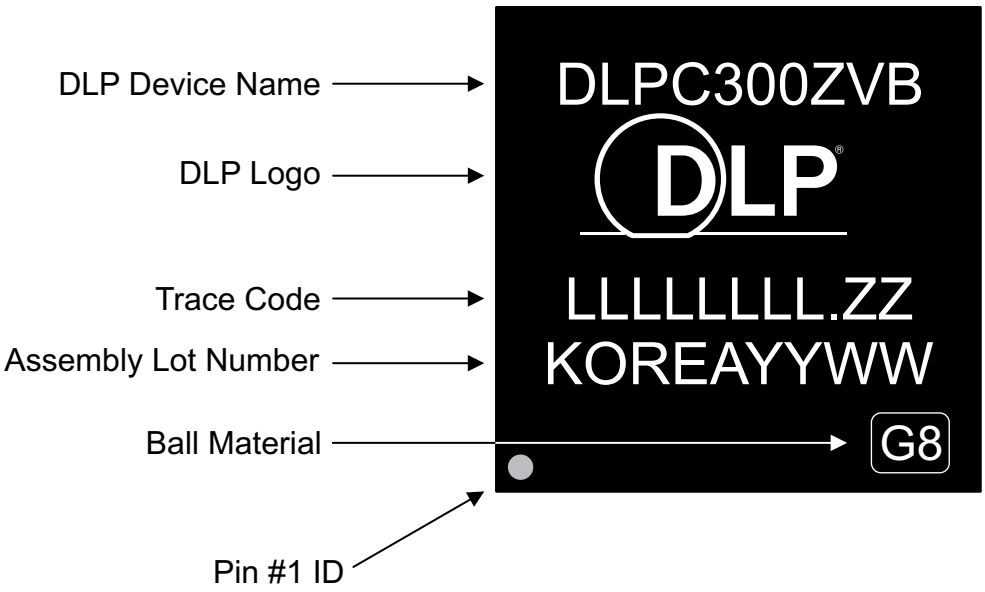

图 **25.** 器件标记

11.2 文档支持

11.2.1 相关文档

- 《*DLP3000 0.3 WVGA 系列 220 DMD* 数据表》，DLPS022
- 《*DLPC300 编程人员指南*》，DLPU004
- 《DLP® 0.3 WVGA 芯片组参考设计》

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

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数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC300ZVB	ACTIVE	NFBGA	ZVB	176	10	Non-RoHS & Non-Green	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

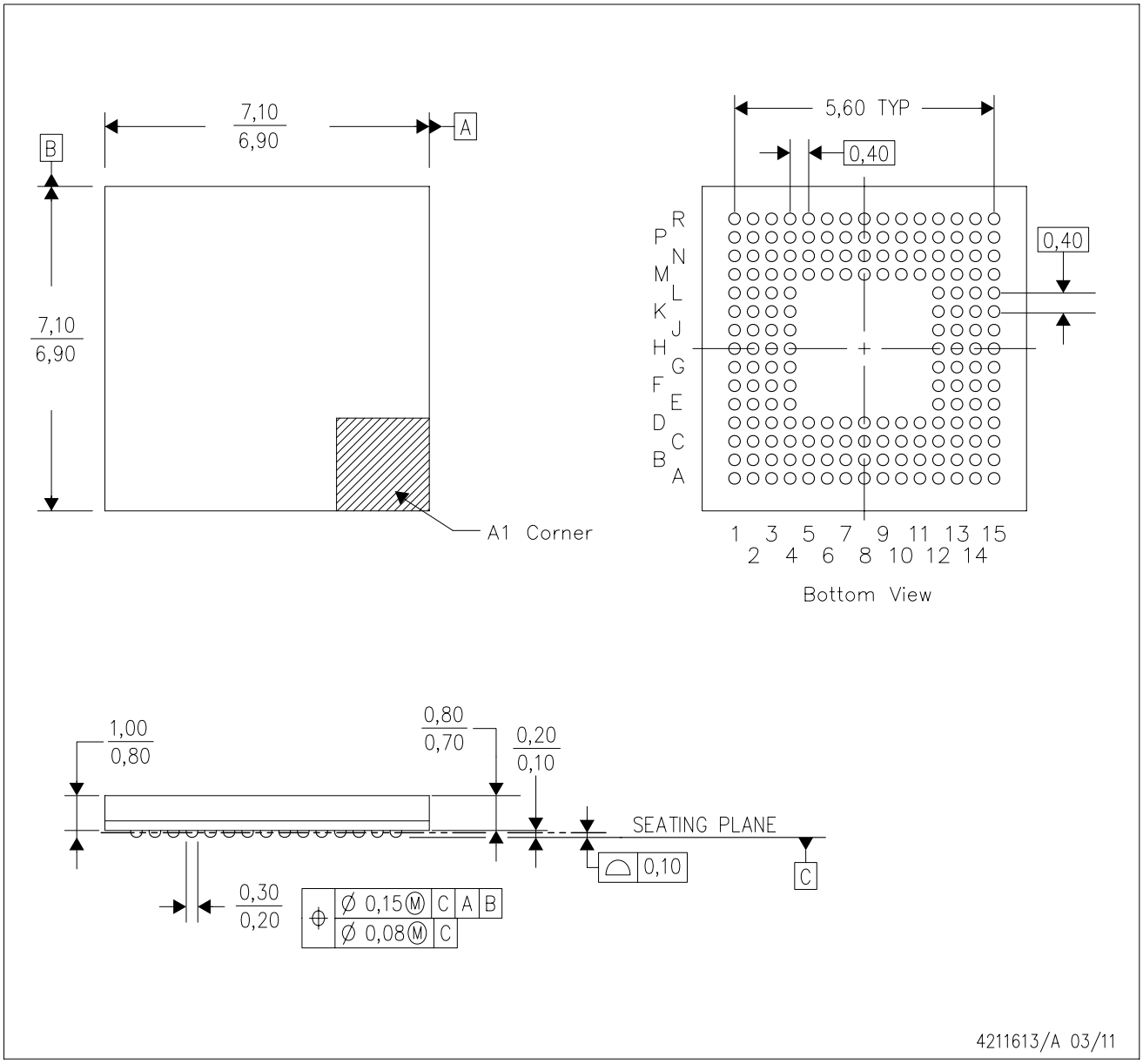
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

ZVB (S–PBGA–N176) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This package is Pb–free.

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