DLPC910 用于 DLP9000XFLS 数字微镜器件 (DMD) 的数字控制器

1 特性

- 用于确保 DLP9000XFLS DMD 可靠运行
- 400MHz 和 480MHz 两种用户可选的输入时钟速率
- 对于持续输入数据流，像素数据速率大于 61 千兆位/秒
- 支持最高可达 15kHz 的高速二进制模式速率
- 采用调制照明后的 8 位灰度模式速率高达 1.8kHz
- 64 位 2x LVDS 数据总线接口
- 支持随机 DMD 行寻址和 Load4 装载
- 与多种用户定义的应用处理器或现场可编程门阵列 (FPGA) 兼容
- 用于通用控制和状态查询的集成 I^2C 接口

2 应用

- 平版印刷
  - 直接成像
  - 平板显示器
  - 印刷电路板制造
- 工业
  - 3D 打印
  - 用于机器视觉的 3D 扫描仪
  - 质量控制
- 显示器
  - 3D 成像
  - 增强现实和信息覆盖

3 说明

DLPC910 器件用于确保 DLP9000XFLS DMD 的可靠运行。 该器件是 DLP® 芯片组中性能最高的芯片之一。

DLPC910 为 DLP9000XFLS DMD 提供一个高速数据和控制接口，以实现高达 15kHz 的二进制模式速率。 如此快速的模式速率使得 DLP 技术力压同类其他空间照明调制器脱颖而出，并且可满足客户设备对于快速、精确和可编程光源控制功能的需求，从而使客户获得战略性优势。 DLPC910 为 DMD 提供所需的镜时钟脉冲和时序信息。 DLPC910 器件具备独特的功能和价值，非常适合为各种平版印刷、工业和高级显示应用提供支持。

在基于 DLP 的电子解决方案中，从 DLPC910 输入端口到被投影图像的图像数据是 100% 数字化的数据。 图像始终保持数字格式，永远不会转换为模拟信号。 DLPC910 会处理数字输入图像并将数据转换为 DMD 所需的图像格式，以确保正确显示。 DMD 随后会将光线导向载入 DMD 中的像素数据所确定的位置。

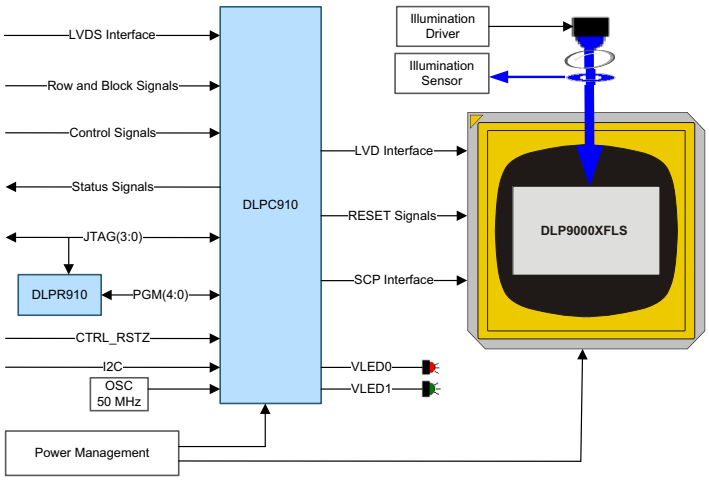
关于 DLPC910 的完整电气和机械规范，请参见 Virtex®-5 产品规范 (www.xilinx.com)。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DLPC910	FCBGA (676)	27.00mm × 27.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用图



目录

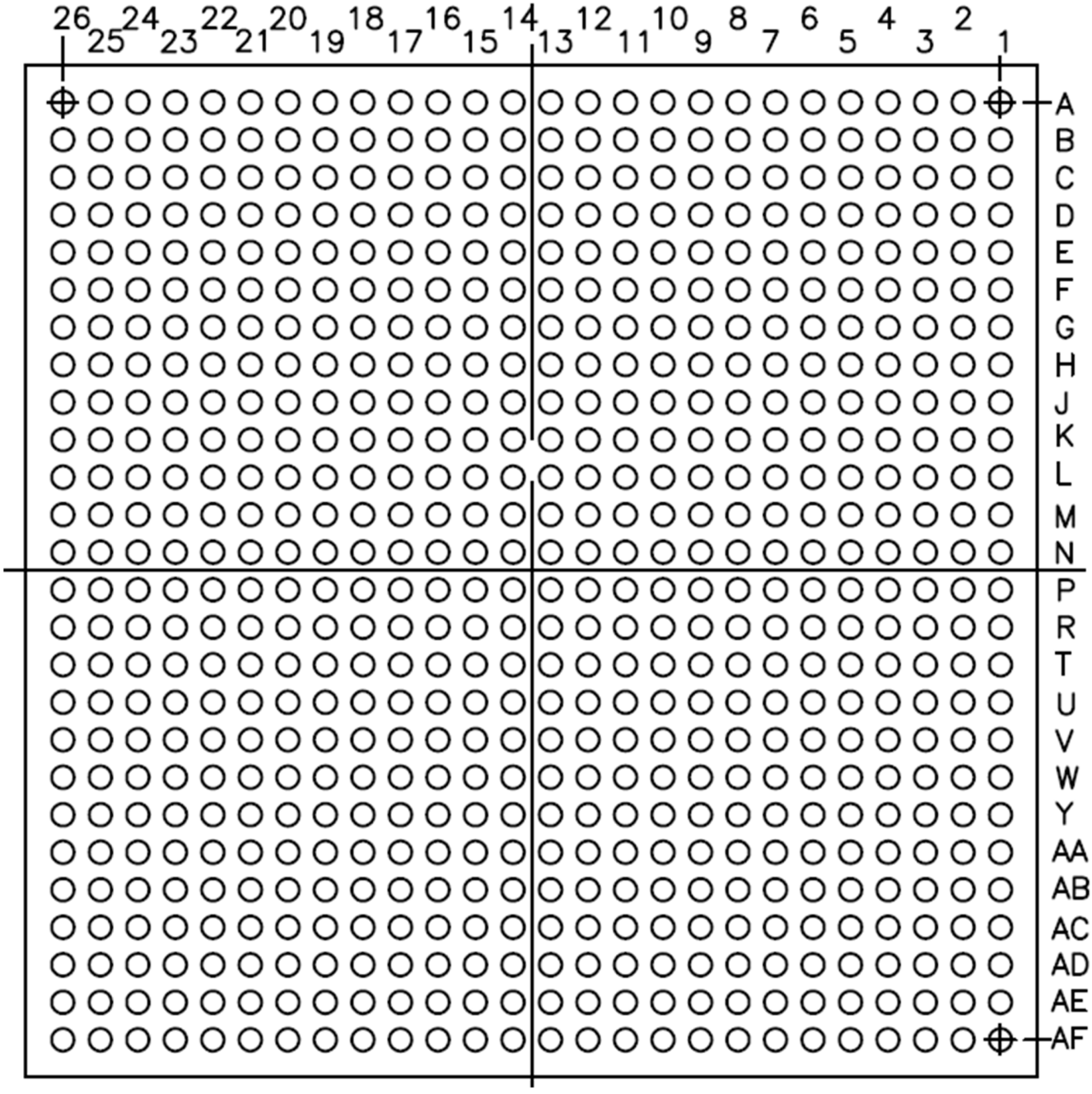
4 修订历史记录

Changes from Original (September 2015) to Revision A **Page**

- 已将器件状态从“产品预览”更改为“量产数据” 1

5 Pin Configuration and Functions

ZYR Package
676-Pin FCBGA
Top View



I/O Type Descriptions

I/O TYPE	DESCRIPTION
PWR	Power
GND	Ground
LVDS_25_NI	LVDS 2.5-V negative input
LVDS_25_PI	LVDS 2.5-V positive input
LVDS_25_NO	LVDS 2.5-V negative output
LVDS_25_PO	LVDS 2.5-V positive output
LVCMOS25_I	LVCMOS 2.5-V input
LVCMOS25_O	LVCMOS 2.5-V output
LVCMOS25_B	LVCMOS 2.5-V bidirectional
LVCMOS33_I	LVCMOS 3.3-V input
LVCMOS33_O	LVCMOS 3.3-V output
LVCMOS33_B	LVCMOS 3.3-V bidirectional
LVDCI_33_O	Low-voltage digitally controlled impedance 3.3-V output
NC	No connection

Pin Functions

PIN		I/O TYPE	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
CTRL_RSTZ	F9	LVCMOS25_I	Lo = 0	-	DLPC910 Reset.
DDC_IIC_ADDR_SEL	AA10	LVCMOS33_I	Hi = 1	-	DLPC910 Slave IIC Address Lo = 0x34, Hi = 0x36. Includes Internal pull-up.
DDC_IIC_SCL	Y8	LVCMOS33_B	-	-	DLPC910 Slave IIC Clock. **Requires an external 1-kΩ pull-up resistor**.
DDC_IIC_SDA	AA8	LVCMOS33_B	-	DDC_IIC_SCL	DLPC910 Slave IIC Data. **Requires an external 1-kΩ pull-up resistor**.
CLKIN_R	E10	LVCMOS25_I	-	Reference clock	50-MHz Reference Clock
RESET_ADDR0	AD18	LVDCI_33_O	Hi	-	Connect to DMD RESET_ADDR0
RESET_ADDR1	AC18	LVDCI_33_O	Hi	-	Connect to DMD RESET_ADDR1
RESET_ADDR2	AC17	LVDCI_33_O	Hi	-	Connect to DMD RESET_ADDR2
RESET_ADDR3	AC16	LVDCI_33_O	Hi	-	Connect to DMD RESET_ADDR3
RESET_MODE0	AC13	LVDCI_33_O	Hi	-	Connect to DMD RESET_MODE0
RESET_MODE1	AD13	LVDCI_33_O	Hi	-	Connect to DMD RESET_MODE1
RESET_SEL0	AD15	LVDCI_33_O	Hi	-	Connect to DMD RESET_SEL0
RESET_SEL1	AC14	LVDCI_33_O	Hi	-	Connect to DMD RESET_SEL1
RESET_STROBE	AD10	LVDCI_33_O	Hi	-	Connect to DMD RESET_STROBE
RESET_OEZ	AD14	LVDCI_33_O	Lo	-	Connect to DMD RESET_OEZ
RESET_IRQZ	AD8	LVCMOS33_I	Lo	-	Connect to DMD RESET_IRQZ
RESET_RSTZ	AB10	LVDCI_33_O	Lo	-	Connect to DMD RESETZ
SCPCLK	AC7	LVDCI_33_O	-	-	Connect to DMD SCP_CLK
SCPDI	AC8	LVCMOS33_I	-	SCPCLK	Connect to DMD SCP_DO
SCPDO	AC9	LVDCI_33_O	-	SCPCLK	Connect to DMD SCP_DI
DMD_SCPENZ	AB9	LVDCI_33_O	Lo	SCPCLK	Connect to DMD SCP_ENZ
DMD_TYPE_0	G11	LVCMOS25_O	Hi	-	Attached DMD Type bit 0
DMD_TYPE_1	G12	LVCMOS25_O	Hi	-	Attached DMD Type bit 1
DMD_TYPE_2	H11	LVCMOS25_O	Hi	-	Attached DMD Type bit 2
DMD_TYPE_3	H12	LVCMOS25_O	Hi	-	Attached DMD Type bit 3
BLKAD_0	E12	LVCMOS25_I	Hi	DDC_DCLK_[A,B,C,D]	Block Address bit 0
BLKAD_1	D13	LVCMOS25_I	Hi	DDC_DCLK_[A,B,C,D]	Block Address bit 1
BLKAD_2	E13	LVCMOS25_I	Hi	DDC_DCLK_[A,B,C,D]	Block Address bit 2
BLKAD_3	F13	LVCMOS25_I	Hi	DDC_DCLK_[A,B,C,D]	Block Address bit 3
BLKMD_0	H13	LVCMOS25_I	Hi	DDC_DCLK_[A,B,C,D]	Block Mode Bit 0
BLKMD_1	H14	LVCMOS25_I	Hi	DDC_DCLK_[A,B,C,D]	Block Mode Bit 1
ROWAD_0	D14	LVCMOS25_I	Hi	-	DMD Row Address bit 0
ROWAD_1	D15	LVCMOS25_I	Hi	-	DMD Row Address bit 1

Pin Functions (continued)

PIN		I/O TYPE	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
ROWAD_2	E15	LVCMOS25_I	Hi	-	DMD Row Address bit 2
ROWAD_3	F14	LVCMOS25_I	Hi	-	DMD Row Address bit 3
ROWAD_4	G14	LVCMOS25_I	Hi	-	DMD Row Address bit 4
ROWAD_5	E16	LVCMOS25_I	Hi	-	DMD Row Address bit 5
ROWAD_6	F15	LVCMOS25_I	Hi	-	DMD Row Address bit 6
ROWAD_7	G15	LVCMOS25_I	Hi	-	DMD Row Address bit 7
ROWAD_8	E17	LVCMOS25_I	Hi	-	DMD Row Address bit 8
ROWAD_9	F17	LVCMOS25_I	Hi	-	DMD Row Address bit 9
ROWAD_10	G16	LVCMOS25_I	Hi	-	DMD Row Address bit 10
ROWMD_0	H17	LVCMOS25_I	Hi	-	DMD Row Mode bit 0
ROWMD_1	H16	LVCMOS25_I	Hi	-	DMD Row Mode bit 1
DDC_DCLK_A_DPN	B21	LVDS_25_NI	-	-	Input Bus A Clock. 100-Ω internal LVDS termination.
DDC_DCLK_A_DPP	C21	LVDS_25_PI	-	-	
DDC_DCLK_B_DPN	A7	LVDS_25_NI	-	-	Input Bus B Clock. 100-Ω internal LVDS termination.
DDC_DCLK_B_DPP	B7	LVDS_25_PI	-	-	
DDC_DCLK_C_DPN	K20	LVDS_25_NI	-	-	Input Bus C Clock. 100-Ω internal LVDS termination.
DDC_DCLK_C_DPP	K21	LVDS_25_PI	-	-	
DDC_DCLK_D_DPN	L5	LVDS_25_NI	-	-	Input Bus D Clock. 100-Ω internal LVDS termination.
DDC_DCLK_D_DPP	K5	LVDS_25_PI	-	-	
DDC_DCLKOUT_A_DPN	N1	LVDS_25_NO	-	-	Output Bus A Clock to DMD.
DDC_DCLKOUT_A_DPP	M1	LVDS_25_PO	-	-	
DDC_DCLKOUT_B_DPN	Y5	LVDS_25_NO	-	-	Output Bus B Clock to DMD.
DDC_DCLKOUT_B_DPP	Y6	LVDS_25_PO	-	-	
DDC_DCLKOUT_C_DPN	AA22	LVDS_25_NO	-	-	Output Bus C Clock to DMD.
DDC_DCLKOUT_C_DPP	AB22	LVDS_25_PO	-	-	
DDC_DCLKOUT_D_DPN	M26	LVDS_25_NO	-	-	Output Bus D Clock to DMD.
DDC_DCLKOUT_D_DPP	M25	LVDS_25_PO	-	-	
DDC_DIN_A0_DPN	A15	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 0. 100-Ω internal LVDS termination.
DDC_DIN_A0_DPP	A14	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A1_DPN	B14	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 1. 100-Ω internal LVDS termination.
DDC_DIN_A1_DPP	C14	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A2_DPN	B16	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 2. 100-Ω internal LVDS termination.
DDC_DIN_A2_DPP	B15	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A3_DPN	C16	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 3. 100-Ω internal LVDS termination.
DDC_DIN_A3_DPP	D16	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A4_DPN	A17	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 4. 100-Ω internal LVDS termination.
DDC_DIN_A4_DPP	B17	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A5_DPN	C17	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 5. 100-Ω internal LVDS termination.
DDC_DIN_A5_DPP	D18	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A6_DPN	A19	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 6. 100-Ω internal LVDS termination.
DDC_DIN_A6_DPP	A18	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A7_DPN	C18	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 7. 100-Ω internal LVDS termination.
DDC_DIN_A7_DPP	B19	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A8_DPN	D19	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 8. 100-Ω internal LVDS termination.
DDC_DIN_A8_DPP	C19	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A9_DPN	B20	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 9. 100-Ω internal LVDS termination.
DDC_DIN_A9_DPP	A20	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A10_DPN	A22	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 10. 100-Ω internal LVDS termination.
DDC_DIN_A10_DPP	B22	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A11_DPN	A24	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 11. 100-Ω internal LVDS termination.
DDC_DIN_A11_DPP	A23	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A12_DPN	C23	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 12. 100-Ω internal LVDS termination.
DDC_DIN_A12_DPP	B24	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A13_DPN	C24	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 13. 100-Ω internal LVDS termination.
DDC_DIN_A13_DPP	D24	LVDS_25_PI	-	DDC_DCLK_A	

Pin Functions (continued)

PIN		I/O TYPE	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
DDC_DIN_A14_DPN	A25	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 14. 100-Ω internal LVDS termination.
DDC_DIN_A14_DPP	B25	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_A15_DPN	C26	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data bit 15. 100-Ω internal LVDS termination.
DDC_DIN_A15_DPP	B26	LVDS_25_PI	-	DDC_DCLK_A	
DDC_DIN_B0_DPN	A12	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 0. 100-Ω internal LVDS termination.
DDC_DIN_B0_DPP	A13	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B1_DPN	B12	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 1. 100-Ω internal LVDS termination.
DDC_DIN_B1_DPP	C13	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B2_DPN	D10	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 2. 100-Ω internal LVDS termination.
DDC_DIN_B2_DPP	D11	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B3_DPN	C12	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 3. 100-Ω internal LVDS termination.
DDC_DIN_B3_DPP	C11	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B4_DPN	A10	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 4. 100-Ω internal LVDS termination.
DDC_DIN_B4_DPP	B11	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B5_DPN	D9	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 5. 100-Ω internal LVDS termination.
DDC_DIN_B5_DPP	C9	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B6_DPN	B10	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 6. 100-Ω internal LVDS termination.
DDC_DIN_B6_DPP	B9	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B7_DPN	A8	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 7. 100-Ω internal LVDS termination.
DDC_DIN_B7_DPP	A9	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B8_DPN	D6	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 8. 100-Ω internal LVDS termination.
DDC_DIN_B8_DPP	D5	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B9_DPN	C7	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 9. 100-Ω internal LVDS termination.
DDC_DIN_B9_DPP	C6	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B10_DPN	B6	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 10. 100-Ω internal LVDS termination.
DDC_DIN_B10_DPP	B5	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B11_DPN	D4	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 11. 100-Ω internal LVDS termination.
DDC_DIN_B11_DPP	D3	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B12_DPN	B4	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 12. 100-Ω internal LVDS termination.
DDC_DIN_B12_DPP	C4	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B13_DPN	C3	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 13. 100-Ω internal LVDS termination.
DDC_DIN_B13_DPP	C2	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B14_DPN	A3	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 14. 100-Ω internal LVDS termination.
DDC_DIN_B14_DPP	A2	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_B15_DPN	B2	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data bit 15. 100-Ω internal LVDS termination.
DDC_DIN_B15_DPP	B1	LVDS_25_PI	-	DDC_DCLK_B	
DDC_DIN_C0_DPN	E20	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 0. 100-Ω internal LVDS termination.
DDC_DIN_C0_DPP	E21	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C1_DPN	F20	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 1. 100-Ω internal LVDS termination.
DDC_DIN_C1_DPP	G20	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C2_DPN	H19	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 2. 100-Ω internal LVDS termination.
DDC_DIN_C2_DPP	J19	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C3_DPN	E23	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 3. 100-Ω internal LVDS termination.
DDC_DIN_C3_DPP	E22	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C4_DPN	F23	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 4. 100-Ω internal LVDS termination.
DDC_DIN_C4_DPP	F22	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C5_DPN	G22	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 5. 100-Ω internal LVDS termination.
DDC_DIN_C5_DPP	G21	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C6_DPN	J20	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 6. 100-Ω internal LVDS termination.
DDC_DIN_C6_DPP	J21	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C7_DPN	H22	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 7. 100-Ω internal LVDS termination.
DDC_DIN_C7_DPP	H21	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C8_DPN	J23	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 8. 100-Ω internal LVDS termination.
DDC_DIN_C8_DPP	H23	LVDS_25_PI	-	DDC_DCLK_C	

Pin Functions (continued)

PIN		I/O TYPE	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
DDC_DIN_C9_DPN	K22	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 9. 100-Ω internal LVDS termination.
DDC_DIN_C9_DPP	K23	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C10_DPN	M19	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 10. 100-Ω internal LVDS termination.
DDC_DIN_C10_DPP	M20	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C11_DPN	M21	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 11. 100-Ω internal LVDS termination.
DDC_DIN_C11_DPP	M22	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C12_DPN	N19	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 12. 100-Ω internal LVDS termination.
DDC_DIN_C12_DPP	P19	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C13_DPN	N21	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 13. 100-Ω internal LVDS termination.
DDC_DIN_C13_DPP	N22	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C14_DPN	P20	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 14. 100-Ω internal LVDS termination.
DDC_DIN_C14_DPP	P21	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_C15_DPN	N23	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data bit 15. 100-Ω internal LVDS termination.
DDC_DIN_C15_DPP	P23	LVDS_25_PI	-	DDC_DCLK_C	
DDC_DIN_D0_DPN	T3	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 0. 100-Ω internal LVDS termination.
DDC_DIN_D0_DPP	R3	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D1_DPN	R5	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 1. 100-Ω internal LVDS termination.
DDC_DIN_D1_DPP	R6	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D2_DPN	R7	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 2. 100-Ω internal LVDS termination.
DDC_DIN_D2_DPP	P6	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D3_DPN	N3	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 3. 100-Ω internal LVDS termination.
DDC_DIN_D3_DPP	P3	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D4_DPN	P4	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 4. 100-Ω internal LVDS termination.
DDC_DIN_D4_DPP	P5	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D5_DPN	N6	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 5. 100-Ω internal LVDS termination.
DDC_DIN_D5_DPP	N7	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D6_DPN	N4	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 6. 100-Ω internal LVDS termination.
DDC_DIN_D6_DPP	M4	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D7_DPN	M7	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 7. 100-Ω internal LVDS termination.
DDC_DIN_D7_DPP	L7	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D8_DPN	K7	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 8. 100-Ω internal LVDS termination.
DDC_DIN_D8_DPP	K6	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D9_DPN	J4	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 9. 100-Ω internal LVDS termination.
DDC_DIN_D9_DPP	J5	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D10_DPN	H7	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 10. 100-Ω internal LVDS termination.
DDC_DIN_D10_DPP	J6	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D11_DPN	G4	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 11. 100-Ω internal LVDS termination.
DDC_DIN_D11_DPP	H4	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D12_DPN	G5	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 12. 100-Ω internal LVDS termination.
DDC_DIN_D12_DPP	H6	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D13_DPN	G7	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 13. 100-Ω internal LVDS termination.
DDC_DIN_D13_DPP	G6	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D14_DPN	F4	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 14. 100-Ω internal LVDS termination.
DDC_DIN_D14_DPP	F5	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DIN_D15_DPN	E5	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data bit 15. 100-Ω internal LVDS termination.
DDC_DIN_D15_DPP	E6	LVDS_25_PI	-	DDC_DCLK_D	
DDC_DOUT_A0_DPN	AE2	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 0 to DMD.
DDC_DOUT_A0_DPP	AF2	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A1_DPN	AD1	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 1 to DMD.
DDC_DOUT_A1_DPP	AE1	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A2_DPN	AC1	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 2 to DMD.
DDC_DOUT_A2_DPP	AC2	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A3_DPN	AB1	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 3 to DMD.
DDC_DOUT_A3_DPP	AB2	LVDS_25_PO	-	DDC_DCLKOUT_A	

Pin Functions (continued)

PIN		I/O TYPE	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
DDC_DOUT_A4_DPN	Y2	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 4 to DMD.
DDC_DOUT_A4_DPP	AA2	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A5_DPN	W1	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 5 to DMD.
DDC_DOUT_A5_DPP	Y1	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A6_DPN	V1	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 6 to DMD.
DDC_DOUT_A6_DPP	V2	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A7_DPN	U1	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 7 to DMD.
DDC_DOUT_A7_DPP	U2	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A8_DPN	R2	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 8 to DMD.
DDC_DOUT_A8_DPP	T2	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A9_DPN	N2	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 9 to DMD.
DDC_DOUT_A9_DPP	M2	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A10_DPN	K1	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 10 to DMD.
DDC_DOUT_A10_DPP	L2	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A11_DPN	K2	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 11 to DMD.
DDC_DOUT_A11_DPP	K3	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A12_DPN	J3	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 12 to DMD.
DDC_DOUT_A12_DPP	H3	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A13_DPN	H2	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 13 to DMD.
DDC_DOUT_A13_DPP	J1	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A14_DPN	H1	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 14 to DMD.
DDC_DOUT_A14_DPP	G1	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_A15_DPN	G2	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Data bit 15 to DMD.
DDC_DOUT_A15_DPP	F2	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_DOUT_B0_DPN	AE5	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 0 to DMD.
DDC_DOUT_B0_DPP	AE6	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B1_DPN	AD3	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 1 to DMD.
DDC_DOUT_B1_DPP	AD4	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B2_DPN	AD5	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 2 to DMD.
DDC_DOUT_B2_DPP	AD6	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B3_DPN	AC3	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 3 to DMD.
DDC_DOUT_B3_DPP	AC4	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B4_DPN	AB5	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 4 to DMD.
DDC_DOUT_B4_DPP	AB6	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B5_DPN	AB7	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 5 to DMD.
DDC_DOUT_B5_DPP	AC6	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B6_DPN	AA5	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 6 to DMD.
DDC_DOUT_B6_DPP	AA4	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B7_DPN	AA7	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 7 to DMD.
DDC_DOUT_B7_DPP	Y7	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B8_DPN	Y3	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 8 to DMD.
DDC_DOUT_B8_DPP	W3	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B9_DPN	W4	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 9 to DMD.
DDC_DOUT_B9_DPP	V4	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B10_DPN	W6	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 10 to DMD.
DDC_DOUT_B10_DPP	W5	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B11_DPN	V7	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 11 to DMD.
DDC_DOUT_B11_DPP	V6	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B12_DPN	U4	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 12 to DMD.
DDC_DOUT_B12_DPP	V3	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B13_DPN	T4	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 13 to DMD.
DDC_DOUT_B13_DPP	T5	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_B14_DPN	U6	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 14 to DMD.
DDC_DOUT_B14_DPP	U5	LVDS_25_PO	-	DDC_DCLKOUT_B	

Pin Functions (continued)

PIN		I/O TYPE	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
DDC_DOUT_B15_DPN	U7	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Data bit 15 to DMD.
DDC_DOUT_B15_DPP	T7	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_DOUT_C0_DPN	T22	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 0 to DMD.
DDC_DOUT_C0_DPP	T23	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C1_DPN	R20	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 1 to DMD.
DDC_DOUT_C1_DPP	R21	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C2_DPN	T19	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 2 to DMD.
DDC_DOUT_C2_DPP	T20	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C3_DPN	U21	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 3 to DMD.
DDC_DOUT_C3_DPP	U22	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C4_DPN	U20	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 4 to DMD.
DDC_DOUT_C4_DPP	U19	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C5_DPN	V23	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 5 to DMD.
DDC_DOUT_C5_DPP	V24	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C6_DPN	V22	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 6 to DMD.
DDC_DOUT_C6_DPP	V21	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C7_DPN	W19	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 7 to DMD.
DDC_DOUT_C7_DPP	V19	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C8_DPN	W23	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 8 to DMD.
DDC_DOUT_C8_DPP	W24	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C9_DPN	Y22	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 9 to DMD.
DDC_DOUT_C9_DPP	Y23	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C10_DPN	Y20	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 10 to DMD.
DDC_DOUT_C10_DPP	Y21	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C11_DPN	AA24	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 11 to DMD.
DDC_DOUT_C11_DPP	AA23	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C12_DPN	AA19	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 12 to DMD.
DDC_DOUT_C12_DPP	AA20	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C13_DPN	AC24	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 13 to DMD.
DDC_DOUT_C13_DPP	AB24	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C14_DPN	AC19	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 14 to DMD.
DDC_DOUT_C14_DPP	AD19	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_C15_DPN	AC22	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Data bit 15 to DMD.
DDC_DOUT_C15_DPP	AC23	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_DOUT_D0_DPN	AB26	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 0 to DMD.
DDC_DOUT_D0_DPP	AC26	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D1_DPN	AA25	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 1 to DMD.
DDC_DOUT_D1_DPP	AB25	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D2_DPN	Y26	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 2 to DMD.
DDC_DOUT_D2_DPP	Y25	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D3_DPN	W26	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 3 to DMD.
DDC_DOUT_D3_DPP	W25	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D4_DPN	U26	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 4 to DMD.
DDC_DOUT_D4_DPP	V26	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D5_DPN	U25	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 5 to DMD.
DDC_DOUT_D5_DPP	U24	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D6_DPN	T25	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 6 to DMD.
DDC_DOUT_D6_DPP	T24	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D7_DPN	R26	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 7 to DMD.
DDC_DOUT_D7_DPP	R25	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D8_DPN	P24	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 8 to DMD.
DDC_DOUT_D8_DPP	P25	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D9_DPN	N24	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 9 to DMD.
DDC_DOUT_D9_DPP	M24	LVDS_25_PO	-	DDC_DCLKOUT_D	

Pin Functions (continued)

PIN		I/O TYPE	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
DDC_DOUT_D10_DPN	L25	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 10 to DMD.
DDC_DOUT_D10_DPP	L24	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D11_DPN	K26	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 11 to DMD.
DDC_DOUT_D11_DPP	K25	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D12_DPN	J26	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 12 to DMD.
DDC_DOUT_D12_DPP	J25	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D13_DPN	J24	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 13 to DMD.
DDC_DOUT_D13_DPP	H24	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D14_DPN	H26	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 14 to DMD.
DDC_DOUT_D14_DPP	G26	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_DOUT_D15_DPN	G25	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Data bit 15 to DMD.
DDC_DOUT_D15_DPP	G24	LVDS_25_PO	-	DDC_DCLKOUT_D	
DDC_SCTRL_AN	R1	LVDS_25_NO	-	DDC_DCLKOUT_A	Output Bus A Serial Control to DMD.
DDC_SCTRL_AP	P1	LVDS_25_PO	-	DDC_DCLKOUT_A	
DDC_SCTRL_BN	AA3	LVDS_25_NO	-	DDC_DCLKOUT_B	Output Bus B Serial Control to DMD.
DDC_SCTRL_BP	AB4	LVDS_25_PO	-	DDC_DCLKOUT_B	
DDC_SCTRL_CN	W20	LVDS_25_NO	-	DDC_DCLKOUT_C	Output Bus C Serial Control to DMD.
DDC_SCTRL_CP	W21	LVDS_25_PO	-	DDC_DCLKOUT_C	
DDC_SCTRL_DN	N26	LVDS_25_NO	-	DDC_DCLKOUT_D	Output Bus D Serial Control to DMD.
DDC_SCTRL_DP	P26	LVDS_25_PO	-	DDC_DCLKOUT_D	
DVALID_A_DPN	D20	LVDS_25_NI	-	DDC_DCLK_A	Input Bus A Data Valid Signal. 100-Ω internal LVDS termination.
DVALID_A_DPP	D21	LVDS_25_PI	-	DDC_DCLK_A	
DVALID_B_DPN	C8	LVDS_25_NI	-	DDC_DCLK_B	Input Bus B Data Valid Signal. 100-Ω internal LVDS termination.
DVALID_B_DPP	D8	LVDS_25_PI	-	DDC_DCLK_B	
DVALID_C_DPN	L19	LVDS_25_NI	-	DDC_DCLK_C	Input Bus C Data Valid Signal. 100-Ω internal LVDS termination.
DVALID_C_DPP	L20	LVDS_25_PI	-	DDC_DCLK_C	
DVALID_D_DPN	L3	LVDS_25_NI	-	DDC_DCLK_D	Input Bus D Data Valid Signal. 100-Ω internal LVDS termination.
DVALID_D_DPP	L4	LVDS_25_PI	-	DDC_DCLK_D	
DDC_VERSION_0	F18	LVCMOS25_O	Hi	-	DLPC910 Firmware Rev Number bit 0
DDC_VERSION_1	G17	LVCMOS25_O	Hi	-	DLPC910 Firmware Rev Number bit 1
DDC_VERSION_2	H18	LVCMOS25_O	Hi	-	DLPC910 Firmware Rev Number bit 2
SPEED_SEL_0	H8	LVCMOS25_I	Hi	-	Speed_Sel[1:0] = 00 400Mhz = 01 480Mhz = 10, 11 Reserved Includes internal pull-ups.
SPEED_SEL_1	H9	LVCMOS25_I	Hi	-	
VSP_ENABLE	E8	LVCMOS25_I	Hi	-	Reserved. Do not connect. Includes internal pull-up.
ECP2_FINISHED	E25	LVCMOS25_O	Hi	-	DLPR910 Initialization complete. Connected to LED.
VLED0	AA17	LVCMOS25_O	Hi = On	-	Power Indicator LED Output.
VLED1	AB17	LVCMOS25_O	Hi = On	-	Heartbeat Indicator LED Output.
WDT_ENBLZ	F25	LVCMOS25_I	Lo	-	DMD Reset Pulse Watchdog Timer Enable
PWR_FLOAT	G9	LVCMOS25_I	Hi	-	Park DMD mirrors.
NS_FLIP	F19	LVCMOS25_I	Hi	-	Top/Bottom image flip on DMD
COMP_DATA	G19	LVCMOS25_I	Hi	DDC_DCLK_[A,B,C,D]	Compliment Data (0 <--> 1)
INIT_ACTIVE	E26	LVCMOS25_O	Hi	-	DLPC910 Initialization Routine Active
RST_ACTIVE	G10	LVCMOS25_O	Hi	-	DMD Mirror Clocking Pulse in progress
RST2BLKZ	E18	LVCMOS25_I	Hi	-	Dual and Quad Block control
TST_PT_0	Y12	LVCMOS33_O	-	-	No connect. For access to test point output route to test via.
TST_PT_1	AA12	LVCMOS33_O	-	-	No connect. For access to test point output route to test via.
TST_PT_2	Y13	LVCMOS33_O	-	-	No connect. For access to test point output route to test via.
TST_PT_3	AA13	LVCMOS33_O	-	-	No connect. For access to test point output route to test via.

Pin Functions (continued)

PIN		I/O TYPE	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
TST_PT_4	AA14	LVCMOS33_O	-	-	No connect. For access to test point output route to test via.
TST_PT_5	AB14	LVCMOS33_O	-	-	No connect. For access to test point output route to test via.
TST_PT_6	AA15	LVCMOS33_O	-	-	No connect. For access to test point output route to test via.
TST_PT_7	AB15	LVCMOS33_O	-	-	No connect. For access to test point output route to test via.
TST_PT_8	C1	LVCMOS25_O	-	-	No connect. For access to test point output route to test via.
TST_PT_9	D1	LVCMOS25_O	-	-	No connect. For access to test point output route to test via.
TST_PT_10	E1	LVCMOS25_O	-	-	No connect. For access to test point output route to test via.
TST_PT_11	E2	LVCMOS25_O	-	-	No connect. For access to test point output route to test via.
TST_PT_12	E3	LVCMOS25_O	-	-	No connect. For access to test point output route to test via.
TST_PT_13	F3	LVCMOS25_O	-	-	No connect. For access to test point output route to test via.
TST_PT_14	E7	LVCMOS25_O	-	-	No connect. For access to test point output route to test via.
TST_PT_15	F7	LVCMOS25_O	-	-	No connect. For access to test point output route to test via.
DLPC_VRN_BANK4	AB12	DCI Reference Voltage	-	-	**Requires an external 49.9-Ω pull-up resistor to 3.3 V**.
DLPC_VRP_BANK4	AC11	DCI Reference Voltage	-	-	**Requires an external 49.9-Ω pull-down resistor to GND**.
LOAD4_ENZ	D25	LVCMOS33_I	Lo	-	Signal enables the Load-4 functionality of the DLP9000XFLS. Includes internal pull-up.
DMD_IRQ	D26	LVCMOS33_O	Hi	-	Signal indicates a DMD voltage is inactive. Includes internal pull-up
DLPC_VBATT	K18	LVCMOS33_I	-	-	DLPC910 VBATT reference. Connect to GND.
DLPC_DONE	K10	LVCOMS33_O	-	-	DLPC910 Initialization configuration complete. Connect to DLPR910 CEZ pin. **Requires 4.7-kΩ pull-up to 3.3 V**.
DLPC_HSWAPEN	L18	LVCMOS33_I	-	-	DLPC910 Configuration. **Requires 4.7-kΩ pull-up to 3.3 V**.
DDC_M0	W18	LVCMOS33_I	-	-	DLPC910 Configuration. Connect to GND
DDC_M1	Y17	LVCMOS33_I	-	-	DLPC910 Configuration. Connect to GND
DDC_M2	V18	LVCMOS33_I	-	-	DLPC910 Configuration. Connect to GND
INTB_DDC	J11	LVCMOS25_O	Hi	-	DLPC910 Configuration. Connect to DLPR910 OE/RESET. **Requires 4.7-kΩ pull-up to 3.3 V**.
PROGB_DDC	J18	LVCMOS25_O	Hi	-	DLPC910 Configuration. Connect to DLPR910 CF. **Requires 4.7-kΩ pull-up to 3.3 V**.
PROM_CCK_DDC	J10	LVCMOS25_O	-	PROM_CCK_DDC	Configuration PROM Clock. Connect to DLPR910 CLK. **Connects to center of voltage divider (100/100-Ω 3.3 V and GND)**.
PROM_D0_DDC	K11	LVCMOS25_I	-	PROM_CCK_DDC	Configuration PROM Data in. Connected to DLPR910 Data 0 (D0)
RDWR_B	P18	LVCMOS25_I	-	-	DLPC910 Configuration. **Requires 1-kΩ pull-down to ground**.
TCK_JTAG	U11	LVCMOS33_I	-	TCK_JTAG	JTAG Clock. Connects to DLPC910, DLPR910, and JTAG header TCK (if user has JTAG they must build their chain accordingly)
TDO_DDC	W10	LVCMOS33_O	-	TCK_JTAG	JTAG Data out of DLPC910. Connects to JTAG return TDO on JTAG header
TDO_XCF16DDC	V11	LVCMOS33_I	-	TCK_JTAG	JTAG Data out of DLPR910 to DLPC910. Connects to DLPR910 TDO (DLPC910 internal signal TDI_0)

Pin Functions (continued)

PIN		I/O TYPE	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
TMS_JTAG	V12	LVCMOS33_I	Hi	TCK_JTAG	JTAG. Connects to DLPC910, DLPR910, and JTAG header TMS
VCCAUX	J8, K17, L8, M17, N8, P17, R8, T17, U8, V17, W8, W16	PWR	-	-	Aux Power. VCC_2P5V
VCCINT	H15, J12, J14, J16, K9, K13, K15, L10, L12, L14, L16, M9, M11, M15, N10, N12, N16, P9, P11, P15, R10, R12, R16, T9, T11, T13, T15, U10, U12, U14, U16, V9, V13, V15, W14, Y15	PWR	-	-	Power. VCC_1P0V
VCCO_0	Y9, W12	PWR	-	-	Power. VCC_3P3V
VCCO_2	AA16, AD17	PWR			
VCCO_4	AB13, AC10	PWR	-	-	
VCCO_1	C10, F11	PWR	-	-	Power. VCC_2P5V
VCCO_3	D17, E14	PWR	-	-	
VCCO_11	F21, H25, J22	PWR	-	-	
VCCO_12	H5, J2, L6	PWR	-	-	
VCCO_13	M23, N20, R24	PWR	-	-	
VCCO_14	R4, V5, W2	PWR	-	-	
VCCO_15	B23,C20, E24	PWR	-	-	
VCCO_16	D7, E4, G8	PWR	-	-	
VCCO_17	T21, V25, W22	PWR	-	-	
VCCO_18	AA6, AB3, AD7	PWR	-	-	
VCCO_21	AC20, AB23, AE24	PWR	-	-	
GND	A1, A6, A11, A16, A21, A26, AA1, AA11, AA21, AA26, AB8, AB18, AC5, AC15, AC25, AD2, AD12, AD22, AE4, AE9, AE14, AE19, AF1, AF6, AF11, AF16, AF21, AF26, B3, B8, B13, B18, C5, C15, C25, D2, D12, D22, E9, E19, F1, F6, F16, F26, G3, G13, G18, G23, H10, H20, J7, J9, J13, J15, J17, K4, K8, K12, K14, K16, K19, K24, L1, L9, L11, L13, L15, L17, L21, L26, M3, M8, M10, M12, M16, M18, N5, N9, N11, N15, N17, N25, P2, P7, P8, P10, P12, P16, P22, R9, R11, R15, R17, R19, T1, T6, T8, T10, T12, T14, T16, T26, U3, U9, U13, U15, U17, U18, U23, V8, V10, V14, V16, V20, W7, W9, W13, W15, W17, Y4, Y14, Y16, Y19, Y24, M13, M14, N13, N14, P13, P14, R13, R14, N18, R18, T18	GND	-	-	
RESERVED_AC12	AC12	LVCMOS33_O	-	-	Route to via for access to pin output.
RESERVED_AD11	AD11	LVCMOS33_O	-	-	Route to via for access to pin output.
RESERVED_AA9	AA9	LVCMOS33_I	-	-	Includes internal pull-up
RESERVED_Y10	Y10	LVCMOS33_I	-	-	Includes internal pull-up
RESERVED_Y11	Y11	LVCMOS33_I	-	-	Includes internal pull-up
RESERVED_AB11	AB11	LVCMOS33_I	-	-	Includes internal pull-up
RESERVED_F10	F10	LVCMOS33_I	-	-	Includes internal pull-up
RESERVED_F8	F8	LVCMOS33_I	-	-	Includes internal pull-up
UNUSED	AD9, AD16, AD20, AD21, AD23, AD24, AD25, AD26, AE7, AE8, AE10, AE11, AE12, AE13, AE15, AE16, AE17, AE18, AE20, AE21, AE22, AE23, AE25, AE26, AF7, AF8, AF9, AF10, AF12, AF13, AF14, AF15, AF17, AF18, AF19, AF20, AF22, AF23, AF24, AF25	NC	-	-	No Connection. Unused Pins. (listed as Xilinx® NC0 - NC42)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
ELECTRICAL					
V_{CCINT}	Supply voltage range (2)		–0.50	1.1	V
V_{CCO}			–0.50	3.75	
V_{CCAUX}			–0.50	3.0	
V_I	Input voltage range (3)	3.3 V	–0.95	4.05	V
		2.5 V	–0.75	V_{CCO} + 0.50	
V_O	Output voltage range (4)	3.3 V	–0.30	V_{CCO} – 0.40	V
		2.5 V	–0.30	V_{CCO} – 0.40	
ENVIRONMENTAL					
T_J	Junction temperature			125	°C
T_{stg}	Storage temperature (ambient)		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Applies to external input and bidirectional buffers.
(4) Applies to external output and bidirectional buffers.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	± 2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	± 1500	

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
ELECTRICAL						
V_{CCINT}	1-V supply voltage, core logic		0.95	1.00	1.05	V
V_{CCO}	2.5-V supply voltage, I/O for VCCO_1,3,11,12,13,14,15,16,17,18,21		1.14	2.50	3.45	V
V_{CCO}	3.3-V supply voltage, I/O for VCCO_0,2,4		3.0	3.30	3.45	V
V_{CCAUX}	2.5-V supply voltage, I/O		2.375	2.500	2.625	V
V_I	Input voltage	3.3-V DCI and CMOS for VCCO_0,2,4	0		V_{CCO}	V
		2. 5-V CMOS for VCCO_1,3,11,12,13,14,15,16,17,18,21	0		V_{CCO}	
		2.5-V LVDS	0.3		2.2	
V_O	Output voltage	3.3-V DCI and CMOS for VCCO_0,2,4	0		V_{CCO}	V
		2.5-V CMOS for VCCO_1,3,11,12,13,14,15,16,17,18,21	0		V_{CCO}	
		2.5-V LVDS	0.825		1.675	
T_A	Operating ambient temperature		0		85	°C
ENVIRONMENTAL						
P_D	Continuous total power dissipation				6	W

6.4 Thermal Information

THERMAL METRIC (1)		DLPC910 ZYR (FCBGA) 676 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	12.1	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	3.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	0.19	°C/W

(1) Refer to the XC5VLX30 product specifications at www.xilinx.com for complete thermal specifications.
(2) In still air.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	3.3-V CMOS	2.0			V
V_{IL}	Low-level input voltage	3.3-V CMOS			0.8	V
V_{OH}	High-level output voltage	3.3-V DCI and CMOS	2.9			V
V_{OL}	Low-level output voltage	3.3-V DCI and CMOS			0.4	V
V_{IH}	High-level input voltage	2.5-V CMOS	1.7			V
V_{IL}	Low-level input voltage	2.5-V CMOS			0.7	V
V_{OH}	High-level output voltage	2.5-V interface	V_{CCO} – 0.4			V
		2.5-V LVDS		1.38		
V_{OL}	Low-level output voltage	2.5-V interface			0.4	V
		2.5-V LVDS		1.03		
C_I	Input capacitance	2.5-V interface		8		pF
		2.5-V LVDS		8		
I_{CCINT}	Supply voltage range, core supply			1.4		mA
I_{CCO}	Supply voltage range, I/O supply			4.2		mA

6.6 Timing Requirements

(see (1))

				MIN	NOM	MAX	UNIT
f_{cd}	Clock frequency, DCLKIN_n (2)		f_{cd} = 400 MHz			400	MHz
			f_{cd} = 480 MHz			480	
f_{cr}	Clock frequency, CLK_R				50		MHz
t_c	Cycle time, DCLKIN_n		f_{cd} = 400 MHz			2.5	ns
			f_{cd} = 480 MHz			2.083	
$t_{w(H)}$	Pulse duration, high	50% to 50% reference points (signal)	f_{cd} = 400 MHz			1.25	ns
			f_{cd} = 480 MHz			1.042	
$t_{w(L)}$	Pulse duration, low	50% to 50% reference points (signal)	f_{cd} = 400 MHz			1.25	ns
			f_{cd} = 480 MHz			1.042	
t_t	Transition time, tt = tf /tr	20% to 80% reference points (signal)	f_{cd} = 400 MHz			0.6	ns
			f_{cd} = 480 MHz			0.5	
t_{jp}	Period Jitter DCLKIN_n (3)				100		ps

(1) It is recommended that the COMP_DATA, NS_FLIP and RST2BLKZ flags be set to one value and not adjusted during normal system operation.
(2) Preferred DDC_DCLK _n duty cycle = 50%
(3) This is the deviation in period from ideal period due solely to high frequency jitter.

Timing Requirements (continued)

(see (1))

				MIN	NOM	MAX	UNIT
t_{sk}	Skew, DIN_A(15-0) to DCLKIN_A			-100		100	ps
	Skew, DIN_B(15-0) to DCLKIN_B			-100		100	
	Skew, DIN_C(15-0) to DCLKIN_C			-100		100	
	Skew, DIN_D(15-0) to DCLKIN_D			-100		100	
	Skew, DVALID_n to DCLKIN_n↑			-100		100	
	Skew, BLK_MD BLK_AD to DCLKIN_n↑ (4)			-100		100	
	Skew, ROWMD or ROWAD to DCLKIN_n↑ (4)			-100		100	
	Skew, STEPVCC to DCLKIN↑ (4)			-100		100	

(4) First edge of DDC_DIN*, ROW*, and BLK* should be synchronous to DVALID rising edge.

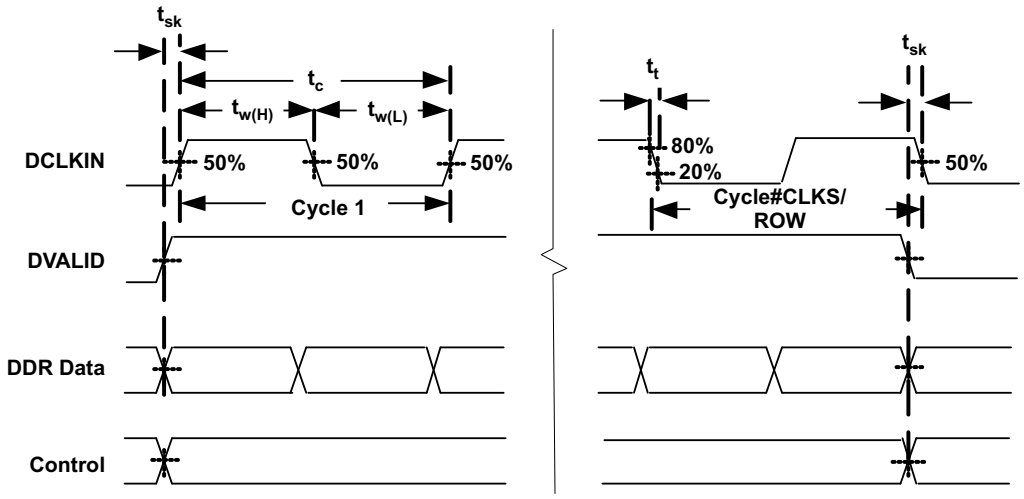


Figure 1. Input Interface Timing

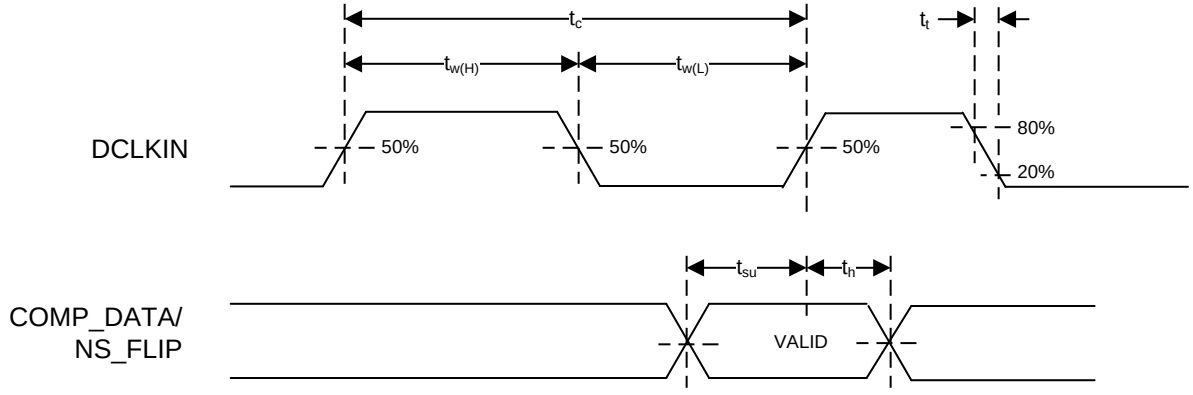


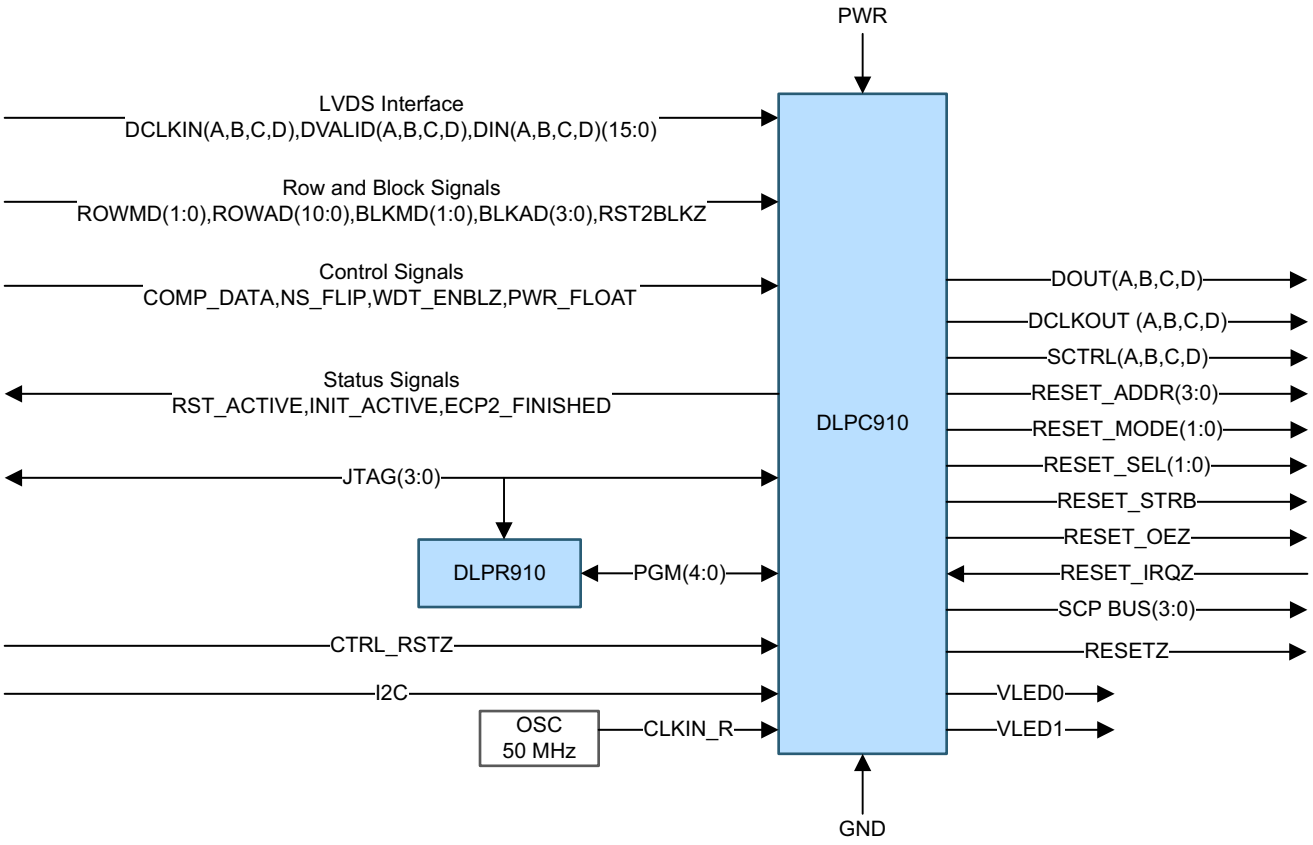
Figure 2. Control Timing

7 Detailed Description

7.1 Overview

The DLPC910 digital controller provides a reliable high speed data pipe to the DMD, where the digital input on the LVDS interface is configured for the required timing requirements of the DMD. The DMD reflects light by using 1-bit binary encoded patterns, where each mirror is a pixel-to-mirror mapping of the pattern.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input LVDS Interface

The data input interface consists of four input data buses: DDC_DIN_A, DDC_DIN_B, DDC_DIN_C, and DDC_DIN_D. Each bus contains 16 differential pairs which are synchronous to the rising and falling edges of its associated DDC_DCLK signal.

7.3.2 Data Clock

The data clock interface consists of four differential pairs: DDC_DCLK_A, DDC_DCLK_B, DDC_DCLK_C, and DDC_DCLK_D. Each must operate continuously. All signals associated with the data clock should be synchronous to these signals. For example, DDC_DIN_A and DVALID_A should be synchronous to the rising edge of DDC_DCLK_A. This clock should be valid prior to releasing CTRL_RSTZ. DDC_DCLK is a DDR clock with data loaded on both rising and falling edges of DDC_DCLK. The jitter on this clock is specified in *Timing Requirements*.

Feature Description (continued)

7.3.3 Data Valid

The data valid interface consists of four differential pairs: DVALID_A, DVALID _B, DVALID _C, and DVALID _D. The DVALID signal should be asserted synchronous to the data it is meant to frame. DVALID can be asserted as:

- Framing individual row loads with breaks between rows, or
- Framing block loads - for example, the DLP9000XFLS with 16 blocks allows framing 100 contiguous row loads, or
- Framing the entire DMD load where the DVALID stays active for all DMD row loads with zero invalid data between rows.

If the DVALID frames DMD blocks or the entire DMD, assure that the block and row control signals are adjusted at the proper locations in the data stream. Refer to *Block Mode Operation* for further information.

7.3.4 Interface Training

The DLPC910 detects the phase differences between the ½ speed clock (used in the device driving the LVDS data) and the internally generated ½ speed data clocks to select a clock phase for data capture. This is done by supplying a simple repeating pattern on all of the data inputs while the INIT_ACTIVE output of the DLPC910 is high/active. The details of the training pattern are described below.

Figure 3 shows a simple block diagram of the training pattern insertion logic.

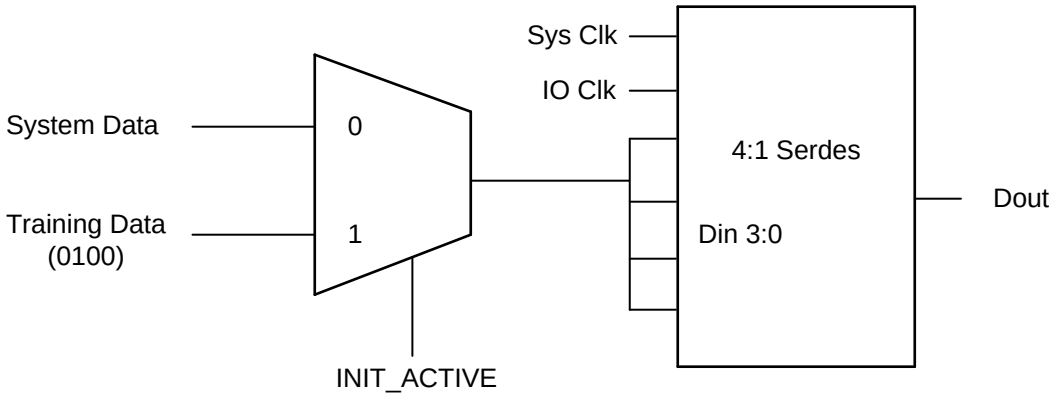


Figure 3. Block Diagram of Training Pattern Logic

The expected training pattern is 0100. In Figure 4, the data input to the 4:1 SERDES cells is captured on the rising edge of the ½ speed system clock. The output latency shown is based on the documentation for the Xilinx SERDES cells. Individual implementation may vary depending on the type of cells, technology, and design technique used.

Feature Description (continued)

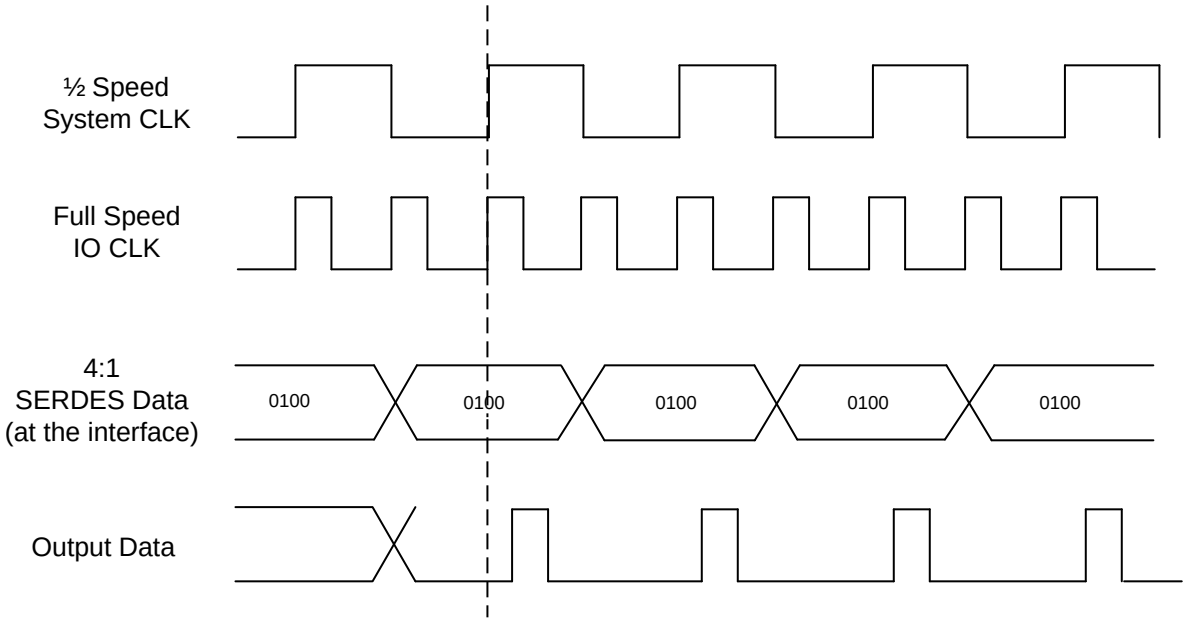


Figure 4. Training Pattern Alignment

NOTE

In Xilinx FPGAs (due to the construction of the ISERDES and OSERDES cells) a pattern of *0010* needs to be applied to the output/transmitting SERDES cells data pins (D1 = 0, D2 = 0, D3 = 1, D4 = 0) in order to receive a result of *0100* (Q1 = 0, Q2 = 1, Q3 = 0, Q4 = 0) at the input/receiving SERDES cell.

The patterns should be applied on all of the data and DVALID pins. In this respect, the interface is treated as a 17 bit interface with DVALID being the 17th data bit. The receiving logic in the DLPC910 adjusts the clock phase until the correct pattern is seen at the inputs. This allows DLPC910 to correctly select a clock phase for data capture and will contribute to a more robust interface. It is important that the training pattern is applied to the DVALID and data inputs of the DLPC910 before reset to the device is de-asserted, as training commences immediately on the de-assertion of reset. The INIT_ACTIVE signal is asserted while the device is held in reset in order to help facilitate this behavior.

7.3.5 Row and Block Interface

7.3.5.1 Row Mode

The DMD incorporates single row write operations using a row address counter that is randomly addressable. ROWMD(1:0) determines the single row write count mode and ROWAD(10:0) determines the single row write address. ROWMD and ROWAD must be asserted and de-asserted synchronously with DVALID. Row address orientation depends on the North or South Flip Flag (NS_FLIP) input to the DLPC910. Refer to *相关文档* for the DMD datasheet regarding orientation of rows, columns, and *Mirror Clocking Pulse* (MCP) blocks. The row address counter does not automatically wrap-around when using the increment row address pointer instruction. After the final row is addressed, the row address pointer must be cleared to 0.

7.3.5.2 Block Mode

The signals RST2BLKZ, BLK_MD and BLK_AD are used to designate which mirror block(s) is to be issued a MCP or a Block Clear.

Feature Description (continued)

7.3.6 Control Interface

7.3.6.1 Complement Data

By setting the COMP_DATA input high (logic *1*), the user is able to command the DMD to internally complement its data inputs prior to loading the data into the mirror array. At least 0.6 ms is needed for the signal to be loaded. This signal should not be used to invert data on a row basis. When used with the *Clear* command, the mirrors are still set to zero regardless of the COMP_DATA bit. The COMP_DATA signal should be kept low during initialization to ensure proper setup of the system.

7.3.6.2 North South Flip

The NS_FLIP signal allows the user to specify the loading direction of rows in the DMD when used with ROWMD = 01. This control has no effect if ROWMD = 10. Table 1 and Table 2 describe the effect of N/S flip. If NS_FLIP is set, this does not reverse the direction of MCP groups. For example, the normal case is to MCP blocks 0 – 15 in order. When NS_FLIP is set, the order of block MCPs must be reversed to 15 – 0. The NS_FLIP signal should be kept low during initialization to ensure proper setup of the system.

Table 1. Row Write Modes - N/S Flip Flag = 0

ROW MD		ROWAD											ACTION
1	0	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	None
0	1	0	0	0	0	0	0	0	0	0	0	0	Increment row address pointer and write the concurrent data into that row
1	0	R	R	R	R	R	R	R	R	R	R	R	Set row address pointer to R and write the concurrent data into that row.
1	1	0	0	0	0	0	0	0	0	0	0	0	Clear row address pointer to 0 and write concurrent data into first row (that is, row *0*).

Table 2. Row Write Modes - N/S Flip Flag = 1

ROW MD		ROWAD											ACTION
1	0	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	None
0	1	0	0	0	0	0	0	0	0	0	0	0	Decrement the row address pointer and write the concurrent data into that row
1	0	R	R	R	R	R	R	R	R	R	R	R	Set the row address pointer to R and write the concurrent data into that row.
1	1	0	0	0	0	0	0	0	0	0	0	0	Set row address pointer to row = last row and write concurrent data into last row (that is, the last row = 1599).

7.3.6.3 Watchdog

The DLPC910 contains a watchdog timer that initiates a global DMD MCP in the event that any DMD reset block has not received a MCP within 10 seconds. This auto-MCP function can be disabled by asserting WDT_ENBLZ high. Disabling the watchdog is not recommended unless the user ensures that a MCP to the entire DMD occurs within 10 seconds. During the time when the DLPC910 is in idle mode or is not operating, it is recommended to exercise the DMD mirrors by continuously loading alternating all-on/all-off patterns.

7.3.6.4 DMD Power Down

For correct power down operation of the DMD, the following power down procedure must be executed.

Prior to power removal, assert PWR_FLOAT and allow approximately 300 µs for the procedure to complete. This procedure will assure the mirrors are in a flat state. Following this procedure, the power can be safely removed. To restart after assertion of PWR_FLOAT, the DLPC910 must be reset by setting CTRL_RSTZ low (logic *0*) for 50ms, and then back to high (logic *1*), or power to the DLPC910 must be cycled.

To avoid leaving a static image on the DMD without removing power, a mirror FLOAT operation can be issued to the DMD. A mirror FLOAT sequence begins by asserting the proper BLK_MD and BLK_AD as described in Table 5. During the following row cycle, the DMD releases the tension under each mirror so that all mirrors are in a relatively flat position. The FLOAT operation takes approximately 300 µs to complete, during which time RST_ACTIVE is asserted. Normal operation may then continue without reseting or cycling power to the DLPC910 or the DMD.

7.3.6.5 Load4

Load4 functionality provides improved global binary pattern rates for applications that can trade diminished vertical resolution for higher pattern rates. Examples of these types of applications are shutter or chopper applications and vertical structured light patterns. Asserting LOAD4_ENZ causes the attached DMD to load 4 rows for every row of data sent, reducing the pattern load time to ¼ of a full DMD load. It does not reduce the MCP timing.

7.3.6.5.1 Load4 Row Addressing

In Load4 mode, automatic increment mode and row address mode can still be used as before, however the largest addressable row will be (1600/4) - 1 = 399. The addressable vertical resolution is reduced by four, although the physical resolution is unchanged.

Automatic increment address mode will automatically increment the row address input by one (or decrement by one for N/S flip). The row address input will be re-mapped as shown in Table 3, where Vres = the vertical resolution of the DMD.

Table 3. Load4 Row Address Mapping

ROW ADDRESS INPUT	PHYSICAL ROWS LOADED ON DMD
0	0, 1, 2, 3
1	4, 5, 6, 7
2	8, 9, 10, 11
3	12, 13, 14, 15
N	4N, 4N+1, 4N+2, 4N+3
(VRes/4) -1	VRes-4, VRes-3, VRes-2, VRes-1

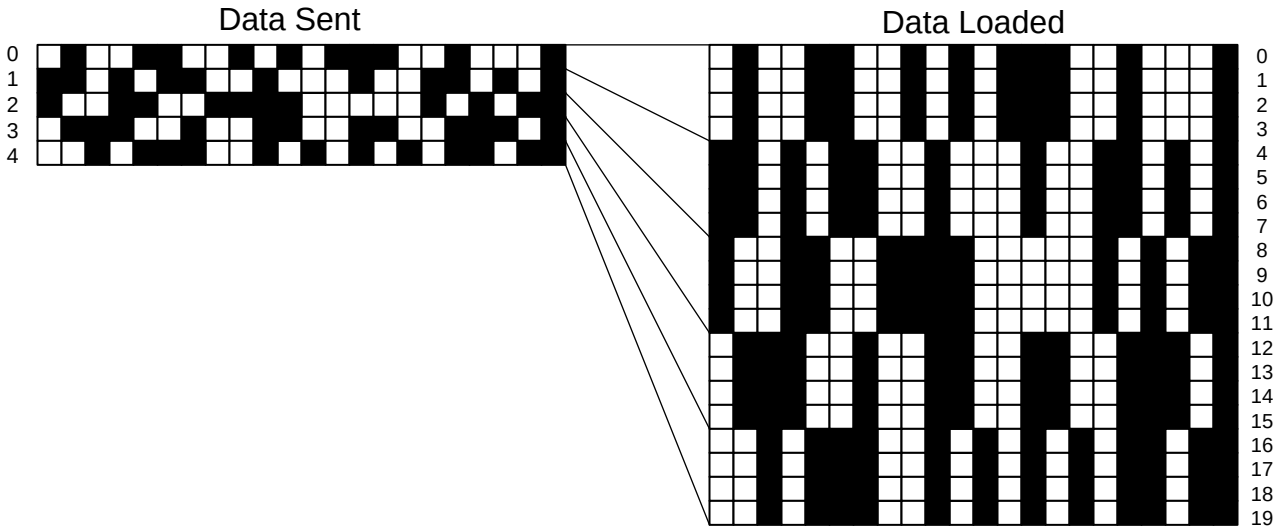


Figure 5. Example Load4 Row Address Mapping

7.3.6.5.2 Load4 Block Clears

While Load4 is enabled, Block Clear requests will be ignored. To load using Load4 followed by Block Clear request(s), simply de-assert LOAD4_ENZ at the beginning of the MCP request(s) preceding the Block Clear request(s). Re-assert LOAD4_ENZ at the beginning of the MCP request(s) preceding the next desired Load4 operation. This will ensure that the DLPC910 controller has sufficient time to disable or enable LOAD4_ENZ before data is loaded or Block Clear(s) are requested. Refer to *Block Clear* regarding block clear operation.

7.3.7 Status Interface

7.3.7.1 ECP2 Finished

When power is applied, the ECP2_FINISHED signal goes high to indicate the DLPC910 has completed loading the configuration from the DLPR910 prom.

7.3.7.2 Initialization Active

The initialization active signal INIT_ACTIVE indicates that the DMD and the DLPC910 digital controller are in an initialization state after power is applied. During this initialization period, the DLPC910 is calibrating the data interface, and initializing the DMD by setting all internal registers to their correct states. Monitoring the INIT_ACTIVE signal should not begin until ECP2_FINISHED goes high. When this signal goes low, the system has completed initialization. System initialization takes approximately 4 ms to complete. Data and command write cycles must not be asserted during the initialization. This signal is driven by a CLK_R register and should be considered an asynchronous signal. Standard synchronization techniques should be applied if monitoring this signal with a synchronous circuit clocked by a clock other than CLK_R. After initialization is complete, a delay of at least 64 clocks should be observed before the first DVALID is asserted (to ensure a clean start up process).

NOTE

The RST2BLKZ, COMP_DATA, and NS_FLIP signals should be kept low during initialization to ensure proper setup of the system.

7.3.7.3 Reset Active

The reset active signal RST_ACTIVE goes high for approximately 4 µs, indicating a MCP operation is in progress. During this time, no additional MCPs will be accepted by the DLPC910 until RST_ACTIVE returns low. RST_ACTIVE does not return to low unless continuous no-op or data loading row cycles are issued.

After PWR_FLOAT is asserted, a Mirror Clocking Pulse is issued, or a mirror Float operation is requested, RST_ACTIVE is asserted to indicate that the operation is in progress. Each RST_ACTIVE pulse applies to one or more MCPs depending on the reset block operation chosen from Table 5. RST_ACTIVE is synchronized to an internal version of DDC_DCLK. As such, circuits in the application FPGA should consider this signal asynchronous and use standard synchronization techniques to assure reliable registering of this signal.

7.3.7.4 DMD_IRQ

The DMD_IRQ signal indicates a DMD power fault of one of the bias, offset, or reset power supplies. If the customer interface wishes to monitor this signal, it must first be enabled in the *DESTOP_INTERRUPT Register*. The cause of the fault should be determined and resolved prior to a system reset to continue operation. The customer interface can also monitor this event by polling the *DESTOP_INTERRUPT Register* via the I^2C interface.

7.3.7.5 LED Indicators

7.3.7.5.1 VLED0

The VLED0 signal is typically connected to an LED to show that the DLPC910 is operating normally. The signal is 1 Hz with 50% duty cycle, otherwise known as the heartbeat.

7.3.7.5.2 VLED1

The VLED1 signal is typically connected to an LED indicator to show the status of system initialization and the status of the clock circuits. The VLED1 signal is asserted only when system initialization is complete and clock circuits are initialized. Logically, these signals are ANDed together to show an indication of the health of the system. If the Phase Locked Loop (PLL) connected to the data clock and the DMD clock are functioning correctly after system initialization, the LED will be illuminated.

7.3.8 Reset and System Clock

7.3.8.1 Controller Reset

The controller reset input CTRL_RSTZ is an active low, asynchronous reset. This reset can be sourced from a voltage supervisor or from the customer interface. Users should note that the chipset will not operate correctly if all DLPC910 power supplies are not in range at the time this reset is released.

7.3.8.2 Main Oscillator Clock

The reference clock, CLKIN_R, supplied from an oscillator must be 50MHz. This is required for the precise timing used to perform the DMD MCP. This clock should be valid prior to releasing CTRL_RSTZ.

7.3.9 I^2C Interface

The I^2C interface is compliant to I^2C specification version 1.0 – 1995, and operates between 100 kHz and 400 kHz clock rate. The interface allows the user to set controller configuration and provides status information such as:

- Controller and DMD identification
- DMD Type
- Versions
- Controller operating status
- Controller operating modes

Each I^2C clock and data I/O requires an external 1K-Ω pull-up resistor to 3.3 V. Depending on the speed that is selected and the loading of the interface, a different pull-up resistor may be required.

7.3.9.1 Configuration Pins

The DDC_IIC_ADDR_SEL input signal allows the user to select the DLPC910 I^2C slave address. When this pin is low, the slave address is 0x34 and when high the slave address is 0x36. If pin is left unconnected, the default slave address is 0x36.

The DDC_IIC_SCL is the master controller input clock. The DDC_IIC_SDA is the bidirectional data signal. Both these signals require a 1-kΩ pull-up resistor.

7.3.9.2 Communications Interface

Communications is performed over the I^2C interface where the DLPC910 is the slave device. The DLPC910 slave address consists of a 7-bit address plus 1 R/W bit. Communicating with the DLPC910 involves writing to or reading from the registers listed in *Register Map*.

7.3.9.2.1 Command Format

All register addresses are 32-bit in size, where each register contains a 32-bit value. The actual valid bits are shown in each respective register. Most registers contain spare or unused bits. These bits should be treated as *don't-care* during a read operation unless otherwise specified. When writing to spare or unused bits, these bits MUST be set to *0*. Both the register address and the data require the least-significant byte to be first and most-significant byte last. A SUB CMD must precede the register address to indicate the type of operation, where a 0xF1 indicates a write operation and a 0xF2 indicates a read operation. The following figures show examples of writing and reading to the DESTOP_BUS_SWAP register.

Figure 6 shows an I2C master writing data to the DLPC910, where 0xF1 is required as the SUB CMD followed by the register address and finally the register data.

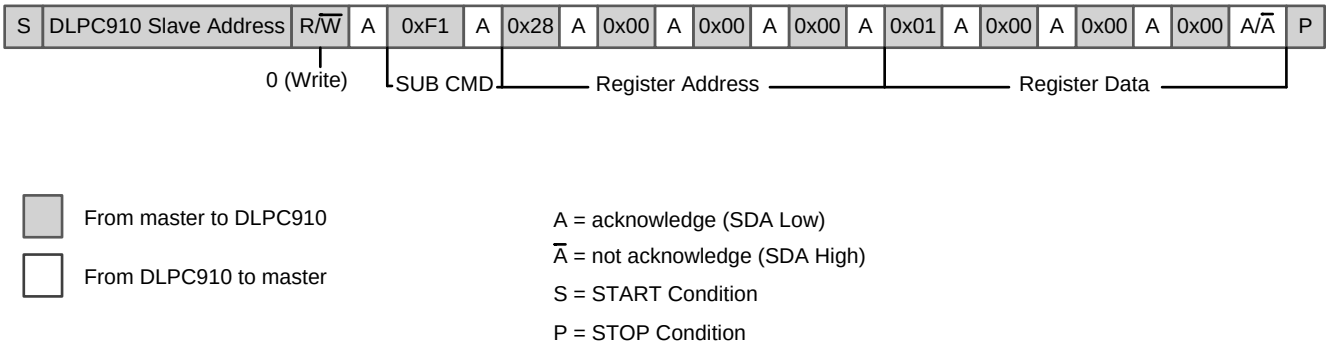


Figure 6. Example I2C Master Writing DLPC910 Register Data

Figure 7 shows an I2C master reading data from the DLPC910, where 0xF2 is required as the SUB CMD followed by the register address. Then the master performs STOP followed by a START to read the register data.

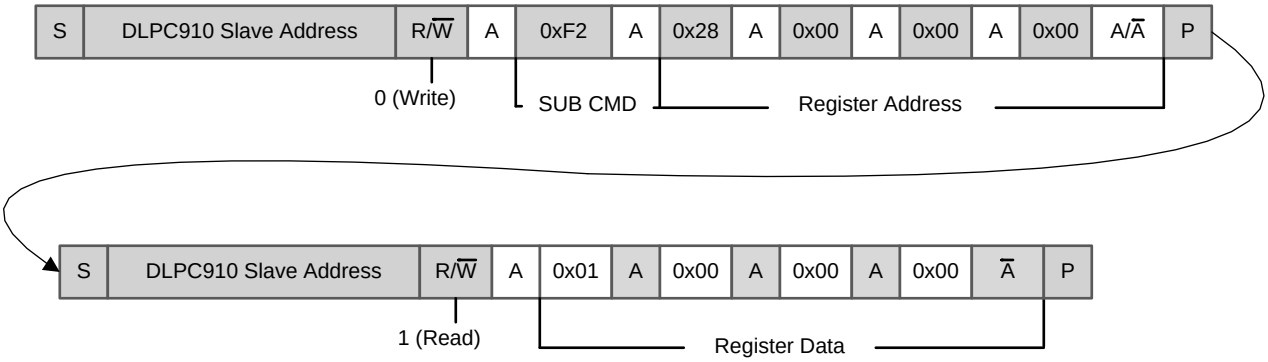


Figure 7. Example I2C Master Reading DLPC910 Register Data

7.3.10 DMD Interface

7.3.10.1 DDC_DOUT

The controller provides four (A, B, C, D) 16-bit wide 2x LVDS output data buses to the DMD with a user selectable bus frequency of 400 or 480 Mhz.

7.3.10.2 DDC_SCTRL

The controller provides four (A, B, C, D) control output buses to the DMD. Each bus provides the necessary control data for the different operating modes of the DMD.

7.3.10.3 DDC_DCLKOUT

The controller provides four (A, B, C, D) clock outputs to the DMD with a clock frequency of 400 or 480 Mhz (user selectable). Both DDC_DOUT and DDC_SCTRL are clocked into the DMD on both the rising and falling edges of the DDC_DCLKOUT.

7.3.10.4 DMD Reset Interface

7.3.10.4.1 Mirror Reset Control

The controller provides the necessary mirror reset control signals to the DMD, which are:

- RESET_ADDR(3:0) – Reset Driver Address Select.
- RESET_MODE(3:0) – Reset Driver Mode Select.
- RESET_SEL(1:0) – Reset Driver Level Select.

- RESET_STRB – Reset Address, Mode, and Level Select latched on rising-edge.

7.3.10.5 Enable and Interrupt Signals

The controller provides the necessary outputs for DMD enables and an input interrupt from the DMD, which are:

- PWRDNZ – Active-low DMD reset.
- RESET_OEZ – Active-low output enable for the DMD reset driver circuits.
- RESETZ – Active-low sets the reset circuits in known state.
- RESET_IRQZ – Active-low input interrupt from the DMD.

7.3.10.6 Serial Control Port

The DLPC910 communicates with the DMD over the SCP bus to perform initialization, set configuration, and retrieve identification information.

7.3.11 Flash PROM Interface

7.3.11.1 JTAG Interface

The JTAG interface has multiple purposes that can be used in the following manner:

- Program the configuration bit stream directly into the DLPC910
- Perform boundary test and debug of the DLPC910
- Program the configuration bit stream directly into the DLPR910YVA PROM (not user configurable)

7.3.11.2 PGM Interface

The PGM(4:0) interface is used by the DLPC910 to read in the configuration bit stream from the attached DLPR910YVA PROM.

7.4 Device Functional Modes

7.4.1 DMD Row Operation

The DMD data is loaded one row at a time with four LVDS buses into the DMD SRAM pixels. The DMD requires all four data buses (A,B,C,D). Each bus consists of a differential clock (DDC_DCLKOUT), a differential control signal (DDC_SCTRL), and 16 differential pairs of LVDS signals (DDC_DOUT[15:0]) that are output from the DLPC910. Data and control are clocked into the DMD on both the rising and falling edges of the DDC_DCLKOUT_[A, B, C, D]. Data loading does not cause mirror switching until a MCP operation is completed.

The number of clocks to load a row can be calculated as:

$$C = P / (D \times E) \quad (1)$$

where

- C = number of clocks per row
- P = number of pixels per row
- D = data bus bit width
- E = 2. (Data is clocked on both the rising an falling edge of DCLK.)

Example:
C = 2560 / (64 × 2) = 20 clocks per row

Row address orientation depends on the North or South Flip Flag (NS_FLIP) input to the DLPC910. Refer to *相关文档* for the DMD datasheet regarding orientation of rows, columns, and MCP blocks. The row address counter does not automatically wrap-around when using the increment row address pointer instruction. After the final row is addressed, the row address pointer must be cleared to 0.

Device Functional Modes (continued)

7.4.1.1 Data and Command Write Cycle

Once initialization is complete (INIT_ACTIVE = 0) the user is free to send data and control information to the DLPC910. When the user asserts the DVALID signal for the LVDS input buses, the DLPC910 begins sampling the LVDS data inputs and synchronously sending this information to the DMD along with row address control information. The row cycle period is exactly 20 CLKS long and begins with DVALID. If DVALID is removed, the DLPC910 stops loading data and control information until DVALID goes active again.

Figure 8 shows an example of data written to the DLPC910 for a single row. Data is written to the DMD 64 bits (16 A bits + 16 B bits + 16 C bits + 16 D bits) on each clock edge. An entire line must be written for data to be latched into memory.

The DMD incorporates single row write operations using a row address counter that is randomly addressable. As shown in Table 1 and Table 2, ROWMD(1:0) determines the single row write count mode and ROWAD(10:0) determines the single row write address. ROWMD and ROWAD must be asserted and de-asserted synchronously with DVALID and must be valid synchronous to the beginning of the data as shown in Figure 8.

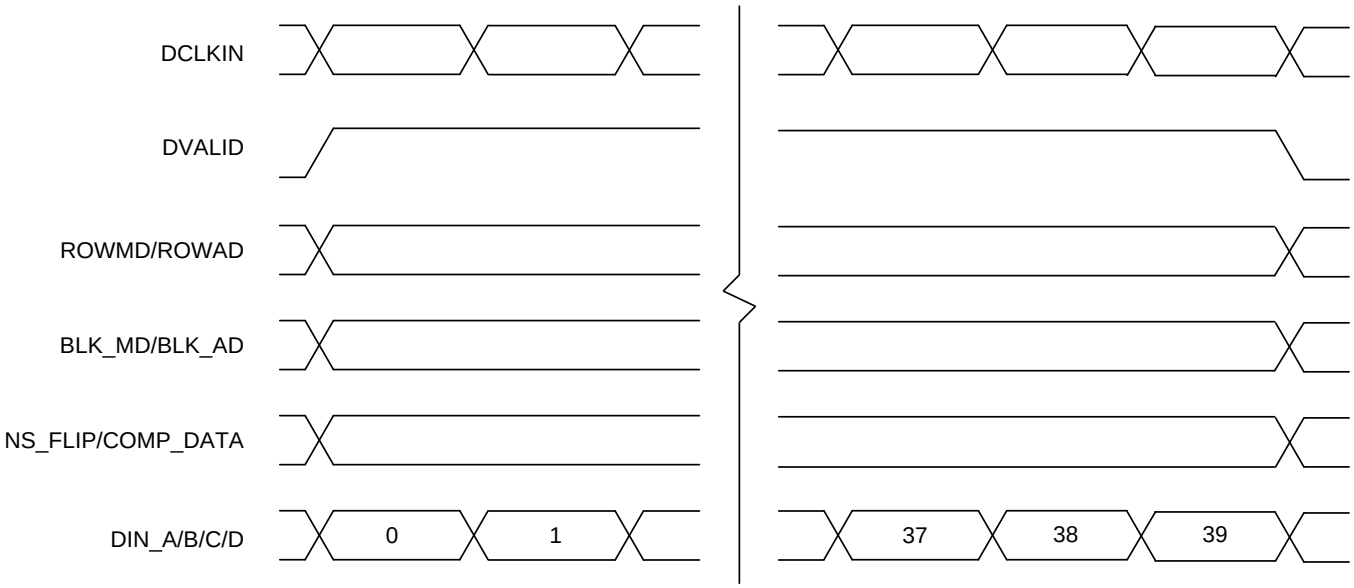


Figure 8. Single Row Write Operation

7.4.2 Block Mode Operation

The DMD mirrors and corresponding SRAM pixels are organized into blocks and each block is broken into rows per BLK as described in Table 4. Mirror blocks are addressed for either the *Mirror Clocking Pulse* or *Block Clear* functions by asserting block control signals at the start of each row data load. RST2BLKZ, BLK_MD and BLK_AD are used as shown in Table 5 to designate which mirror block(s) is to be issued a MCP or a Block Clear. Refer to *相关文档* for the DMD datasheet regarding block location information.

- The clear operation sets all of the SRAM pixels in the designated block to logic zero during the current row cycle.
- It is possible to issue a MCP to a block while loading a different block.
- It is not possible to clear a block while writing to a different block.
- It is not necessary to clear a block if it is going to be reloaded with new data (just like a normal memory cell).
- It is recommended that RST2BLKZ, COMP, and NS_FLIP be set to one value and not adjusted during normal system operation.
- A change in RST2BLKZ is not immediately effective and will require more than one row load cycle to complete.

Device Functional Modes (continued)

NOTE

RST2BLKZ, COMP_DATA, and NS_FLIP need to be kept low during initialization for proper setup of the system.

Table 4. Example DMD Characteristics

TYPE	DMD_TYPE	COLS	ROWS	BLKS	ROWS PER BLK	CLKS PER ROW	#DATA IN
DLP9000XFLS - 0.9 WQXGA Type A	0×F	2560	1600	16	100	20	64

Table 5. Block Operations

RST2BKLZ	BLK_MD 1	BLK_MD 2	BLK_AD 3	BLK_AD 2	BLK_AD 1	BLK_AD 0	OPERATION
X	0	0	X	X	X	X	None
X	0	1	0	0	0	0	Clear block 00
X	0	1	0	0	0	1	Clear block 01
X	0	1	0	0	1	0	Clear block 02
X	0	1	0	0	1	1	Clear block 03
X	0	1	0	1	0	0	Clear block 04
X	0	1	0	1	0	1	Clear block 05
X	0	1	0	1	1	0	Clear block 06
X	0	1	0	1	1	1	Clear block 07
X	0	1	1	0	0	0	Clear block 08
X	0	1	1	0	0	1	Clear block 09
X	0	1	1	0	1	0	Clear block 10
X	0	1	1	0	1	1	Clear block 11
X	0	1	1	1	0	0	Clear block 12
X	0	1	1	1	0	1	Clear block 13
X	0	1	1	1	1	0	Clear block 14
X	0	1	1	1	1	1	Clear block 15
X	1	0	0	0	0	0	Reset block 00
X	1	0	0	0	0	1	Reset block 01
X	1	0	0	0	1	0	Reset block 02
X	1	0	0	0	1	1	Reset block 03
X	1	0	0	1	0	0	Reset block 04
X	1	0	0	1	0	1	Reset block 05
X	1	0	0	1	1	0	Reset block 06
X	1	0	0	1	1	1	Reset block 07
X	1	0	1	0	0	0	Reset block 08
X	1	0	1	0	0	1	Reset block 09
X	1	0	1	0	1	0	Reset block 10
X	1	0	1	0	1	1	Reset block 11
X	1	0	1	1	0	0	Reset block 12
X	1	0	1	1	0	1	Reset block 13
X	1	0	1	1	1	0	Reset block 14
X	1	0	1	1	1	1	Reset block 15
0	1	1	0	0	0	0	Reset blocks 00-01
0	1	1	0	0	0	1	Reset blocks 02-03
0	1	1	0	0	1	0	Reset blocks 04-05
0	1	1	0	0	1	1	Reset blocks 06-07
0	1	1	0	1	0	0	Reset blocks 08-09
0	1	1	0	1	0	1	Reset blocks 10-11
0	1	1	0	1	1	0	Reset blocks 12-13

Table 5. Block Operations (continued)

RST2BKLZ	BLK_MD 1	BLK_MD 2	BLK_AD 3	BLK_AD 2	BLK_AD 1	BLK_AD 0	OPERATION
0	1	1	0	1	1	1	Reset blocks 14-15
1	1	1	0	0	0	X	Reset blocks 00-03
1	1	1	0	0	1	X	Reset blocks 04-07
1	1	1	0	1	0	X	Reset blocks 08-11
1	1	1	0	1	1	X	Reset blocks 12-15
X	1	1	1	0	X	X	Reset blocks 00-15
X	1	1	1	1	X	X	Float blocks 00-15

7.4.3 Block Clear

The DMD incorporates block clear operations using the BLK_MD and BLK_AD signals as shown in Table 5. The block address does not automatically increment and must be set to the desired block to be cleared. Block clear operation writes logic zero data to all the SRAM cells in one DMD block regardless of the COMP_DATA input state. It is not possible to clear a DMD block while writing to a different block. BLK_MD and BLK_AD are asserted to perform a MCP on the block(s) that have been cleared. The customer interface should introduces a delay on the last block(s) that were issued a MCP to allow the mirrors to become stable.**Each Block Clear operation must be followed by two no-op row load cycles.** Therefore, 16 total Block Clear commands and 32 total no-op row cycles are required to clear the entire DMD array.

7.4.4 Mirror Clocking Pulse

A Mirror Clocking Pulse (MCP) sequence begins by asserting BLK_MD and BLK_AD for a single, dual, quad, or global block operation as defined in Table 5. A MCP causes a reset on the block(s), and the data stored in the block(s) takes effect on the mirrors of the DMD. Shortly after a MCP has been issued, RST_ACTIVE goes high for approximately 4 µs, indicating a MCP operation is in progress. During this time, no additional MCPs may be initiated until RST_ACTIVE returns low. RST_ACTIVE does not return to low unless continuous no-op or data loading row cycles are issued. A typical single block load phased sequence in which consecutive DMD blocks are loaded is illustrated in Figure 10. A MCP time is identical for single, dual, quad or global block operations.

Note that it may take longer to complete a MCP on a block than it does to load a block. The block load time may be calculated as:

Block Load Time = Clock Period × number CLKS per ROW × number ROWS per BLK

Table 6. DMD Block Load Time at 480 MHz DMD Clock

DMD	MINIMUM BLOCK LOAD TIME
DLP9000XFLS	4.167 µsec

For any case which involves sending a MCP or a Block Clear without data loading, the customer interface must send no-op row cycles. This can be accomplished by asserting DVALID, while holding ROWMD at 00 and BLKMD at 00 for 20 clock cycles, as in Figure 9. Following the loading of all rows in a block or the entire DMD, at least one no-op row cycle must be completed to initiate the MCP. If the MCP is asserted prior to loading all rows in a block or the entire DMD, rows which were not updated will show old data. Additional MCP operations may not be initiated until RST_ACTIVE is low. Block Clear operations for the DMD must be followed by two consecutive no-op row cycle commands.

To obtain full utilization of the DMD bandwidth, load four blocks and then issue a MCP to the four blocks concurrently by setting RST2BLKZ to *1* and BLK_MD to *11* with the appropriate address in BLK_AD. This is illustrated in Figure 12.

It is possible to load other blocks while the block(s) previously issued a MCP is settling. This is illustrated in Figure 11 and Figure 12, where blocks are reloaded while the mirror setting time is ocurring. It is also possible to load other blocks while previously loaded block(s) have an outstanding RST_ACTIVE. This is illustrated in Figure 12, where block 0 is loaded while RST_ACTIVE is asserted for blocks 12-15.

NOTE

While RST_ACTIVE is high for 4 µs, the data for the block(s) being issued a MCP should not be changed to allow the mirrors to become stable. The RST_ACTIVE does not include the mirror settling period. A short delay of 6 µs should be introduced during the last block(s) that is issued a MCP. The mirror settling time is illustrated in Figure 10, Figure 11, Figure 12, and Figure 13, where the customer interface introduces a delay on the last block(s) that were issued a MCP to allow the mirrors to become stable.

Figure 10, Figure 11, Figure 12, and Figure 13 all show an exposure period. Once the customer interface has issued all required MCPs and the proper mirror settling time has been applied, the customer interface may pulse an illumination source onto the DMD during this period. The exposure period is user adjustable; however, increasing the exposure period decreases the pattern rate. Refer to *Application Curves* regarding exposure period.

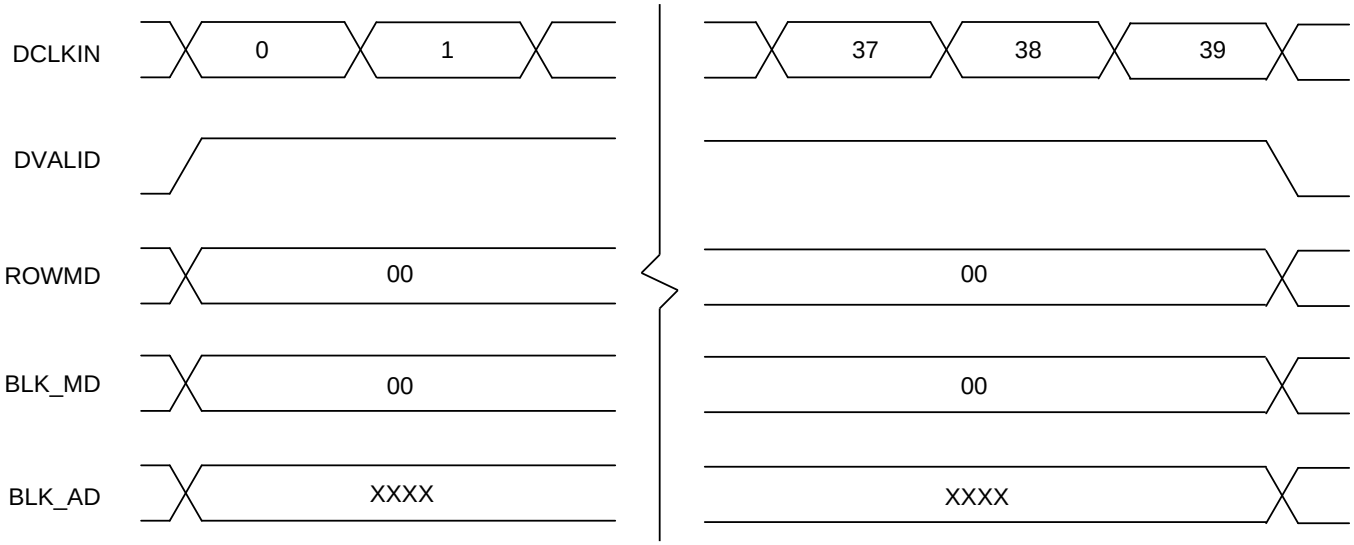


Figure 9. DMD No-op Row Cycle

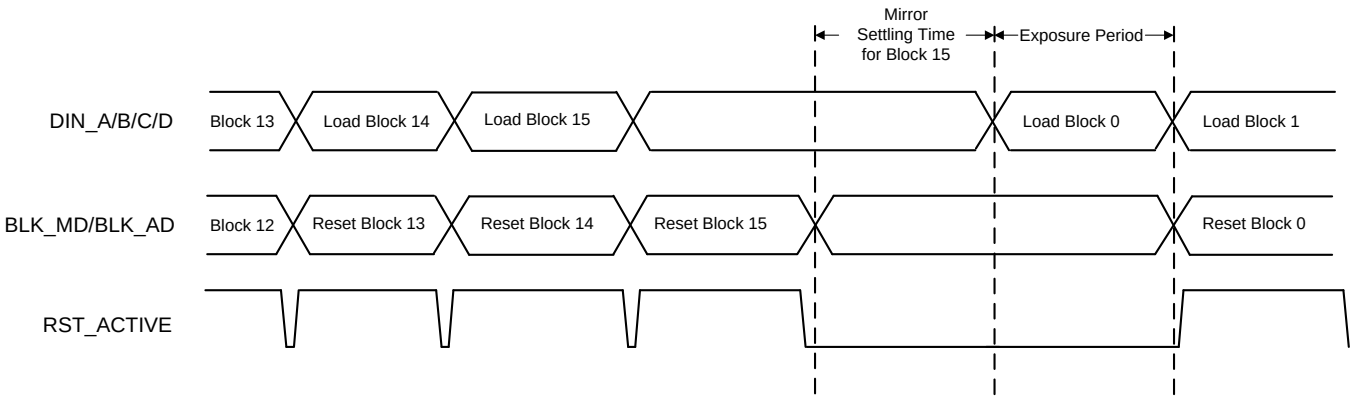


Figure 10. Single Block Load Phased Sequence

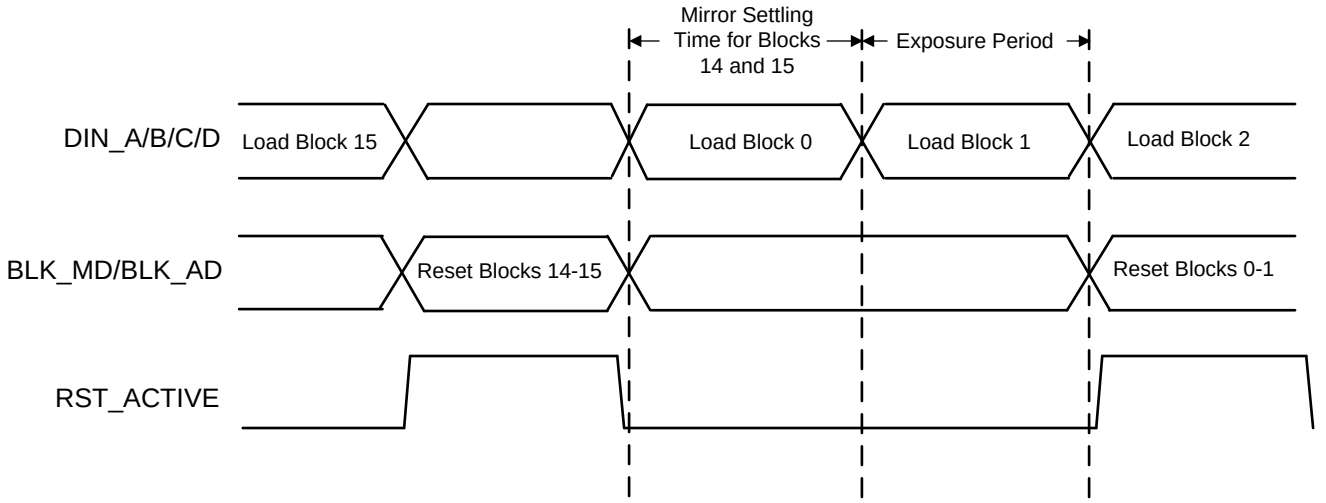


Figure 11. Dual Block Load Phased Sequence

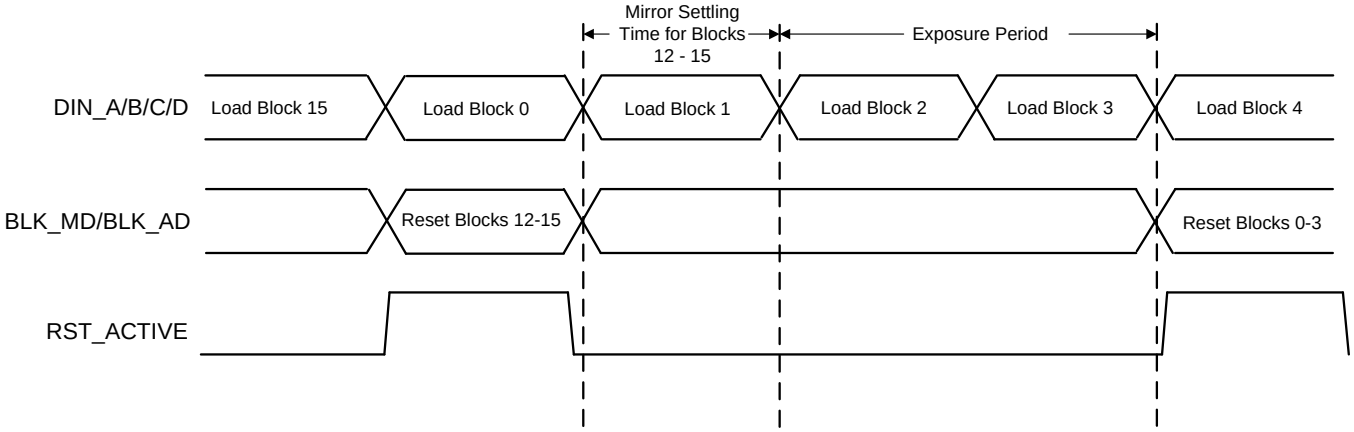


Figure 12. Quad Block Load Phased Sequence

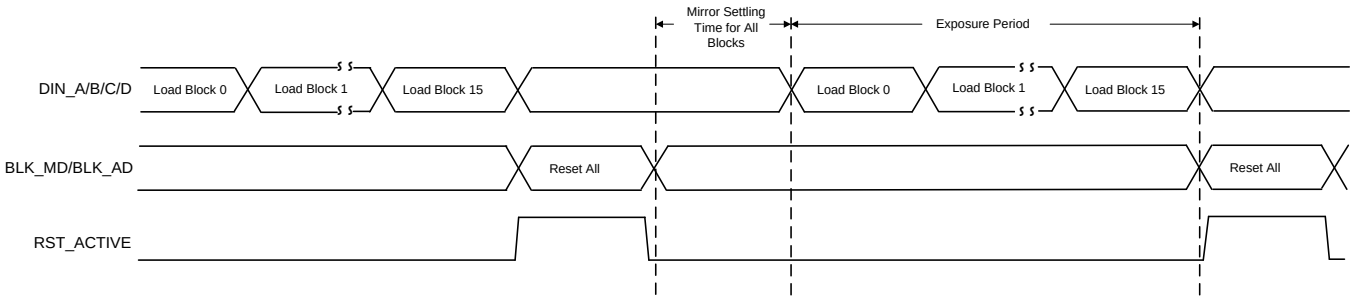


Figure 13. Full DMD Global Load Sequence

Note: After a MCP or Block Clear command is given, RST_ACTIVE may not be asserted until up to 60ns (depending on the clock frequency) after the command. While RST_ACTIVE is asserted, no other command should be given.

7.4.5 DMD Array Subset

It is possible to use a subset of the DMD array including individual MCP blocks. The driving software/hardware MUST ensure that the MCP rate for the number of blocks in the subset plus the mirror settling time does not exceed 50 kHz.

Load4 functionality is primarily intended to be used with global MCPs. However, it is possible to use a subset of the DMD array including individual MCP blocks. The driving software/hardware MUST ensure that the MCP rate for the number of blocks in the Load4 subset plus the mirror settling time does not exceed 50 kHz.

7.4.6 Global Mirror Clocking Pulse Consideration

A Global MCP (BLK_MD = 11 and BLK_AD = 10XX), takes the same amount of time as the single, dual, and quad block MCP. In addition to requiring a no-op row cycle to initiate a global MCP, a row cycle (either no-op or data loading) is also required to complete the operation. If the customer interface is monitoring RST_ACTIVE to determine when to send a subsequent row cycle, it will never see RST_ACTIVE transition low. One method of operation would be to continue sending no-op row cycles until RST_ACTIVE goes low then continue loading data with real row cycles. Another method of operation is to delay greater than 10 µs, then start loading new data to DMD.

7.5 Register Map

7.5.1 Register Table Overview

Table 7 lists the I^2C accessible memory mapped registers for the DLPC910. Access to the I^2C registers should not begin unitl INIT_ACTIVE has transitioned low (logic *0*).

Table 7. Communication Registers

ADDRESS	REGISTER NAME	DESCRIPTION	SIZE
0x0000 0x0004 0x0008	DESTOP_INTERRUPT	DESTOP Interrupt Status	32
0x000C	MAIN_STATUS	Main Status	32
0x0010	DESTOP_CAL	DESTOP input calibration status	32
0x0014	DESTOP_DMD_ID_REG	Connected DMD ID	32
0x0018	DESTOP_CATBITS_REG	Connected DMD fuse catalog bits	32
0x001C	DESTOP_910VERSION_REG	DLPC910 Version Number	32
0x0020	DESTOP_RESET_REG	Reset status signals	32
0x0024	DESTOP_INFIFO_STATUS	Input interface FIFO status	32
0x0028	DESTOP_BUS_SWAP	Output bus swap	32
0x002C	DESTOP_DMDCTRL	DMD Control Register	32
0x0030	DESTOP_BIT_FLIP	Output data bus bit reversal/flip	32

7.5.1.1 DESTOP_INTERRUPT Register

The DESTOP_INTERRUPT register is used for controlling the interrupt source. Interrupts can be enabled, disabled, cleared and read independently.

Table 8. DESTOP_INTERRUPT Register

ADDRESS (1) (2) (3) (4)	BITS	DESCRIPTION	RESET	TYPE
0x0000 0x0004 0x0008	0	SPARE	0x0	R/W
	1	SPARE	0x0	R
	2	A DMD IRQZ event occurred. The only existing source for this event is a DMD power fault indicating bias, offset, or reset power supplies have become inactive. The cause of the fault should be determined and resolved prior to a system reset to continue operation. (5)	0x0	R/W
	3	SPARE	0x0	R
	31:4	UNUSED	0x0	R

(1) Interrupt status can be obtained by reading 0x0000 or 0x0004 address.
(2) Interrupt bits are asserted either by the corresponding H/W events or by S/W writing a 1 to the target bit of 0x0004 address.
(3) Interrupt bits are cleared by S/W writing a 1 to the target bit in 0x0000 address.
(4) Interrupts are enabled by setting the appropriate bits in register 0x0008.
(5) This bit must be cleared after a power cycle or a reset to the DLPC910.

7.5.1.2 MAIN_STATUS Register

The MAIN_STATUS register is used for reading the status of the DLPC910. The register can be polled during operation to obtain the current state of the DLPC910.

Table 9. MAIN_STATUS Register

ADDRESS	BITS	DESCRIPTION	RESET	TYPE
0x000C	0	DMD initialization in progress flag	0x0	R
		0 - No DMD initialization activity		
		1 - DMD initialization in progress		
	1	DMD initialization in progress flag 1	0x0	R
		0 - No DMD stage 1 initialization activity		
		1 - DMD stage 1 initialization activity in progress		
	2	DMD initialization in progress flag 2	0x0	R
		0 - No DMD stage 2 initialization activity		
		1 - DMD stage 2 initialization activity in progress		
	3	DMD supports AB channels	0x0	R
		0 - Operation of DMD AB buses not enabled		
		1 - Operation of DMD AB buses enabled		
	4	DMD supports CD channels	0x0	R
		0 - Operation of DMD CD buses not enabled		
		1 - Operation of DMD CD buses enabled		
	5	Input interface calibration in progress	0x0	R
		0 - Input interface calibration inactive		
		1 - Input interface calibration in progress		
	6	DVALID alignment on interface A ok	0x0	R
		0 - DVALID alignment invalid on channel A		
		1 - DVALID alignment correct on channel A		
	7	DVALID alignment on interface B ok	0x0	R
		0 - DVALID alignment invalid on channel B		
		1 - DVALID alignment correct on channel B		
	8	DVALID alignment on interface C ok	0x0	R
		0 - DVALID alignment invalid on channel C		
		1 - DVALID alignment correct on channel C		
	9	DVALID alignment on interface D ok	0x0	R
		0 - DVALID alignment invalid on channel D		
		1 - DVALID alignment correct on channel D		
	10	System PLL locked flag	0x0	R
		0 - PLL not locked		
		1 - PLL locked		
	11	Reference PLL locked flag	0x0	R
		0 - PLL not locked		
		1 - PLL locked		
	31:12:00	UNUSED	0x0	R

7.5.1.3 DESTOP_CAL Register

The DESTOP_CAL register is used for reading the calibration state of the LVDS input buses of the DLPC910. The calibration occurs during the initialization after power is applied to the DLPC910.

Table 10. DESTOP_CAL Register

ADDRESS	BITS	DESCRIPTION	RESET	TYPE
0x0010	0	Input Channel A Calibration complete:	0x0	R
		0 - Channel A Calibration in progress		
		1 - Channel A Calibration complete		
	1	Input Channel B Calibration complete:	0x0	R
		0 - Channel B Calibration in progress		
		1 - Channel B Calibration complete		
	2	Input Channel C Calibration complete:	0x0	R
		0 - Channel C Calibration in progress		
		1 - Channel C Calibration complete		
	3	Input Channel D Calibration complete:	0x0	R
		0 - Channel D Calibration in progress		
		1 - Channel D Calibration complete		
	31:04:00	UNUSED	0x0	R

7.5.1.4 DESTOP_DMD_ID_REG Register

The DESTOP_DMD_ID_REG register is used for reading the identification of the DMD connected to the DLPC910. If the DLPC910 determines the DMD is not supported, the DLPC910 will halt all operations.

Table 11. DESTOP_DMD_ID_REG Register

ADDRESS	BITS	DESCRIPTION	RESET	TYPE
0x0014	31:0	Read-only register containing the ID of the connected DMD.	0x0	R

7.5.1.5 DESTOP_CATBITS_REG Register

The DESTOP_CATBITS_REG register is used for reading the remainder of identification of the DMD connected to the DLPC910. If the DLPC910 determines the DMD is not supported, the DLPC910 will halt all operations.

Table 12.

ADDRESS	BITS	DESCRIPTION	RESET	TYPE
0x0018	3:0	Read-only register containing the 4 remaining ID bits of the connected DMD.	0x0	R
	31:4	UNUSED	0x0	R

7.5.1.6 DESTOP_VERSION Register

The DESTOP_VERSION is used for obtaining the DLPR910 prom configuration program version.

Table 13. DESTOP_VERSION Register

ADDRESS	BITS	DESCRIPTION (Read-only register of the DLPC910 version number)	RESET	TYPE
0x001C	3:0	Major	0x1	R
	7:4	Minor	0x0	R
	15:8	Revision	0x0	R
	31:16	UNUSED	0x0	R

7.5.1.7 DESTOP_RESET_REG Register

The DESTOP_RESET_REG register is used for reading the current state of the MCP. Reading this register while the DLPC910 is loading data to the DMD may always indicate a “1”. It is best to monitor the actual RST_ACTIVE output signal of the DLPC910 to obtain the real state of the MCP.

Table 14. DESTOP_RESET_REG Register

ADDRESS	BITS	DESCRIPTION	RESET	TYPE
0x0020	0	RESET Operation in progress bit: (Mirror clocking pulse) 0 - Reset inactive 1 - Reset active	0x0	R
	31:1	UNUSED	0x0	R

7.5.1.8 DESTOP_INFIFO_STATUS Register

The DESTOP_INFIFO_STATUS register is used for validating there is data in the input bus FIFO buffers. An empty FIFO buffer may indicate that the DVALID is not properly set for the data on the input data bus.

Table 15. DESTOP_INFIFO_STATUS Register

ADDRESS	BITS	DESCRIPTION	RESET	TYPE
0x0024	0	Channel A input FIFO status: 0 - Channel A FIFO has data 1 - Channel A FIFO is empty	0x0	R
	1	Channel B input FIFO status: 0 - Channel B FIFO has data 1 - Channel B FIFO is empty	0x0	R
	2	Channel C input FIFO status: 0 - Channel C FIFO has data 1 - Channel C FIFO is empty	0x0	R
	3	Channel D input FIFO status: 0 - Channel D FIFO has data 1 - Channel D FIFO Is empty	0x0	R
	31:4	UNUSED	0x0	R

7.5.1.9 DESTOP_BUS_SWAP Register

The DESTOP_BUS_SWAP register is used for configuring the DLPC910 output LVDS buses to the DMD. To simplify board layout design, swapping the buses may reduce routing constraints. If the buses are swapped in hardware, then the appropriate setting that matches the hardware must be set after a power cycle or a reset to the DLPC910.

Table 16. DESTOP_BUS_SWAP Register

ADDRESS	BITS	DESCRIPTION	RESET	TYPE
0x0028	0	Enables Bus swap for A and B output DMD buses. SCTRLs for A and B output buses are also swapped. 0 = un-swapped (default) 1 = swapped	0x0	R/W
	1	Enables Bus swap for C and D output DMD buses. SCTRLs for C and D output buses are also swapped. 0 = un-swapped (default) 1 = swapped	0x0	R/W
	31:2	UNUSED	0x0	R

7.5.1.10 DESTOP_DMDCTRL Register

The DESTOP_DMDCTRL register can be used in place of the external DLPC910 control inputs to control the functions described. Bit-0 must be set to “1” to gain control of the functions. Bit-5 is available regardless of the state of bit-0.

Table 17. DESTOP_DMDCTRL Register

ADDRESS	BITS	DESCRIPTION (1)	RESET	TYPE
0x002C	0	Enables DMD control of the functions that are normally controlled on external pins. 0 = Controlled from external pins (default) 1 = Controlled from the I2C interface	0x0	R/W
	1	NS_FLIP. Sets the orientation of the top and bottom of the DMD. 0 = Un-flipped (default) 1 = Flipped	0x0	R/W
	2	DATA_COMP. Sets a DMD mode that inverts all of the incoming data. 0 = Normal (default) 1 = Data is inverted at the DMD	0x0	R/W
	3	LOAD_FOUR. Activates the Load4 function of the DMD. Each row written is loaded to 4 consecutive locations. 0 = Load4 mode is active 1 = Normal (default)	0x1	R/W
	4	RST2BLKZ. Activates the RST2BLKZ function of the DMD. Refer to Table 5 for setting RST2BLKZ.	0x1	R/W

(1) When bit 0 is set to *1*, bits 1, 2, 3, and 4 override their respective external control inputs.

7.5.1.11 DESTOP_BIT_FLIP Register

The DESTOP_BIT_FLIP register is used for configuring the DLPC910 output LVDS buses to the DMD. To simplify board layout design, flipping individual buses may reduce routing constraints. If the buses are flipped in hardware, then the appropriate setting that matches the hardware must be set after a power cycle or a reset to the DLPC910.

Table 18. DESTOP_BIT_FLIP Register

ADDRESS	BITS	DESCRIPTION	RESET	TYPE
0x0030	0	Reverses the Data bits for bus A (b'15 = b'0, b'0 = b'15) 0 = un-flipped (default) 1 = flipped	0x0	R/W
	1	Reverses the Data bits for bus B (b'15 = b'0, b'0 = b'15) 0 = un-flipped (default) 1 = flipped	0x0	R/W
	2	Reverses the Data bits for bus C (b'15 = b'0, b'0 = b'15) 0 = un-flipped (default) 1 = flipped	0x0	R/W
	3	Reverses the Data bits for bus D (b'15 = b'0, b'0 = b'15) 0 = un-flipped (default) 1 = flipped	0x0	R/W
	31:4	UNUSED	0x0	R

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLPC910 controller verifies the DMD connected in the application system, uses that information to select appropriate configuration data for the DMD, and then initializes the DMD to ready it for operation.

The DLPC910 controller receives streaming 64-bit parallel input data and associated syncs from an external applications processor and passes the 64-bit data on to the DLP9000X DMD with the appropriate DMD timing and control information. It also receives embedded instructions from the applications processor to assist in determination of which DMD rows to load and which DMD mirror blocks to activate at any given moment in time.

8.2 Typical Application

Direct-write digital imaging is regularly used in high-end lithography printing. This mask-less technology offers continuous run of printing by changing the digitally created patterns without stopping the imaging head. The DLPC910 digital controller, coupled with the DLP9000XFLS DMD, offers an ideal back-end imager that takes in digital images at 2560 × 1600 in resolution to achieve speeds greater than 61 Gigabits per second (Gbps).

8.2.1 High Speed Lithography Application

As high-end lithography pushes the high speed printing envelope, providing a higher resolution imager is a must to achieve the demanding through-put of present and future printing technology. Figure 14 shows a system that offers both a speed boost and a four million pixel DMD. The main chipset components that make up this system are the DLPC910ZYR, the DLPR910YVA, and the DLP9000XFLS. With a few additional discrete components for power regulation and clock circuitry, a compact, and yet high performance design can be achieved.

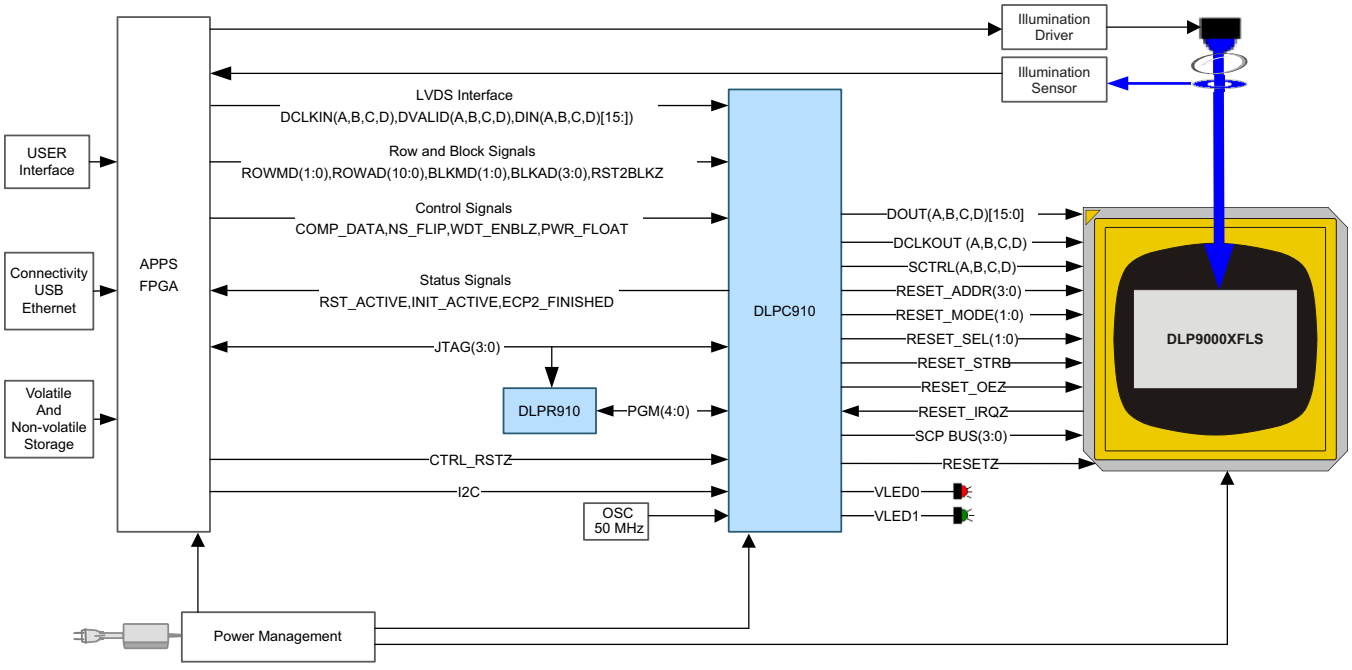


Figure 14. Typical High Speed Lithography Application

Typical Application (continued)

8.2.1.1 Design Requirements

The DLPC910 interface is made up of several buses and controls signals as shown in the following list. The LVDS input buses provides the means of loading data to the DLPC910 and the LVDS output buses provide the data to DMD. Each input and output LVDS bus has an associated clock which clocks the data into the DLPC910 or into the DLP9000X. Row and Block control signals define the type of mirror clock pulse to use after all the data is loaded into the DLP9000X.

- LVDS differential inputs
  - DDC_DCLK 4 buses
  - DVALID 4 buses
  - DDC_DIN 4 buses
- LVDS differential outputs. Refer to *LVDS Output Bus Skew* for recommendations on trace lengths.
  - DDC_DOUT 4 buses
  - DDC_DCLKOUT 4 buses
  - DDC_SCTRL 4 buses
- Control output signals
  - DMD RESET
  - DMD SCP
- Row and Block control input signals
  - ROWMD
  - ROWAD
  - BLKMD
  - BLKAD
  - RST2BLKZ
- Control input signals
  - COMP_DATA
  - NS_FLIP
  - WDT_ENBLZ
  - PWR_FLOAT
  - LOAD4_ENZ
- Status output signals
  - RST_ACTIVE
  - INIT_ACTIVE
  - ECP2_FINISHED
  - DMD_IRQ
- Controller reset
  - CTRL_RSTZ
- DLPR910 interface
  - PGM(4:0)
  - JTAG(3:0)

8.2.1.2 Detailed Design Procedure

After power is applied to the DLPC910, the APPS FPGA should monitor the ECP2_FINISHED signal to determine when the DLPC910 has completed loading the configuration from the DLPR910. The APPS FPGA next monitors the INIT_ACTIVE signal to determine when the DLPC910 has completed its internal initialization routines and has configured the DMD for normal operation. An alternate method is to request the initialization status using the I2C interface. Information regarding initialization, versions, and IDs can be requested through this interface.

Typical Application (continued)

Prior to activating the DVALID signals to the DLPC910, the ROWMD, ROWAD, BLKMD, BLKAD, and RST2BLKZ control input signals must be in the desired state for the desired operation to take effect on the DLP9000X DMD. Once the control signals are set, the Apps FPGA activates DVALID and starts loading data using the DDC_DIN and DDC_DCLK buses. After all data is loaded for the desired DMD operation, the DVALID signal is de-asserted, and the BLKMD, BLKAD, and RST2BLKZ control signals are set prior to the assertion of the next DVALID. When DVALID is activated, the MCP causes the prior data to take effect on the mirrors of the DMD. The Apps FPGA should then monitor the RST_ACTIVE pin to determine when the mirror clock pulse has completed in order to perform the next MCP. During the time that the RST_ACTIVE is asserted, the Apps FPGA could be loading data into DMD rows that do not belong to the same block of rows that currently has an outstanding MCP.

8.2.1.3 Application Curves

In this particular application, the performance plot shown in Figure 15 shows the maximum loaded and displayed pixels per second when the exposure period is set to its minimum for the different reset modes. When the exposure period is increased, the pixels per second will decrease. Refer to *Mirror Clocking Pulse* for more information regarding exposure period.

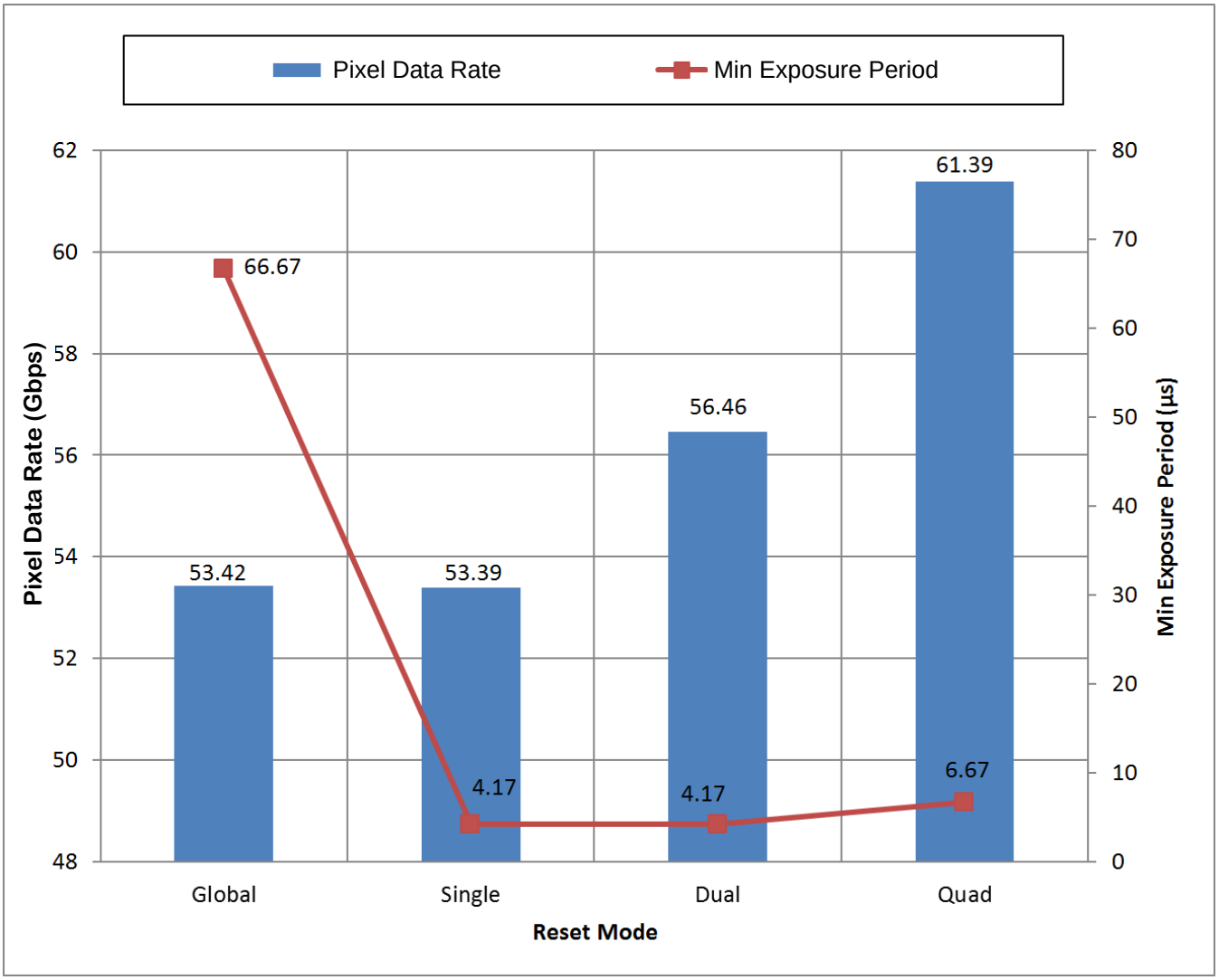


Figure 15. Performance Plot at 480 MHz DDC_DCLK

9 Power Supply Recommendations

9.1 Power Supply Distribution and Requirements

The DLPC910ZYR, the DLPR910YVA, and the DLP9000XFLS DMD are powered by a power distribution as shown in Figure 16.

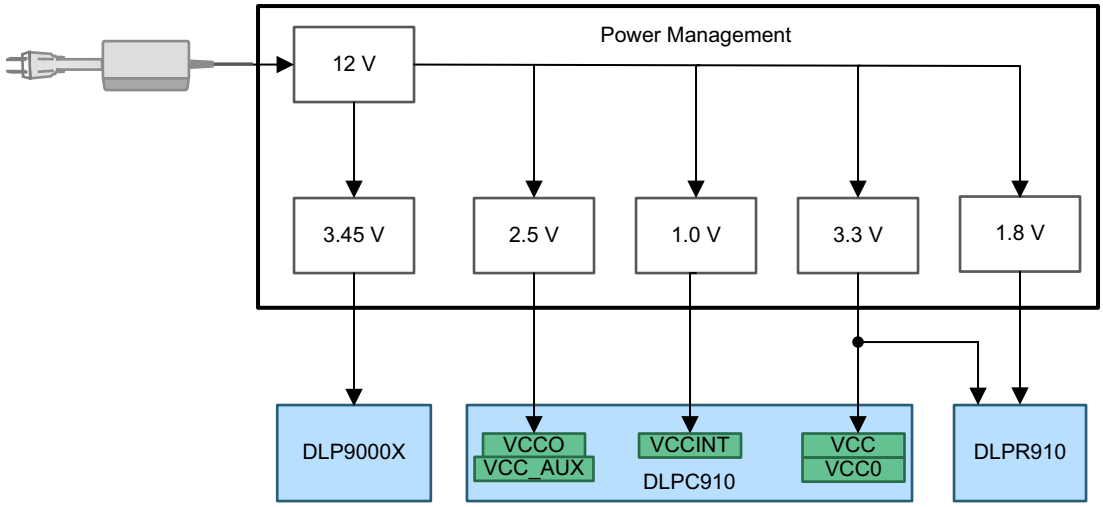


Figure 16. Power Distribution

9.2 Power Down Sequence

Prior to power removal, the Apps FPGA should assert PWR_FLOAT and allow approximately 300 µs for the procedure to complete. This procedure will assure the mirrors are in a flat state. Following this procedure, the power can be safely removed. To restart after assertion of PWR_FLOAT, the DLPC910 must be reset (CTRL_RSTZ low then high) or power must be cycled.

10 Layout

10.1 Layout Guidelines

One of the most important factors to gain good performance is designing the PCB with the highest quality signal integrity possible. The following PCB design guidelines provide a reference of an interconnect system..

10.1.1 PCB Design Standards

PCBs should be designed and built in accordance with the industry specifications shown in Table 19.

Table 19. Industry Design Specifications

INDUSTRY SPECIFICATION	APPLICABLE TO
IPC-2221 and IPC2222, Type 3, Class X, at Level B producibility	Board design
IPC-6011 and IPC-6012, Class 2	PWB fabrication
IPC-SM-840, Class 3, Color Green	Finished PWB solder mask
UL94V-0 Flammability Rating and Marking	Finished PWB
UL796 Rating and Marking	Finished PWB

PCB Fabrication:

- Configuration: Asymmetric dual strip-line
- Etch thickness : 1.0-oz copper (1.2 mil)
- Flex etch thickness: 0.5-oz copper (0.6 mil)
- Single-ended signal impedance: 50 Ω (±10%)
- Differential signal impedance: 100 Ω (±10%)

PCB Stack-up:

- Ground planes for proper return path.
- Power planes for proper supply to circuits.
- Dielectric material with a low Loss-Tangent, for example: Hitachi 679gs or equivalent, (Er): 3.8 (nominal).

10.1.2 Signal Layers

The PCB signal layers should follow typical good practice guidelines including:

- Layer changes should be minimized for single-ended signals.
- Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.
- Stubs should be avoided.
- Low-frequency signals should be routed on the outer layers.
- Differential pair signals should be routed first.
- Pin swapping on components is not allowed.
- Polarized capacitors should have the same orientation.

The PCB should have a solder mask on the top and bottom layers.

- The mask should not cover the vias.
- Except for fine pitch devices (pitch ≤ 0.032 inches). The copper pads and the solder mask cutout should be of the same size.
- Solder mask between pads of fine pitch devices should be removed.
- In the BGA package, the copper pads and the solder mask cutout should be of the same size.

High-speed connectors that meet the following requirements should be used:

- Differential crosstalk: < 5%
- Differential impedance: 90 to 110 Ω for all LVDS signal pairs

Routing requirements for right-angle connectors:

- When using right-angle connectors, LVDS signal P-N pairs should be routed in the same row to minimize delay mismatch.
- When using right-angle connectors, propagation delay difference for each row should be accounted for on associated PCB etch lengths.

10.1.3 General PCB Routing

Fiducials for automatic component insertion should be 0.05-inch copper with a 0.1-inch cutout (antipad). Fiducials for optical auto insertion are placed on three corners of both sides of the PCB.

10.1.3.1 Trace Minimum Spacing

BGA escape routing can be routed with 3.7-mils width and 4.3-mils spacing, as long as the escape nets are less than 1-inch long, to allow two traces to fit between vias. After signals escape the BGA field, trace width should be widened to achieve the desired impedance and spacing.

All single-ended 50-ohm signals must have a minimum spacing of 10 mils relative to other signals. Other special trace spacing requirements are listed in Table 20.

Table 20. Trace Minimum Spending

SIGNAL	PWR	GND	SINGLE-ENDED (1)	DIFFERENTIAL PAIRS	UNIT
				Pair-to-Pair (2)	
PWR	20 (3)	10	15	15	mils
GND	10		5	5	mils
CLKIN_R	15	5	30	30	mils
DDC_DCLK_[A,B,C,D]_DP[N,P]	15	5	30	30	mils
DDC_DCLKOUT_[A,B,C,D]_DP[N,P]	15	5	30	30	mils
DDC_DIN_[A,B,C,D][0:15]_DP[N,P]	15	5	30	30	mils
DDC_DOUT_[A,B,C,D][0:15]_DP[N,P]	15	5	30	30	mils
DDC_SCTRL_[A,B,C,D][N,P]	15	5	30	30	mils
DVALID_[A,B,C,D]_DP[N,P]	15	5	30	30	mils
Escape routing in ball field	15	5	4.3	4.3	mils
All other signals	15	5	30	30	mils

(1) Signal spacing relative to other single-end signals.
(2) Signal spacing relative to other differential pairs.
(3) PWR relative to other power sources. Not same power source.

10.1.3.2 Trace Widths and Lengths

Table 21. Trace Widths and Lengths

SIGNAL	MIN WIDTHS	MAX LENGTHS (1)	MAXIMUM TRACE MISMATCH		UNIT
			N-to-P	Pair-to-pair	
PWR	25				mils
GND	15 (2)				mils
CLKIN_R	7	350			mils
DDC_DCLK_[A,B,C,D]_DP[N,P]	Layout specific (3)	Layout specific (4)	10		mils
DDC_DIN_[A,B,C,D][0:15]_DP[N,P]			10	50 (5)	mils
DVALID_[A,B,C,D]_DP[N,P]			10	50 (5)	mils
DDC_DCLKOUT_[A,B,C,D]_DP[N,P]			10		mils
DDC_DOUT_[A,B,C,D][0:15]_DP[N,P]			10	50 (5)	mils
DDC_SCTRL_[A,B,C,D][N,P]			10	50 (5)	mils
All other signals	7				mils

(1) Signal routing length includes escape routing.
(2) Make width of GND trace as wide as the pin it is connected to, when possible.
(3) Minimum widths to achieve impedance matching.
(4) Keep lengths as short as possible.
(5) Relative to its clock system. Refer to to identify the clock system associated with the signals.

10.1.3.2.1 LVDS Output Bus Skew

To minimize instantaneous AC current switching in the DMD, the LVDS output bus trace lengths should differ to produce a recommneded 100-200 ps skew from one bus to another. Table 22 shows two examples how buses can be skewed assuming 180-200 ps per 1000 mils. Keep in mind the total skew from one bus to another should be kept below the maximum skew for the DMD. Refer to *相关文档* for the DMD datasheet regarding maximum DMD LVDS input bus skew.

Table 22. Example LVDS Output Bus Skew

Bus Group	Example 1 Bus Group Trace Lengths	Example 2 Bus Group Trace Lengths	UNIT
DDC_DCLKOUT_A DDC_DOUT_A DDC_SCTRL_A	7454	7454	mils
DDC_DCLKOUT_B DDC_DOUT_B DDC_SCTRL_B	5257	7454	mils
DDC_DCLKOUT_C DDC_DOUT_C DDC_SCTRL_C	6936	5257	mils
DDC_DCLKOUT_D DDC_DOUT_D DDC_SCTRL_D	5886	5257	mils

10.1.3.3 Trace Impedance and Routing Priority

For best performance, it is recommended that the trace impedance for differential signals as in Table 23.

All signals should be 50-ohms controlled impedance unless otherwise noted in Table 23.

Table 23. Trace Impedance

SIGNALS	DIFFERENTIAL IMPEDANCE
DDC_DCLK_[A,B,C,D]_DP[N,P]	100 Ω ± 10%
DDC_DCLKOUT_[A,B,C,D]_DP[N,P]	100 Ω ± 10%
DDC_DIN_[A,B,C,D][0:15]_DP[N,P]	100 Ω ± 10%
DDC_DOUT_[A,B,C,D][0:15]_DP[N,P]	100 Ω ± 10%
DDC_SCTRL_[A,B,C,D][N,P]	100 Ω ± 10%
DVALID_[A,B,C,D]_DP[N,P]	100 Ω ± 10%

Table 24 lists the routing priority and layer assignments of the signals.

Table 24. Routing Priority

SIGNALS	Priority
DDC_DCLKOUT_[A,B,C,D]_DP[N,P]	1
DDC_DOUT_[A,B,C,D][0:15]_DP[N,P]	1
DDC_SCTRL_[A,B,C,D][N,P]	2
DDC_DCLK_[A,B,C,D]_DP[N,P]	2
DDC_DIN_[A,B,C,D][0:15]_DP[N,P]	3
DVALID_[A,B,C,D]_DP[N,P]	3
BLKAD_[0:3], BLKMD_[0:1], ROWAD_[0:10], ROWMD_[0:1]	4
RESET_ADDR[0:3], RESET_MODE[0:1], RESET_SEL[0:1], RESET_STROBE, RESET_OEZ, RESET_IRQZ, RESET_RSTZ	5
SCPCLK, SCPDI, SCPDO, DMD_SCPENZ	6
CLKIN_R	7
All other single-ended signals	8

10.1.4 Power and Ground Planes

The following are recommendations for best performance:

- Solid ground planes between each signal routing layer.
- Solid power planes for voltages.
- Power and ground pins should be connected to these planes through a via for each pin.
- Trace lengths for the component power and ground pins should be minimized to 0.100 inches or less.

- Vias should be spaced out to avoid forming slots on the power planes.
- High speed signals should not cross over a slot in the adjacent power planes.
- Placing extra vias is not required if there are sufficient ground vias due to normal ground connections of devices.

10.1.5 Power Vias

Power and Ground pins of each component shall be connected to the power and ground planes with a via for each pin. Avoid sharing vias to the power plane among multiple power pins, where possible. Trace lengths for component power and ground pins should be minimized (ideally, less than 0.100 inch). Unused or spare device pins that are connected to power or ground may be connected together with a single via to power or ground. The minimum spacing between vias shall be 0.050 inch to prevent slots from being developed on the ground plane.

10.1.6 Decoupling

Decoupling capacitors must be located as near as possible to the DLPC910 voltage supply pins. Capacitors should not share vias. The DLPC910 power pins can be connected directly to the decoupling capacitor (no via) if the trace is less than 0.03 inches. Otherwise the component should be tied to the voltage or ground plane through a separate via. All capacitors should be connected to the power planes with trace lengths less than 0.05 inches.

10.1.7 Flex Connector Plating

For designs using the Texas Instruments designed reference flex cable, plate all the pad area on the top layer of flex connection with a minimum of 35 and maximum 50 micro-inches of electrolytic hard gold over a minimum of 100 micro-inches of electrolytic nickel.

10.2 Layout Example

The PCB layer design may vary depending on system design. However, careful attention is required to meet design considerations. Table 25 shows a layer signal definition and Figure 17 shows a PCB stack-up. The PCB stack-up uses Hitachi 679gs as the dielectric material to improve the signal slew rate. Although the material shown is Rogers Theta, it is the same material as the Hitachi 679gs.

Table 25. Layer Definition

Top:	Signal
2:	GND
3:	Signal
4:	GND
5:	Signal
6:	GND
7:	Signal
8:	GND
9:	Split Power
10:	Split Power
11:	GND
12:	Signal
13:	GND
14:	Signal
15:	GND
16:	Signal
17:	GND
Bottom:	Signal

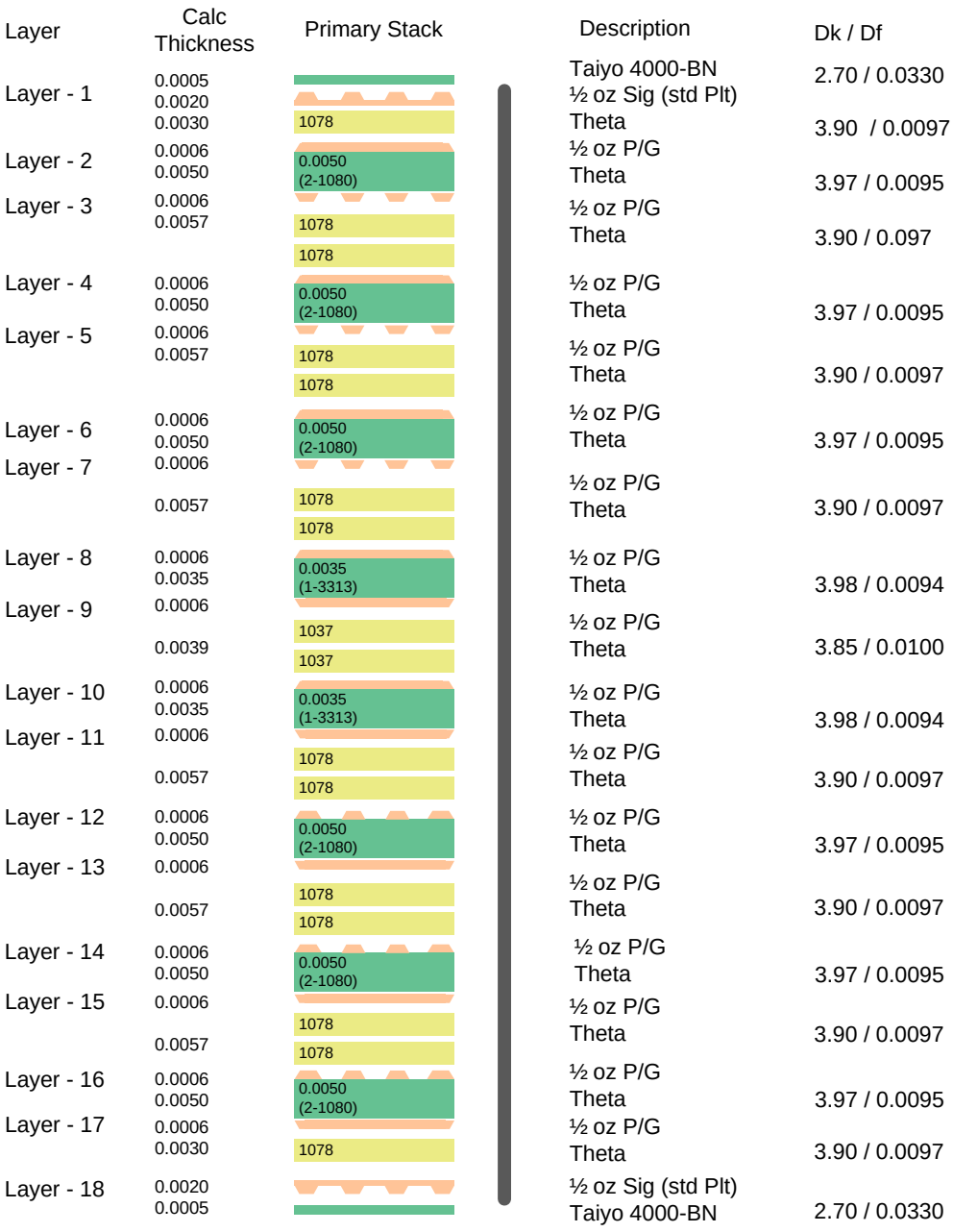


Figure 17. PCB Stack-Up

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

表 **26.** 部件号说明

TI 部件号	说明
DLPC910ZYR	DLPC910 数字控制器

11.1.2 器件标记

器件标记由德州仪器 (TI) 的供应商控制。 德州仪器 (TI) 封装包括 TI 部件号标识。

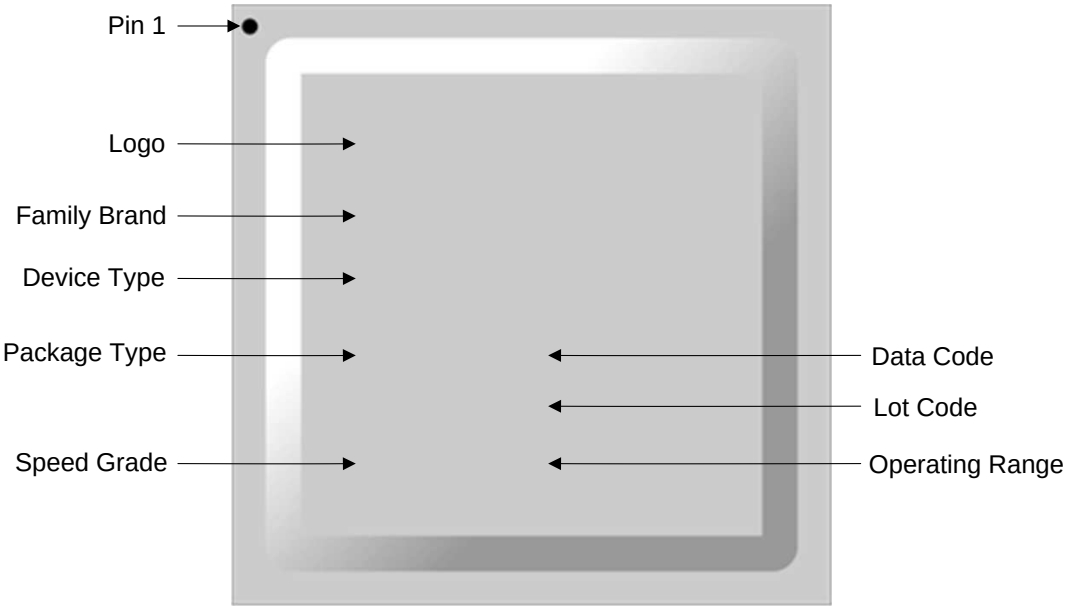


图 **18. DLPC910** 器件标记

11.2 文档支持

11.2.1 相关文档

以下文档包含关于 DLPC910 配套芯片组组件的更多信息：

- 《DLPR910YVA PROM 数据表》（文献编号：DLPS065）
- 《DLP9000XFLS DMD 数据表》（文献编号：DLPS036）

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
DLP is a registered trademark of Texas Instruments Inc.
Virtex, Xilinx are registered trademarks of Xilinx, Inc.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或"增强型塑料"的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC910ZYR	ACTIVE	FCBGA	ZYR	676	1	TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

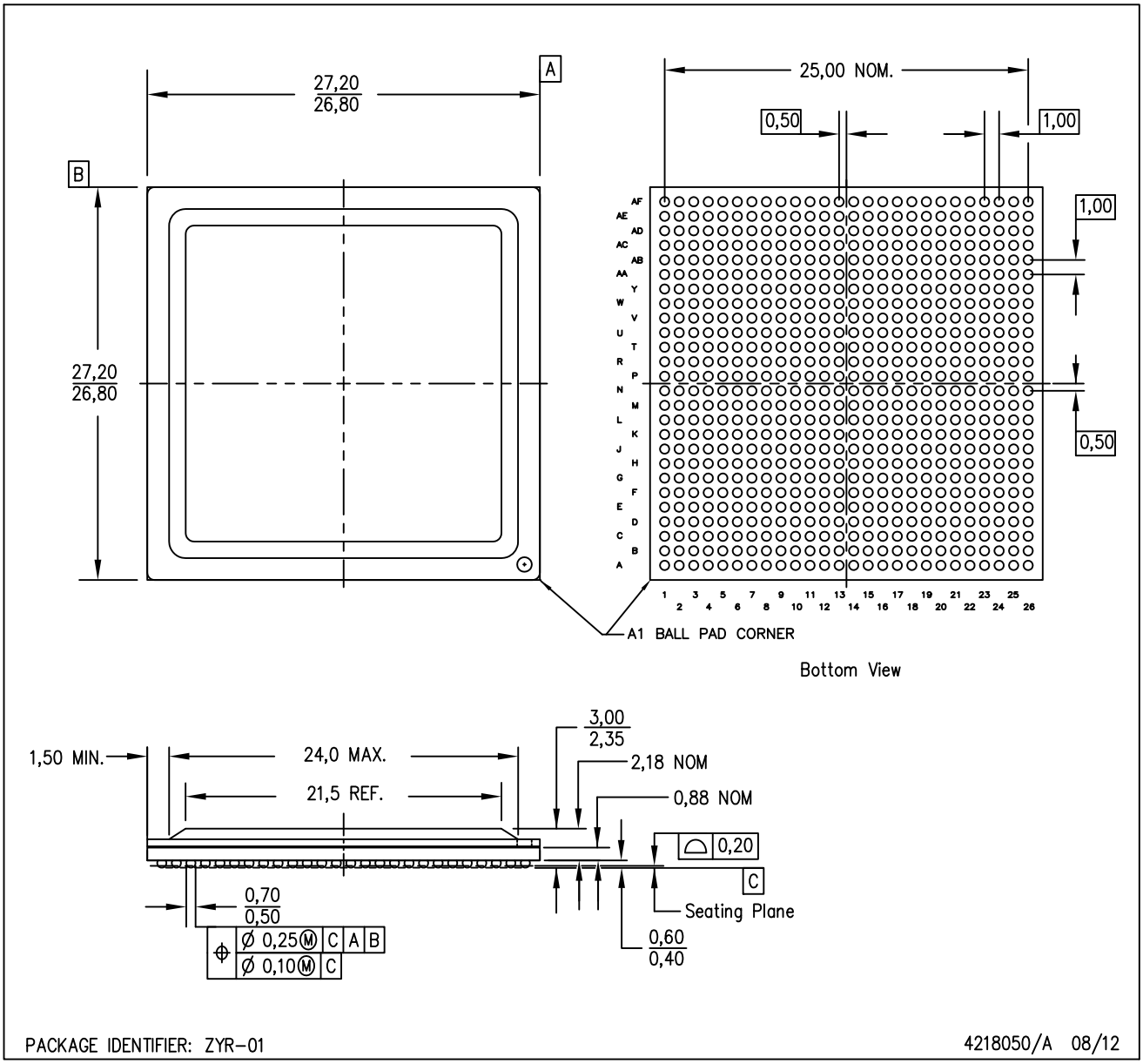
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

ZYR (S–PBGA–N676) PLASTIC BALL GRID ARRAY



PACKAGE IDENTIFIER: ZYR–01 4218050/A 08/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free solder ball.

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122