DLPR910 配置 PROM

1 特性

- 预编程的 Xilinx®PROM 用于配置 DLPC910ZYR
- 数据传输速率高达 33Mbps
- 兼容 1.8V 到 3.3V 的 I/O 引脚
- 1.8V 内核电源电压
- 工作温度范围：-40°C 至 +85°C

2 应用

- 平版印刷
  - 直接成像
  - 平板显示器
  - 印刷电路板制造
- 工业
  - 3D 打印
  - 用于机器视觉的 3D 扫描仪
  - 质量控制
- 显示器
  - 3D 成像
  - 智能和自适应照明
  - 增强现实和信息覆盖

3 说明

DLPR910 器件是一款经编程的 PROM，用于正确配置 DLPC910，从而为 DLP9000X 数字微镜器件 (DMD) 和 DLP6500 系列 DMD 的可靠运行提供支持。DLPR910 配置确保了 DLPC910 能够采用随机行寻址选项和 Load4 能力，以大于 61 千兆位/秒 (Gbps) 的像素数据速率（对于 DLP9000X）和高达 24Gbps 的像素数据速率（对于 DLP6500 系列）运行 DMD。中添加了 DLPR4101“Load 4”增强功能

DLPR910 器件属于 DLP®高级照明控制产品组合中的多组件芯片组。一套专用的芯片组能够使开发人员更加轻松地访问 DMD 并使用高速而独立的微镜控制。

DLPC910 配置程序仅在 DLPR910 内可用。DLPR910 需要与 DLPC910 和 DLP9000X DMD 或 DLP6500 系列 DMD搭配使用，以确保芯片组可靠运行。

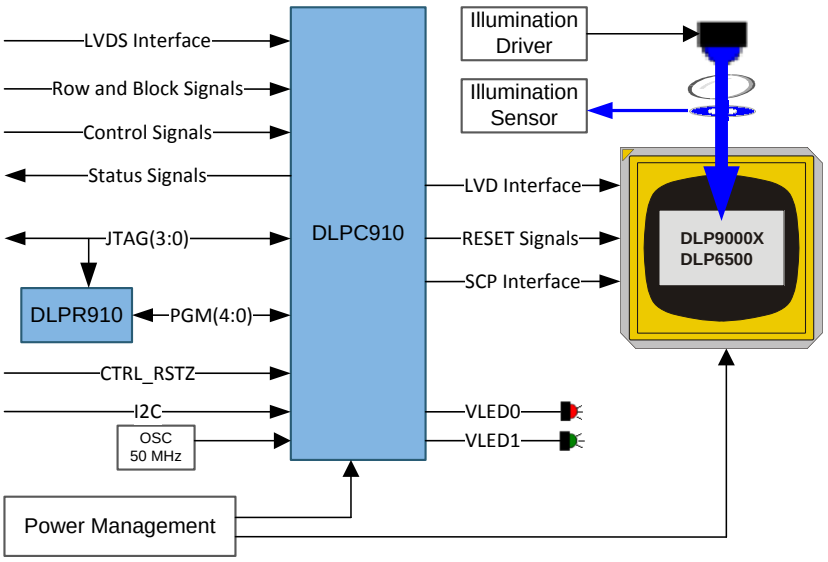
关于 DLPR910 的完整电气和机械规范，请参见 XCF16P 产品规范 (www.xilinx.com)。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DLPR910	DSBGA (48)	8.00mm × 9.00mm × 1.20mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (October 2015) to Revision B **Page**

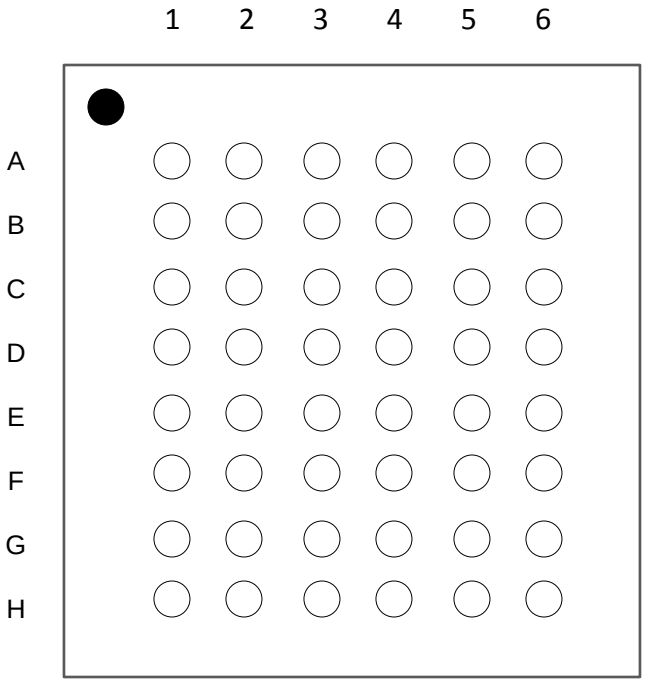
- 更新了*说明*以包含其他支持的 DMD。 ... 1
- Update document to include additional supported DMD in *Detailed Description*. ... 7
- Added typical application schematic for newly supported DMD in *Typical Application* ... 10
- 更新了*器件标记*。 ... 12

Changes from Original (September 2015) to Revision A **Page**

- 将器件状态从“产品预览”更改为“生产数据” ... 1

5 Pin Configuration and Functions

YVA Package
48-Pin DSBGA
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
GND	A1	G	Ground
GND	A2	G	Ground
OE/$\overline{\text{RESET}}$	A3	I/O	Output Enable/$\overline{\text{RESET}}$ (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA and CLKOUT outputs are placed in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable. **Pin must be pulled High using an external 4.7-kΩ pull-up to V_{CCO}.**
DNC	A4	—	Do Not Connect. Leave unconnected.
D6	A5	—	Do Not Connect. Leave unconnected.
D7	A6	—	Do Not Connect. Leave unconnected.
V_{CCINT}	B1	P	Positive 1.8-V supply voltage for internal logic.
V_{CCO}	B2	P	Positive 3.3-V and 1.8-V supply voltage connected to the output voltage drivers and internal buffers.
CLK	B3	I	Configuration clock input. Each rising edge on the CLK input increments the internal address counter. **Pin must be pulled High and Low using an external 100-Ω pull-up to V_{CCO} and an external 100-Ω pull-down to Ground. Place resistors close to pin.**
($\overline{\text{CE}}$)	B4	I	Chip Enable Input. When ($\overline{\text{CE}}$) is High, the device is put into low-power standby mode, the address counter is reset, and the DATA and CLKOUT outputs are placed in a high impedance state.
D5	B5	—	Do Not Connect. Leave unconnected.
GND	B6	G	Ground

(1) P = Power
G = Ground
I = Input
O = Output

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BUSY	C1	—	Do Not Connect. Leave unconnected.
CLKOUT	C2	—	Do Not Connect. Leave unconnected.
DNC	C3	—	Do Not Connect. Leave unconnected.
DNC	C4	—	Do Not Connect. Leave unconnected.
D4	C5	—	Do Not Connect. Leave unconnected.
V_{CCO}	C6	P	Positive 3.3-V and 1.8-V supply voltage connected to the output voltage drivers and internal buffers.
($\overline{CF}$)	D1	I	Configuration pin. **The ($\overline{CF}$) pin must be pulled High using an external 4.7-kΩ pull-up to V_{CCO}**. Selects serial mode configuration.
($\overline{CEO}$)	D2	—	Do Not Connect. Leave unconnected.
DNC	D3	—	Do Not Connect. Leave unconnected.
DNC	D4	—	Do Not Connect. Leave unconnected.
D3	D5	—	Do Not Connect. Leave unconnected.
V_{CCO}	D6	P	Positive 3.3-V and 1.8-V supply voltage connected to the output voltage drivers and internal buffers.
V_{CCINT}	E1	P	Positive 1.8-V supply voltage for internal logic.
TMS	E2	I	JTAG Mode Select Input. TMS has an internal 50-kΩ resistive pull-up to V_{CCJ}.
DNC	E3	—	Do Not Connect. Leave unconnected.
DNC	E4	—	Do Not Connect. Leave unconnected.
D2	E5	—	Do Not Connect. Leave unconnected.
TDO	E6	O	JTAG Serial Data Output. TDO has an internal 50-kΩ resistive pull-up to V_{CCJ}.
GND	F1	G	Ground
DNC	F2	—	Do Not Connect. Leave unconnected.
DNC	F3	—	Do Not Connect. Leave unconnected.
DNC	F4	—	Do Not Connect. Leave unconnected.
GND	F5	G	Ground
GND	F6	G	Ground
TDI	G1	I	JTAG Serial Data Input. TDI has an internal 50k-Ω resistive pull-up to V_{CCJ}.
DNC	G2	—	Do Not Connect. Leave unconnected.
REV_SEL0	G3	I	Revision Select [1:0] Inputs. When the ($\overline{EN\_EXT\_SEL}$) is Low, the Revision Select pins are used to select the design revision to be enabled. The Revision Select [1:0] inputs have an internal 50-kΩ resistive pull-up to V_{CCO}. **The (REV_SEL0) pin must be pulled Low using an external 10-kΩ pull-down to Ground**. **The (REV_SEL1) pin must be connected to Ground**.
REV_SEL1	G4	I	
V_{CCO}	G5	P	Positive 3.3-V and 1.8-V supply voltage connected to the output voltage drivers and internal buffers.
V_{CCINT}	G6	P	Positive 1.8-V supply voltage for internal logic.
GND	H1	G	Ground
VCCJ	H2	P	Positive 3.3-V JTAG I/O supply voltage connected to the TDO output voltage driver and TCK, TMS and TDI input buffers.
TCK	H3	I	JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.
($\overline{EN\_EXT\_SEL}$)	H4	I	External Selection Input. ($\overline{EN\_EXT\_SEL}$) has an internal 50-kΩ resistive pull- up to V_{CCO}. **The ($\overline{EN\_EXT\_SEL}$) pin must be connected to Ground**.
D1	H5	—	Do Not Connect. Leave unconnected.
D0	H6	O	DATA output pin to provide data for configuring the DLPC910 in serial mode.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (see (1) (2))

			MIN	MAX	UNIT
V_{CCINT}	Internal supply voltage	Relative to ground	–0.5	2.7	V
V_{CCO}	I/O supply voltage	Relative to ground	–0.5	4.0	V
V_{IN}	Input voltage with respect to ground	V_{CCO} < 2.5 V	–0.5	3.6	V
		V_{CCO} ≥ 2.5 V	–0.5	3.6	V
V_{TS}	Voltage applied to high-impedance output	V_{CCO} < 2.5 V	–0.5	3.6	V
		V_{CCO} ≥ 2.5 V	–0.5	3.6	V
T_J	Junction temperature			125	°C
T_{stg}	Storage temperature, ambient		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA. During transitions, the device pins can undershoot to –2 V or overshoot to 7 V, provided this overshoot or undershoot lasts less then 10 ns and with the forcing current being limited to 200 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2) (3)	2000	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC Standard JESD22-A114A (C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CCINT}	Internal voltage supply		1.65	1.8	2.0	V
V_{CCO}	Supply voltage for output drivers	3.3-V operation	3.0	3.3	3.6	V
V_{IL}	Low-level input voltage	3.3-V operation	0	–	0.8	V
V_{IH}	High-level input voltage	3.3-V operation	2.0	–	3.6	V
V_O	Output voltage		0	–	V_{CCO}	V
t_{IN}	Input signal transition time (measured between 10% V_{CCO} and 90% V_{CCO})		–	–	500	ns
T_A	Operating ambient temperature		–40	–	85	°C

6.4 Thermal Information

Refer to the XCF16P product specifications at www.xilinx.com.

6.5 Electrical Characteristics

Refer to the XCF16P product specifications at www.xilinx.com.

6.6 Supply Voltage Requirements for Power-On Reset and Power-Down

(see (1))

		MIN	MAX	UNIT
t_{VCC}	V_{CCINT} rise time from 0 V to nominal voltage (2)	0.2	50	ms
V_{CCPOR}	POR threshold for V_{CCINT} supply	0.5	–	V
t_{OER}	OE/$\overline{\text{RESET}}$ release delay following POR (3)	0.5	30	ms
V_{CCPD}	Power-down threshold for V_{CCINT} supply	–	0.5	V
t_{RST}	Time required to trigger a device reset when the V_{CCINT} supply drops below the maximum V_{CCPD} threshold	10	–	ms

(1) V_{CCINT}, V_{CCO}, and V_{CCJ} supplies can be applied in any order.
(2) At power up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified T_{VCC} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Figure 6, in the Xilinx XCF16P (v2.18) Product Specification for more information.
(3) If the V_{CCINT} and V_{CCO} supplies do not reach their respective recommended operating conditions before the OE/$\overline{\text{RESET}}$ pin is released, then the configuration data from the PROM is not available at the recommended threshold levels. The configuration sequence must be delayed until both V_{CCINT} and V_{CCO} have reached their recommended operating conditions.

6.7 Timing Requirements

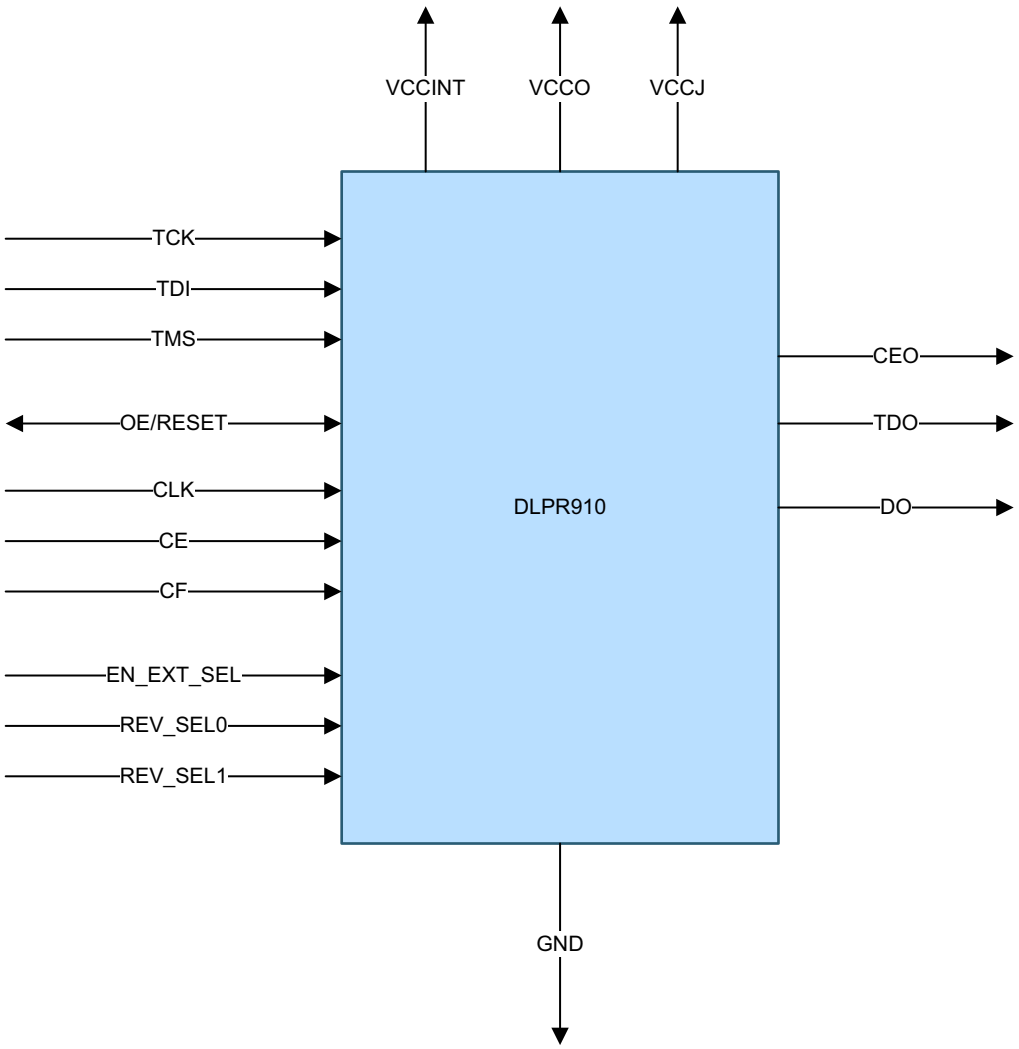
Refer to the XCF16P product specifications at www.xilinx.com.

7 Detailed Description

7.1 Overview

The configuration bit stream stored in the DLPR910 supports reliable operation of the DLPC910 with the DLP9000X DMD or the DLP6500 family of DMDs. The DLPC910 digital controller loads this configuration bit stream from the DLPR910.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Data Interface

7.3.1.1 Data Outputs

The DLPR910 is configured for serial mode operation, where D0 is the data output pin. D0 output pin provides a serial connection to the DLPC910, where the configuration is read out by the DLPC910.

7.3.1.2 Configuration Clock Input

The configuration CLK is connected to the DLPC910 in master mode, where the DLPC910 provides the clock pulses to read the configuration from the DLPR910.

Feature Description (continued)

7.3.1.3 Output Enable and Reset

When the OE/(RESET) input is held low, the address counter is reset and the Data and CLKOUT outputs are placed in high-impedance state. **OE/(RESET) must be pulled High using an external 4.7-kΩ pull-up to V_{CCO}.**

7.3.1.4 Chip Enable

The (CE) input is asserted by the DLPC910 to enable the Data and CLKOUT outputs. When (CE) is held high, the DLPR910 address counter is reset, and the Data and CLKOUT outputs are placed in high-impedance states.

7.3.1.5 Configuration Pulse

The DLPR910 is configured in serial mode when the Configuration Pulse (CF) is held high and (CE) and OE are enabled. New data is available a short time after each rising clock edge.

7.3.1.6 Revision Selection

REV_SEL_0, REV_SEL_1, and (EN_EXT_SEL) signals are used for selecting which revision to be the default. Setting all three signals to GND will default to revision 0 for simple DLPR910 setup.

7.4 Device Functional Modes

To successfully program the DLPC910 upon power-up, the DLPR910 must be configured and connected to the DLPC910 as shown in Figure 1.

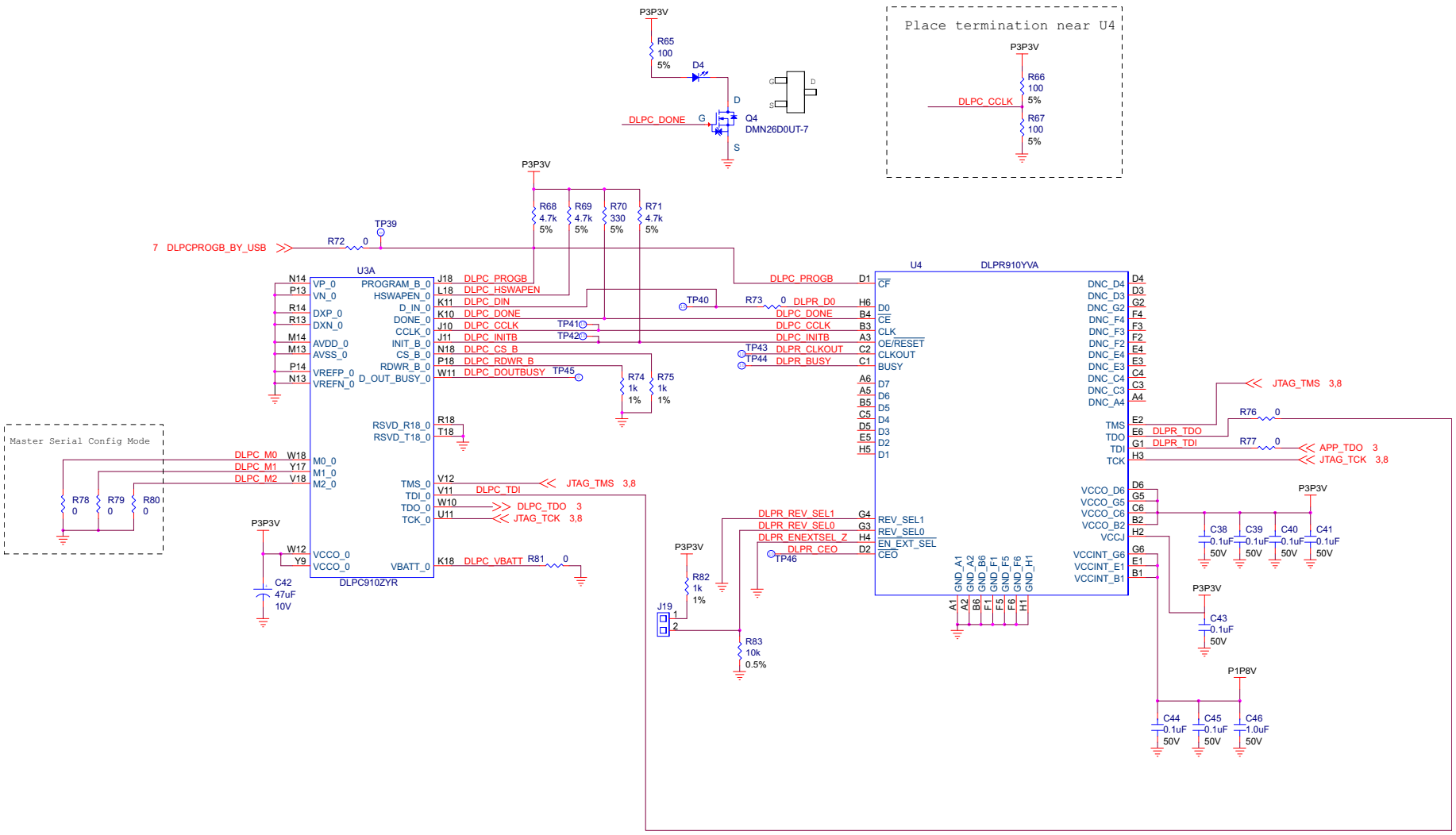


Figure 1. DLPC910 and DLPR910 Connection Schematic

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLPR910 configuration PROM comes pre-programmed with configuration code for the DLPC910. Upon power-up, the DLPC910 and the DLPR910 handshake with each other to enable configuration information to be sent from the DLPR910 to the DLPC910, such that the DLPC910 can configure itself for proper operation within the application. Without the DLPR910 properly connected to the DLPC910 in the application system, the DLPC910 would not be able to boot itself and the system would remain inoperable.

8.2 Typical Application

A typical use case for a high speed lithography application is shown in Figure 2 and in Figure 3. Both applications offer continuous run of printing by changing the digitally created patterns without stopping the imaging head. The DLPR910 prom configures the DLPC910 digital controller to reliably operate with the DLP9000X DMD or the DLP6500 DMDs. These chipset combinations provide an ideal back-end imager that takes in digital images at 2560 × 1600 and 1920 x 1080 in resolution to achieve speeds greater than 61 Gigabits per second (Gbps) and 24 Gbps respectively. For complete details of this typical application refer to the DLPC910 data sheet listed in *相关文档*.

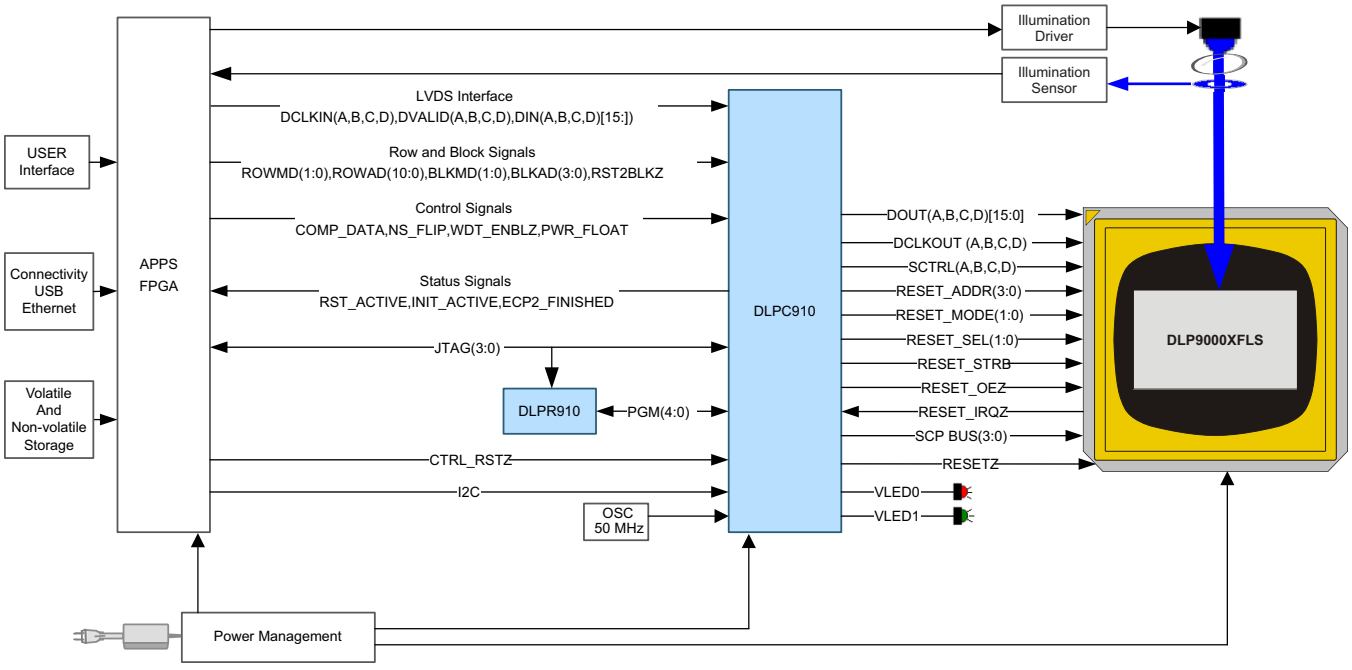


Figure 2. Typical High Speed DLP9000X Application Schematic

Typical Application (continued)

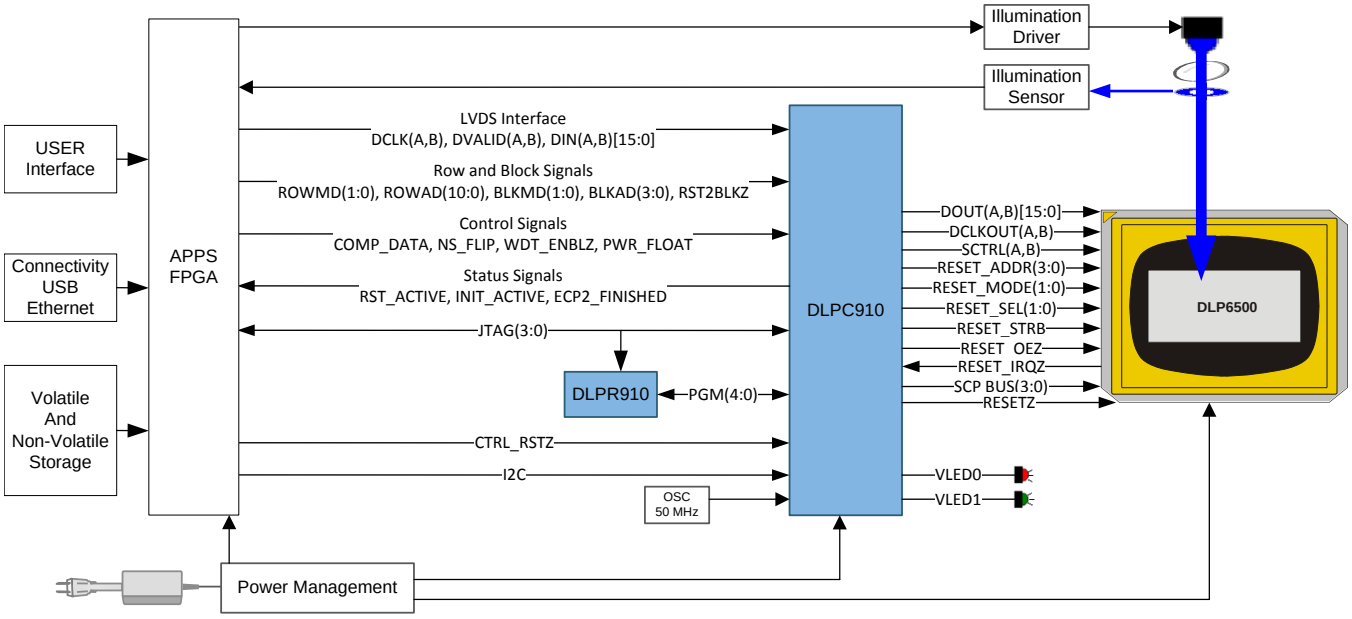


Figure 3. Typical High Speed DLP6500 Application Schematic

8.2.1 Design Requirements

The DLPR910 is part of a multi-chipset solution, and it is required to be coupled with the DLPC910 for reliable operation of the DLP9000X DMD or the DLP6500 family of DMDs. For more information, refer to the DLPC910 datasheet listed in *相关文档*.

9 Power Supply Recommendations

The DLPR910 uses two power supply rails as shown in Table 1.

Table 1. DLPR910 Power Supply Rails

SUPPLY	POWER PINS	COMMENTS
1.8 V	V_{CCINT1}, V_{CCINT2}, and V_{CCINT3}	All V_{CCINT} pins must be connected with a 0.1-µF decoupling capacitor to GND.
3.3 V	V_{CCO1},V_{CCO2},V_{CCO3}, V_{CCO4}, and V_{CCJ}	All V_{CCO} and V_{CCJ} pins must be connected with a 0.1-µF decoupling capacitor to GND.

10 Layout

10.1 Layout Guidelines

The DLPR910 is part of a multi-chipset solution, and it is required to be coupled with the DLPC910 for reliable operation of the DLP9000X DMD or the DLP6500 family of DMDs. Refer to the DLPC910 datasheet listed in *相关文档* for a layout example for this multi-chipset solution.

11 器件和文档支持

11.1 器件支持

11.1.1 器件兼容性

TI 器件型号	早于“B”版本的 DMD(1)	“B”版本或更高版本的 DMD(1)
DLPR910YVA	兼容	不兼容
DLPR910AYVA	兼容	兼容

(1) 请参阅“器件和文档支持”下每个单独的 DMD 产品说明书，以确定 DMD 的位置和版本。

11.1.2 器件命名规则

表 2. 器件型号 说明

TI 器件型号	说明	参考编号
DLPR910AYVA	DLPR910 配置 PROM	2514595-0002

11.1.3 器件标记

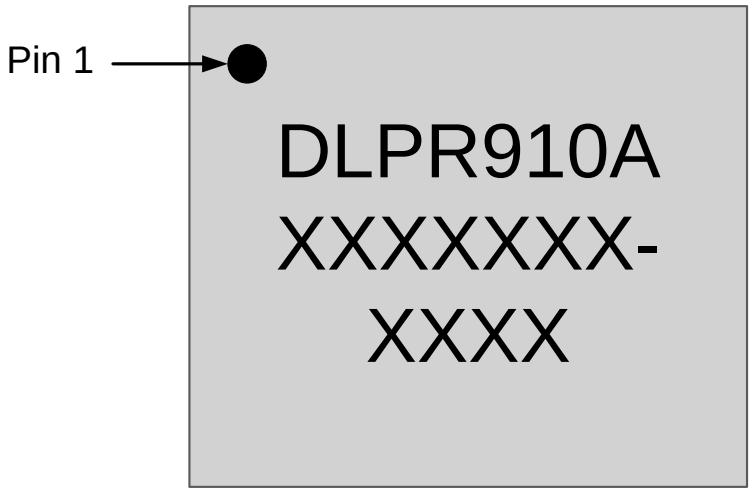


图 4. DLPR910 器件标记

其中 XXXXXXX-XXXX 是表 2 中的参考号。

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- DLPC910ZYR 产品说明书 (DLPS064)
- DLP9000(X) 产品说明书 (DLPS036)
- DLP6500 A 类产品说明书 (DLPS040)
- DLP6500 S600 产品说明书 (DLPS053)
- 《XCF16P 数据表》(www.xilinx.com)

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

E2E is a trademark of Texas Instruments.
DLP is a registered trademark of Texas Instruments.
Xilinx is a registered trademark of Xilinx, Inc.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。要获得这份数据表的浏览器版本，请查阅左侧导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPR910AYVA	ACTIVE	DSBGA	YVA	48	1	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

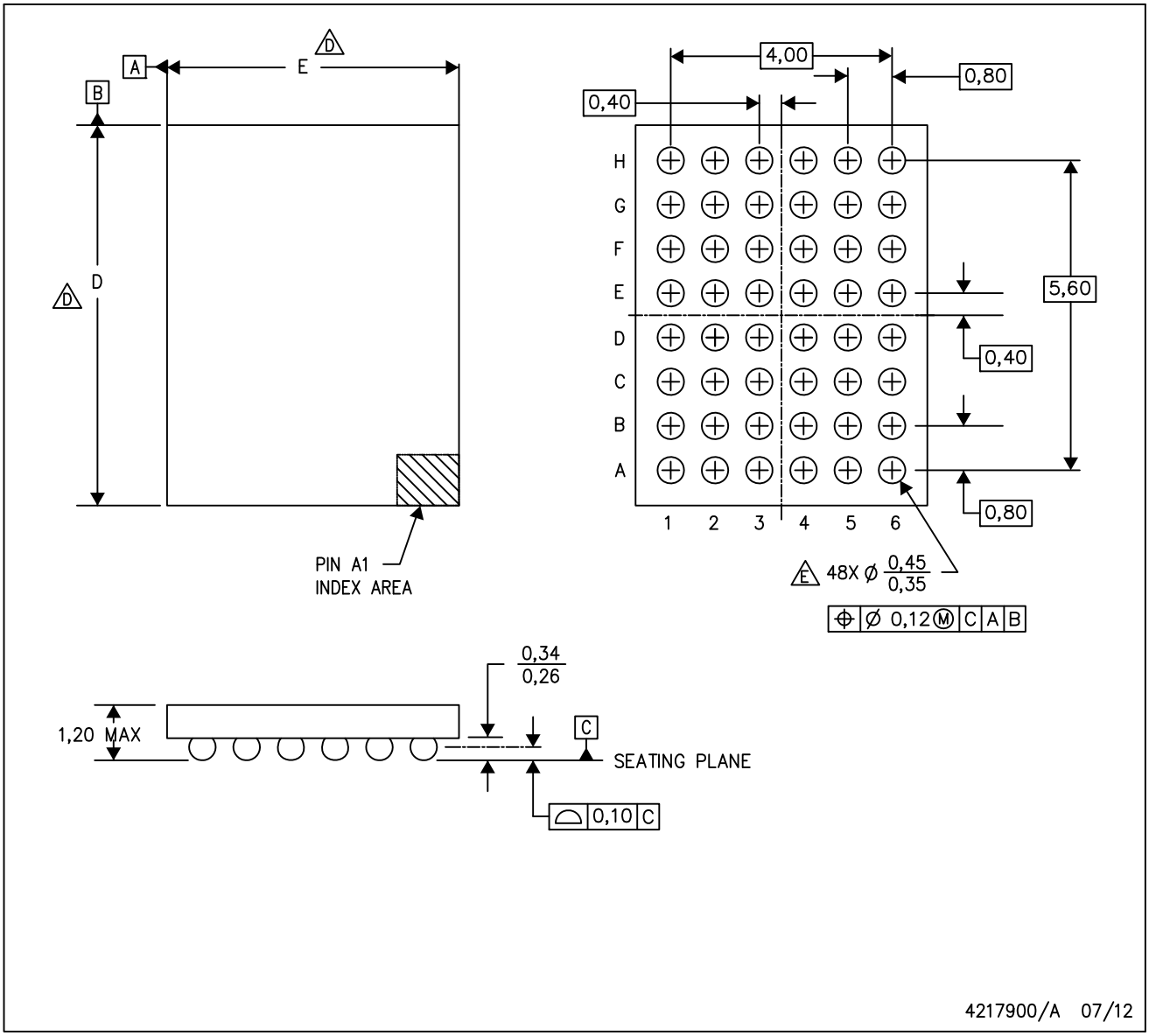
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

YVA (R–XBGA–N48) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population.
6 x 8 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

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