DLP3010LC 0.3 720p DMD

1 Features

- 0.3-Inch (7.93-mm) diagonal micromirror array
  - 1280 × 720 array of aluminum micrometer-sized mirrors, in an orthogonal layout
  - 5.4 – micron micromirror pitch
  - ±17° micromirror tilt (relative to flat surface)
  - Side illumination for optimal efficiency and optical engine size
  - Polarization independent aluminum micromirror surface
- 8-Bit SubLVDS input data bus
- Dedicated DLPC3478 display and light controller and DLPA200x or DLPA300x PMIC/LED driver for reliable operation

2 Applications

- Integrated display and 3D depth capture
  - Smart phone, tablets, laptop, camera
  - Battery-powered mobile accessory
- 3D depth capture: 3D camera, 3D reconstruction, AR/VR, dental scanner
- 3D machine vision: robotics, metrology, in-line inspection (AOI)
- 3D biometrics: facial and finger print recognition
- Light exposure: 3D printers, programmable spatial and temporal light exposure

3 Description

The DLP3010LC digital micromirror device (DMD) is a digitally controlled micro-opto-electromechanical system (MOEMS) spatial light modulator (SLM). When coupled to an appropriate optical system, the DMD displays a very crisp and high quality image or video. This DMD is a component of the chipset comprising the DMD, DLPC3478 display and light controller, and DLPA200x/DLPA300x PMIC/LED driver. The compact physical size of this DMD coupled with the controller and the PMIC/LED driver provides a complete system solution that enables small form factor, low power, and high-resolution, light-control applications like such as 3D scanners.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP3010LC	FQK (57)	18.20-mm × 7.00-mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

DLP3010LC 0.3 720p Chipset

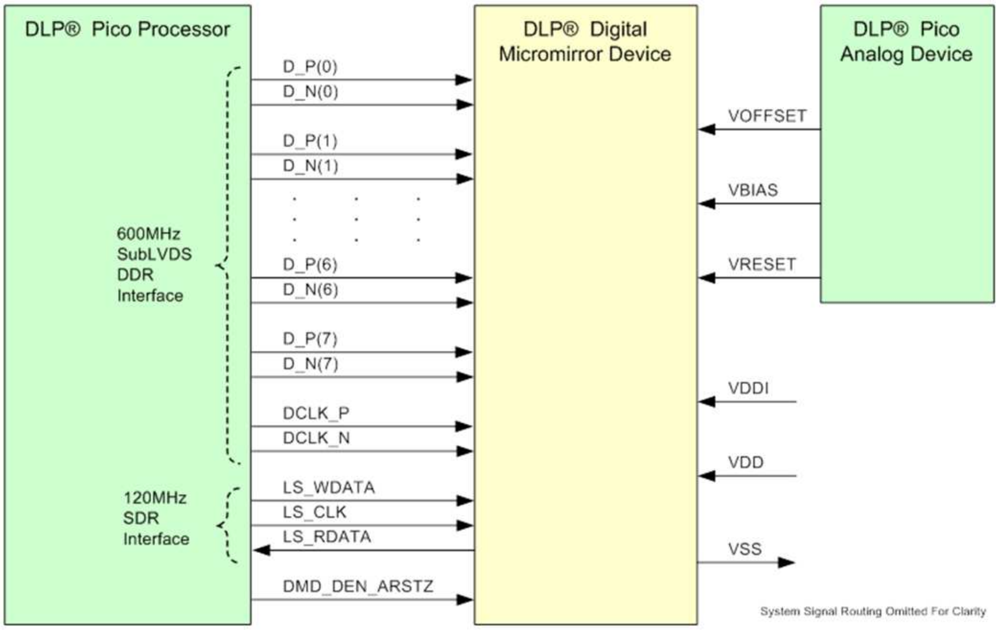


Table of Contents

1 **Features** 1
2 **Applications** 1
3 **Description** 1
4 **Revision History** 2
5 **Pin Configuration and Functions** 3
6 **Specifications** 6
  6.1 Absolute Maximum Ratings 6
  6.2 Storage Conditions 7
  6.3 ESD Ratings 7
  6.4 Recommended Operating Conditions 7
  6.5 Thermal Information 10
  6.6 Electrical Characteristics 10
  6.7 Timing Requirements 11
  6.8 Switching Characteristics 16
  6.9 System Mounting Interface Loads 16
  6.10 Physical Characteristics of the Micromirror Array . 17
  6.11 Micromirror Array Optical Characteristics 18
  6.12 Window Characteristics 20
  6.13 Chipset Component Usage Specification 20
  6.14 Software Requirements 20
7 **Detailed Description** 21
  7.1 Overview 21
  7.2 Functional Block Diagram 22
  7.3 Feature Description 23
  7.4 Device Functional Modes 23
  7.5 Optical Interface and System Image Quality Considerations 23
  7.6 Micromirror Array Temperature Calculation 24
  7.7 Micromirror Landed-On/Landed-Off Duty Cycle 25
8 **Application and Implementation** 29
  8.1 Application Information 29
  8.2 Typical Application 29
9 **Power Supply Recommendations** 32
  9.1 DMD Power Supply Power-Up Procedure 32
  9.2 DMD Power Supply Power-Down Procedure 32
  9.3 Power Supply Sequencing Requirements 33
10 **Layout** 35
  10.1 Layout Guidelines 35
  10.2 Layout Example 35
11 **Device and Documentation Support** 36
  11.1 Device Support 36
  11.2 Documentation Support 36
  11.3 Related Links 36
  11.4 Communnity Resources 36
  11.5 Trademarks 37
  11.6 Electrostatic Discharge Caution 37
  11.7 Glossary 37
12 **Mechanical, Packaging, and Orderable Information** 37

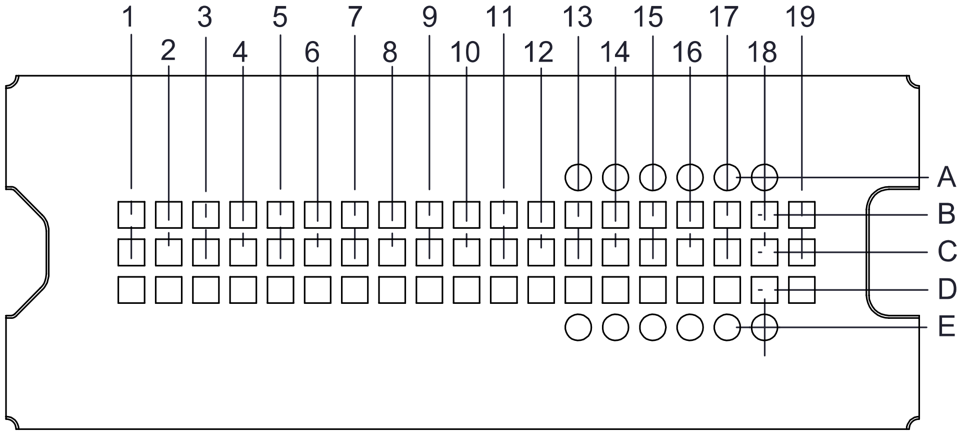
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2020	*	Initial release.

5 Pin Configuration and Functions

FQK Package
57-Pin LGA
(Bottom View)



Pin Functions – Connector Pins(1)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH(2) (mm)
NAME	NO.					
DATA INPUTS						
D_N(0)	C9	I	SubLVDS	Double	Data, Negative	10.54
D_P(0)	B9	I	SubLVDS	Double	Data, Positive	10.54
D_N(1)	D10	I	SubLVDS	Double	Data, Negative	13.14
D_P(1)	D11	I	SubLVDS	Double	Data, Positive	13.14
D_N(2)	C11	I	SubLVDS	Double	Data, Negative	14.24
D_P(2)	B11	I	SubLVDS	Double	Data, Positive	14.24
D_N(3)	D12	I	SubLVDS	Double	Data, Negative	14.35
D_P(3)	D13	I	SubLVDS	Double	Data, Positive	14.35
D_N(4)	D4	I	SubLVDS	Double	Data, Negative	5.89
D_P(4)	D5	I	SubLVDS	Double	Data, Positive	5.89
D_N(5)	C5	I	SubLVDS	Double	Data, Negative	5.45
D_P(5)	B5	I	SubLVDS	Double	Data, Positive	5.45
D_N(6)	D6	I	SubLVDS	Double	Data, Negative	8.59
D_P(6)	D7	I	SubLVDS	Double	Data, Positive	8.59
D_N(7)	C7	I	SubLVDS	Double	Data, Negative	7.69
D_P(7)	B7	I	SubLVDS	Double	Data, Positive	7.69
DCLK_N	D8	I	SubLVDS	Double	Clock, Negative	8.10
DCLK_P	D9	I	SubLVDS	Double	Clock, Positive	8.10
CONTROL INPUTS						
LS_WDATA	C12	I	LPSDR(1)	Single	Write data for low speed interface.	7.16
LS_CLK	C13	I	LPSDR	Single	Clock for low-speed interface	7.89

---

(1) Low speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

(2) Net trace lengths inside the package:
Relative dielectric constant for the FQK ceramic package is 9.8.
Propagation speed = 11.8 / sqrt (9.8) = 3.769 inches/ns.
Propagation delay = 0.265 ns/inch = 265 ps/inch = 10.43 ps/mm.

Pin Functions – Connector Pins[1] (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[2] (mm)
NAME	NO.					
DMD_DEN_ARSTZ	C14	I	LPSDR		Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode.	
LS_RDATA	C15	O	LPSDR	Single	Read data for low-speed interface	
POWER[3]						
VBIAS	C1	Power			Supply voltage for positive bias level at micromirrors	
VBIAS	C18	Power				
VOFFSET	D1	Power			Supply voltage for HVCMOS core logic. Supply voltage for stepped high level at micromirror address electrodes. Supply voltage for offset level at micromirrors.	
VOFFSET	D17	Power				
VRESET	B1	Power			Supply voltage for negative reset level at micromirrors.	
VRESET	B18	Power				
VDD	B6	Power			Supply voltage for LVCMOS core logic. Supply voltage for LPSDR inputs. Supply voltage for normal high level at micromirror address electrodes.	
VDD	B10	Power				
VDD	B19	Power				
VDD	C6	Power				
VDD	C10	Power				
VDD	C19	Power				
VDD	D2	Power				
VDD	D18	Power				
VDD	D19	Power				
VDDI	B2	Power			Supply voltage for SubLVDS receivers.	
VDDI	C2	Power				
VDDI	C3	Power				
VDDI	D3	Power				
VSS	B3	Ground			Common return. Ground for all power.	
VSS	B4	Ground				
VSS	B8	Ground				
VSS	B12	Ground				
VSS	B13	Ground				
VSS	B14	Ground				
VSS	B15	Ground				
VSS	B16	Ground				
VSS	B17	Ground				
VSS	C4	Ground				
VSS	C8	Ground				
VSS	C16	Ground				
VSS	C17	Ground				
VSS	D14	Ground				
VSS	D15	Ground				
VSS	D16	Ground				

(3) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.

Pin Functions – Test Pads

NUMBER	SYSTEM BOARD
A13	Do not connect
A14	Do not connect
A15	Do not connect
A16	Do not connect
A17	Do not connect
A18	Do not connect
E13	Do not connect
E14	Do not connect
E15	Do not connect
E16	Do not connect
E17	Do not connect
E18	Do not connect

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

			MIN	MAX	UNIT
Supply voltage	VDD	Supply voltage for LVCMOS core logic (2) Supply voltage for LPSDR low speed interface	–0.5	2.3	V
	VDDI	Supply voltage for SubLVDS receivers (2)	–0.5	2.3	V
	VOFFSET	Supply voltage for HVCMOS and micromirror electrode (2)(3)	–0.5	11	V
	VBIAS	Supply voltage for micromirror electrode (2)	–0.5	19	V
	VRESET	Supply voltage for micromirror electrode (2)	–15	0.5	V
	| VDDI–VDD |	Supply voltage delta (absolute value) (4)		0.3	V
	| VBIAS–VOFFSET |	Supply voltage delta (absolute value) (5)		11	V
	| VBIAS–VRESET |	Supply voltage delta (absolute value) (6)		34	V
Input voltage	Input voltage for other inputs LPSDR (2)		–0.5	VDD + 0.5	V
	Input voltage for other inputs SubLVDS (2)(7)		–0.5	VDDI + 0.5	V
Input pins	| VID |	SubLVDS input differential voltage (absolute value) (7)		810	mV
	IID	SubLVDS input differential current		10	mA
Clock frequency	f_{clock}	Clock frequency for low speed interface LS_CLK		130	MHz
	f_{clock}	Clock frequency for high speed interface DCLK		560	MHz
Environmental	T_{ARRAY} and T_{WINDOW}	Temperature – operational (8)	–20	90	°C
		Temperature – non-operational (8)	–40	90	°C
	T_{DP}	Dew Point Temperature - operating and non-operating (non-condensing)		81	°C
	$\|T_{DELTA}\|$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1 (9)		30	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above or below the *Recommended Operating Conditions* for extended periods may affect device reliability.

(2) All voltage values are with respect to the ground terminals (VSS). The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET.

(3) VOFFSET supply transients must fall within specified voltages.

(4) Exceeding the recommended allowable absolute voltage difference between VDDI and VDD may result in excessive current draw.

(5) Exceeding the recommended allowable absolute voltage difference between VBIAS and VOFFSET may result in excessive current draw.

(6) Exceeding the recommended allowable absolute voltage difference between VBIAS and VRESET may result in excessive current draw.

(7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.

(8) The highest temperature of the active array (as calculated by the *Micromirror Array Temperature Calculation*) or of any point along the Window Edge as defined in Figure 19. The locations of thermal test points TP2 and TP3 in Figure 19 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.

(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 19. The window test points TP2 and TP3 shown in Figure 19 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

6.2 Storage Conditions

applicable for the DMD as a component or non-operational in a system

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	85	°C
$T_{DP\text{-}AVG}$	Average dew point temperature, (non-condensing)(1)		24	°C
$T_{DP\text{-}ELR}$	Elevated dew point temperature range, (non-condensing)(2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		6	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE(4)					
VDD	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.65	1.8	1.95	V
VDDI	Supply voltage for SubLVDS receivers	1.65	1.8	1.95	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode(5)	9.5	10	10.5	V
VBIAS	Supply voltage for mirror electrode	17.5	18	18.5	V
VRESET	Supply voltage for micromirror electrode	–14.5	–14	–13.5	V
|VDDI–VDD|	Supply voltage delta (absolute value)(6)			0.3	V
|VBIAS–VOFFSET|	Supply voltage delta (absolute value)(7)			10.5	V
|VBIAS–VRESET|	Supply voltage delta (absolute value)(8)			33	V
CLOCK FREQUENCY					
f_{clock}	Clock frequency for low speed interface LS_CLK(9)	108		120	MHz
f_{clock}	Clock frequency for high speed interface DCLK(10)	300		600	MHz
	Duty cycle distortion DCLK	44%		56%	
SUBLVDS INTERFACE(10)					
$\| V_{ID} \|$	SubLVDS input differential voltage (absolute value) Figure 9, Figure 10	150	250	350	mV
V_{CM}	Common mode voltage Figure 9, Figure 10	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage Figure 9, Figure 10	575		1225	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance Figure 11	80	100	120	Ω
	100-Ω differential PCB trace	6.35		152.4	mm

(1) *Recommended Operating Conditions* are applicable after the DMD is installed in the final product.
(2) The functional performance of the device specified in this datasheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.
(3) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET.
(4) All voltage values are with respect to the ground pins (VSS).
(5) VOFFSET supply transients must fall within specified maximum voltages.
(6) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.
(7) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(8) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit.
(9) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(10) Refer to the SubLVDS timing requirements in *Timing Requirements*.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	NOM	MAX	UNIT
ENVIRONMENTAL					
T_{ARRAY}	Array Temperature – long-term operational(11)(12)(13)(14)	0		40 to 70(13)	°C
	Array Temperature - short-term operational, 25 hr max(12)(15)	–20		–10	
	Array Temperature - short-term operational, 500 hr max(12)(15)	–10		0	
	Array Temperature – short-term operational, 500 hr max(12)(15)	70		75	
$\|T_{DELTA}\|$	Absolute Temperature difference between any point on the window edge and the ceramic test point TP1 (16)			30	°C
T_{WINDOW}	Window temperature – operational(11)(17)			90	°C
$T_{DP\text{-}AVG}$	Average dew point temperature (non-condensing)(18)			24	°C
$T_{DP\text{-}ELR}$	Elevated dew point temperature range (non-condensing)(19)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			6	Months
ILL_{UV}	Illumination wavelengths < 420 nm(11)			0.68	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 420 nm and 700 nm			Thermally limited	
ILL_{IR}	Illumination wavelengths > 700 nm			10	mW/cm^2
ILL_{θ}	Illumination marginal ray angle(20)			55	deg

(11) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination will reduce device lifetime.
(12) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 19 and the Package Thermal Resistance using *Micromirror Array Temperature Calculation*.
(13) Per Figure 1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *Micromirror Landed-On/Landed-Off Duty Cycle* for a definition of micromirror landed duty cycle.
(14) Long-term is defined as the usable life of the device
(15) Short-term is the total cumulative time over the useful life of the device.
(16) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in Figure 19. The window test points TP2 and TP3 shown in Figure 19 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(17) Window temperature is the highest temperature on the window edge shown in Figure 19. The locations of thermal test points TP2 and TP3 in Figure 19 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(18) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(19) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
(20) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including Pond of Micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.

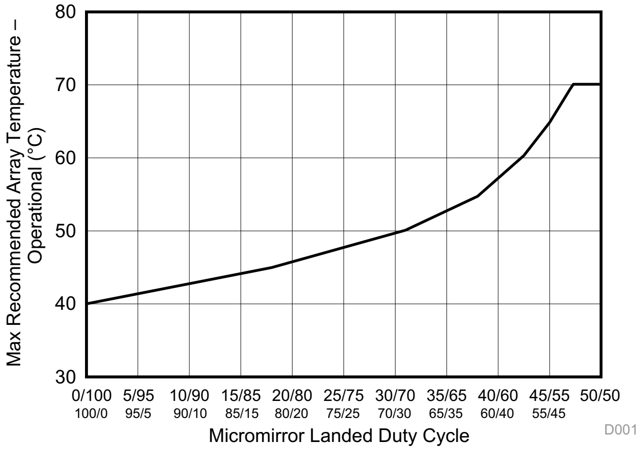


Figure 1. Maximum Recommended Array Temperature (Derating Curve)

6.5 Thermal Information

THERMAL METRIC(1)		DLP3010 FQK (LGA) 57 PINS	UNIT
Thermal resistance	Active area to test point 1 (TP1)(1)	5.4	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: VDD(3)(4)	VDD = 1.95 V			60.5	mA
		VDD = 1.8 V		54		
I_{DDI}	Supply current: VDDI(3)(4)	VDDI = 1.95 V			16.5	mA
		VDD = 1.8 V		11.3		
I_{OFFSET}	Supply current: VOFFSET(5)(6)	VOFFSET = 10.5 V			2.2	mA
		VOFFSET = 10 V		1.5		
I_{BIAS}	Supply current: VBIAS(5)(6)	VBIAS = 18.5 V			0.6	mA
		VBIAS = 18 V		0.3		
I_{RESET}	Supply current: VRESET(6)	VRESET = –14.5 V			2.4	mA
		VRESET = –14 V		1.7		
POWER(7)						
P_{DD}	Supply power dissipation: VDD(3)(4)	VDD = 1.95 V			118	mW
		VDD = 1.8 V		97.2		
P_{DDI}	Supply power dissipation: VDDI(3)(4)	VDDI = 1.95 V			32	mW
		VDD = 1.8 V		20		
P_{OFFSET}	Supply power dissipation: VOFFSET(5)(6)	VOFFSET = 10.5 V			23	mW
		VOFFSET = 10 V		15		
P_{BIAS}	Supply power dissipation: VBIAS(5)(6)	VBIAS = 18.5 V			11	mW
		VBIAS = 18 V		6		
P_{RESET}	Supply power dissipation: VRESET(6)	VRESET = –14.5 V			35	mW
		VRESET = –14 V		24		
P_{TOTAL}	Supply power dissipation: Total			162.2	219	mW
LPSDR INPUT(8)						
$V_{IH(DC)}$	DC input high voltage(9)		0.7 × VDD		VDD + 0.3	V
$V_{IL(DC)}$	DC input low voltage(9)		–0.3		0.3 × VDD	V
$V_{IH(AC)}$	AC input high voltage(9)		0.8 × VDD		VDD + 0.3	V
$V_{IL(AC)}$	AC input low voltage(9)		–0.3		0.2 × VDD	V
ΔV_T	Hysteresis ($V_{T+} – V_{T–}$)	Figure 12	0.1 × VDD		0.4 × VDD	V

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2) All voltage values are with respect to the ground pins (VSS).
(3) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.
(4) Supply power dissipation based on non–compressed commands and data.
(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(6) Supply power dissipation based on 3 global resets in 200 µs.
(7) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.
(8) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low-Power Double Data Rate (LPDDR)* JESD209B.

Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
I_{IL}	Low–level input current	VDD = 1.95 V; V_I = 0 V	–100			nA
I_{IH}	High–level input current	VDD = 1.95 V; V_I = 1.95 V			100	nA
LPSDR OUTPUT(10)						
V_{OH}	DC output high voltage	I_{OH} = –2 mA	0.8 × VDD			V
V_{OL}	DC output low voltage	I_{OL} = 2 mA			0.2 × VDD	V
CAPACITANCE						
C_{IN}	Input capacitance LPSDR	*f* = 1 MHz			10	pF
	Input capacitance SubLVDS	*f* = 1 MHz			10	pF
C_{OUT}	Output capacitance	*f* = 1 MHz			10	pF
C_{RESET}	Reset group capacitance	*f* = 1 MHz; (720 × 160) micromirrors	200		220	pF

(10) LPSDR specification is for pin LS_RDATA.

6.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

			MIN	NOM	MAX	UNIT
LPSDR						
t_r	Rise slew rate(1)	(30% to 80%) × VDD, Figure 3	1		3	V/ns
t_f	Fall slew rate(1)	(70% to 20%) × VDD, Figure 3	1		3	V/ns
t_r	Rise slew rate(2)	(20% to 80%) × VDD, Figure 4	0.25			V/ns
t_f	Fall slew rate(2)	(80% to 20%) × VDD, Figure 4	0.25			V/ns
t_c	Cycle time LS_CLK,	Figure 2	7.7	8.3		ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points, Figure 2	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points, Figure 2	3.1			ns
t_{su}	Setup time	LS_WDATA valid before LS_CLK ↑, Figure 2	1.5			ns
t_h	Hold time	LS_WDATA valid after LS_CLK ↑, Figure 2	1.5			ns
t_{WINDOW}	Window time(1)(3)	Setup time + Hold time, Figure 2	3			ns
$t_{DERATING}$	Window time derating(1)(3)	For each 0.25 V/ns reduction in slew rate below 1 V/ns, Figure 6		0.35		ns
SubLVDS						
t_r	Rise slew rate	20% to 80% reference points, Figure 5	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points, Figure 5	0.7	1		V/ns
t_c	Cycle time DCLK,	Figure 7	1.79	1.85		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points, Figure 7	0.79			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points, Figure 7	0.79			ns
t_{su}	Setup time	D(0:3) valid before DCLK ↑ or DCLK ↓, Figure 7				
t_h	Hold time	D(0:3) valid after DCLK ↑ or DCLK ↓, Figure 7				

---

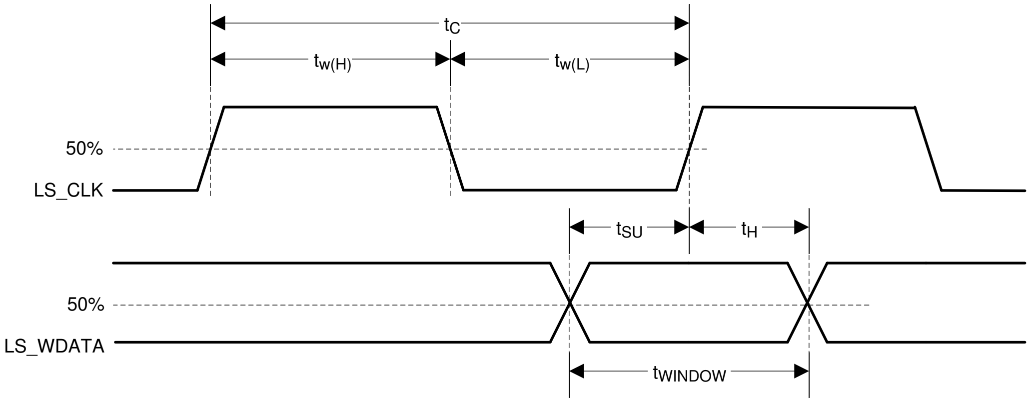
(1) Specification is for LS_CLK and LS_WDATA pins. Refer to LPSDR input rise slew rate and fall slew rate in Figure 3.
(2) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in Figure 4.
(3) Window time derating example: 0.5-V/ns slew rate increases the window time by 0.7 ns, from 3 to 3.7 ns.

Timing Requirements (continued)

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

			MIN	NOM	MAX	UNIT
t_{WINDOW}	Window time	Setup time + Hold time, Figure 7, Figure 8			0.3	ns
$t_{LVDS\text{-}ENABLE+REFGEN}$	Power-up receiver[4]				2000	ns

(4) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.



Low-speed interface is LPSDR and adheres to the *Electrical Characteristics* and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

Figure 2. LPSDR Switching Parameters

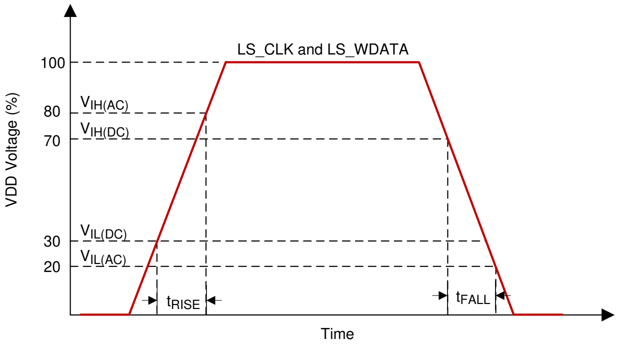


Figure 3. LPSDR Input Slew Rate

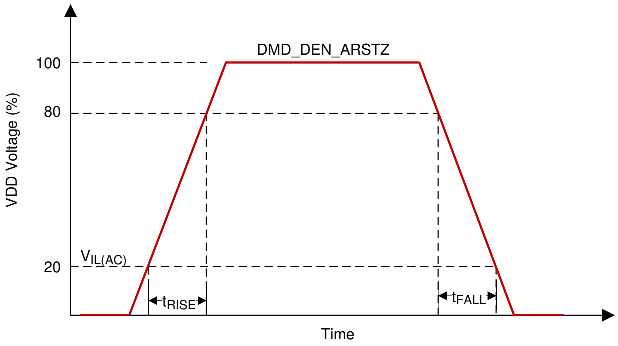


Figure 4. LPSDR Input Slew Rate

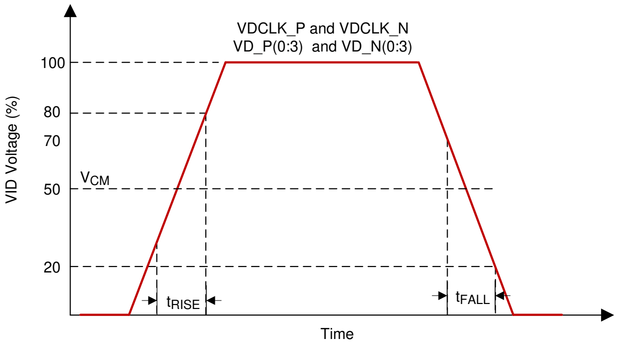


Figure 5. SubLVDS Input Rise and Fall Slew Rate

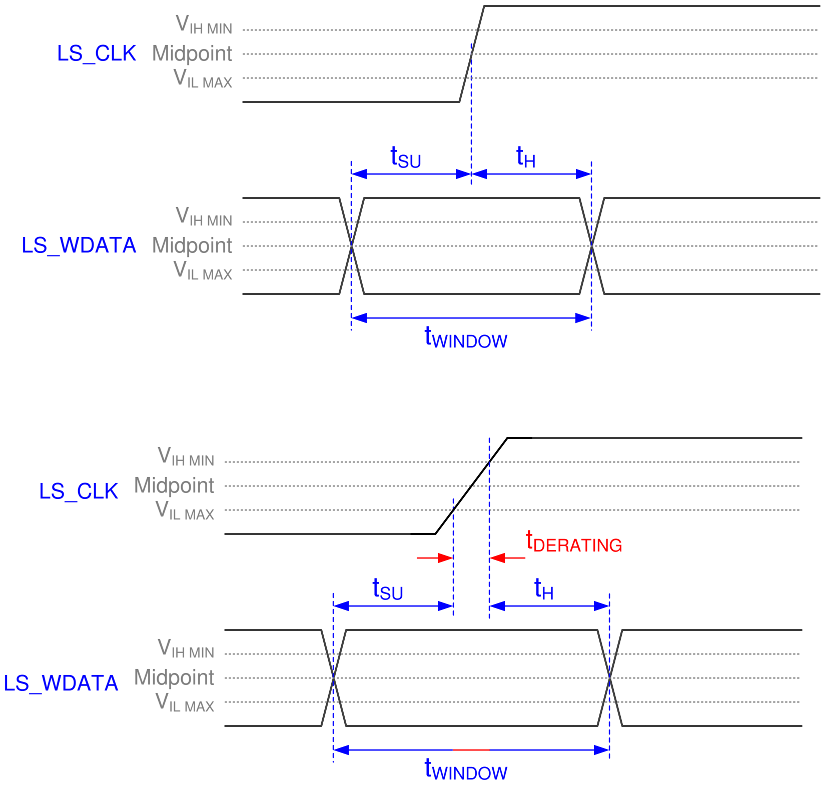


Figure 6. Window Time Derating Concept

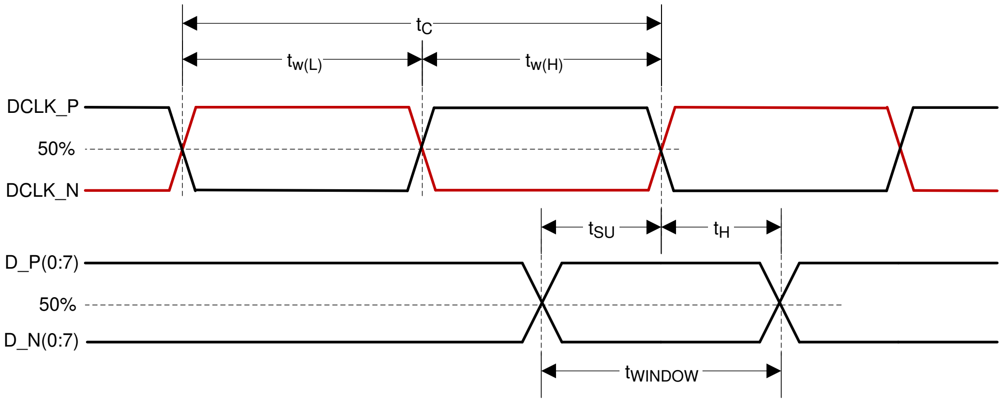
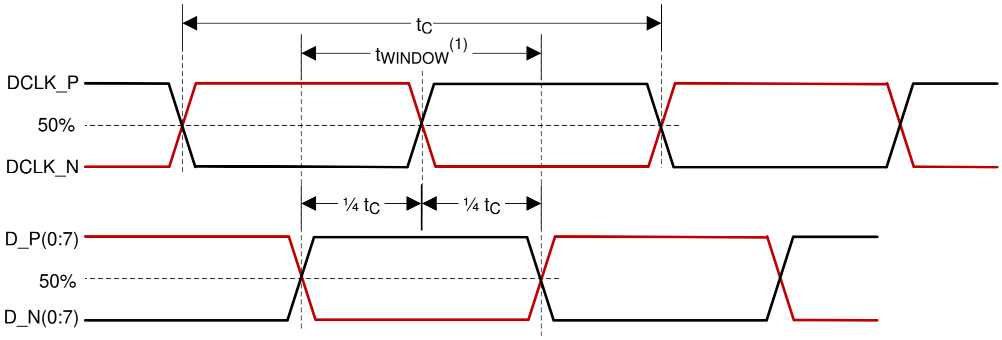


Figure 7. SubLVDS Switching Parameters



(1) High-speed training scan window

(2) Refer to *High-Speed Interface* for details

Figure 8. High-Speed Training Scan Window

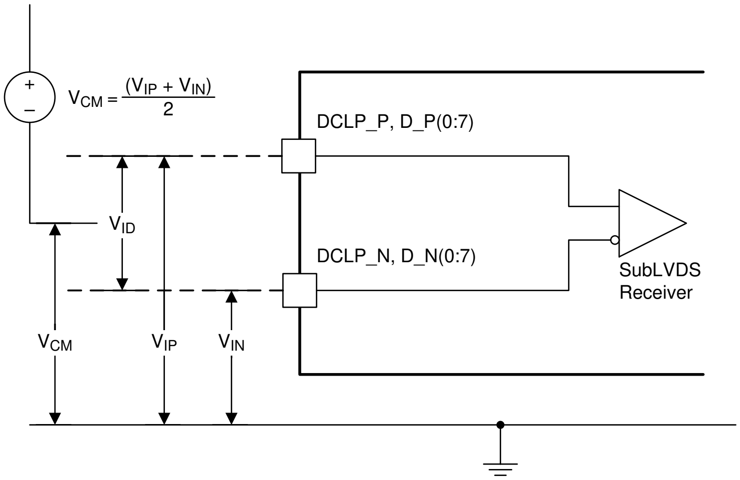


Figure 9. SubLVDS Voltage Parameters

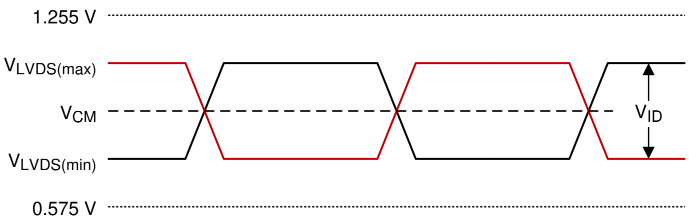


Figure 10. SubLVDS Waveform Parameters

$$V_{SubLVDS(max)} = V_{CM(max)} + ½ \times |V_{ID(max)}|$$

$$V_{SubLVDS(min)} = V_{CM(min)} – ½ \times |V_{ID(max)}|$$

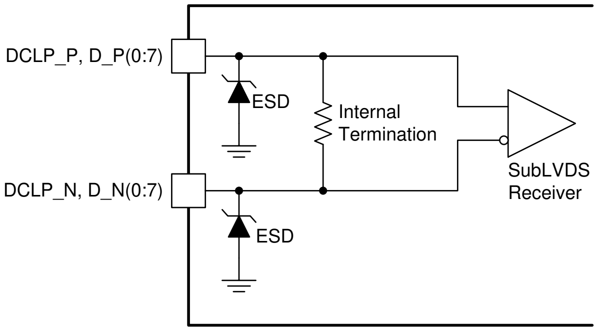


Figure 11. SubLVDS Equivalent Input Circuit

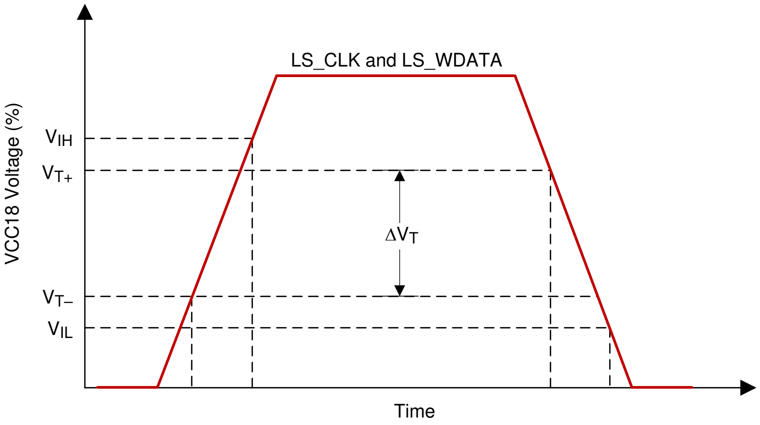


Figure 12. LPSDR Input Hysteresis

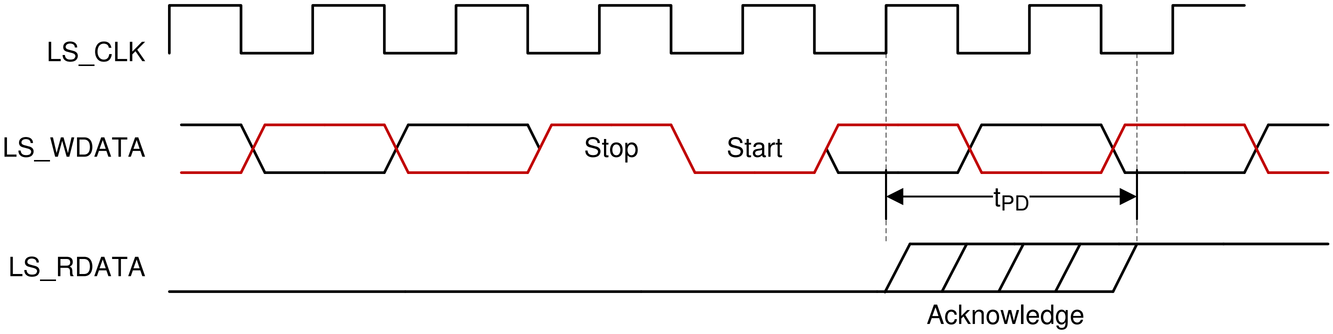
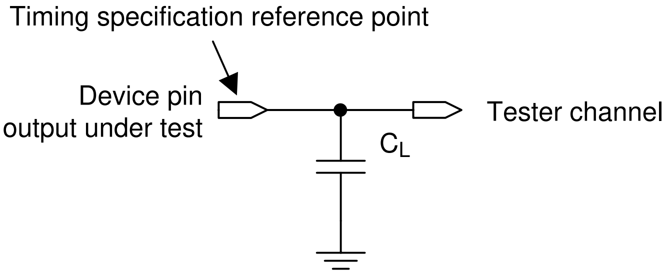


Figure 13. LPSDR Read Out



See *Timing* for more information.

Figure 14. Test Load Circuit for Output Propagation Measurement

6.8 Switching Characteristics(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, Clock to Q, rising edge of LS_CLK input to LS_RDATA output. Figure 13	C_L = 5 pF			11.1	ns
		C_L = 10 pF			11.3	ns
		C_L = 85 pF			15	ns
	Slew rate, LS_RDATA		0.5			V/ns
	Output duty cycle distortion, LS_RDATA		40%		60%	

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

6.9 System Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:	Electrical Interface Area (see Figure 15)			125	N
	Clamping and Thermal Interface Area (see Figure 15)			67	N

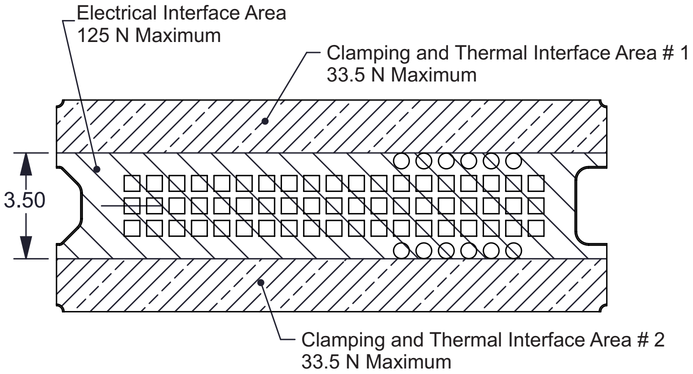


Figure 15. System Interface Loads

6.10 Physical Characteristics of the Micromirror Array

PARAMETER			VALUE	UNIT
	Number of active columns	See Figure 16	1280	micromirrors
	Number of active rows	See Figure 16	720	micromirrors
ε	Micromirror (pixel) pitch	See Figure 17	5.4	µm
	Micromirror active array width	Micromirror pitch × number of active columns; see Figure 16	6.912	mm
	Micromirror active array height	Micromirror pitch × number of active rows; see Figure 16	3.888	mm
	Micromirror active border	Pond of micromirror (POM)(1)	20	micromirrors/side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

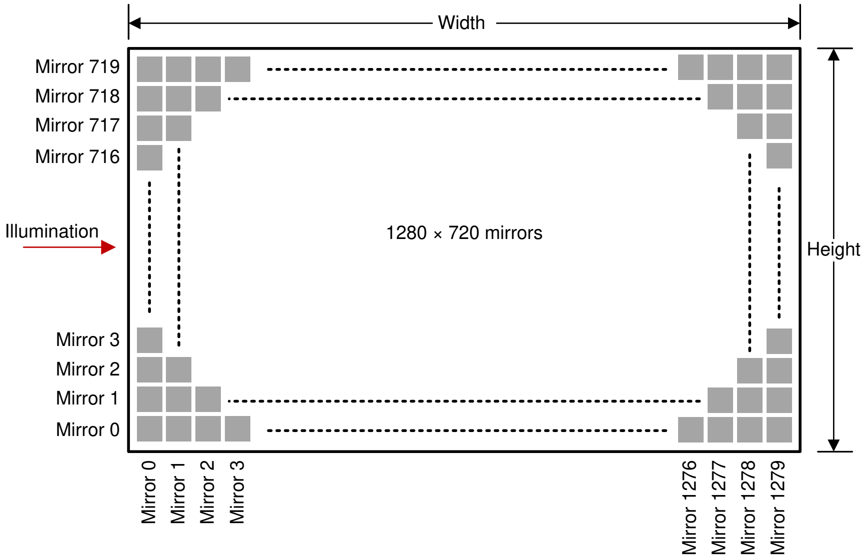


Figure 16. Micromirror Array Physical Characteristics

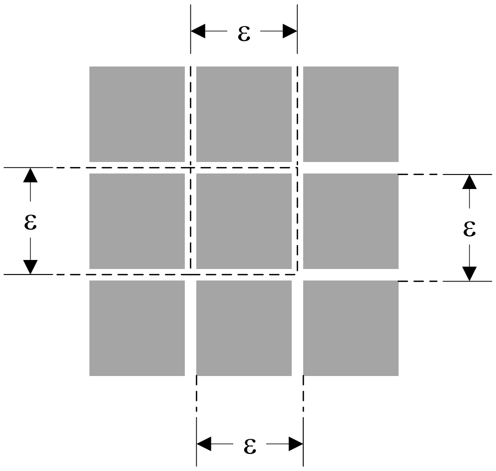


Figure 17. Mirror (Pixel) Pitch

6.11 Micromirror Array Optical Characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle	DMD landed state(1)		17		degrees
Micromirror tilt angle tolerance(2)(3)(4)(5)		–1.4		1.4	degrees
Micromirror tilt direction(6)(7)	Landed ON state		180		degrees
	Landed OFF state		270		
Micromirror crossover time(8)	Typical Performance		1	3	µs
Micromirror switching time(9)	Typical Performance	10			
Number of out-of-specification micromirrors(10)	Adjacent micromirrors			0	micromirrors
	Non-adjacent micromirrors			10	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction.
(7) Micromirror tilt direction is measured as in a typical polar coordinate system: measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
(8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(9) The minimum time between successive transitions of a micromirror.
(10) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states within the specified Micromirror Switching Time.

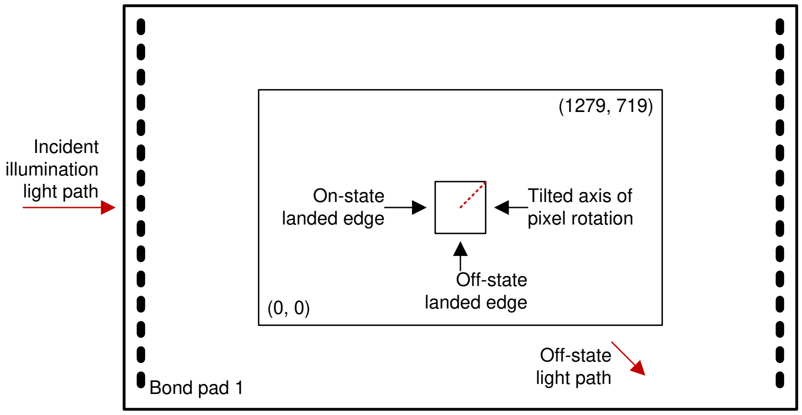


Figure 18. Landed Pixel Orientation and Tilt

6.12 Window Characteristics

PARAMETER(1)		**MIN**	**NOM**	**MAX**	**UNIT**
Window material designation			Corning Eagle XG		
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture(2)				See (2)	
Illumination overfill(3)				See (3)	
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
Window Transmittance, single-pass through both surfaces and glass	Average over the wavelength range 420 to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) See *Optical Interface and System Image Quality Considerations* for more information.
(2) See the package mechanical characteristics for details regarding the size and location of the window aperture.
(3) The active area of the DLP3010LC device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.

6.13 Chipset Component Usage Specification

The DLP3010LC is a component of one or more TI DLP® chipsets. Reliable function and operation of the DLP3010LC requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

6.14 Software Requirements

CAUTION

The DLP3010LC DMD has mandatory software requirements. Refer to *Software Requirements for TI DLP® Pico™ TRP Digital Micromirror Devices* application report for additional information. Failure to use the specified software will result in failure at power up.

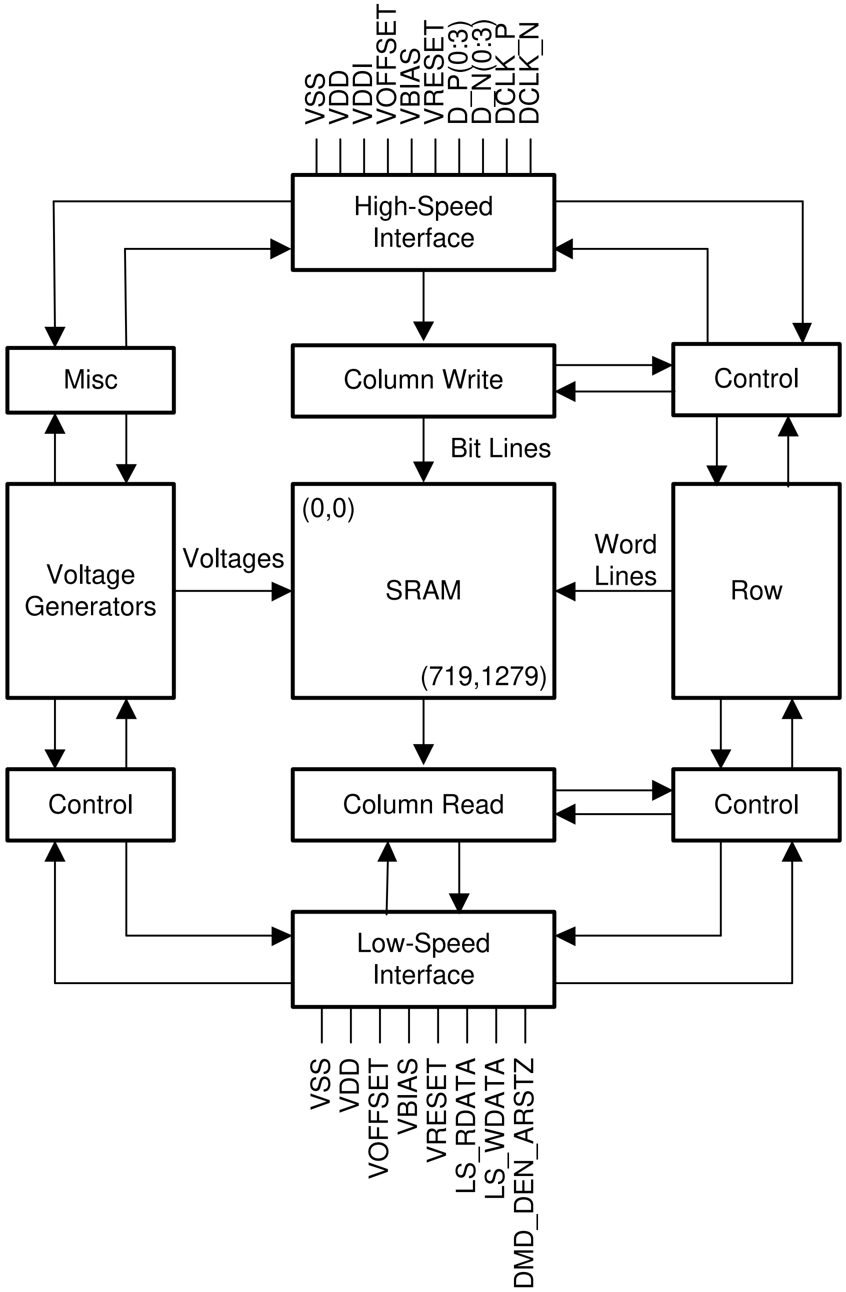
7 Detailed Description

7.1 Overview

The DLP3010LC DMD is a 0.3 inch diagonal spatial light modulator of aluminum micromirrors. Pixel array size is 1280 columns by 720 rows in a square grid pixel arrangement. The electrical interface is Sub Low Voltage Differential Signaling (SubLVDS) data.

This DMD is part of the chipset that includes the DLP3010LC DMD, DLPC3478 display and light controller and DLPA200x/DLPA300x PMIC/LED driver. To ensure reliable operation, this DMD must always be used with DLPC3478 display and light controller and DLPA200x/DLPA300x PMIC/LED driver.

7.2 Functional Block Diagram



(1) Details omitted for clarity
(2) Orientation is not representative of optical system
(3) Scale is not representative of layout

7.3 Feature Description

7.3.1 Power Interface

The power management IC, DLPA200x/DLPA300x, contains 3 regulated DC supplies for the DMD reset circuitry: VBIAS, VRESET and VOFFSET, as well as the 2 regulated DC supplies for the DLPC3478 controller.

7.3.2 Low-Speed Interface

The Low Speed Interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low–speed clock, and LS_WDATA is the low speed data input.

7.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs, with a dedicated clock.

7.3.4 Timing

The data sheet provides timing test results at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Figure 14 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is intended for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC3478 controller. See the DLPC3478 controller data sheet or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area is typically the same. Ensure this angle does not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat–state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and/or active area may occur.

Optical Interface and System Image Quality Considerations (continued)

7.5.1.2 Pupil Match

The optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and/or active area. These artifacts may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.1.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Be sure to design an illumination optical system that limits light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular optical architecture, overfill light may require further reduction below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

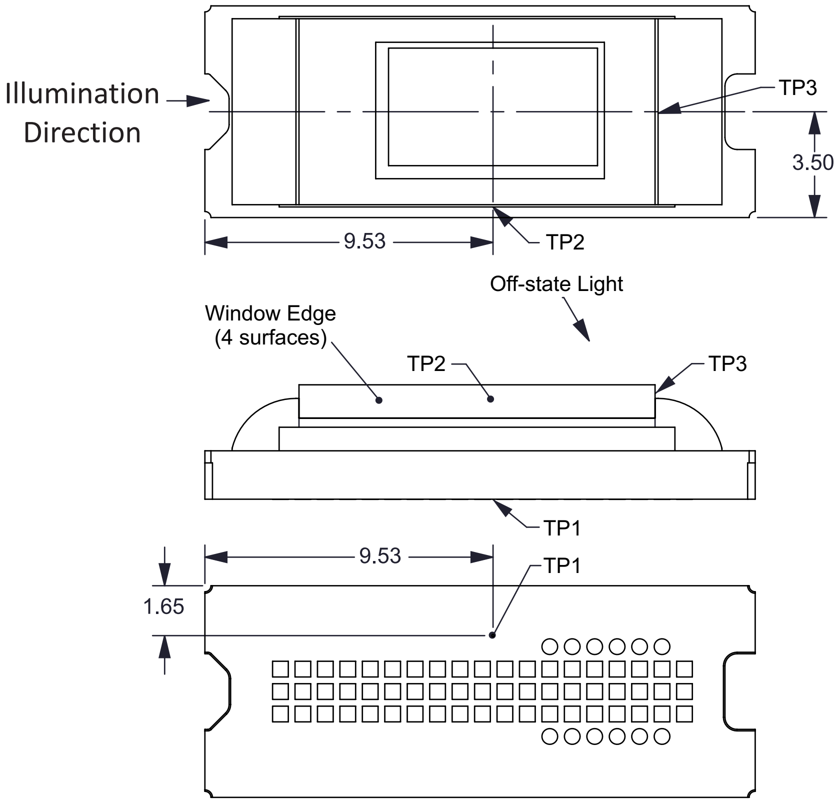


Figure 19. DMD Thermal Test Points

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the ceramic package thermal resistance, the electrical power dissipation, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

$$Q_{ILLUMINATION} = (C_{L2W} \times SL) \quad (3)$$

where

Micromirror Array Temperature Calculation (continued)

- T_{ARRAY} = Computed DMD array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 location in Figure 19
- $R_{ARRAY–TO–CERAMIC}$ = DMD package thermal resistance from array to outside ceramic (°C/W) specified in *Thermal Information*
- Q_{ARRAY} = Total DMD power; electrical plus absorbed (calculated) (W)
- $Q_{ELECTRICAL}$ = Nominal DMD electrical power dissipation (W)
- C_{L2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
- SL = Measured ANSI screen lumens (lm)

The electrical power dissipation of the DMD varies and depends on the voltages, data rates and operating frequencies. Use a nominal electrical power dissipation of 0.1 W to calculate array temperature. Absorbed optical power from the illumination source varies and depends on the operating state of the micromirrors and the intensity of the light source. Equation 1 through Equation 3 are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant CL2W is based on the DMD micromirror array characteristics. The conversion constant assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00266 W/lm.

The following is a sample calculation for typical projection application:

$T_{CERAMIC}$ = 55°C (measured)

SL = 300 lm (measured)

$Q_{ELECTRICAL}$ = 0.100 W

CL2W = 0.00266 W/lm

Q_{ARRAY} = 0.100 W + (0.00266 W/lm × 300 lm) = 0.898 W

T_{ARRAY} = 55°C + (0.898 W × 5.4°C/W) = 59.85°C

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On and Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 75/25 indicates that the referenced pixel is in the ON state 75% of the time (and in the OFF state 25% of the time), whereas 25/75 indicates that the pixel is in the OFF state 75% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

When assessing landed duty cycle, the time spent switching from the current state to the opposite state is considered negligible and is thus ignored.

Because a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) nominally add to 100.In practice, image processing algorithms in the DLP chipset can result a total of less that 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

It is the symmetry or asymmetry of the landed duty cycle that is relevant. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

Micromirror Landed-On/Landed-Off Duty Cycle (continued)

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect the usable life of the DMD. This interaction can be used to reduce the impact that an asymmetrical landed duty cycle has on the useable life of the DMD. Figure 1 describes this relationship. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD temperature that the DMD should be operated at for a give long-term average landed duty cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel depends on the image content being displayed by that pixel.

In the simplest case for example, when the system displays pure-white on a given pixel for a given time period, that pixel operates very close to a 100/0 landed duty cycle during that time period. Likewise, when the system displays pure-black, the pixel operates very close to a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in Table 1.

Table 1. Grayscale Value and Landed Duty Cycle

Grayscale Value	Nominal Landed Duty Cycle
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

To account for color rendition (and continuing to ignore image processing for this example) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where *color cycle time* describes the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the nominal landed duty cycle of a given pixel can be calculated as shown in Equation 4:

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_\%} \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_\%} \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_\%} \times \text{Blue\_Scale\_Value}) \quad (4)$$

where

- Red_Cycle_% represents the percentage of the frame time that red displays to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green displays to achieve the desired white point
- Blue_Cycle_% represents the percentage of the frame time that blue displays to achieve the desired white point

For example, assume that the ratio of red, green and blue color cycle times are as listed in Table 2 (in order to achieve the desired white point) then the resulting nominal landed duty cycle for various combinations of red, green, blue color intensities are as shown in Table 3.

Table 2. Example Landed Duty Cycle for Full-Color Pixels

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage
50%	20%	30%

Table 3. Color Intensity Combinations

Red Scale Value	Green Scale Value	Blue Scale Value	Nominal Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to consider when estimating the landed duty cycle is any applied image processing. In the DLPC34xx controller family, the two functions which influence the actual landed duty cycle are Gamma and IntelliBright™, and bitplane sequencing rules.

Gamma is a power function of the form Output_Level = A × Input_Level^{Gamma}, where A is a scaling factor that is typically set to 1.

In the DLPC34xx controller family, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in Figure 20.

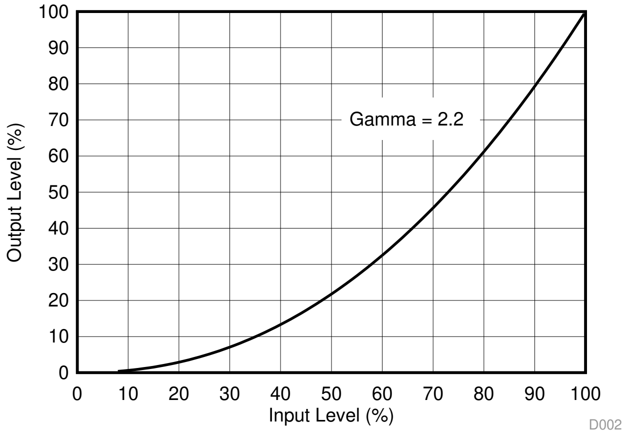


Figure 20. Example of Gamma = 2.2

As shown in Figure 20, when the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value is 13% after gamma is applied. Because gamma has a direct impact on the displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

The IntelliBright algorithm content adaptive illumination control (CAIC) and local area brightness boost (LABB) also apply transform functions on the gray scale level of each pixel.

But while the amount of gamma correction applied to every pixel (of every frame) is constant (the exponent, gamma, is constant), CAIC and LABB are both adaptive functions that can apply a different amounts of either boost or compression to every pixel of every frame.

The CAIC and LABB algorithms receive no information regarding any previous gain or boost processing. In cases where the application performs any processing of the input data before the image reaches the DLPC3478 controller, unexpected behavior such as saturation may occur.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application depends primarily on the optical architecture of the system and the format of the data coming into the DLPC3478 controller. The new high-tilt pixel in the side-illuminated DMD increases brightness performance and enables a smaller system electronics footprint for thickness constrained applications. Applications include

- Integrated display and 3D depth capture
  - Smart phone, tablets, laptop, camera
  - Battery-powered mobile accessory
- 3D depth capture: 3D camera, 3D reconstruction, AR/VR, dental scanner
- 3D machine vision: robotics, metrology, in-line inspection (AOI)
- 3D biometrics: facial and finger print recognition
- Light exposure: 3D printers, programmable spatial and temporal light exposure

DMD power-up and power-down sequencing is strictly controlled by the DLPA200x/DLPA300x. Refer to *Power Supply Recommendations* for power-up and power-down specifications. DLP3010LC DMD reliability is specified when used with DLPC3478 controller and DLPA200x/DLPA300x PMIC/LED driver only.

8.2 Typical Application

DLP3010LC DMD with DLPC3478 controller enables high accuracy and very small form factor 3D depth scanner products. Figure 21 shows a typical 3D depth scanner system block diagram using external pattern streaming mode.

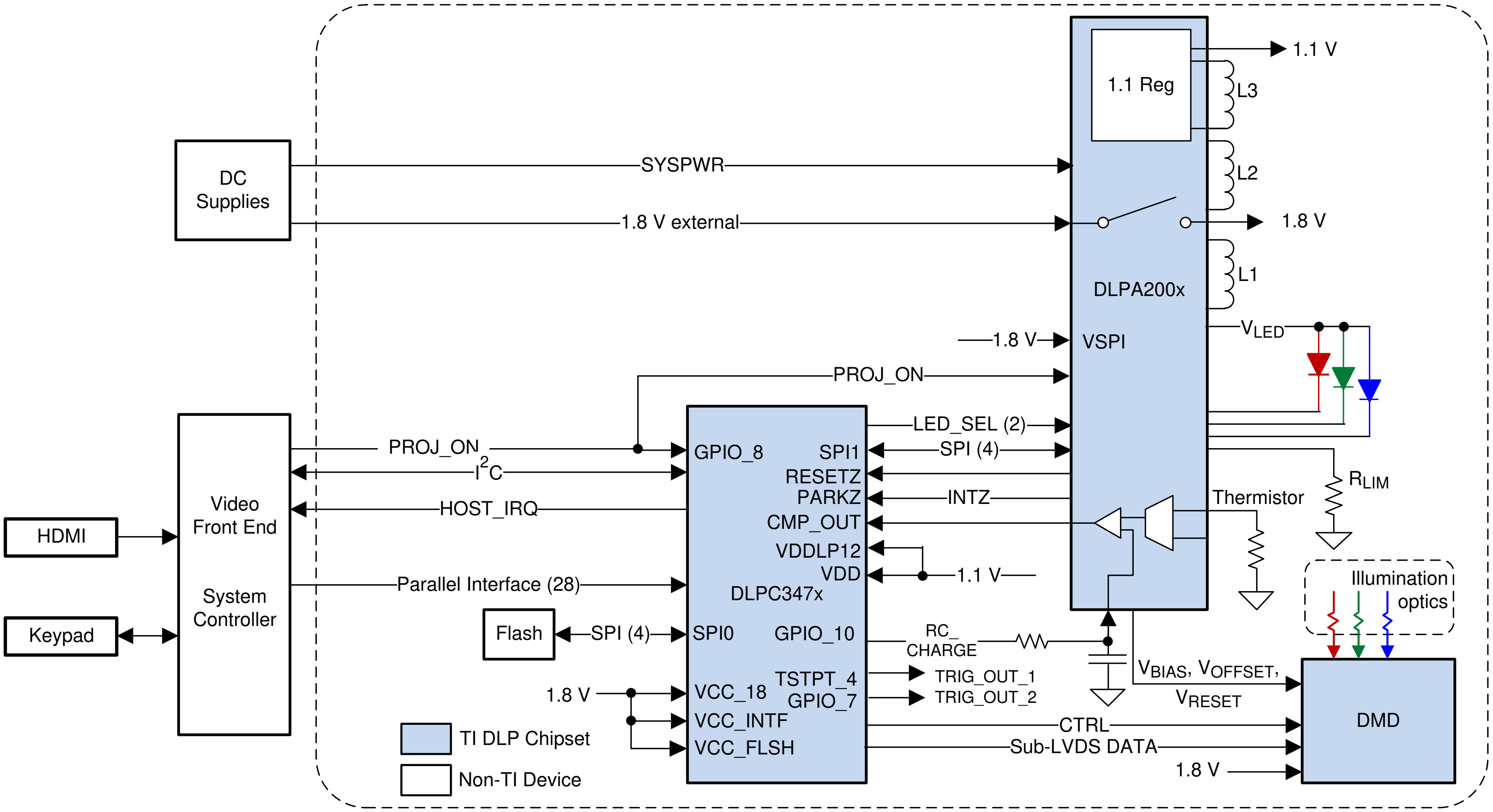


Figure 21. Typical Application

8.2.1 Design Requirements

A high-accuracy 3D depth scanner product can be created by using a DLP chipset comprised of DLP3010 DMD, DLPC3478 controller and DLPA200x or DLPA300x PMIC/LED driver. The DLPC3478 simplifies the pattern generation, the DLPA200x or DLPA300x provides the needed analog functions and the DMD displays the required patterns for accurate 3D depth scanning.

In addition to the three DLP devices in the chipset, other IC components may be needed. At a minimum, this design requires a flash device to store the software and firmware to control the DLPC3478 .

Red, green, and blue LEDs typically supply the illumination light that is applied to the DMD. These LEDs are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector. In addition to LEDs, other light sources like laser diodes, vertical-cavity surface-emitting laser (VCSEL) are also supported.

The parallel interface connects the DLPC3478 controller to the host processing for receiving patterns or video data. Connect an I^2C interface to the host processor to send commands to the DLPC3478 controller. The battery (SYSPWR) and a regulated 1.8-V supply are the only power supplies needed external to the projector in case of DLPA200x. The DLPA300x supplies 1.8 V without external regulator. A single signal (PROJ_ON) controls the entire DLP system power. When PROJ_ON is high, the DLP system turns on and when PROJ_ON is low, the DLPC3478 turns off. When the DLPC3478 is off, the DLP system draws only a few microamperes of current on SYSPWR. When PROJ_ON is low, the 1.8-V power supply can remain at 1.8 V for use by other sub systems. When PROJ_ON is low, the DLPA200x or DLPA300x draws no current on the 1.8-V supply.

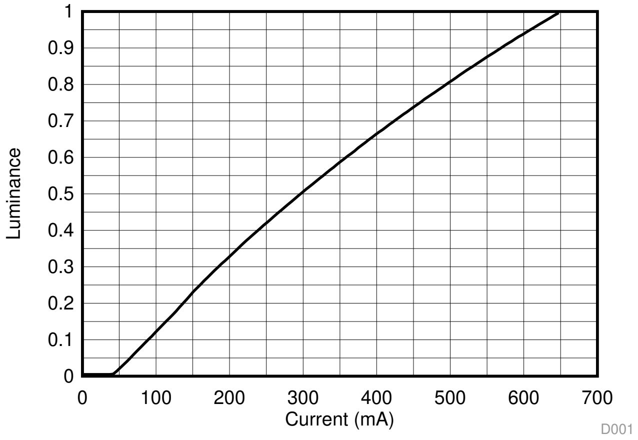
8.2.2 Detailed Design Procedure

For more information on connecting the DLPC3478, the DLPA200x/DLPA300x, and the DMD, see the reference design schematic. Based on the reference schematic a small circuit board can be created. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve a reliable projector.

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

8.2.3 Application Curve

This device drives current time-sequentially though the LEDs. As the LED currents through the red, green, and blue LEDs increases, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents as shown in Figure 22. For the LED currents shown, assumed that the same current amplitude is applied to the red, green, and blue.



$I_{LED(red)} = I_{LED(green)} = I_{LED(blue)}$

Figure 22. Luminance vs Current

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{DD}
- V_{DDI}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLPAxxxx device.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in Figure 23.

V_{BIAS}, V_{DD}, V_{DDI}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.

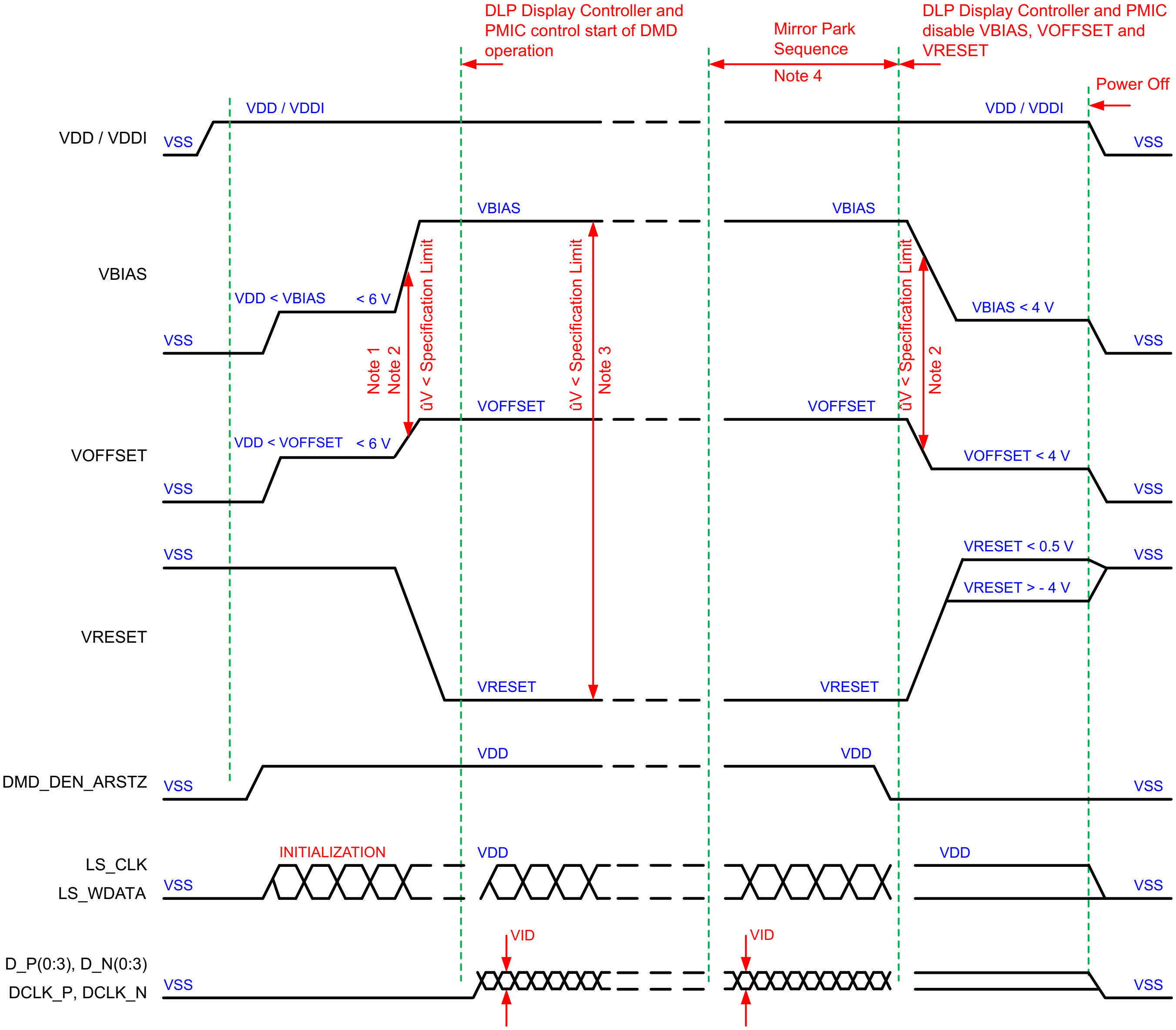
9.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{DD} and V_{DDI} must always start and settle before V_{OFFSET}, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in *Recommended Operating Conditions*. Refer to Table 4 for power-up delay requirements.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS} and V_{OFFSET}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in *Absolute Maximum Ratings* , in *Recommended Operating Conditions*, and in Power Supply Sequencing Requirements.
- During power-up, LPSDR input pins must not be driven high until after V_{DD} /V_{DDI} have settled at operating voltages listed in *Recommended Operating Conditions*.

9.2 DMD Power Supply Power-Down Procedure

- Power-down sequence is the reverse order of the previous power-up sequence. During power-down, V_{DD} and V_{DDI} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within 4 V of ground.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in *Recommended Operating Conditions*.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS} and V_{OFFSET}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in *Absolute Maximum Ratings* , in *Recommended Operating Conditions*, and in Power Supply Sequencing Requirements.
- During power-down, LPSDR input pins must be less than V_{DD} /V_{DDI} specified in *Recommended Operating Conditions*.

9.3 Power Supply Sequencing Requirements



(1) Refer to Table 4 and Figure 24 for critical power-up sequence delay requirements.

(2) To prevent excess current, the supply voltage delta $|V_{BIAS} - V_{OFFSET}|$ must be less than specified in Recommended Operating Conditions. OEMs may find that the most reliable way to ensure this is to power V_{OFFSET} prior to V_{BIAS} during power-up and to remove V_{BIAS} prior to V_{OFFSET} during power-down. Refer to Table 4 and Figure 24 for power-up delay requirements.

(3) To prevent excess current, the supply voltage delta $|V_{BIAS} - V_{RESET}|$ must be less than specified limit shown in Recommended Operating Conditions.

(4) When system power is interrupted, the ASIC driver initiates hardware power-down that disables V_{BIAS}, V_{RESET} and V_{OFFSET} after the Micromirror Park Sequence. Software power-down disables V_{BIAS}, V_{RESET}, and V_{OFFSET} after the Micromirror Park Sequence through software control.

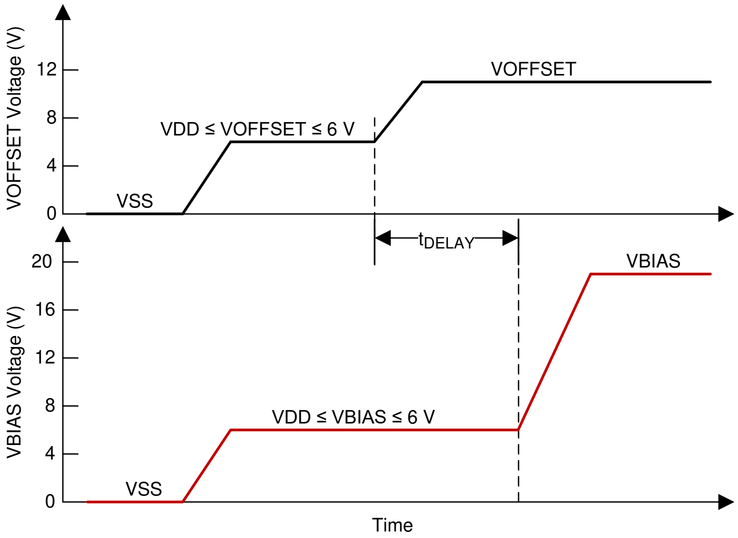
(5) Drawing is not to scale and details are omitted for clarity.

Figure 23. Power Supply Sequencing Requirements (Power Up and Power Down)

Power Supply Sequencing Requirements (continued)

Table 4. Power-Up Sequence Delay Requirement

PARAMETER		MIN	MAX	UNIT
t_{DELAY}	Delay requirement from V_{OFFSET} power up to V_{BIAS} power up	2		ms
V_{OFFSET}	Supply voltage level during power–up sequence delay (see Figure 24)		6	V
V_{BIAS}	Supply voltage level during power–up sequence delay (see Figure 24)		6	V



A. Refer to Table 4 for V_{OFFSET} and V_{BIAS} supply voltage levels during power-up sequence delay.

Figure 24. Power-Up Sequence Delay Requirement

10 Layout

10.1 Layout Guidelines

There are no specific layout guidelines for the DMD as typically DMD is connected using a board to board connector to a flex cable. Flex cable provides the interface of data and control signals between the DLPC3478 controller and the DLP3010LC DMD. For detailed layout guidelines refer to the layout design files. Some layout guideline for the flex cable interface with DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer Figure 25.
- Minimum of two 100-nF decoupling capacitor close to VBIAS. Capacitor C6 and C7 in Figure 25.
- Minimum of two 100-nF decoupling capacitor close to VRST. Capacitor C9 and C8 in Figure 25.
- Minimum of two 220-nF decoupling capacitor close to VOFS. Capacitor C5 and C4 in Figure 25.
- Minimum of four 100-nF decoupling capacitor close to VDDI and VDD. Capacitor C1, C2, C3 and C10 in Figure 25.

10.2 Layout Example

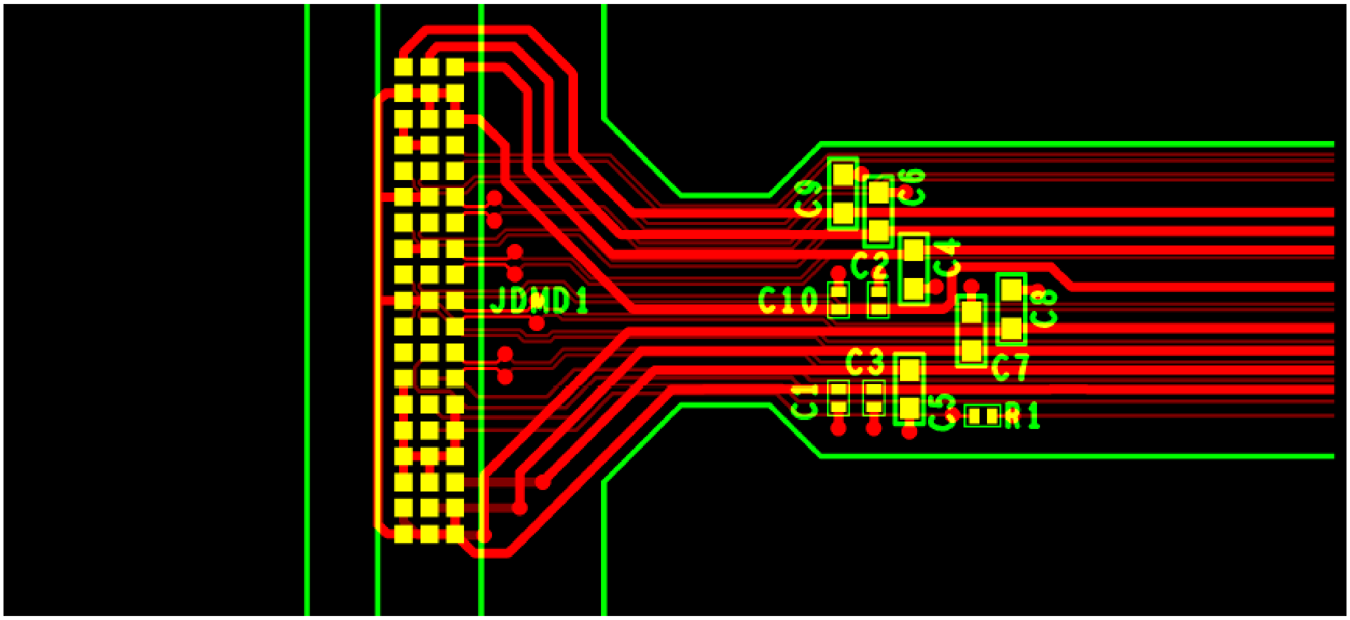


Figure 25. Power Supply Connections

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

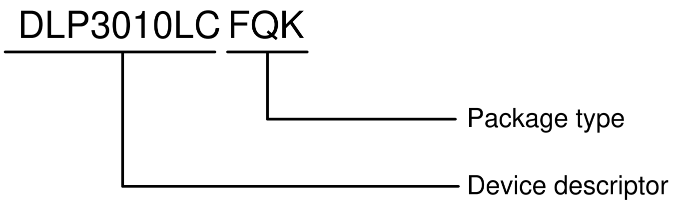


Figure 26. Part Number Description

11.1.2 Device Markings

The device marking includes the legible character string GHJJJJK DLP3010LCFQK. GHJJJJK is the lot trace code. DLP3010LCFQK is the orderable device number.

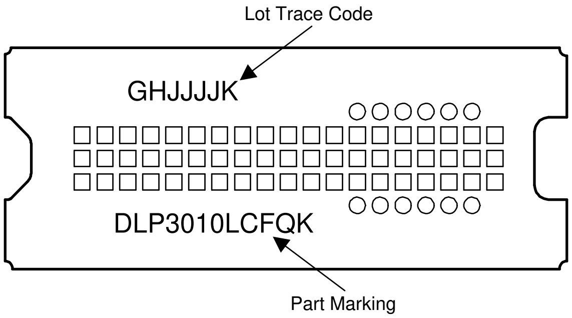


Figure 27. DMD Marking

11.2 Documentation Support

11.3 Related Links

Table 5 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLPC3478	Click here	Click here	Click here	Click here	Click here
DLPA2000	Click here	Click here	Click here	Click here	Click here
DLPA2005	Click here	Click here	Click here	Click here	Click here
DLPA3000	Click here	Click here	Click here	Click here	Click here
DLPA3005	Click here	Click here	Click here	Click here	Click here

11.4 Communnity Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

Pico, IntelliBright, E2E are trademarks of Texas Instruments.
DLP is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP3010LCFQK	ACTIVE	CLGA	FQK	57	120	RoHS & Green	Call TI	N / A for Pkg Type	0 to 70		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

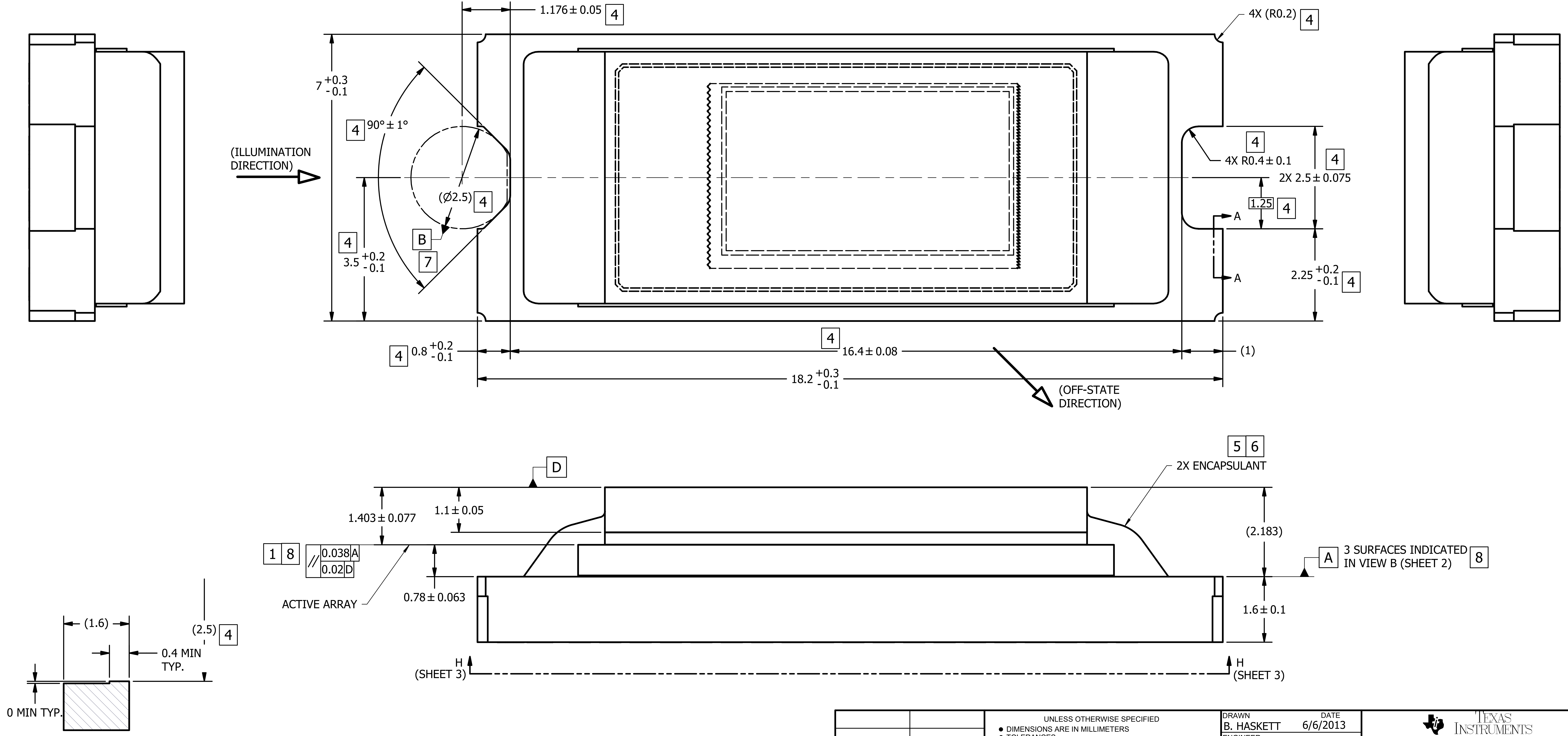
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW C (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
7. DATUM B IS DEFINED BY A DIA. 2.5 PIN, WITH A FLAT ON THE SIDE FACING TOWARD THE CENTER OF THE ACTIVE ARRAY, AS SHOWN IN VIEW B (SHEET 2).
8. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.

REVISIONS

REV	DESCRIPTION	DATE	BY
A	ECO 2133835: INITIAL RELEASE	6/6/2013	BMH
B	ECO 2134093: CORRECT WINDOW THK TOL, ZONE B6	6/17/2013	BMH
C	ECO 2186947: ADD APERTURE SLOTS PICTORIALLY	4/8/2020	PPC



SECTION A-A
NOTCH OFFSETS

	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

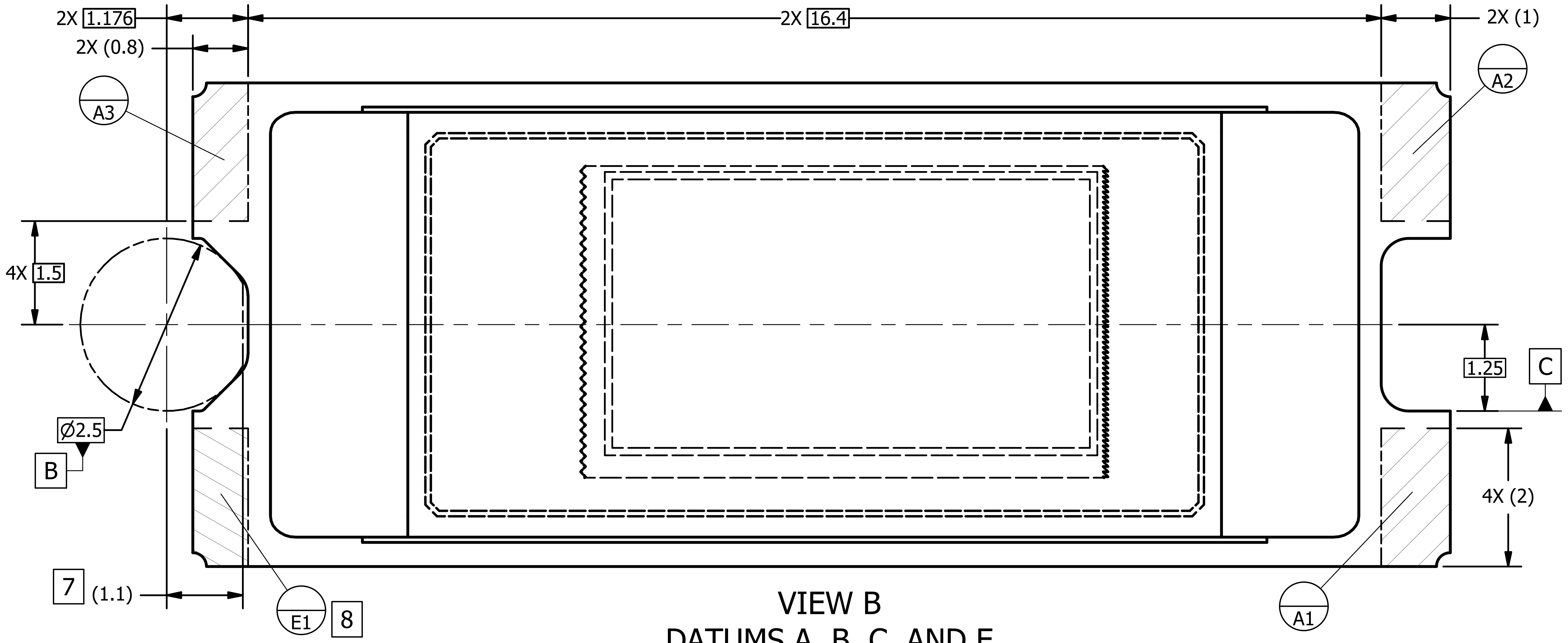
UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  ANGLES ± 1°
  2 PLACE DECIMALS ± 0.25
  1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	B. HASKETT	6/6/2013
ENGINEER	B. HASKETT	6/6/2013
QA/CE	P. KONRAD	6/7/2013
CM	S. SUSI	6/6/2013
	S. CROFF	6/10/2013
APPROVED	R. LONG	6/6/2013

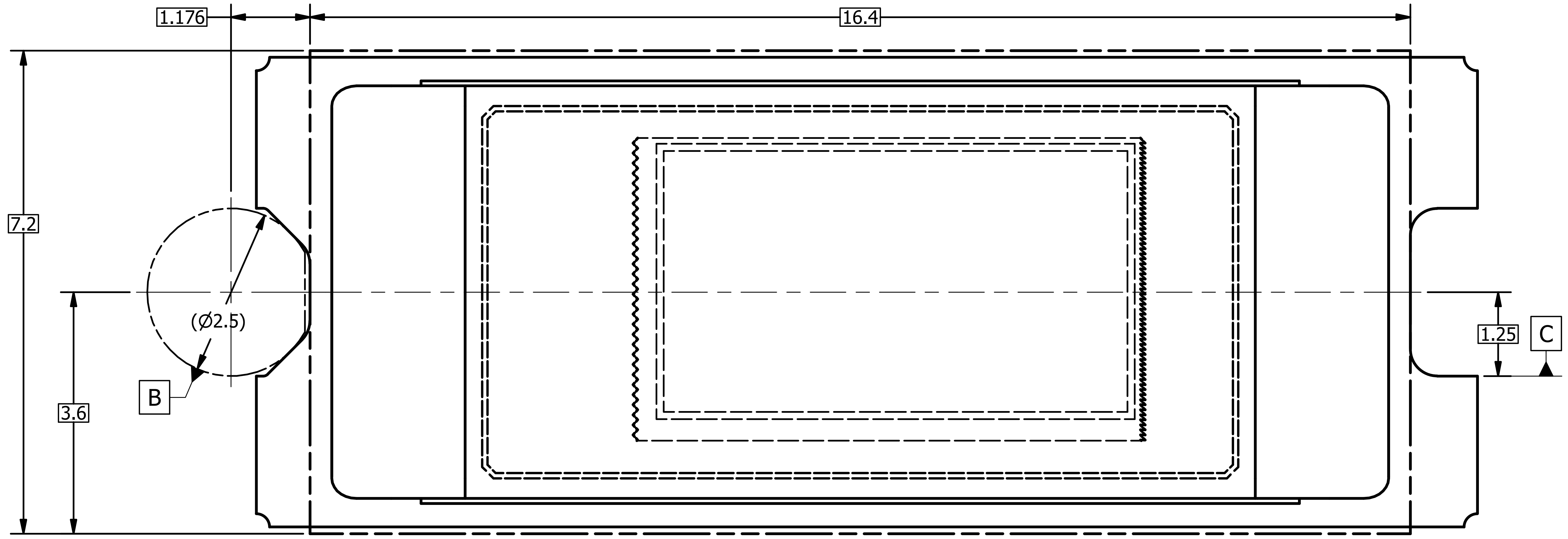
TEXAS INSTRUMENTS
Dallas Texas

TITLE
ICD, MECHANICAL, DMD,
.3 720p SERIES 245
(FQK PACKAGE)

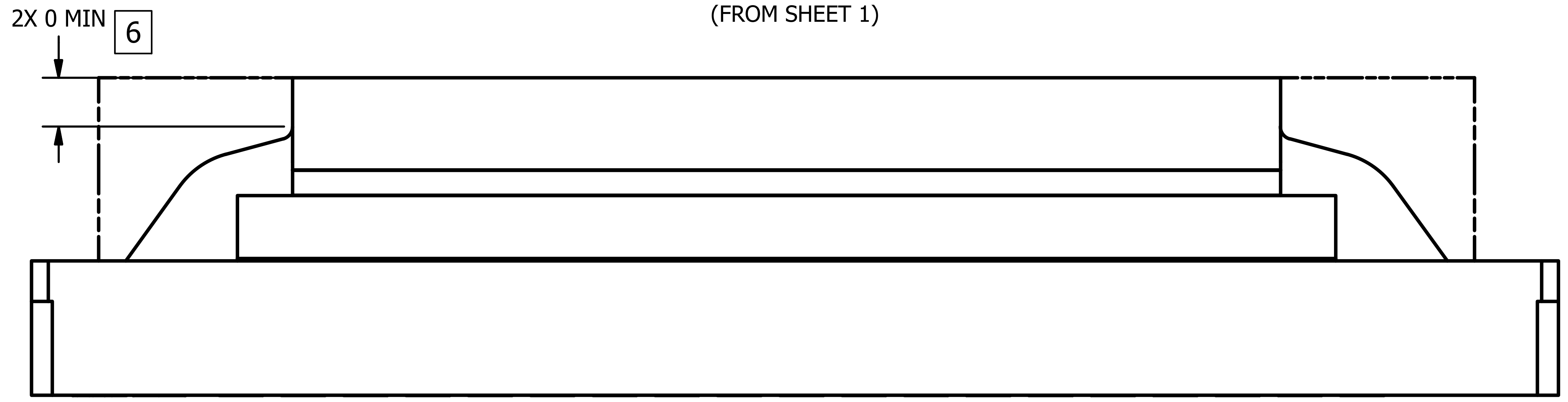
SIZE D | DWG NO 2512014 | REV C
SCALE 20:1 | SHEET 1 OF 3



VIEW B
DATUMS A, B, C, AND E
(FROM SHEET 1)



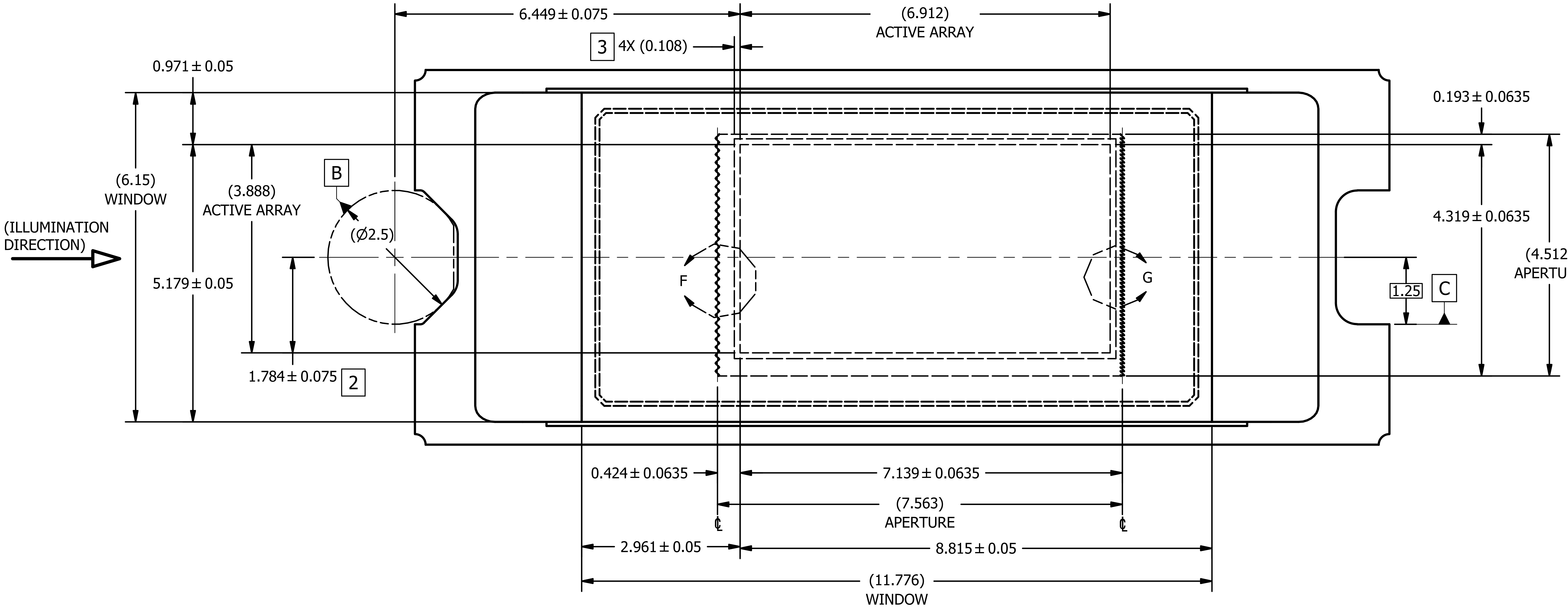
VIEW C 5
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
(FROM SHEET 1)



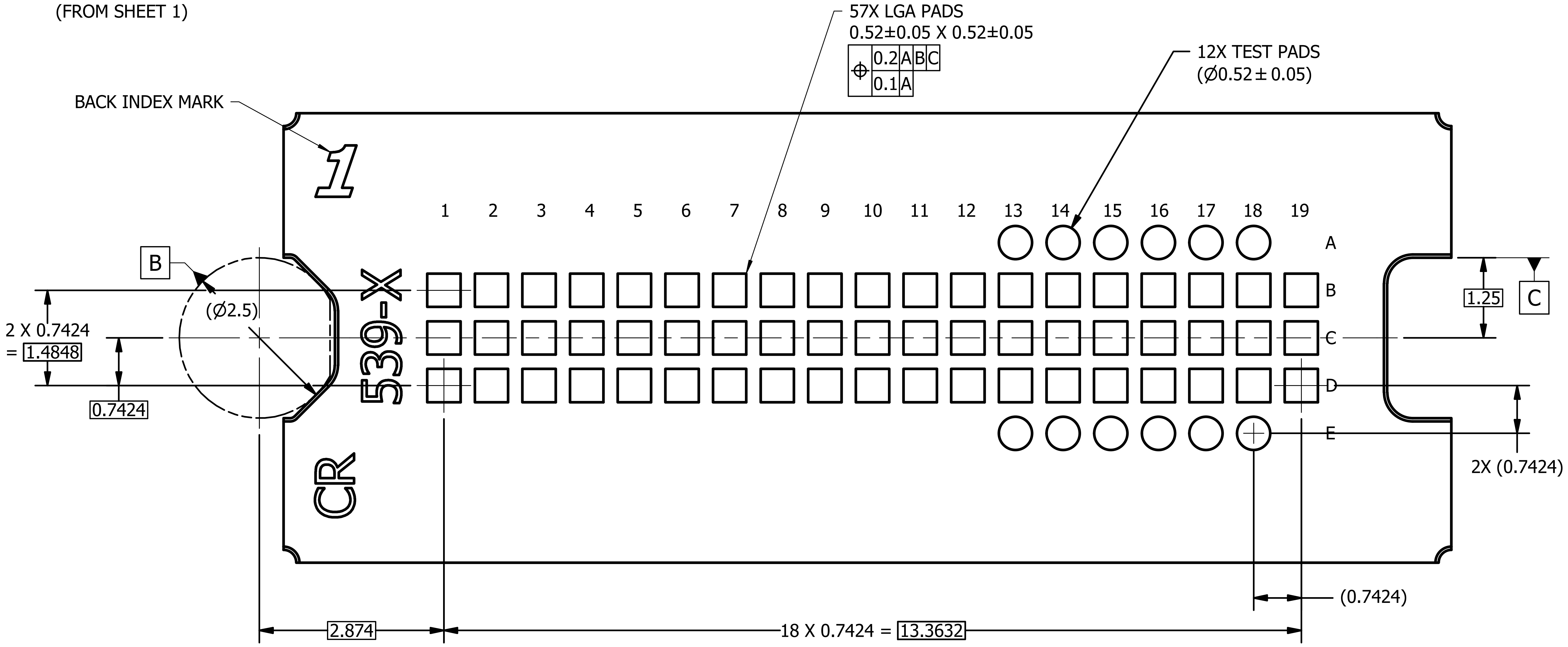
VIEW D
ENCAPSULANT MAXIMUM HEIGHT

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 6/6/2013	SIZE D	DWG NO 2512014
			SCALE	SHEET 2 OF 3

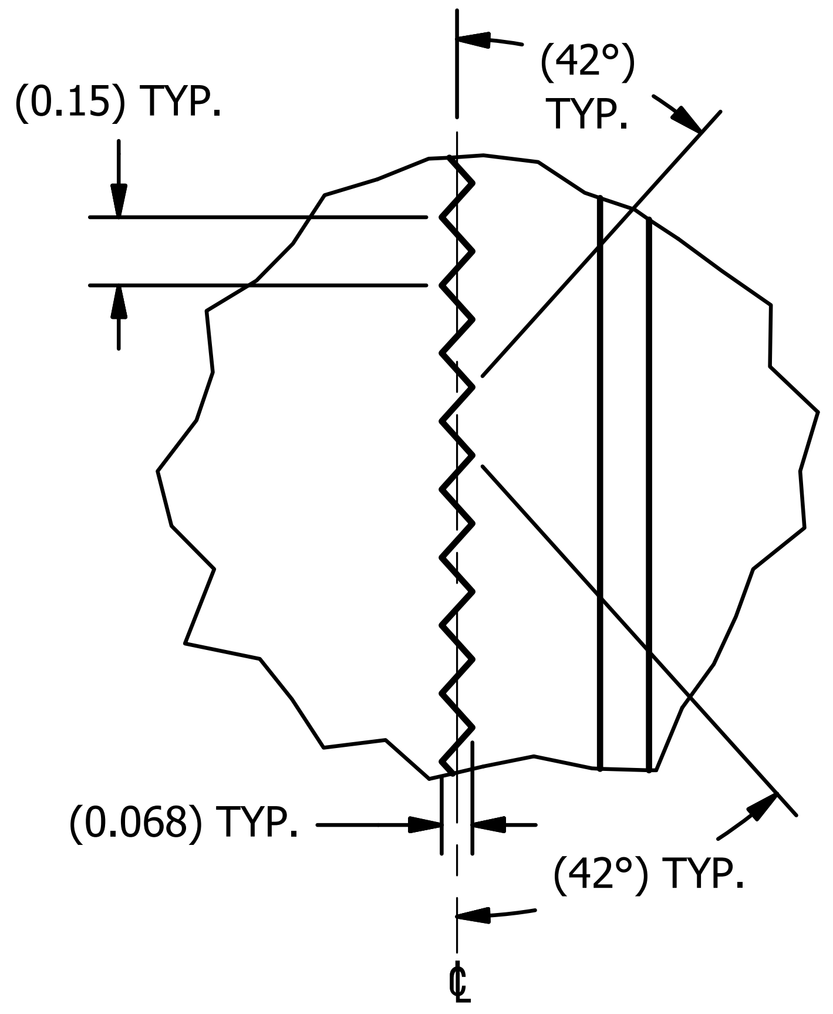
REV C



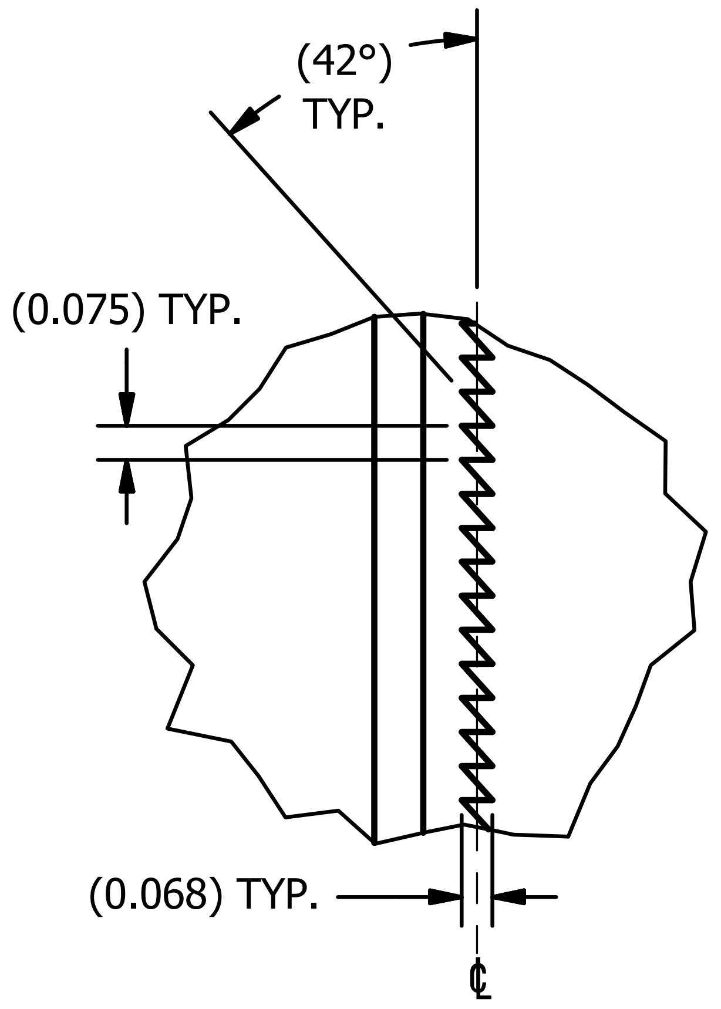
VIEW E
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



VIEW H-H
BACK SIDE METALLIZATION
(FROM SHEET 1)



DETAIL F
APERTURE LEFT EDGE
SCALE 60 : 1



DETAIL G
APERTURE RIGHT EDGE
SCALE 60 : 1

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 6/6/2013	SIZE D	DWG NO 2512014	REV C
			SCALE	SHEET 3 OF 3	

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated